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IS42S86400B
IS42S16320B, IS45S16320B

64M x 8, 32M x 16
512Mb SYNCHRONOUS DRAM

DECEMBER 2011

FEATURES

- Clock frequency: 166, 143, 133 MHz
- Fully synchronous; all signals referenced to a positive clock edge
- Internal bank for hiding row access/precharge
- Power supply

	VDD	VDDQ
IS42/45S16320B	3.3V	3.3V
IS42S86400B	3.3V	3.3V

- LVTTL interface
- Programmable burst length
  – (1, 2, 4, 8, full page)
- Programmable burst sequence: Sequential/Interleave
- Auto Refresh (CBR)
- Self Refresh
- 8K refresh cycles every 16ms (A2 grade) or 64 ms (Commercial, Industrial, A1 grade)
- Random column address every clock cycle
- Programmable $\overline{CAS}$ latency (2, 3 clocks)
- Burst read/write and burst read/single write operations capability
- Burst termination by burst stop and precharge command
- Available in 54-pin TSOP-II and 54-ball W-BGA (x16 only)
- Operating Temperature Range:
  Commercial: 0°C to +70°C
  Industrial: -40°C to +85°C
  Automotive, A1: -40°C to +85°C
  Automotive, A2: -40°C to +105°C

OVERVIEW

ISSI's 512Mb Synchronous DRAM achieves high-speed data transfer using pipeline architecture. All inputs and outputs signals refer to the rising edge of the clock input. The 512Mb SDRAM is organized as follows.

IS42S86400B	IS42/45S16320B
16Mx8x4 Banks	8M x16x4 Banks
54-pin TSOPII	54-pin TSOPII
	54-ball W-BGA

KEY TIMING PARAMETERS

Parameter	-6	-7	-75E	Unit
Clk Cycle Time				
$\overline{CAS}$ Latency = 3	6	7	–	ns
$\overline{CAS}$ Latency = 2	10	10	7.5	ns
Clk Frequency				
$\overline{CAS}$ Latency = 3	166	143	–	Mhz
$\overline{CAS}$ Latency = 2	100	100	133	Mhz
Access Time from Clock				
$\overline{CAS}$ Latency = 3	5.4	5.4	–	ns
$\overline{CAS}$ Latency = 2	6	6	5.5	ns

DEVICE OVERVIEW

The 512Mb SDRAM is a high speed CMOS, dynamic random-access memory designed to operate in 3.3V V_{DD} and 3.3V V_{DDQ} memory systems containing 536,870,912 bits. Internally configured as a quad-bank DRAM with a synchronous interface. Each 134,217,728-bit bank is organized as 8,192 rows by 1024 columns by 16 bits. Each of the x8's 134,217,728-bit banks is organized as 8,192 rows by 2048 columns by 8 bits.

The 512Mb SDRAM includes an AUTO REFRESH MODE, and a power-saving, power-down mode. All signals are registered on the positive edge of the clock signal, CLK. All inputs and outputs are LVTTL compatible.

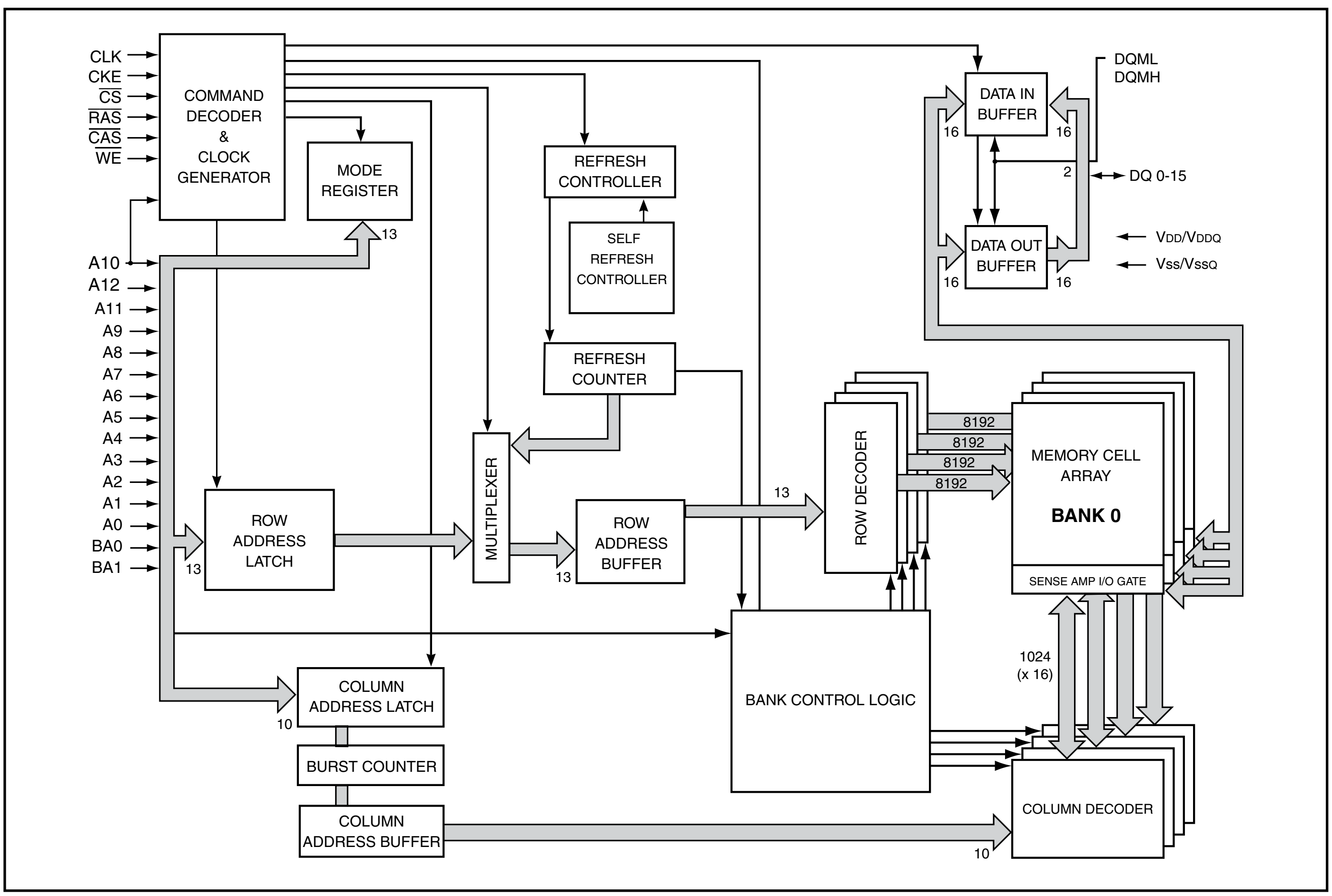
The 512Mb SDRAM has the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time and the capability to randomly change column addresses on each clock cycle during burst access.

A self-timed row precharge initiated at the end of the burst sequence is available with the AUTO PRECHARGE function enabled. Precharge one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

SDRAM read and write accesses are burst oriented starting at a selected location and continuing for a programmed number of locations in a programmed sequence. The registration of an ACTIVE command begins accesses, followed by a READ or WRITE command. The ACTIVE command in conjunction with address bits registered are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A12 select the row). The READ or WRITE commands in conjunction with address bits registered are used to select the starting column location for the burst access.

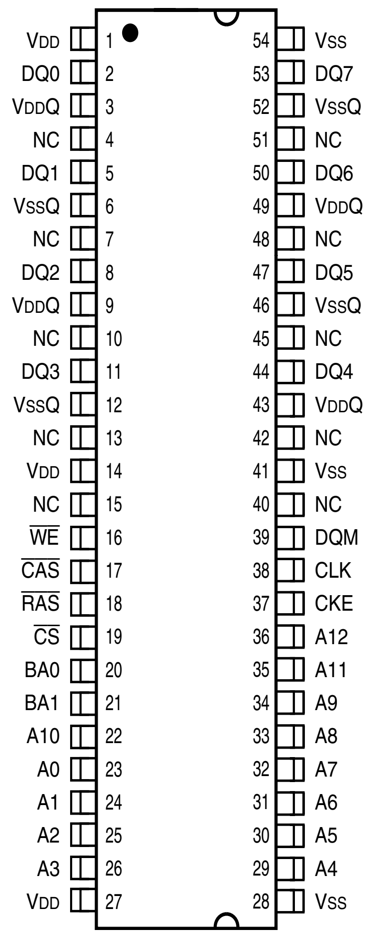
Programmable READ or WRITE burst lengths consist of 1, 2, 4 and 8 locations or full page, with a burst terminate option.

FUNCTIONAL BLOCK DIAGRAM (FOR 8MX16X4 BANKS SHOWN)



PIN CONFIGURATIONS

54 pin TSOP - Type II for x8



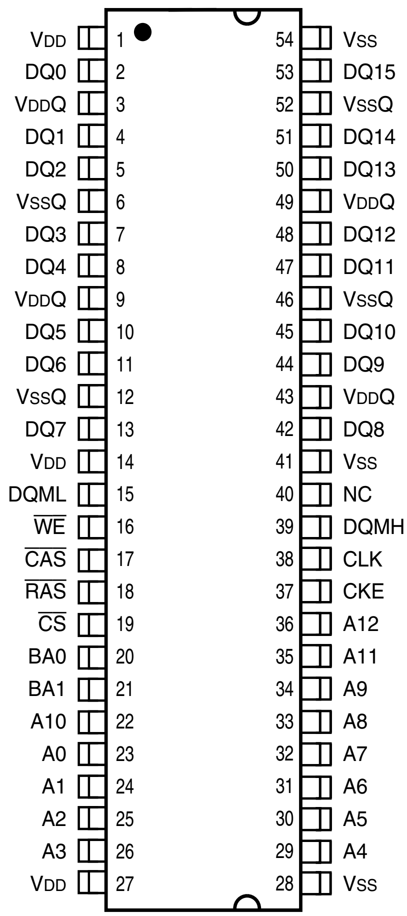
PIN DESCRIPTIONS

A0-A12	Row Address Input
A0-A9, A11	Column Address Input
BA0, BA1	Bank Select Address
DQ0 to DQ7	Data I/O
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command

$\overline{WE}$	Write Enable
DQM	Data Input/Output Mask
VDD	Power
Vss	Ground
VDDQ	Power Supply for I/O Pin
VssQ	Ground for I/O Pin
NC	No Connection

PIN CONFIGURATIONS

54 pin TSOP - Type II for x16



PIN DESCRIPTIONS

A0-A12	Row Address Input
A0-A9	Column Address Input
BA0, BA1	Bank Select Address
DQ0 to DQ15	Data I/O
CLK	System Clock Input
CKE	Clock Enable
$\overline{\text{CS}}$	Chip Select
$\overline{\text{RAS}}$	Row Address Strobe Command
$\overline{\text{CAS}}$	Column Address Strobe Command

$\overline{\text{WE}}$	Write Enable
DQML	x16 Lower Byte, Input/Output Mask
DQMH	x16 Upper Byte, Input/Output Mask
V_{DD}	Power
Vss	Ground
V_{DDQ}	Power Supply for I/O Pin
V_{SSQ}	Ground for I/O Pin
NC	No Connection

PIN CONFIGURATION

54-ball W-BGA for x16 (Top View) (11.00 mm x 13.00 mm Body, 0.8 mm Ball Pitch)
package code: B

	1	2	3	4	5	6	7	8	9
A	VSS	DQ15	VSSQ				VDDQ	DQ0	VDD
B	DQ14	DQ13	VDDQ				VSSQ	DQ2	DQ1
C	DQ12	DQ11	VSSQ				VDDQ	DQ4	DQ3
D	DQ10	DQ9	VDDQ				VSSQ	DQ6	DQ5
E	DQ8	NC	VSS				VDD	DQML	DQ7
F	DQMH	CLK	CKE				$\overline{CAS}$	$\overline{RAS}$	$\overline{WE}$
G	A12	A11	A9				BA0	BA1	$\overline{CS}$
H	A8	A7	A6				A0	A1	A10
J	VSS	A5	A4				A3	A2	VDD

PIN DESCRIPTIONS

A0-A12	Row Address Input
A0-A9	Column Address Input
BA0, BA1	Bank Select Address
DQ0 to DQ15	Data I/O
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command
$\overline{WE}$	Write Enable
DQML	x16 Lower Byte Input/Output Mask
DQMH	x16 Upper Byte Input/Output Mask
V_{DD}	Power
Vss	Ground
V_{DDQ}	Power Supply for I/O Pin
V_{SSQ}	Ground for I/O Pin
NC	No Connection

PIN FUNCTIONS

Symbol	Type	Function (In Detail)
A0-A12	Input Pin	Address Inputs: A0-A12 are sampled during the ACTIVE command (row-address A0-A12) and READ/WRITE command (column address A0-A9 (x16); A0-A9, A11 (x8); with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
BA0, BA1	Input Pin	Bank Select Address: BA0 and BA1 defines which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
$\overline{\text{CAS}}$	Input Pin	$\overline{\text{CAS}}$, in conjunction with the $\overline{\text{RAS}}$ and $\overline{\text{WE}}$, forms the device command. See the "Command Truth Table" for details on device commands.
CKE	Input Pin	The CKE input determines whether the CLK input is enabled. The next rising edge of the CLK signal will be valid when is CKE HIGH and invalid when LOW. When CKE is LOW, the device will be in either power-down mode, clock suspend mode, or self refresh mode. CKE is an asynchronous input.
CLK	Input Pin	CLK is the master clock input for this device. Except for CKE, all inputs to this device are acquired in synchronization with the rising edge of this pin.
$\overline{\text{CS}}$	Input Pin	The $\overline{\text{CS}}$ input determines whether command input is enabled within the device. Command input is enabled when $\overline{\text{CS}}$ is LOW, and disabled with $\overline{\text{CS}}$ is HIGH. The device remains in the previous state when $\overline{\text{CS}}$ is HIGH.
DQML, DQMH	Input Pin	DQML and DQMH control the lower and upper bytes of the I/O buffers. In read mode,DQML and DQMH control the output buffer. WhenDQML orDQMH is LOW, the corresponding buffer byte is enabled, and when HIGH, disabled. The outputs go to the HIGH impedance state whenDQML/DQMH is HIGH. This function corresponds to $\overline{\text{OE}}$ in conventional DRAMs. In write mode,DQML and DQMH control the input buffer. When DQML or DQMH is LOW, the corresponding buffer byte is enabled, and data can be written to the device. WhenDQML or DQMH is HIGH, input data is masked and cannot be written to the device. For IS42/45S16320B only.
DQM	Input Pin	For IS42S86400B only.
DQ_0-DQ_7 (x8) or DQ_0-DQ_{15} (x16)	Input/Output	Data on the Data Bus is latched on DQ pins during Write commands, and buffered for output after Read commands.
$\overline{\text{RAS}}$	Input Pin	$\overline{\text{RAS}}$, in conjunction with $\overline{\text{CAS}}$ and $\overline{\text{WE}}$, forms the device command. See the "Command Truth Table" item for details on device commands.
$\overline{\text{WE}}$	Input Pin	$\overline{\text{WE}}$, in conjunction with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$, forms the device command. See the "Command Truth Table" item for details on device commands.
V_{DDQ}	Power Supply Pin	V_{DDQ} is the output buffer power supply.
V_{DD}	Power Supply Pin	V_{DD} is the device internal power supply.
V_{SSQ}	Power Supply Pin	V_{SSQ} is the output buffer ground.
V_{SS}	Power Supply Pin	V_{SS} is the device internal ground.

GENERAL DESCRIPTION

READ

The READ command selects the bank from BA0, BA1 inputs and starts a burst read access to an active row. Inputs A0-A9 (x16); A0-A9, A11 (x8) provides the starting column location. When A10 is HIGH, this command functions as an AUTO PRECHARGE command. When the auto precharge is selected, the row being accessed will be precharged at the end of the READ burst. The row will remain open for subsequent accesses when AUTO PRECHARGE is not selected. DQ's read data is subject to the logic level on the DQM inputs two clocks earlier. When a given DQM signal was registered HIGH, the corresponding DQ's will be High-Z two clocks later. DQ's will provide valid data when the DQM signal was registered LOW.

WRITE

A burst write access to an active row is initiated with the WRITE command. BA0, BA1 inputs selects the bank, and the starting column location is provided by inputs A0-A9 (x16); A0-A9, A11 (x8). Whether or not AUTO-PRECHARGE is used is determined by A10.

The row being accessed will be precharged at the end of the WRITE burst, if AUTO PRECHARGE is selected. If AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses.

A memory array is written with corresponding input data on DQ's and DQM input logic level appearing at the same time. Data will be written to memory when DQM signal is LOW. When DQM is HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. BA0, BA1 can be used to select which bank is precharged or they are treated as "Don't Care". A10 determined whether one or all banks are precharged. After executing this command, the next command for the selected bank(s) is executed after passage of the period t_{RP}, which is the period required for bank precharging. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

AUTO PRECHARGE

The AUTO PRECHARGE function ensures that the precharge is initiated at the earliest valid stage within a burst. This function allows for individual-bank precharge without requiring an explicit command. A10 to enable the AUTO PRECHARGE function in conjunction with a specific READ or WRITE command. For each individual READ or WRITE command, auto precharge is either enabled or disabled. AUTO PRECHARGE does not apply except in full-page burst mode. Upon completion of the READ or WRITE burst, a precharge of the bank/row that is addressed is automatically performed.

AUTO REFRESH COMMAND

This command executes the AUTO REFRESH operation. The row address and bank to be refreshed are automatically generated during this operation. The stipulated period (t_{RC}) is required for a single refresh operation, and no other commands can be executed during this period. This command is executed at least 8192 times for every 64ms. During an AUTO REFRESH command, address bits are "Don't Care". This command corresponds to CBR Auto-refresh.

BURST TERMINATE

The BURST TERMINATE command forcibly terminates the burst read and write operations by truncating either fixed-length or full-page bursts and the most recently registered READ or WRITE command prior to the BURST TERMINATE.

COMMAND INHIBIT

COMMAND INHIBIT prevents new commands from being executed. Operations in progress are not affected, apart from whether the CLK signal is enabled

NO OPERATION

When $\overline{CS}$ is low, the NOP command prevents unwanted commands from being registered during idle or wait states.

LOAD MODE REGISTER

During the LOAD MODE REGISTER command the mode register is loaded from A0-A12. This command can only be issued when all banks are idle.

ACTIVE COMMAND

When the ACTIVE COMMAND is activated, BA0, BA1 inputs selects a bank to be accessed, and the address inputs on A0-A12 selects the row. Until a PRECHARGE command is issued to the bank, the row remains open for accesses.

COMMAND TRUTH TABLE

Function	CKE n – 1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA1	BA0	A10	A12, A11 A9 - A0
Device deselect (DESL)	H	×	H	×	×	×	×	×	×	×
No operation (NOP)	H	×	L	H	H	H	×	×	×	×
Burst stop (BST)	H	×	L	H	H	L	×	×	×	×
Read	H	×	L	H	L	H	V	V	L	V
Read with auto precharge	H	×	L	H	L	H	V	V	H	V
Write	H	×	L	H	L	L	V	V	L	V
Write with auto precharge	H	×	L	H	L	L	V	V	H	V
Bank activate (ACT)	H	×	L	L	H	H	V	V	V	V
Precharge select bank (PRE)	H	×	L	L	H	L	V	V	L	×
Precharge all banks (PALL)	H	×	L	L	H	L	×	×	H	×
CBR Auto-Refresh (REF)	H	H	L	L	L	H	×	×	×	×
Self-Refresh (SELF)	H	L	L	L	L	H	×	×	×	×
Mode register set (MRS)	H	×	L	L	L	L	L	L	L	V

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data.

DQM TRUTH TABLE

Function	CKE n-1	CKE n	DQMH	DQML
Data write / output enable	H	×	L	L
Data mask / output disable	H	×	H	H
Upper byte write enable / output enable	H	×	L	×
Lower byte write enable / output enable	H	×	×	L
Upper byte write inhibit / output disable	H	×	H	×
Lower byte write inhibit / output disable	H	×	×	H

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data.

CKE TRUTH TABLE

Current State /Function	CKE n – 1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Activating Clock suspend mode entry	H	L	×	×	×	×	×
Any Clock suspend mode	L	L	×	×	×	×	×
Clock suspend mode exit	L	H	×	×	×	×	×
Auto refresh command Idle (REF)	H	H	L	L	L	H	×
Self refresh entry Idle (SELF)	H	L	L	L	L	H	×
Power down entry Idle	H	L	×	×	×	×	×
Self refresh exit	L	H	L	H	H	H	×
	L	H	H	×	×	×	×
Power down exit	L	H	×	×	×	×	×

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data.

FUNCTIONAL TRUTH TABLE

Current State	CS	RAS	CAS	WE	Address	Command	Action
Idle	H	X	X	X	X	DESL	Nop or Power Down(2)
	L	H	H	H	X	NOP	Nop or Power Down(2)
	L	H	H	L	X	BST	Nop or Power Down
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL (3)
	L	H	L	L	A, CA, A10	WRIT/ WRITA	ILLEGAL(3)
	L	L	H	H	BA, RA	ACT	Row activating
	L	L	H	L	BA, A10	PRE/PALL	Nop
	L	L	L	H	X	REF/SELF	Auto refresh or Self-refresh(4)
	L	L	L	L	OC, BA1=L	MRS	Mode register set
Row Active	H	X	X	X	X	DESL	Nop
	L	H	H	H	X	NOP	Nop
	L	H	H	L	X	BST	Nop
	L	H	L	H	BA, CA, A10	READ/READA	Begin read (5)
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	Begin write (5)
	L	L	H	H	BA, RA	ACT	ILLEGAL (3)
	L	L	H	L	BA, A10	PRE/PALL	Precharge Precharge all banks(6)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Read	H	X	X	X	X	DESL	Continue burst to end to Row active
	L	H	H	H	X	NOP	Continue burst to end Row Row active
	L	H	H	L	X	BST	Burst stop, Row active
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, begin new read (7)
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, begin write (7,8)
	L	L	H	H	BA, RA	ACT	ILLEGAL (3)
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst Precharging
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Write	H	X	X	X	X	DESL	Continue burst to end Write recovering
	L	H	H	H	X	NOP	Continue burst to end Write recovering
	L	H	H	L	X	BST	Burst stop, Row active
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, start read : Determine AP (7,8)
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, new write : Determine AP (7)
	L	L	H	H	BA, RA	RA ACT	ILLEGAL (3)
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst Precharging (9)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data, BA= Bank Address, CA+Column Address, RA=Row Address, OC= Op-Code

FUNCTIONAL TRUTH TABLE Continued:

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
Read with auto Precharging	H	×	×	×	×	DESL	Continue burst to end, Precharge
	L	H	H	H	x	NOP	Continue burst to end, Precharge
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL (11)
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL (11)
	L	L	H	H	BA, RA	ACT	ILLEGAL (3)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (11)
	L	L	L	H	×	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Write with Auto Precharge	H	×	×	×	×	DESL	Continue burst to end, Write recovering with auto precharge
	L	H	H	H	×	NOP	Continue burst to end, Write recovering with auto precharge
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL(11)
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL (11)
	L	L	H	H	BA, RA	ACT	ILLEGAL (3,11)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (3,11)
	L	L	L	H	×	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Precharging	H	×	×	×	×	DESL	Nop, Enter idle after tRP
	L	H	H	H	×	NOP	Nop, Enter idle after tRP
	L	H	H	L	×	BST	Nop, Enter idle after tRP
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL (3)
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL (3)
	L	L	H	H	BA, RA	ACT	ILLEGAL(3)
	L	L	H	L	BA, A10	PRE/PALL	Nop Enter idle after tRP
	L	L	L	H	×	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Row Activating	H	×	×	×	×	DESL	Nop, Enter bank active after tRCD
	L	H	H	H	×	NOP	Nop, Enter bank active after tRCD
	L	H	H	L	×	BST	Nop, Enter bank active after tRCD
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL (3)
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL (3)
	L	L	H	H	BA, RA	ACT	ILLEGAL (3,9)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (3)
	L	L	L	H	×	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data, BA= Bank Address, CA+Column Address, RA=Row Address, OC= Op-Code

FUNCTIONAL TRUTH TABLE Continued:

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
Write Recovering	H	×	×	×	×	DESL	Nop, Enter row active after tDPL
	L	H	H	H	×	NOP	Nop, Enter row active after tDPL
	L	H	H	L	×	BST	Nop, Enter row active after tDPL
	L	H	L	H	BA, CA, A10	READ/READA	Begin read (8)
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	Begin new write
	L	L	H	H	BA, RA	ACT	ILLEGAL (3)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (3)
	L	L	L	H	×	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Write Recovering with Auto Precharge	H	×	×	×	×	DESL	Nop, Enter precharge after tDPL
	L	H	H	H	×	NOP	Nop, Enter precharge after tDPL
	L	H	H	L	×	BST	Nop, Enter row active after tDPL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL(3,8,11)
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL (3,11)
	L	L	H	H	BA, RA	ACT	ILLEGAL (3,11)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (3,11)
	L	L	L	H	×	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Refresh	H	×	×	×	×	DESL	Nop, Enter idle after tRC
	L	H	H	×	×	NOP/BST	Nop, Enter idle after tRC
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL
	L	L	L	H	×	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Mode Register Accessing	H	×	×	×	×	DESL	Nop, Enter idle after 2 clocks
	L	H	H	H	×	NOP	Nop, Enter idle after 2 clocks
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	×	BA, CA, A10	READ/WRITE	ILLEGAL
	L	L	×	×	BA, RA	ACT/PRE/PALL REF/MRS	ILLEGAL

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data, BA= Bank Address, CA+Column Address, RA=Row Address, OC= Op-Code

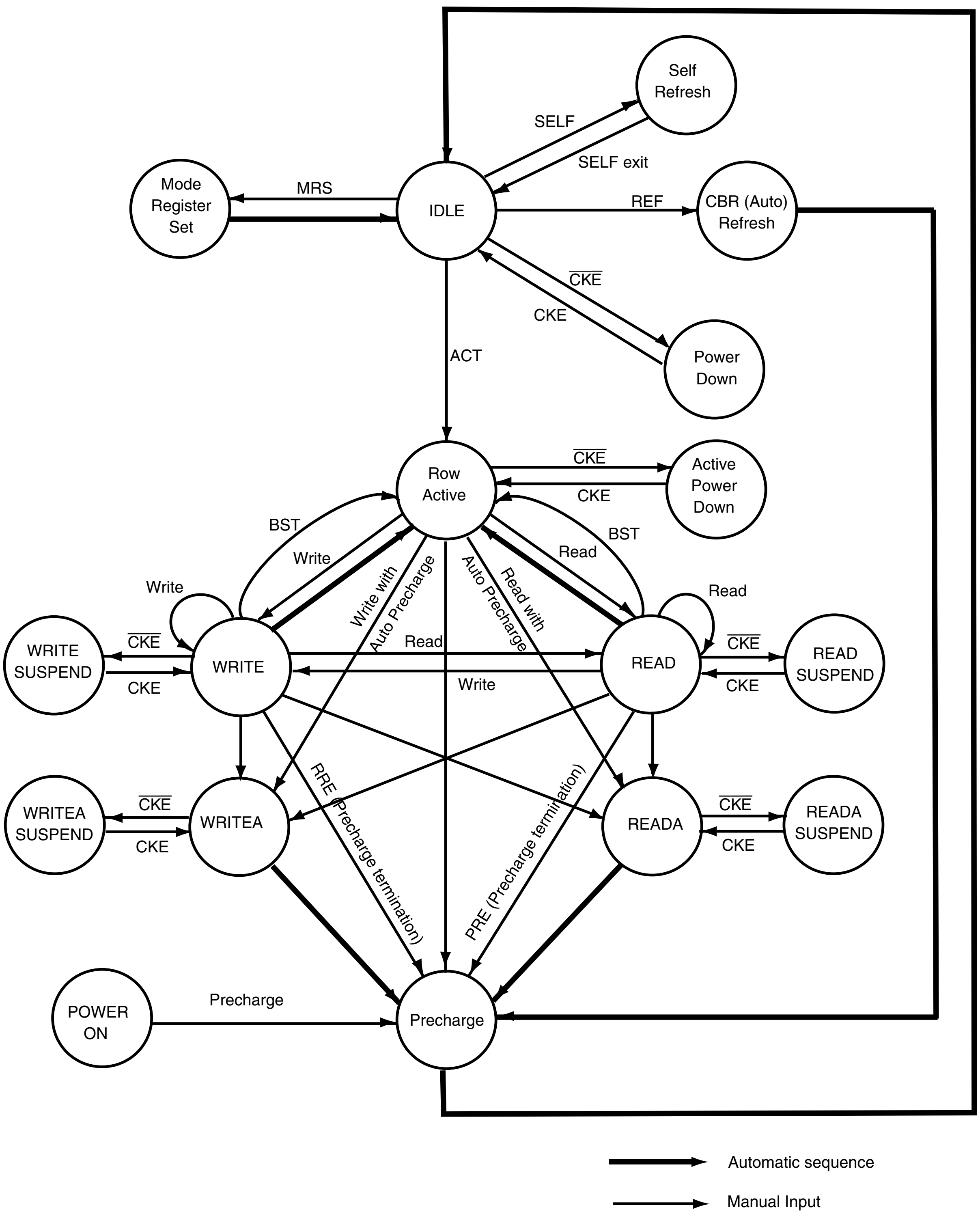
Notes:
1. All entries assume that CKE is active (CKEn-1=CKEn=H).
2. If both banks are idle, and CKE is inactive (Low), the device will enter Power Down mode. All input buffers except CKE will be disabled.
3. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
4. If both banks are idle, and CKE is inactive (Low), the device will enter Self-Refresh mode. All input buffers except CKE will be disabled.
5. Illegal if tRCD is not satisfied.
6. Illegal if tRAS is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
9. Must mask preceding data which don't satisfy tDPL.
10. Illegal if tRRD is not satisfied.
11. Illegal for single bank, but legal for other banks.

CKE RELATED COMMAND TRUTH TABLE[1]

Current State	Operation	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Self-Refresh (S.R.)	INVALID, CLK (n - 1) would exit S.R.	H	X	X	X	X	X	X
	Self-Refresh Recovery[2]	L	H	H	X	X	X	X
	Self-Refresh Recovery[2]	L	H	L	H	H	X	X
	Illegal	L	H	L	H	L	X	X
	Illegal	L	H	L	L	X	X	X
	Maintain S.R.	L	L	X	X	X	X	X
Self-Refresh Recovery	Idle After t_{RC}	H	H	H	X	X	X	X
	Idle After t_{RC}	H	H	L	H	H	X	X
	Illegal	H	H	L	H	L	X	X
	Illegal	H	H	L	L	X	X	X
	Begin clock suspend next cycle[5]	H	L	H	X	X	X	X
	Begin clock suspend next cycle[5]	H	L	L	H	H	X	X
	Illegal	H	L	L	H	L	X	X
	Illegal	H	L	L	L	X	X	X
	Exit clock suspend next cycle[2]	L	H	X	X	X	X	X
	Maintain clock suspend	L	L	X	X	X	X	X
Power-Down (P.D.)	INVALID, CLK (n - 1) would exit P.D.	H	X	X	X	X	X	—
	EXIT P.D. --> Idle[2]	L	H	X	X	X	X	X
	Maintain power down mode	L	L	X	X	X	X	X
All Banks Idle	Refer to operations in Operative Command Table	H	H	H	X	X	X	—
	Refer to operations in Operative Command Table	H	H	L	H	X	X	—
	Refer to operations in Operative Command Table	H	H	L	L	H	X	—
	Auto-Refresh	H	H	L	L	L	H	X
	Refer to operations in Operative Command Table	H	H	L	L	L	L	Op - Code
	Refer to operations in Operative Command Table	H	L	H	X	X	X	—
	Refer to operations in Operative Command Table	H	L	L	H	X	X	—
	Refer to operations in Operative Command Table	H	L	L	L	H	X	—
	Self-Refresh[3]	H	L	L	L	L	H	X
	Refer to operations in Operative Command Table	H	L	L	L	L	L	Op - Code
	Power-Down[3]	L	X	X	X	X	X	X
Any state other than listed above	Refer to operations in Operative Command Table	H	H	X	X	X	X	X
	Begin clock suspend next cycle[4]	H	L	X	X	X	X	X
	Exit clock suspend next cycle	L	H	X	X	X	X	X
	Maintain clock suspend	L	L	X	X	X	X	X

Notes:
1. H : High level, L : low level, X : High or low level (Don't care).
2. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
3. Power down and Self refresh can be entered only from the both banks idle state.
4. Must be legal command as defined in Operative Command Table.
5. Illegal if t_{XSR} is not satisfied.

STATE DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters		Rating	Unit
$V_{DD\ MAX}$	Maximum Supply Voltage		–1.0 to +4.6	V
$V_{DDQ\ MAX}$	Maximum Supply Voltage for Output Buffer		–1.0 to +4.6	V
V_{IN}	Input Voltage		–1.0 to V_{DD} + 0.5	V
V_{OUT}	Output Voltage		–1.0 to V_{DDQ} + 0.5	V
$P_{D\ MAX}$	Allowable Power Dissipation		1	W
I_{CS}	Output Shorted Current		50	mA
T_{OPR}	Operating Temperature	Com. Ind. A1 A2	0 to +70 -40 to +85 -40 to +85 -40 to +105	°C
T_{STG}	Storage Temperature		–65 to +150	°C

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are referenced to Vss.

DC RECOMMENDED OPERATING CONDITIONS

(T_A = 0°C to +70°C for Commercial grade. T_A = -40°C to +85°C for Industrial and A1 grade. T_A = -40°C to +105°C for A2 grade)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
V_{DDQ}	I/O Supply Voltage	3.0	3.3	3.6	V
V_{IH}(1)	Input High Voltage	2.0	—	V_{DDQ} + 0.3	V
V_{IL}(2)	Input Low Voltage	-0.3	—	+0.8	V

Note:
1. V_{IH} (overshoot): V_{IH} (max) = V_{DDQ} +1.2V (PULSE WIDTH $\leq$ 3ns).
2. V_{IL} (undershoot): V_{IH} (min) = -1.2V (PULSE WIDTH $\leq$ 3ns).
3. All voltages are referenced to Vss.

CAPACITANCE CHARACTERISTICS (At T_A = 0 to +25°C, V_{DD} = V_{DDQ} = 3.3 ± 0.3V)

Symbol	Parameter	Min.	Max.	Unit
C_{IN1}	Input Capacitance: CLK	2.5	3.5	pF
C_{IN2}	Input Capacitance:All other input pins	2.5	3.8	pF
$C_{I/O}$	Data Input/Output Capacitance: DQS	4.0	6.0	pF

DC ELECTRICAL CHARACTERISTICS 1 (Recommended Operation Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	-6	-7	-75E	Unit
I_{DD1} (1)	Operating Current	One bank active, CL = 3, BL = 1, $t_{CLK} = t_{CLK}$ (min), $t_{RC} = t_{RC}$ (min)	160	140	160	mA
I_{DD2P}	Precharge Standby Current (In Power-Down Mode)	CKE ≤ V_{IL} (MAX), t_{CK} = 15ns	4	4	4	mA
I_{DD2PS}	Precharge Standby Current (In Power-Down Mode)	CKE ≤ V_{IL} (MAX), CLK ≤ V_{IL} (MAX)	4	4	4	mA
I_{DD2N} (2)	Precharge Standby Current (In Non Power-Down Mode)	$\overline{CS}$ ≥ Vcc - 0.2V, CKE ≥ V_{IH} (MIN) t_{CK} = 15ns	35	35	35	mA
I_{DD2NS}	Precharge Standby Current (In Non Power-Down Mode)	$\overline{CS}$ ≥ Vcc - 0.2V, CKE ≥ V_{IH} (MIN) or CKE ≤ V_{IL} (MAX), All inputs stable	20	20	20	mA
I_{DD3P}	Active Standby Current (Power-Down Mode)	CKE ≤ V_{IL} (MAX), t_{CK} = 15ns	6	6	6	mA
I_{DD3PS}	Active Standby Current (Power-Down Mode)	CKE ≤ V_{IL} (MAX), CLK ≤ V_{IL} (MAX)	6	6	6	mA
I_{DD3N} (2)	Active Standby Current (In Non Power-Down Mode)	$\overline{CS}$ ≥ Vcc - 0.2V, CKE ≥ V_{IH} (MIN) t_{CK} = 15ns	55	55	55	mA
I_{DD3NS}	Active Standby Current (In Non Power-Down Mode)	$\overline{CS}$ ≥ Vcc - 0.2V, CKE ≥ V_{IH} (MIN) or CKE ≤ V_{IL} (MAX), All inputs stable	30	30	30	mA
I_{DD4}	Operating Current	All banks active, BL = 4, CL = 3, $t_{CK} = t_{CK}$ (min)	180	150	180	mA
I_{DD5}	Auto-Refresh Current	$t_{RC} = t_{RC}$ (min), $t_{CLK} = t_{CLK}$ (min)	350	300	350	mA
I_{DD6}	Self-Refresh Current	CKE ≤ 0.2V	6	6	6	mA

Notes:

1. I_{DD} (MAX) is specified at the output open condition.
2. Input signals are changed one time during 30ns.

DC ELECTRICAL CHARACTERISTICS 2 (Recommended Operation Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{IL}	Input Leakage Current	0V ≤ Vin ≤ Vcc, with pins other than the tested pin at 0V	-5	5	µA
I_{OL}	Output Leakage Current	Output is disabled, 0V ≤ Vout ≤ Vcc,	-5	5	µA
V_{OH}	Output High Voltage Level	I_{OH} = -2mA	2.4	—	V
V_{OL}	Output Low Voltage Level	I_{OL} = 2mA	—	0.4	V

AC ELECTRICAL CHARACTERISTICS (1,2,3)

Symbol	Parameter		-6 Min.	-6 Max.	-7 Min.	-7 Max.	-75E Min.	-75E Max.	Units
t_{CK3}	Clock Cycle Time	$\overline{CAS}$ Latency = 3	6	—	7	—	—	—	ns
t_{CK2}		$\overline{CAS}$ Latency = 2	10	—	10	—	7.5	—	ns
t_{AC3}	Access Time From CLK	$\overline{CAS}$ Latency = 3	—	5.4	—	5.4	—	—	ns
t_{AC2}		$\overline{CAS}$ Latency = 2	—	6	—	6	—	5.5	ns
t_{CH}	CLK HIGH Level Width		2.5	—	2.5	—	2.5	—	ns
t_{CL}	CLK LOW Level Width		2.5	—	2.5	—	2.5	—	ns
t_{OH3}	Output Data Hold Time	$\overline{CAS}$ Latency = 3	2.7	—	2.7	—	2.7	—	ns
t_{OH2}		$\overline{CAS}$ Latency = 2	2.7	—	2.7	—	2.7	—	ns
t_{LZ}	Output LOW Impedance Time		0	—	0	—	0	—	ns
t_{HZ3}	Output HIGH Impedance Time		2.7	5.4	2.7	5.4	—	—	ns
t_{HZ2}	Output HIGH Impedance Time		2.7	6	2.7	6	2.7	5.5	ns
t_{DS}	Input Data Setup Time(2)		1.5	—	1.5	—	1.5	—	ns
t_{DH}	Input Data Hold Time(2)		0.8	—	0.8	—	0.8	—	ns
t_{AS}	Address Setup Time(2)		1.5	—	1.5	—	1.5	—	ns
t_{AH}	Address Hold Time(2)		0.8	—	0.8	—	0.8	—	ns
t_{CKS}	CKE Setup Time(2)		1.5	—	1.5	—	1.5	—	ns
t_{CKH}	CKE Hold Time(2)		0.8	—	0.8	—	0.8	—	ns
t_{CMS}	Command Setup Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)(2)		1.5	—	1.5	—	1.5	—	ns
t_{CMH}	Command Hold Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)(2)		0.8	—	0.8	—	0.8	—	ns
t_{RC}	Command Period (REF to REF / ACT to ACT)		60	—	70	—	60	—	ns
t_{RAS}	Command Period (ACT to PRE)		42	100K	49	100K	45	100K	ns
t_{RP}	Command Period (PRE to ACT)		18	—	20	—	15	—	ns
t_{RCD}	Active Command To Read / Write Command Delay Time		18	—	20	—	15	—	ns
t_{RRD}	Command Period (ACT [0] to ACT[1])		12	—	14	—	15	—	ns
t_{DPL}	Input Data To Precharge Command Delay time		12	—	14	—	15	—	ns
t_{DAL}	Input Data To Active / Refresh Command Delay time (During Auto-Precharge)		30	—	35	—	30	—	ns
t_{MRD}	Mode Register Program Time		12	—	14	—	15	—	ns
t_{DDE}	Power Down Exit Setup Time		6	—	7	—	7.5	—	ns
t_{XSR}	Exit Self-Refresh to Active Time(4)		66	—	77	—	67.5	—	ns
t_{T}	Transition Time		0.3	1.2	0.3	1.2	0.3	1.2	ns
t_{REF}	Refresh Cycle Time (8192)								
		$T_A \leq 70^oC$ Com., Ind., A1, A2	—	64	—	64	—	64	ms
		$T_A \leq 85^oC$ Ind., A1, A2	—	64	—	64	—	64	ms
		$T_A > 85^oC$ A2	—	—	—	16	—	—	ms

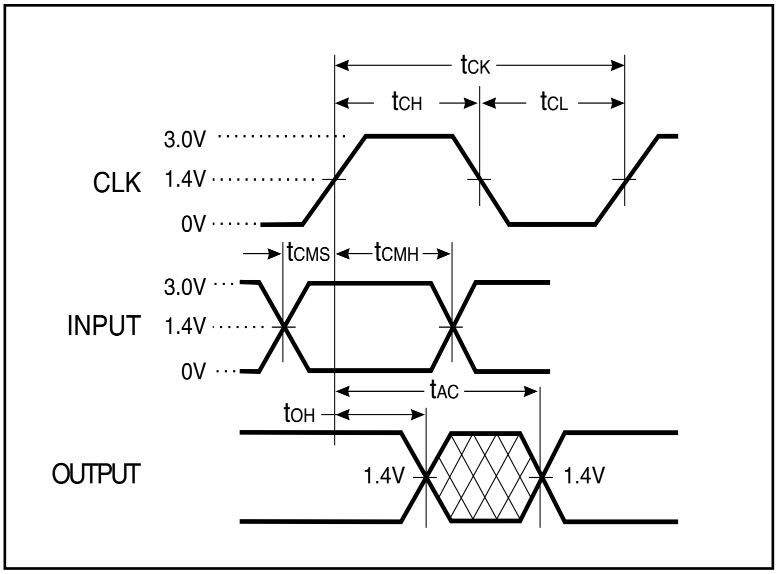
Notes:
1. The power-on sequence must be executed before starting memory operation.
2. Measured with t_T = 1 ns. If clock rising time is longer than 1ns, (t_T /2 - 0.5) ns should be added to the parameter.
3. The reference level is 1.4V when measuring input signal timing. Rise and fall times are measured between V_{IH}(min.) and V_{IL} (max).
4. Self-Refresh Mode is not supported for A2 grade with $T_A > +85^oC$.

OPERATING FREQUENCY / LATENCY RELATIONSHIPS

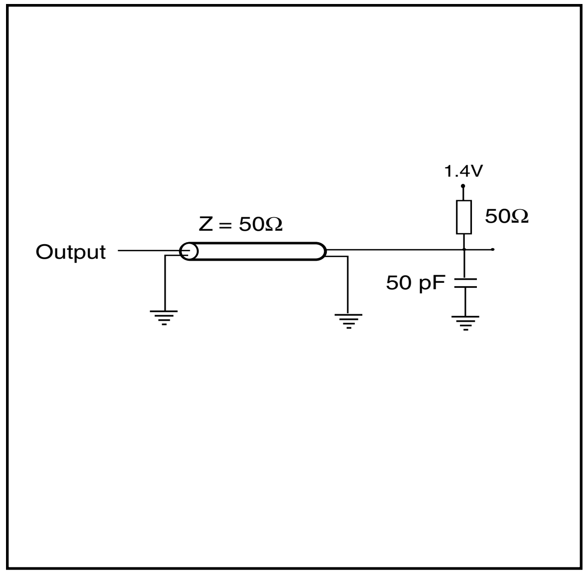
SYMBOL	PARAMETER		-6	-7	-75E	UNITS
—	Clock Cycle Time	$\overline{CAS}$ Latency = 3	6	7	—	ns
		$\overline{CAS}$ Latency = 2	10	10	7.5	ns
—	Operating Frequency	$\overline{CAS}$ Latency = 3	166	143	—	MHz
		$\overline{CAS}$ Latency = 2	100	100	133	MHz
t_{CAC}	$\overline{CAS}$ Latency	$\overline{CAS}$ Latency = 3	3	3	—	cycle
		$\overline{CAS}$ Latency = 2	2	2	2	cycle
t_{RCD}	Active Command To Read/Write Command Delay Time	$\overline{CAS}$ Latency = 3	3	3	—	cycle
		$\overline{CAS}$ Latency = 2	2	2	2	cycle
t_{RAC}	$\overline{RAS}$ Latency (t_{RCD} + t_{CAC})	$\overline{CAS}$ Latency = 3	6	6	—	cycle
		$\overline{CAS}$ Latency = 2	4	4	4	cycle
t_{RC}	Command Period (REF to REF / ACT to ACT)	$\overline{CAS}$ Latency = 3	10	10	—	cycle
		$\overline{CAS}$ Latency = 2	6	7	8	cycle
t_{RAS}	Command Period (ACT to PRE)	$\overline{CAS}$ Latency = 3	7	7	—	cycle
		$\overline{CAS}$ Latency = 2	5	5	6	cycle
t_{RP}	Command Period (PRE to ACT)	$\overline{CAS}$ Latency = 3	3	3	—	cycle
		$\overline{CAS}$ Latency = 2	2	2	2	cycle
t_{RRD}	Command Period (ACT[0] to ACT [1])		2	2	2	cycle
t_{CCD}	Column Command Delay Time (READ, READA, WRIT, WRITA)		1	1	1	cycle
t_{DPL}	Input Data To Precharge Command Delay Time		2	2	2	cycle
t_{DAL}	Input Data To Active/Refresh Command Delay Time	$\overline{CAS}$ Latency = 3	5	5	—	cycle
	(During Auto-Precharge)	$\overline{CAS}$ Latency = 2	4	4	4	cycle
t_{RBD}	Burst Stop Command To Output in HIGH-Z Delay Time	$\overline{CAS}$ Latency = 3	3	3	—	cycle
	(Read)	$\overline{CAS}$ Latency = 2	2	2	2	cycle
t_{WBD}	Burst Stop Command To Input in Invalid Delay Time (Write)		0	0	0	cycle
t_{RQL}	Precharge Command To Output in HIGH-Z Delay Time	$\overline{CAS}$ Latency = 3	3	3	—	cycle
	(Read)	$\overline{CAS}$ Latency = 2	2	2	2	cycle
t_{WDL}	Precharge Command To Input in Invalid Delay Time (Write)		0	0	0	cycle
t_{PQL}	Last Output To Auto-Precharge Start Time (Read)	$\overline{CAS}$ Latency = 3	-2	-2	—	cycle
		$\overline{CAS}$ Latency = 2	-1	-1	-1	cycle
t_{QMD}	DQM To Output Delay Time (Read)		2	2	2	cycle
t_{DMD}	DQM To Input Delay Time (Write)		0	0	0	cycle
t_{MRD}	Mode Register Set To Command Delay Time		2	2	2	cycle

AC TEST CONDITIONS

Input Load



Output Load



AC TEST CONDITIONS

Parameter	Rating
AC Input Levels	0V to 3.0V
Input Rise and Fall Times	1 ns
Input Timing Reference Level	1.4V
Output Timing Measurement Reference Level	1.4V

FUNCTIONAL DESCRIPTION

The 512Mb SDRAMs are quad-bank DRAMs which operate at 3.3V and include a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 134,217,728-bit banks is organized as 8,192 rows by 1024 columns by 16 bits or 8192 rows by 2048 columns by 8bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0-A12 select the row). The address bits A0-A9 (x16); A0-A9, A11 (x8) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

SDRAMs must be powered up and initialized in a predefined manner.

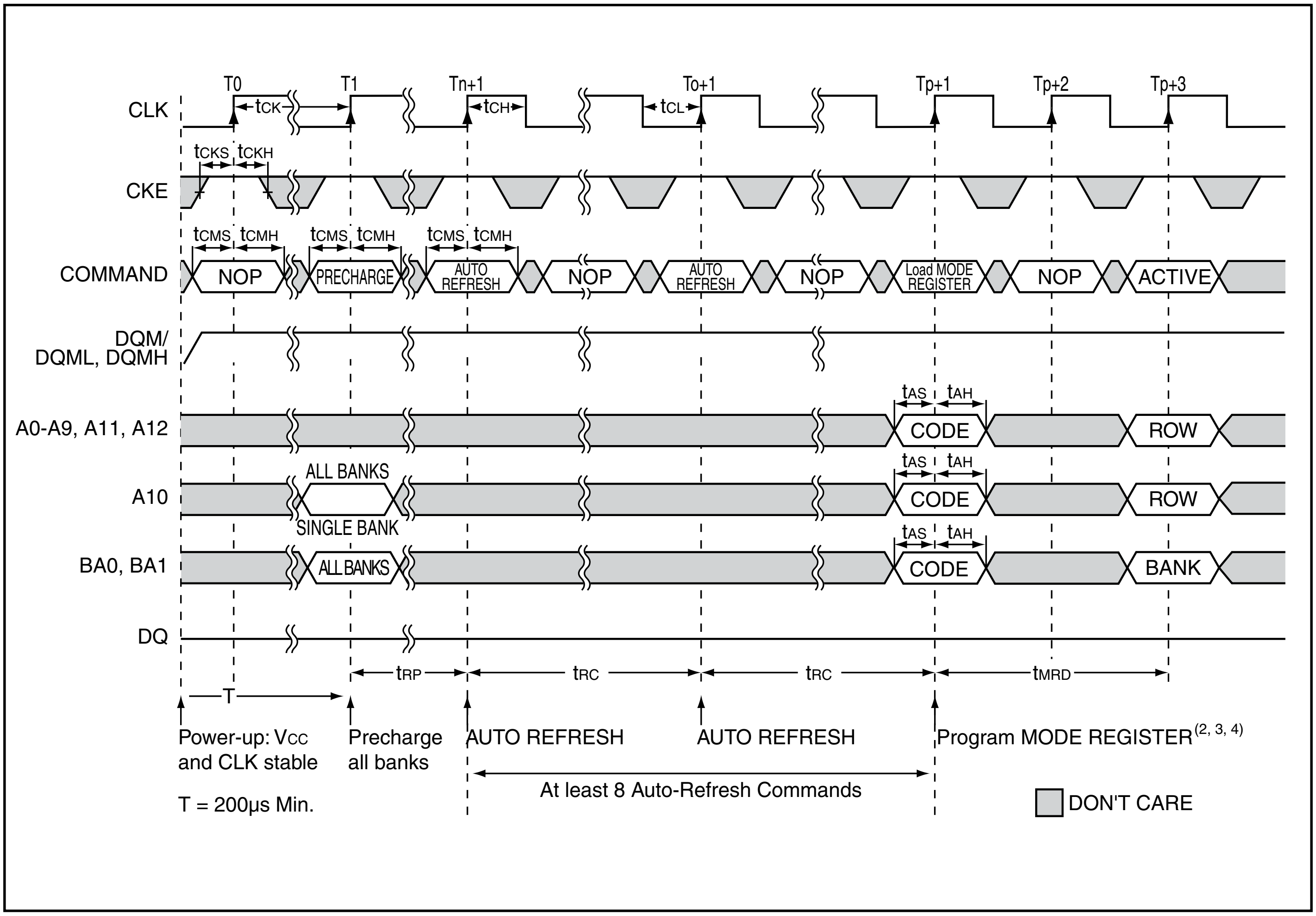
The 512Mb SDRAM is initialized after the power is applied to V_{DD} and V_{DDQ} (simultaneously) and the clock is stable with DQM High and CKE High.

A 100µs delay is required prior to issuing any command other than a COMMAND INHIBIT or a NOP. The COMMAND INHIBIT or NOP may be applied during the 100us period and should continue at least through the end of the period.

With at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied once the 100µs delay has been satisfied. All banks must be precharged. This will leave all banks in an idle state after which at least eight AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is then ready for mode register programming.

The mode register should be loaded prior to applying any operational command because it will power up in an unknown state.

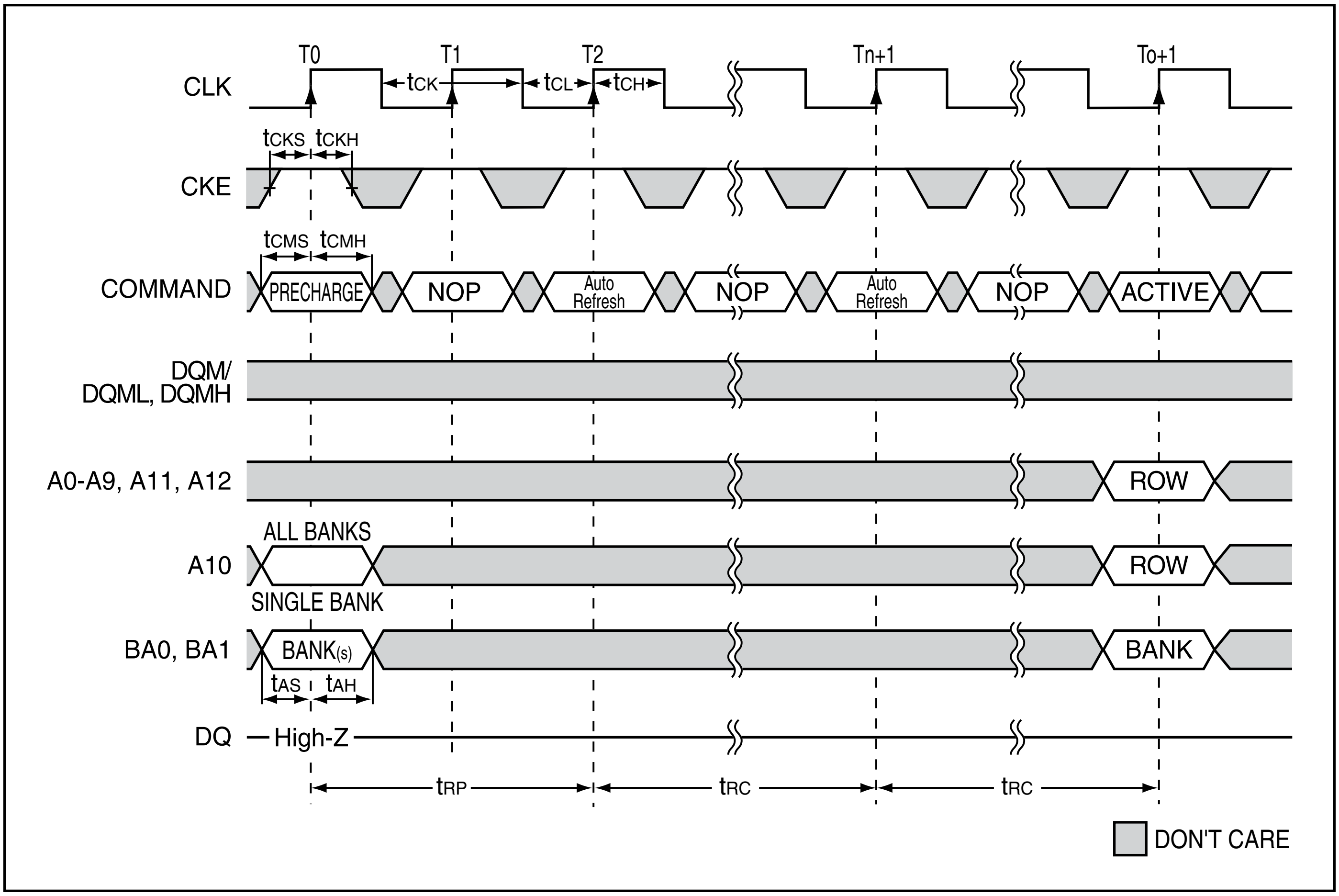
INITIALIZE AND LOAD MODE REGISTER(1)



Notes:

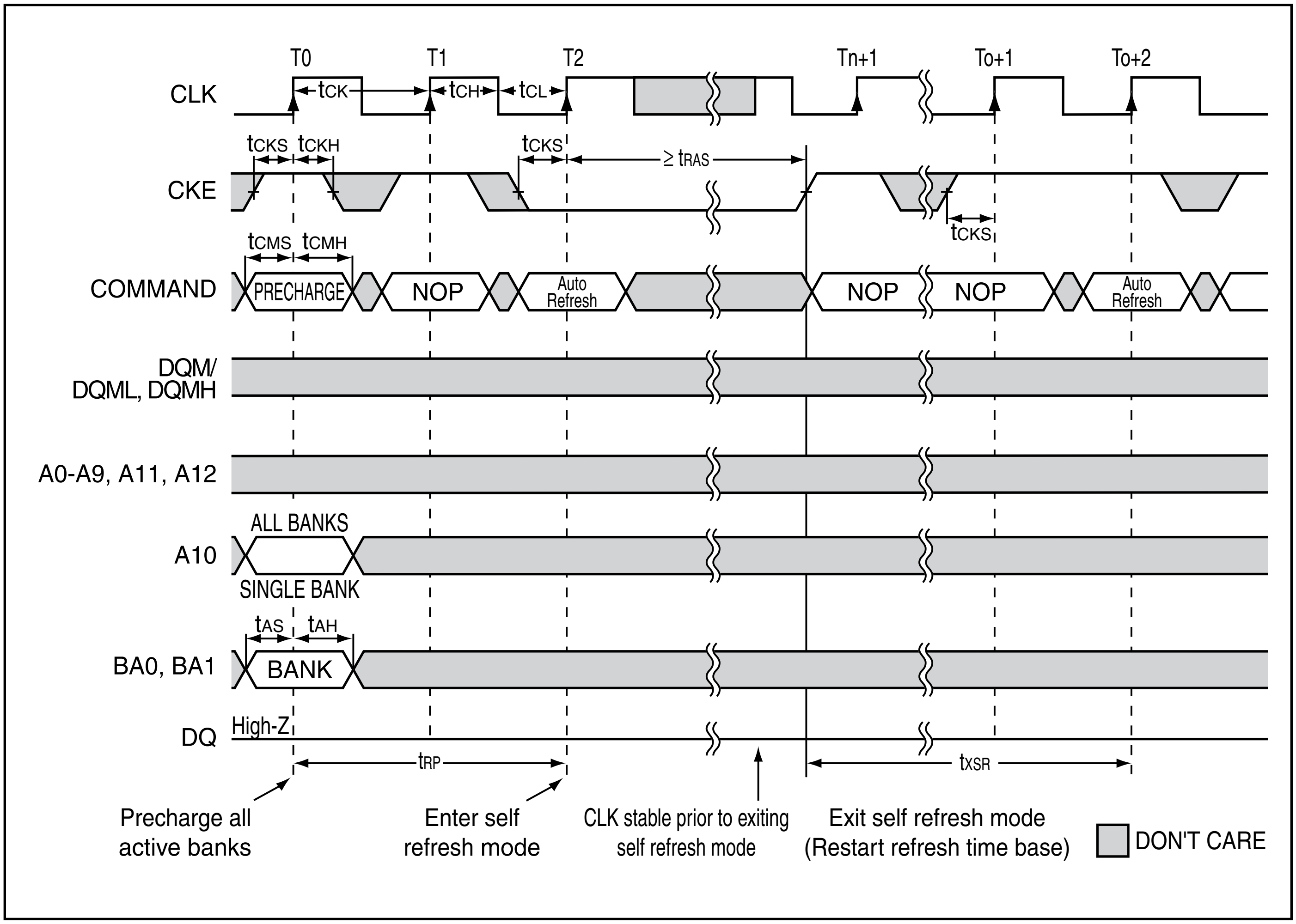
1. If $\overline{CS}$ is High at clock High time, all commands applied are NOP.
2. The Mode register may be loaded prior to the Auto-Refresh cycles if desired.
3. JEDEC and PC100 specify three clocks.
4. Outputs are guaranteed High-Z after the command is issued.

AUTO-REFRESH CYCLE



Notes:
1. $\overline{CAS}$ latency = 2, 3

SELF-REFRESH CYCLE



Note:
1. Self-Refresh Mode is not supported for A2 grade with T_A > +85°C.

REGISTER DEFINITION

Mode Register

The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in MODE REGISTER DEFINITION.

The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0-M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4- M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the WRITE burst mode, and M10, M11, and M12 are reserved for future use.

The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

MODE REGISTER DEFINITION

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Bus (Ax)
Reserved[(1)]					Write Burst Mode	Operating Mode		Latency Mode			Burst Type	Burst Length			Mode Register (Mx)

Burst Length

M2	M1	M0	M3=0	M3=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

Burst Type

M3	Type
0	Sequential
1	Interleaved

Latency Mode

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Operating Mode

M8	M7	M6-M0	Mode
0	0	Defined	Standard Operation
—	—	—	All Other States Reserved

Write Burst Mode

M9	Mode
0	Programmed Burst Length
1	Single Location Access

1. To ensure compatibility with future devices, should program BA1, BA0, A12, A11, A10 = "0"

BURST LENGTH

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in MODE REGISTER DEFINITION. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4 or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A9 (x16) or A1-A9, A11 (x8) when the burst length is set to two; by A2-A9 (x16) or A1-A9, A11 (x8) when the burst length is set to four; and by A3-A9 (x16) or A1-A9, A11 (x8) when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in BURST DEFINITION table.

BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
			A 0		
2			0	0-1	0-1
			1	1-0	1-0
		A 1	**A 0**		
		0	0	0-1-2-3	0-1-2-3
4		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
	A 2	**A 1**	**A 0**		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
8	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0-A9 (x16) n = A0-A9, A11 (x8) (location 0-y)			Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... …Cn - 1, Cn…	Not Supported