Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

IS42S32400E

4M x 32
128Mb SYNCHRONOUS DRAM

PRELIMINARY INFORMATION
AUGUST 2008

FEATURES

- Clock frequency: 166, 143 MHz
- Fully synchronous; all signals referenced to a positive clock edge
- Internal bank for hiding row access/precharge
- Power supply

	V_{DD}	V_{DDQ}
IS42S32400E	3.3V	3.3V

- LVTTL interface
- Programmable burst length
  – (1, 2, 4, 8, full page)
- Programmable burst sequence: Sequential/Interleave
- Auto Refresh (CBR)
- Self Refresh
- 4096 refresh cycles every 64 ms
- Random column address every clock cycle
- Programmable $\overline{CAS}$ latency (2, 3 clocks)
- Burst read/write and burst read/single write operations capability
- Burst termination by burst stop and precharge command
- Available in Industrial Temperature
- Available in 86-pin TSOP-II and 90-ball FBGA
- Available in Lead-free

OVERVIEW

ISSI's 128Mb Synchronous DRAM achieves high-speed data transfer using pipeline architecture. All inputs and outputs signals refer to the rising edge of the clock input. The 128Mb SDRAM is organized in 1Meg x 32 bit x 4 Banks.

KEY TIMING PARAMETERS

Parameter	-6	-7	Unit
Clk Cycle Time			
$\overline{CAS}$ Latency = 3	6	7	ns
$\overline{CAS}$ Latency = 2	8	10	ns
Clk Frequency			
$\overline{CAS}$ Latency = 3	166	143	Mhz
$\overline{CAS}$ Latency = 2	125	100	Mhz
Access Time from Clock			
$\overline{CAS}$ Latency = 3	5.4	5.4	ns
$\overline{CAS}$ Latency = 2	6.5	6.5	ns

DEVICE OVERVIEW

The 128Mb SDRAM is a high speed CMOS, dynamic random-access memory designed to operate in 3.3V V_{DD} and 3.3V V_{DDQ} memory systems containing 134,217,728 bits. Internally configured as a quad-bank DRAM with a synchronous interface. Each 33,554,432-bit bank is organized as 4,096 rows by 256 columns by 32 bits.

The 128Mb SDRAM includes an AUTO REFRESH MODE, and a power-saving, power-down mode. All signals are registered on the positive edge of the clock signal, CLK. All inputs and outputs are LVTTL compatible.

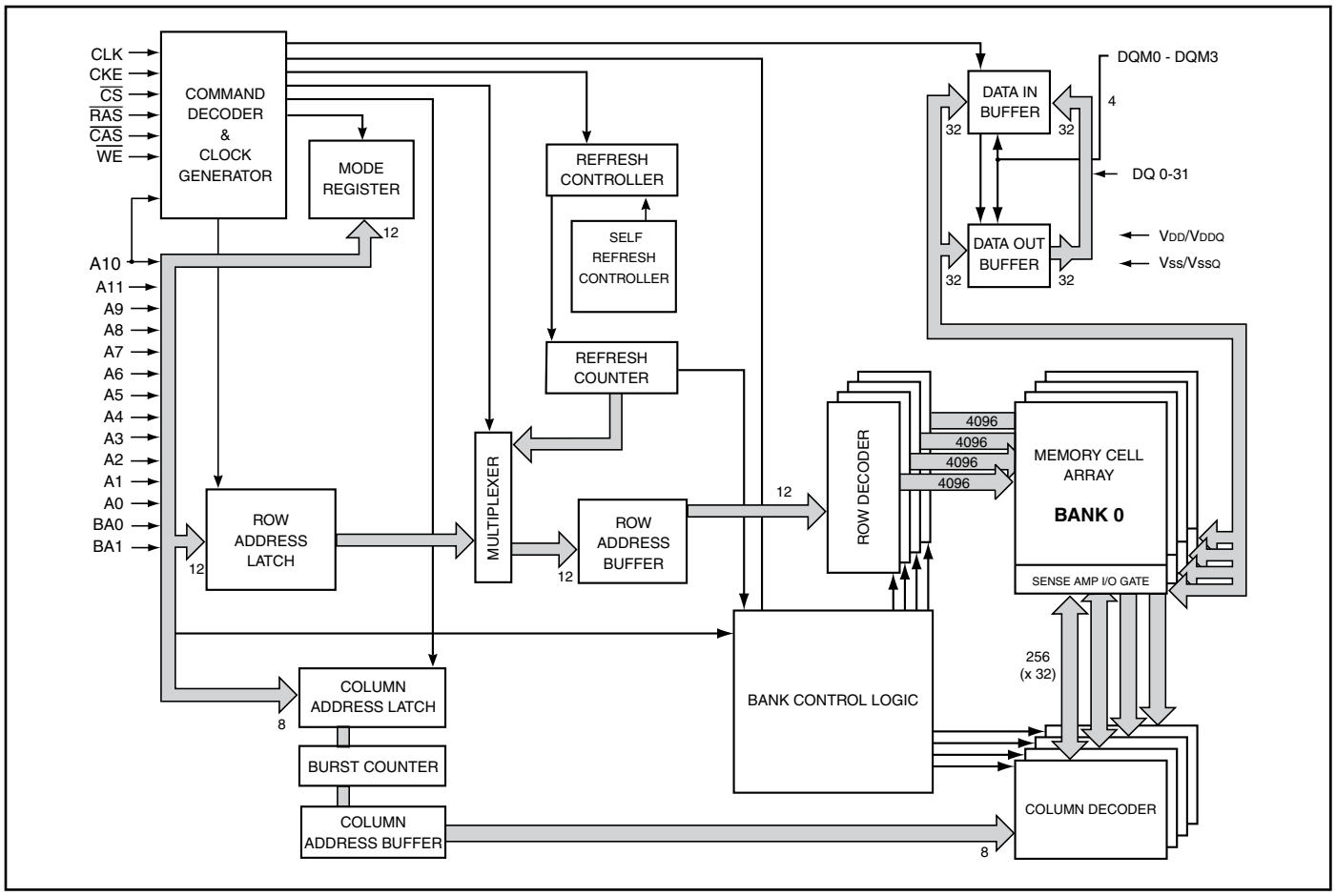
The 128Mb SDRAM has the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time and the capability to randomly change column addresses on each clock cycle during burst access.

A self-timed row precharge initiated at the end of the burst sequence is available with the AUTO PRECHARGE function enabled. Precharge one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

SDRAM read and write accesses are burst oriented starting at a selected location and continuing for a programmed number of locations in a programmed sequence. The registration of an ACTIVE command begins accesses, followed by a READ or WRITE command. The ACTIVE command in conjunction with address bits registered are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11 select the row). The READ or WRITE commands in conjunction with address bits registered are used to select the starting column location for the burst access.

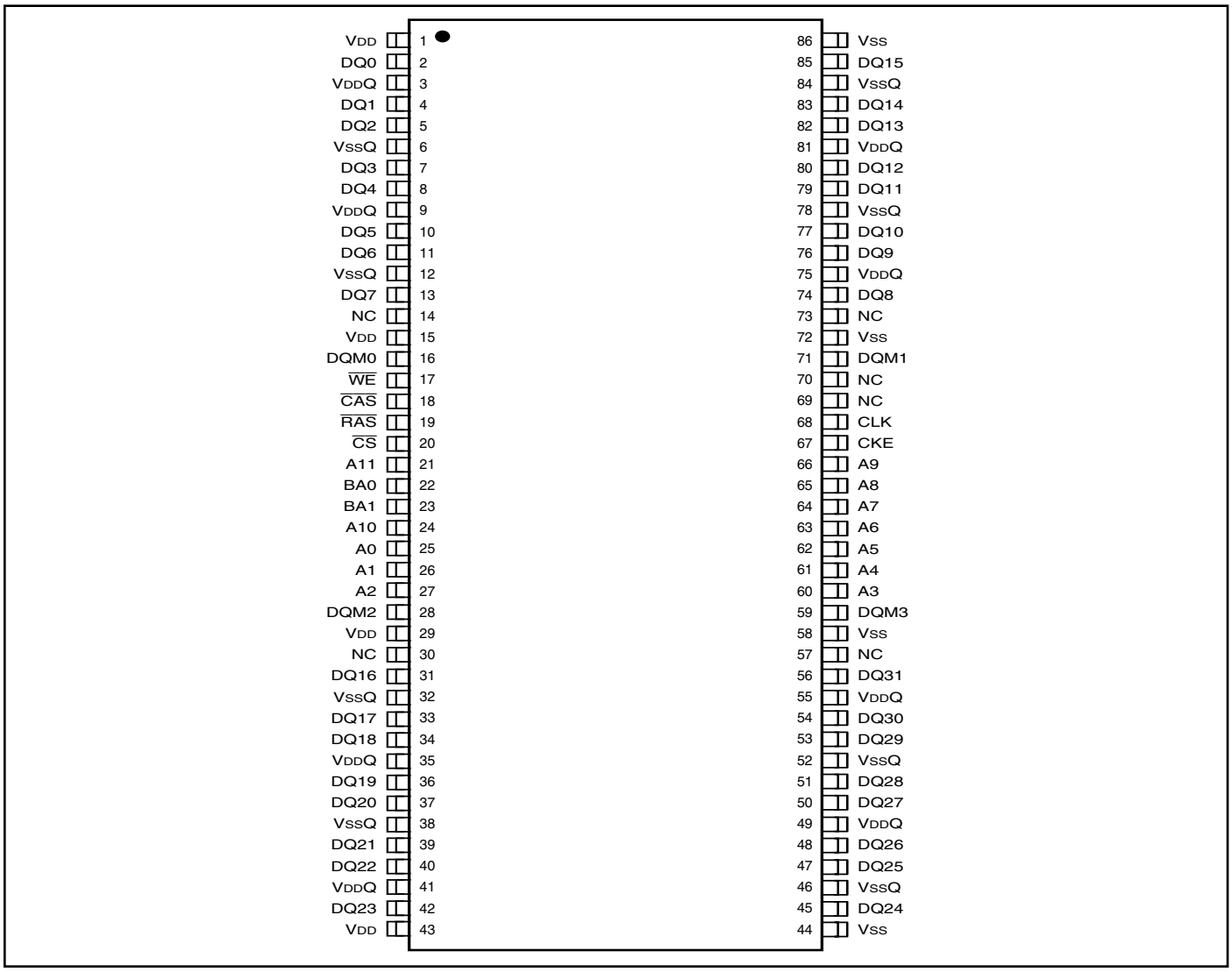
Programmable READ or WRITE burst lengths consist of 1, 2, 4 and 8 locations or full page, with a burst terminate option.

FUNCTIONAL BLOCK DIAGRAM (FOR 1MX32X4 BANKS)



PIN CONFIGURATIONS

86 pin TSOP - Type II for x32



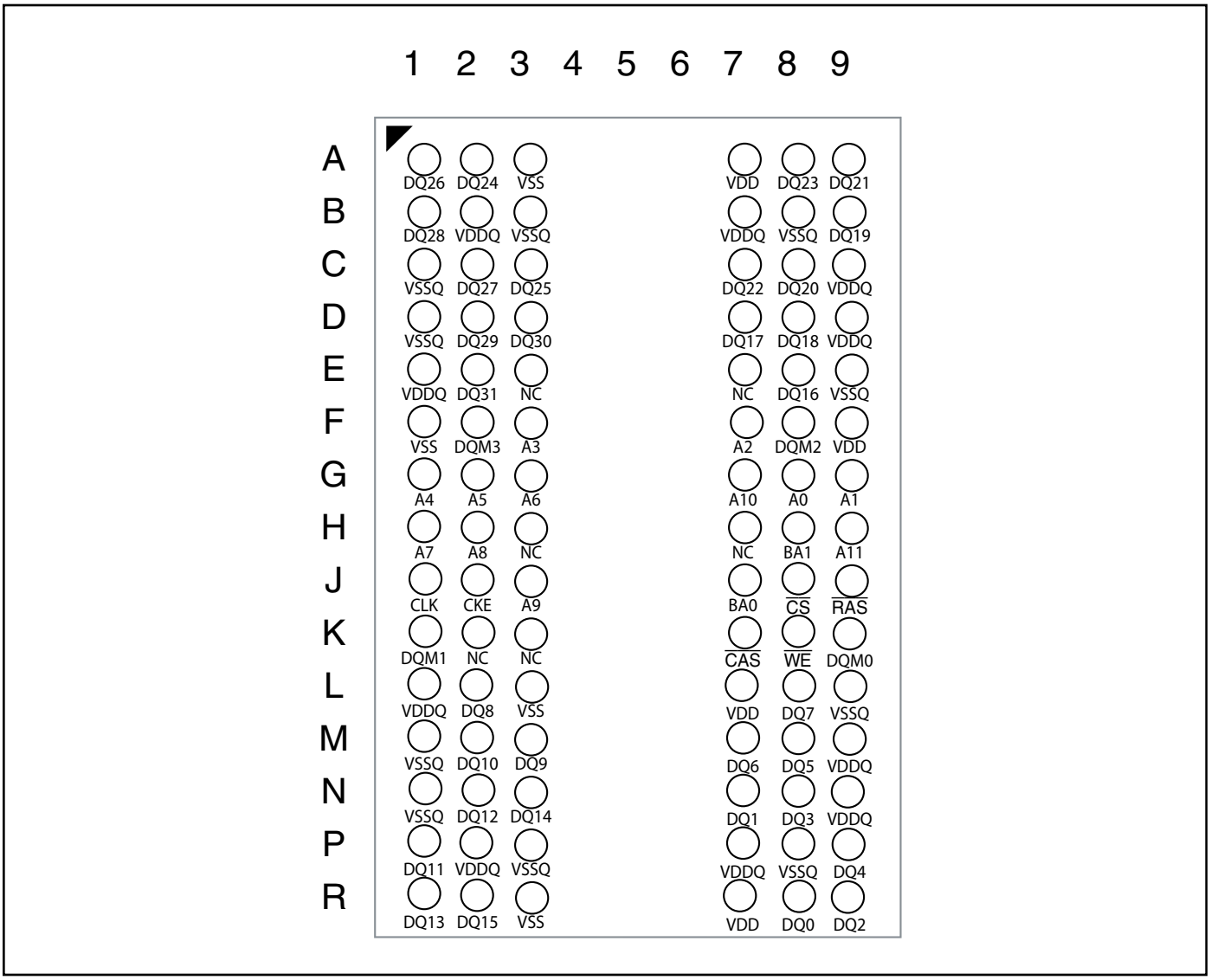
PIN DESCRIPTIONS

A0-A11	Row Address Input
A0-A7	Column Address Input
BA0, BA1	Bank Select Address
DQ0 to DQ31	Data I/O
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command

$\overline{WE}$	Write Enable
DQM0-DQM3	x32 Input/Output Mask
V_{DD}	Power
Vss	Ground
V_{DDQ}	Power Supply for I/O Pin
V_{SSQ}	Ground for I/O Pin
NC	No Connection

PIN CONFIGURATION

PACKAGE CODE: B 90 BALL FBGA (Top View) (8.00 mm x 13.00 mm Body, 0.8 mm Ball Pitch)



PIN DESCRIPTIONS

A0-A11	Row Address Input
A0-A7	Column Address Input
BA0, BA1	Bank Select Address
DQ0 to DQ31	Data I/O
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command

$\overline{WE}$	Write Enable
DQM0-DQM3	x32 Input/Output Mask
V_{DD}	Power
Vss	Ground
V_{DDQ}	Power Supply for I/O Pin
V_{SSQ}	Ground for I/O Pin
NC	No Connection

PIN FUNCTIONS

Symbol	Type	Function (In Detail)
A0-A11	Input Pin	Address Inputs: A0-A11 are sampled during the ACTIVE command (row-address A0-A11) and READ/WRITE command (column address A0-A7), with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
BA0, BA1	Input Pin	Bank Select Address: BA0 and BA1 defines which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
$\overline{CAS}$	Input Pin	$\overline{CAS}$, in conjunction with the $\overline{RAS}$ and $\overline{WE}$, forms the device command. See the "Command Truth Table" for details on device commands.
CKE	Input Pin	The CKE input determines whether the CLK input is enabled. The next rising edge of the CLK signal will be valid when is CKE HIGH and invalid when LOW. When CKE is LOW, the device will be in either power-down mode, clock suspend mode, or self refresh mode. CKE is an asynchronous input.
CLK	Input Pin	CLK is the master clock input for this device. Except for CKE, all inputs to this device are acquired in synchronization with the rising edge of this pin.
$\overline{CS}$	Input Pin	The $\overline{CS}$ input determines whether command input is enabled within the device. Command input is enabled when $\overline{CS}$ is LOW, and disabled with $\overline{CS}$ is HIGH. The device remains in the previous state when $\overline{CS}$ is HIGH.
DQM0-DQM3	Input Pin	DQM0 - DQM3 control the four bytes of the I/O buffers (DQ0-DQ31). In read mode, DQMn control the output buffer. When DQMn is LOW, the corresponding buffer byte is enabled, and when HIGH, disabled. The outputs go to the HIGH impedance state whenDQMn is HIGH. This function corresponds to $\overline{OE}$ in conventional DRAMs. In write mode, DQMn control the input buffer. When DQMn is LOW, the corresponding buffer byte is enabled, and data can be written to the device. When DQMn is HIGH, input data is masked and cannot be written to the device.
DQ0-DQ31	Input/Output Pin	Data on the Data Bus is latched on these pins during Write commands, and buffered after Read commands.
$\overline{RAS}$	Input Pin	$\overline{RAS}$, in conjunction with $\overline{CAS}$ and $\overline{WE}$, forms the device command. See the "Command Truth Table" item for details on device commands.
$\overline{WE}$	Input Pin	$\overline{WE}$, in conjunction with $\overline{RAS}$ and $\overline{CAS}$, forms the device command. See the "Command Truth Table" item for details on device commands.
V_{DDQ}	Power Supply Pin	V_{DDQ} is the output buffer power supply.
V_{DD}	Power Supply Pin	V_{DD} is the device internal power supply.
V_{SSQ}	Power Supply Pin	V_{SSQ} is the output buffer ground.
V_{SS}	Power Supply Pin	V_{SS} is the device internal ground.

GENERAL DESCRIPTION

READ

The READ command selects the bank from BA0, BA1 inputs and starts a burst read access to an active row. Inputs A0-A7 provides the starting column location. When A10 is HIGH, this command functions as an AUTO PRECHARGE command. When the auto precharge is selected, the row being accessed will be precharged at the end of the READ burst. The row will remain open for subsequent accesses when AUTO PRECHARGE is not selected. DQ's read data is subject to the logic level on the DQM inputs two clocks earlier. When a given DQM signal was registered HIGH, the corresponding DQ's will be High-Z two clocks later. DQ's will provide valid data when the DQM signal was registered LOW.

WRITE

A burst write access to an active row is initiated with the WRITE command. BA0, BA1 inputs selects the bank, and the starting column location is provided by inputs A0-A7. Whether or not AUTO-PRECHARGE is used is determined by A10.

The row being accessed will be precharged at the end of the WRITE burst, if AUTO PRECHARGE is selected. If AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses.

A memory array is written with corresponding input data on DQ's and DQM input logic level appearing at the same time. Data will be written to memory when DQM signal is LOW. When DQM is HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. BA0, BA1 can be used to select which bank is precharged or they are treated as "Don't Care". A10 determined whether one or all banks are precharged. After executing this command, the next command for the selected bank(s) is executed after passage of the period t_{RP}, which is the period required for bank precharging. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

AUTO PRECHARGE

The AUTO PRECHARGE function ensures that the precharge is initiated at the earliest valid stage within a burst. This function allows for individual-bank precharge without requiring an explicit command. A10 to enable the AUTO PRECHARGE function in conjunction with a specific READ or WRITE command. For each individual READ or WRITE command, auto precharge is either enabled or disabled. AUTO PRECHARGE does not apply except in full-page burst mode. Upon completion of the READ or WRITE burst, a precharge of the bank/row that is addressed is automatically performed.

AUTO REFRESH COMMAND

This command executes the AUTO REFRESH operation. The row address and bank to be refreshed are automatically generated during this operation. The stipulated period (t_{RC}) is required for a single refresh operation, and no other commands can be executed during this period. This command is executed at least 4096 times for every 64ms. During an AUTO REFRESH command, address bits are "Don't Care". This command corresponds to CBR Auto-refresh.

BURST TERMINATE

The BURST TERMINATE command forcibly terminates the burst read and write operations by truncating either fixed-length or full-page bursts and the most recently registered READ or WRITE command prior to the BURST TERMINATE.

COMMAND INHIBIT

COMMAND INHIBIT prevents new commands from being executed. Operations in progress are not affected, apart from whether the CLK signal is enabled

NO OPERATION

When $\overline{CS}$ is low, the NOP command prevents unwanted commands from being registered during idle or wait states.

LOAD MODE REGISTER

During the LOAD MODE REGISTER command the mode register is loaded from A0-A11. This command can only be issued when all banks are idle.

ACTIVE COMMAND

When the ACTIVE COMMAND is activated, BA0, BA1 inputs selects a bank to be accessed, and the address inputs on A0-A11 selects the row. Until a PRECHARGE command is issued to the bank, the row remains open for accesses.

COMMAND TRUTH TABLE

Function	CKE n – 1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA1	BA0	A10	A11 A9 - A0
Device deselect (DESL)	H	×	H	×	×	×	×	×	×	×
No operation (NOP)	H	×	L	H	H	H	×	×	×	×
Burst stop (BST)	H	×	L	H	H	L	×	×	×	×
Read	H	×	L	H	L	H	V	V	L	V
Read with auto precharge	H	×	L	H	L	H	V	V	H	V
Write	H	×	L	H	L	L	V	V	L	V
Write with auto precharge	H	×	L	H	L	L	V	V	H	V
Bank activate (ACT)	H	×	L	L	H	H	V	V	V	V
Precharge select bank (PRE)	H	×	L	L	H	L	V	V	L	×
Precharge all banks (PALL)	H	×	L	L	H	L	×	×	H	×
CBR Auto-Refresh (REF)	H	H	L	L	L	H	×	×	×	×
Self-Refresh (SELF)	H	L	L	L	L	H	×	×	×	×
Mode register set (MRS)	H	×	L	L	L	L	L	L	L	V

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data.

DQM TRUTH TABLE

Function	CKE n-1	CKE n	DQM U	DQM L
Data write / output enable	H	×	L	L
Data mask / output disable	H	×	H	H
Upper byte write enable / output enable	H	×	L	×
Lower byte write enable / output enable	H	×	×	L
Upper byte write inhibit / output disable	H	×	H	×
Lower byte write inhibit / output disable	H	×	×	H

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data.

CKE TRUTH TABLE

Current State /Function	CKE n – 1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Activating Clock suspend mode entry	H	L	×	×	×	×	×
Any Clock suspend mode	L	L	×	×	×	×	×
Clock suspend mode exit	L	H	×	×	×	×	×
Auto refresh command Idle (REF)	H	H	L	L	L	H	×
Self refresh entry Idle (SELF)	H	L	L	L	L	H	×
Power down entry Idle	H	L	×	×	×	×	×
Self refresh exit	L	H	L	H	H	H	×
	L	H	H	×	×	×	×
Power down exit	L	H	×	×	×	×	×

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data.

FUNCTIONAL TRUTH TABLE

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
Idle	H	X	X	X	X	DESL	Nop or Power Down(2)
	L	H	H	H	X	NOP	Nop or Power Down(2)
	L	H	H	L	X	BST	Nop or Power Down
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL (3)
	L	H	L	L	A, CA, A10	WRIT/ WRITA	ILLEGAL(3)
	L	L	H	H	BA, RA	ACT	Row activating
	L	L	H	L	BA, A10	PRE/PALL	Nop
	L	L	L	H	X	REF/SELF	Auto refresh or Self-refresh(4)
	L	L	L	L	OC, BA1=L	MRS	Mode register set
Row Active	H	X	X	X	X	DESL	Nop
	L	H	H	H	X	NOP	Nop
	L	H	H	L	X	BST	Nop
	L	H	L	H	BA, CA, A10	READ/READA	Begin read (5)
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	Begin write (5)
	L	L	H	H	BA, RA	ACT	ILLEGAL (3)
	L	L	H	L	BA, A10	PRE/PALL	Precharge Precharge all banks(6)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Read	H	X	X	X	X	DESL	Continue burst to end to Row active
	L	H	H	H	X	NOP	Continue burst to end Row Row active
	L	H	H	L	X	BST	Burst stop, Row active
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, begin new read (7)
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, begin write (7,8)
	L	L	H	H	BA, RA	ACT	ILLEGAL (3)
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst Precharging
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Write	H	X	X	X	X	DESL	Continue burst to end Write recovering
	L	H	H	H	X	NOP	Continue burst to end Write recovering
	L	H	H	L	X	BST	Burst stop, Row active
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, start read : Determine AP (7,8)
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, new write : Determine AP (7)
	L	L	H	H	BA, RA	RA ACT	ILLEGAL (3)
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst Precharging (9)
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data, BA= Bank Address, CA+Column Address, RA=Row Address, OC= Op-Code

FUNCTIONAL TRUTH TABLE Continued:

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
Read with auto Precharging	H	×	×	×	×	DESL	Continue burst to end, Precharge
	L	H	H	H	x	NOP	Continue burst to end, Precharge
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL (11)
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL (11)
	L	L	H	H	BA, RA	ACT	ILLEGAL (3)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (11)
	L	L	L	H	×	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Write with Auto Precharge	H	×	×	×	×	DESL	Continue burst to end, Write recovering with auto precharge
	L	H	H	H	×	NOP	Continue burst to end, Write recovering with auto precharge
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL(11)
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL (11)
	L	L	H	H	BA, RA	ACT	ILLEGAL (3,11)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (3,11)
	L	L	L	H	×	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Precharging	H	×	×	×	×	DESL	Nop, Enter idle after tRP
	L	H	H	H	×	NOP	Nop, Enter idle after tRP
	L	H	H	L	×	BST	Nop, Enter idle after tRP
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL (3)
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL (3)
	L	L	H	H	BA, RA	ACT	ILLEGAL(3)
	L	L	H	L	BA, A10	PRE/PALL	Nop Enter idle after tRP
	L	L	L	H	×	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Row Activating	H	×	×	×	×	DESL	Nop, Enter bank active after tRCD
	L	H	H	H	×	NOP	Nop, Enter bank active after tRCD
	L	H	H	L	×	BST	Nop, Enter bank active after tRCD
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL (3)
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL (3)
	L	L	H	H	BA, RA	ACT	ILLEGAL (3,9)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (3)
	L	L	L	H	×	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data, BA= Bank Address, CA+Column Address, RA=Row Address, OC= Op-Code

FUNCTIONAL TRUTH TABLE Continued:

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
Write Recovering	H	×	×	×	×	DESL	Nop, Enter row active after tDPL
	L	H	H	H	×	NOP	Nop, Enter row active after tDPL
	L	H	H	L	×	BST	Nop, Enter row active after tDPL
	L	H	L	H	BA, CA, A10	READ/READA	Begin read (8)
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	Begin new write
	L	L	H	H	BA, RA	ACT	ILLEGAL (3)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (3)
	L	L	L	H	×	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Write Recovering	H	×	×	×	×	DESL	Nop, Enter precharge after tDPL
with Auto	L	H	H	H	×	NOP	Nop, Enter precharge after tDPL
Precharge	L	H	H	L	×	BST	Nop, Enter row active after tDPL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL(3,8,11)
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL (3,11)
	L	L	H	H	BA, RA	ACT	ILLEGAL (3,11)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (3,11)
	L	L	L	H	×	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Refresh	H	×	×	×	×	DESL	Nop, Enter idle after tRC
	L	H	H	×	×	NOP/BST	Nop, Enter idle after tRC
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL
	L	L	L	H	×	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Mode Register	H	×	×	×	×	DESL	Nop, Enter idle after 2 clocks
Accessing	L	H	H	H	×	NOP	Nop, Enter idle after 2 clocks
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	×	BA, CA, A10	READ/WRITE	ILLEGAL
	L	L	×	×	BA, RA	ACT/PRE/PALL REF/MRS	ILLEGAL

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data, BA= Bank Address, CA+Column Address, RA=Row Address, OC= Op-Code

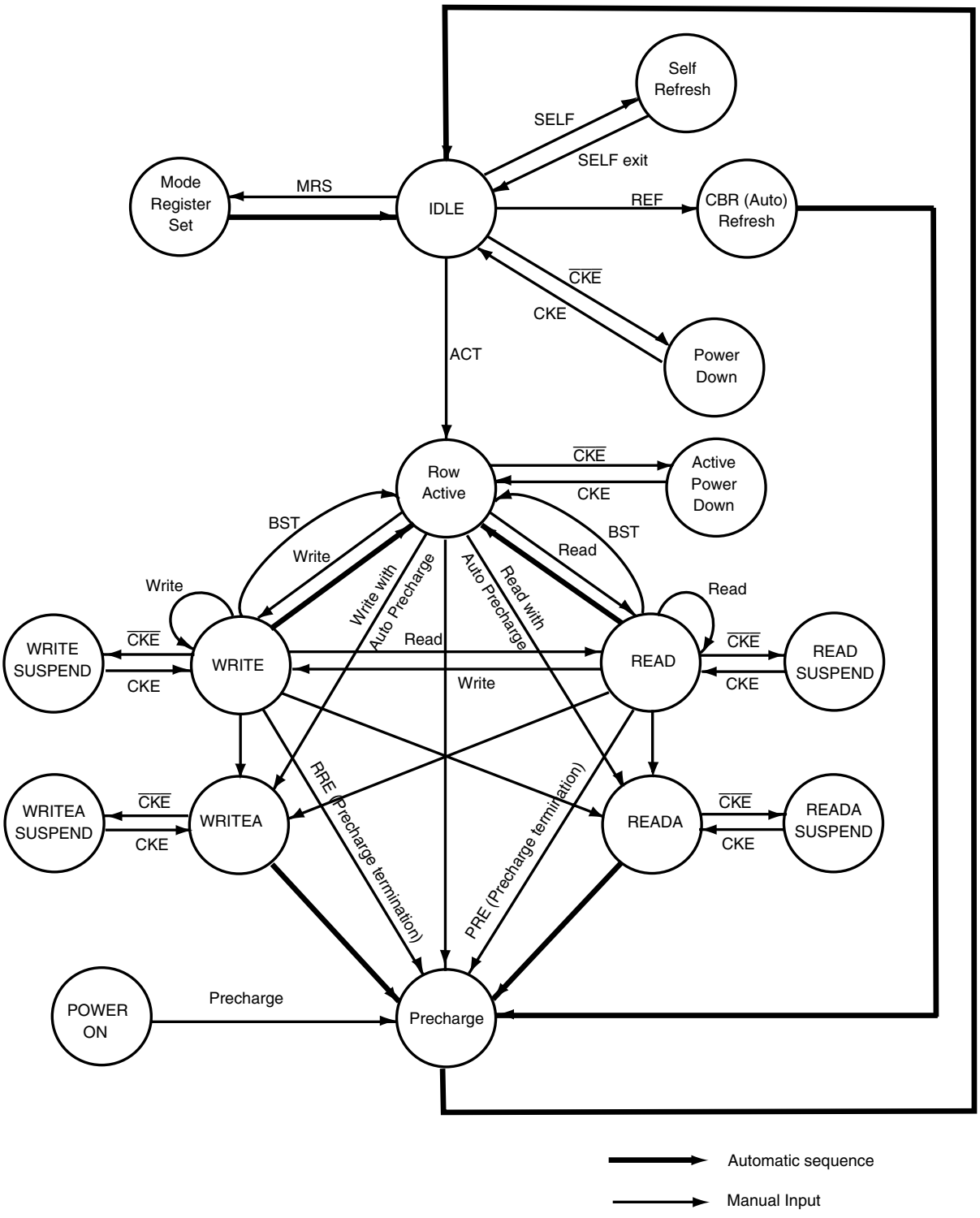
Notes:
1. All entries assume that CKE is active (CKEn-1=CKEn=H).
2. If both banks are idle, and CKE is inactive (Low), the device will enter Power Down mode. All input buffers except CKE will be disabled.
3. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
4. If both banks are idle, and CKE is inactive (Low), the device will enter Self-Refresh mode. All input buffers except CKE will be disabled.
5. Illegal if tRCD is not satisfied.
6. Illegal if tRAS is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
9. Must mask preceding data which don't satisfy tDPL.
10. Illegal if tRRD is not satisfied.
11. Illegal for single bank, but legal for other banks.

CKE RELATED COMMAND TRUTH TABLE(1)

Current State	Operation	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Self-Refresh (S.R.)	INVALID, CLK (n - 1) would exit S.R.	H	X	X	X	X	X	X
	Self-Refresh Recovery(2)	L	H	H	X	X	X	X
	Self-Refresh Recovery(2)	L	H	L	H	H	X	X
	Illegal	L	H	L	H	L	X	X
	Illegal	L	H	L	L	X	X	X
	Maintain S.R.	L	L	X	X	X	X	X
Self-Refresh Recovery	Idle After t_{RC}	H	H	H	X	X	X	X
	Idle After t_{RC}	H	H	L	H	H	X	X
	Illegal	H	H	L	H	L	X	X
	Illegal	H	H	L	L	X	X	X
	Begin clock suspend next cycle(5)	H	L	H	X	X	X	X
	Begin clock suspend next cycle(5)	H	L	L	H	H	X	X
	Illegal	H	L	L	H	L	X	X
	Illegal	H	L	L	L	X	X	X
	Exit clock suspend next cycle(2)	L	H	X	X	X	X	X
	Maintain clock suspend	L	L	X	X	X	X	X
Power-Down (P.D.)	INVALID, CLK (n - 1) would exit P.D.	H	X	X	X	X	X	—
	EXIT P.D. --> Idle(2)	L	H	X	X	X	X	X
	Maintain power down mode	L	L	X	X	X	X	X
Both Banks Idle	Refer to operations in Operative Command Table	H	H	H	X	X	X	—
	Refer to operations in Operative Command Table	H	H	L	H	X	X	—
	Refer to operations in Operative Command Table	H	H	L	L	H	X	—
	Auto-Refresh	H	H	L	L	L	H	X
	Refer to operations in Operative Command Table	H	H	L	L	L	L	Op - Code
	Refer to operations in Operative Command Table	H	L	H	X	X	X	—
	Refer to operations in Operative Command Table	H	L	L	H	X	X	—
	Refer to operations in Operative Command Table	H	L	L	L	H	X	—
	Self-Refresh(3)	H	L	L	L	L	H	X
	Refer to operations in Operative Command Table	H	L	L	L	L	L	Op - Code
	Power-Down(3)	L	X	X	X	X	X	X
Any state	Refer to operations in Operative Command Table	H	H	X	X	X	X	X
other than	Begin clock suspend next cycle(4)	H	L	X	X	X	X	X
listed above	Exit clock suspend next cycle	L	H	X	X	X	X	X
	Maintain clock suspend	L	L	X	X	X	X	X

Notes:
1. H : High level, L : low level, X : High or low level (Don't care).
2. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
3. Power down and Self refresh can be entered only from the both banks idle state.
4. Must be legal command as defined in Operative Command Table.
5. Illegal if t_{XSR} is not satisfied.

STATE DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters		Rating	Unit
$V_{DD\ MAX}$	Maximum Supply Voltage		–0.5 to +4.6	V
$V_{DDQ\ MAX}$	Maximum Supply Voltage for Output Buffer		–0.5 to +4.6	V
V_{IN}	Input Voltage		–0.5 to V_{DD} + 0.5	V
V_{OUT}	Output Voltage		–1.0 to V_{DDQ} + 0.5	V
$P_{D\ MAX}$	Allowable Power Dissipation		1	W
I_{CS}	Output Shorted Current		50	mA
T_{OPR}	Operating Temperature	Com. Ind.	0 to +70 –40 to +85	°C
T_{STG}	Storage Temperature		–65 to +150	°C

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are referenced to Vss.

DC RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
V_{DDQ}	I/O Supply Voltage	3.0	3.3	3.6	V
V_{IH}(1)	Input High Voltage	2.0	—	V_{DDQ} + 1.2	V
V_{IL}(2)	Input Low Voltage	-0.3	—	+0.8	V

Note:

1. V_{IH} (max) = V_{DDQ} +1.2V (PULSE WIDTH ≤ 3NS).
2. V_{IL} (min) = -1.2V (PULSE WIDTH ≤ 3NS).
3. All voltages are referenced to Vss.

CAPACITANCE CHARACTERISTICS (At T_A = 0 to +25°C, V_{DD} = V_{DDQ} = 3.3 ± 0.3V)

Symbol	Parameter	Min.	Max.		Unit
			-6	-7	
C_{IN1}	Input Capacitance: CLK	2.5	3.5	4.0	pF
C_{IN2}	Input Capacitance:All other input pins	2.5	3.8	5.0	pF
$C_{I/O}$	Data Input/Output Capacitance:I/Os	4.0	6.5	6.5	pF

DC ELECTRICAL CHARACTERISTICS 1 (Recommended Operation Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	-6	-7	Unit
I_{DD1} (1)	Operating Current	One bank active, CL = 3, BL = 1, t_{CLK} = t_{CLK} (min), t_{RC} = t_{RC} (min)	140	120	mA
I_{DD2P}	Precharge Standby Current (In Power-Down Mode)	CKE ≤ V_{IL} (MAX), t_{CK} = 15ns	2	2	mA
I_{DD2PS}	Precharge Standby Current (In Power-Down Mode)	CKE ≤ V_{IL} (MAX), CLK ≤ V_{IL} (MAX)	1	1	mA
I_{DD2N} (2)	Precharge Standby Current (In Non Power-Down Mode)	$\overline{CS}$ ≥ V_{DD} - 0.2V, CKE ≥ V_{IH} (MIN) t_{CK} = 15ns	25	25	mA
I_{DD2NS}	Precharge Standby Current (In Non Power-Down Mode)	$\overline{CS}$ ≥ V_{DD} - 0.2V, CKE ≥ V_{IH} (MIN) or CKE ≤ V_{IL} (MAX), All inputs stable	15	15	mA
I_{DD3N} (2)	Active Standby Current (In Non Power-Down Mode)	$\overline{CS}$ ≥ V_{DD} - 0.2V, CKE ≥ V_{IH} (MIN) t_{CK} = 15ns	30	30	mA
I_{DD3NS}	Active Standby Current (In Non Power-Down Mode)	$\overline{CS}$ ≥ V_{DD} - 0.2V, CKE ≥ V_{IH} (MIN) or CKE ≤ V_{IL} (MAX), All inputs stable	20	20	mA
I_{DD3P}	Active Standby Current (Power-Down Mode)	CKE ≤ V_{IL} (MAX), t_{CK} = 15ns	2	2	mA
I_{DD3PS}	Active Standby Current (Power-Down Mode)	CKE ≤ V_{IL} (MAX), CLK ≤ V_{IL} (MAX)	2	2	mA
I_{DD4}	Operating Current	All banks active, BL = 4, CL = 3, t_{CK} = t_{CK} (min)	180	130	mA
I_{DD5}	Auto-Refresh Current	t_{RC} = t_{RC} (min), t_{CLK} = t_{CLK} (min)	180	160	mA
I_{DD6}	Self-Refresh Current	CKE ≤ 0.2V	2	2	mA

Notes:

1. I_{DD} (MAX) is specified at the output open condition.
2. Input signals are changed one time during 30ns.

DC ELECTRICAL CHARACTERISTICS 2 (Recommended Operation Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{IL}	Input Leakage Current	0V ≤ Vin ≤ V_{DD}, with pins other than the tested pin at 0V	-10	10	µA
I_{OL}	Output Leakage Current	Output is disabled, 0V ≤ Vout ≤ V_{DD},	-10	10	µA
V_{OH}	Output High Voltage Level	I_{OH} = -2mA	2.4	—	V
V_{OL}	Output Low Voltage Level	I_{OL} = 2mA	—	0.4	V

AC ELECTRICAL CHARACTERISTICS (1,2,3)

			-6		-7		
Symbol	**Parameter**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{CK3}	Clock Cycle Time	$\overline{CAS}$ Latency = 3	6	—	7	—	ns
t_{CK2}		$\overline{CAS}$ Latency = 2	8	—	10	—	ns
t_{AC3}	Access Time From CLK	$\overline{CAS}$ Latency = 3	—	5.4	—	5.4	ns
t_{AC2}		$\overline{CAS}$ Latency = 2	—	6.5	—	6.5	ns
t_{CHI}	CLK HIGH Level Width		2.5	—	2.5	—	ns
t_{CL}	CLK LOW Level Width		2.5	—	2.5	—	ns
t_{OH3}	Output Data Hold Time	$\overline{CAS}$ Latency = 3	2.7	—	2.7	—	ns
t_{OH2}		$\overline{CAS}$ Latency = 2	2.7	—	3	—	ns
t_{LZ}	Output LOW Impedance Time		0	—	0	—	ns
t_{HZ}	Output HIGH Impedance Time		2.7	5.4	2.7	5.4	ns
t_{DS}	Input Data Setup Time(2)		1.5	—	1.5	—	ns
t_{DH}	Input Data Hold Time(2)		0.8	—	0.8	—	ns
t_{AS}	Address Setup Time(2)		1.5	—	1.5	—	ns
t_{AH}	Address Hold Time(2)		0.8	—	0.8	—	ns
t_{CKS}	CKE Setup Time(2)		1.5	—	1.5	—	ns
t_{CKH}	CKE Hold Time(2)		0.8	—	0.8	—	ns
t_{CS}	Command Setup Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)(2)		1.5	—	1.5	—	ns
t_{CH}	Command Hold Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)(2)		0.8	—	0.8	—	ns
t_{RC}	Command Period (REF to REF / ACT to ACT)		60	—	67.5	—	ns
t_{RAS}	Command Period (ACT to PRE)		42	100K	45	100K	ns
t_{RP}	Command Period (PRE to ACT)		18	—	20	—	ns
t_{RCD}	Active Command To Read / Write Command Delay Time		18	—	20	—	ns
t_{RRD}	Command Period (ACT [0] to ACT[1])		12	—	14	—	ns
t_{DPL}	Input Data To Precharge Command Delay time		12	—	14	—	ns
t_{DAL}	Input Data To Active / Refresh Command Delay time (During Auto-Precharge)		30	—	34	—	ns
t_{MRD}	Mode Register Program Time		12	—	15	—	ns
t_{DDE}	Power Down Exit Setup Time		6	—	7.5	—	ns
t_{XSR}	Self-Refresh Exit Time		70	—	70	—	ns
t_T	Transition Time		1	10	1	10	ns
t_{REF}	Refresh Cycle Time (4096)		—	64	—	64	ms

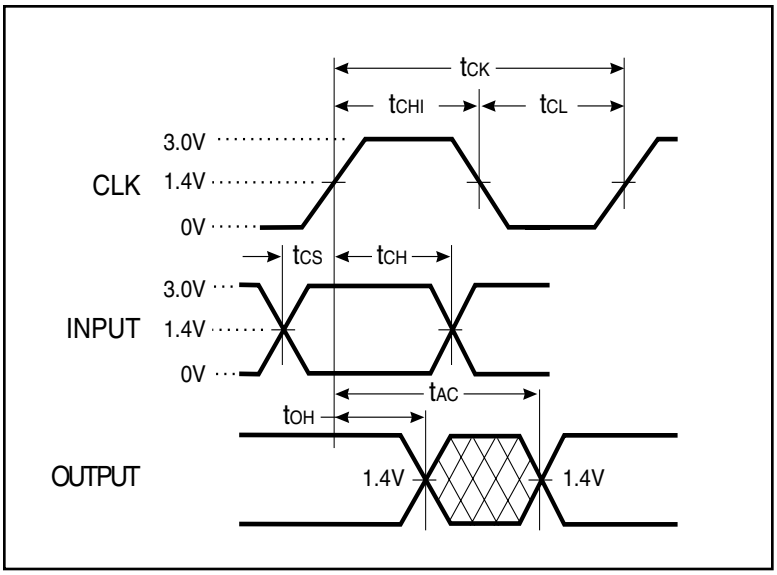
Notes:
1. The power-on sequence must be executed before starting memory operation.
2. Measured with t_T = 1 ns. If clock rising time is longer than 1ns, (t_R /2 - 0.5) ns should be added to the parameter.
3. The reference level is 1.4V when measuring input signal timing. Rise and fall times are measured between V_{IH}(min.) and V_{IL} (max).

OPERATING FREQUENCY / LATENCY RELATIONSHIPS

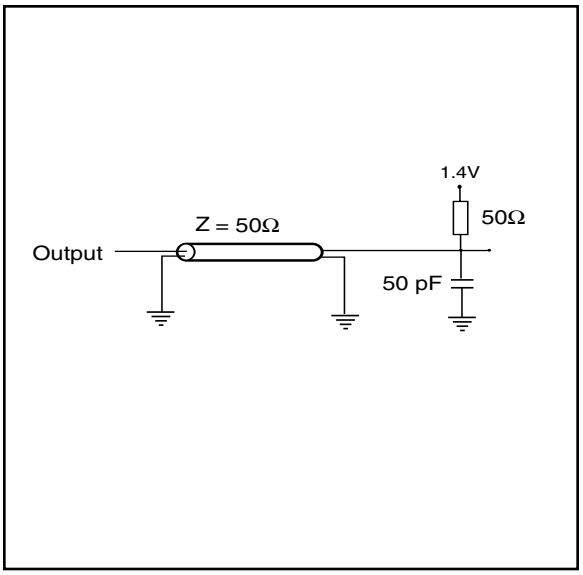
SYMBOL	PARAMETER				UNITS
—	Clock Cycle Time		6	7	ns
—	Operating Frequency		166	143	MHz
t_{CAC}	$\overline{CAS}$ Latency		3	3	cycle
t_{RCD}	Active Command To Read/Write Command Delay Time		3	3	cycle
t_{RAC}	$\overline{RAS}$ Latency (t_{RCD} + t_{CAC})	$\overline{CAS}$ Latency = 3	6	6	cycle
		$\overline{CAS}$ Latency = 2	—	—	
t_{RC}	Command Period (REF to REF / ACT to ACT)		10	10	cycle
t_{RAS}	Command Period (ACT to PRE)		7	7	cycle
t_{RP}	Command Period (PRE to ACT)		3	3	cycle
t_{RRD}	Command Period (ACT[0] to ACT [1])		2	2	cycle
t_{CCD}	Column Command Delay Time (READ, READA, WRIT, WRITA)		1	1	cycle
t_{DPL}	Input Data To Precharge Command Delay Time		2	2	cycle
t_{DAL}	Input Data To Active/Refresh Command Delay Time (During Auto-Precharge)		5	5	cycle
t_{RBD}	Burst Stop Command To Output in HIGH-Z Delay Time (Read)	$\overline{CAS}$ Latency = 3	3	3	cycle
		$\overline{CAS}$ Latency = 2	—	—	
t_{WBD}	Burst Stop Command To Input in Invalid Delay Time (Write)		0	0	cycle
t_{RQL}	Precharge Command To Output in HIGH-Z Delay Time (Read)	$\overline{CAS}$ Latency = 3	3	3	cycle
		$\overline{CAS}$ Latency = 2	—	—	
t_{WDL}	Precharge Command To Input in Invalid Delay Time (Write)		0	0	cycle
t_{PQL}	Last Output To Auto-Precharge Start Time (Read)	$\overline{CAS}$ Latency = 3	-2	–2	cycle
		$\overline{CAS}$ Latency = 2	—	—	
t_{QMD}	DQM To Output Delay Time (Read)		2	2	cycle
t_{DMD}	DQM To Input Delay Time (Write)		0	0	cycle
t_{MRD}	Mode Register Set To Command Delay Time		2	2	cycle

AC TEST CONDITIONS

Input Load



Output Load



AC TEST CONDITIONS

Parameter	Rating
AC Input Levels	0V to 3.0V
Input Rise and Fall Times	1 ns
Input Timing Reference Level	1.4V
Output Timing Measurement Reference Level	1.4V

FUNCTIONAL DESCRIPTION

The 128Mb SDRAMs are quad-bank DRAMs which operate at 3.3V and include a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 33,554,432-bit banks is organized as 4,096 rows by 256 columns by 32 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0-A11 select the row). The address bits A0-A7 registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

SDRAMs must be powered up and initialized in a predefined manner.

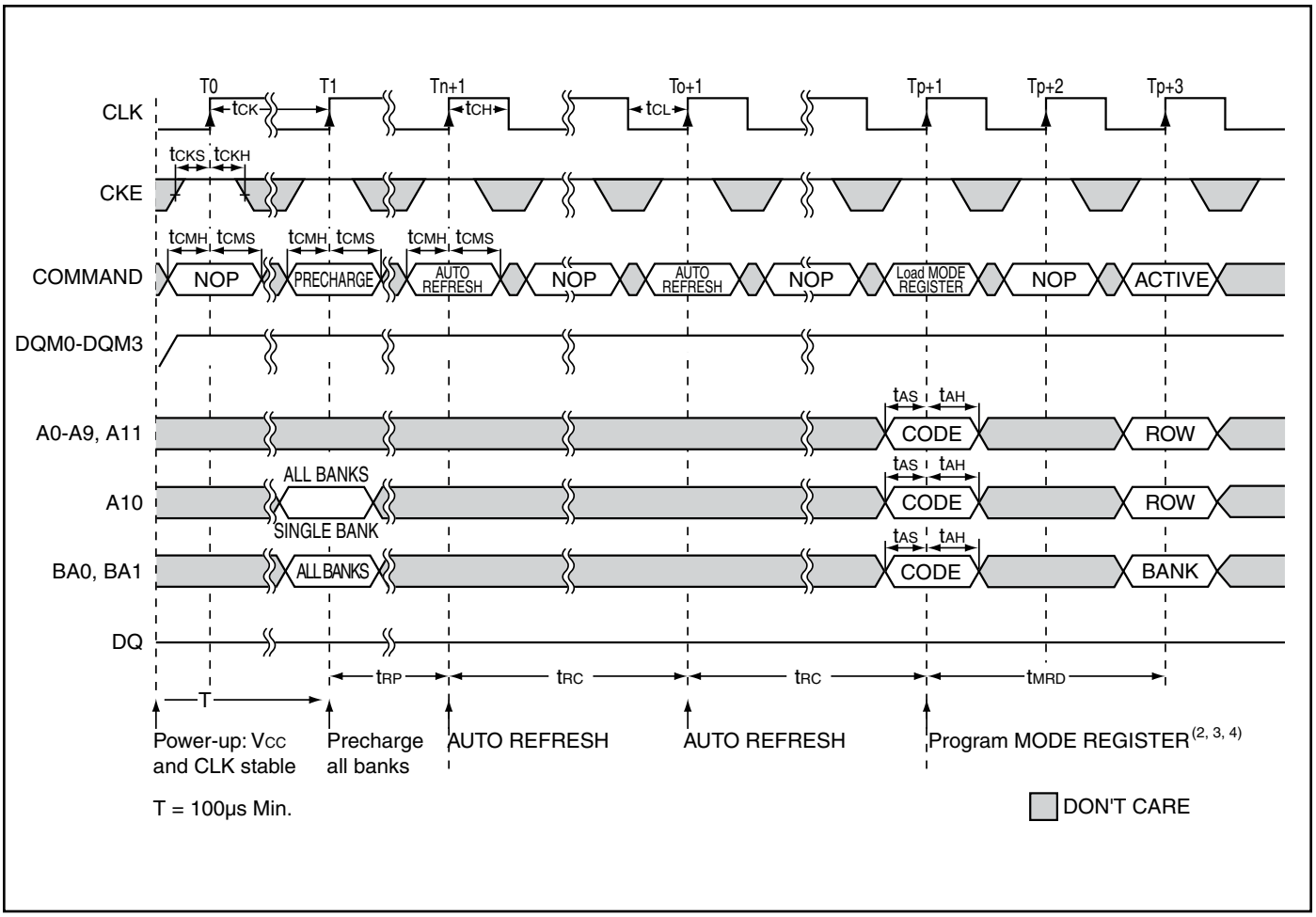
The 128M SDRAM is initialized after the power is applied to V_{DD} and V_{DDQ} (simultaneously) and the clock is stable with DQM High and CKE High.

A 100µs delay is required prior to issuing any command other than a COMMAND INHIBIT or a NOP. The COMMAND INHIBIT or NOP may be applied during the 100µs period and should continue at least through the end of the period.

With at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied once the 100µs delay has been satisfied. All banks must be precharged. This will leave all banks in an idle state after which at least two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is then ready for mode register programming.

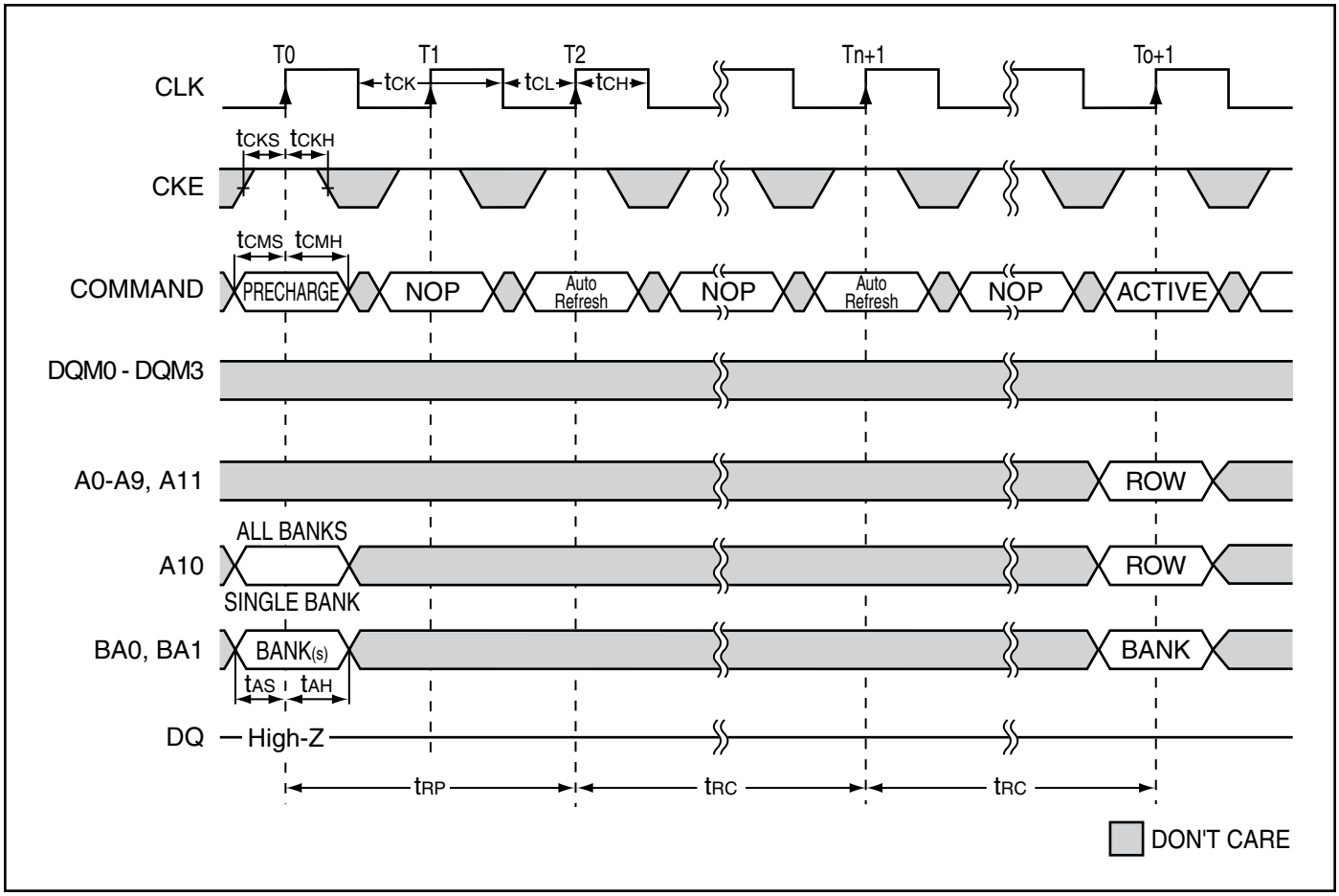
The mode register should be loaded prior to applying any operational command because it will power up in an unknown state.

INITIALIZE AND LOAD MODE REGISTER(1)



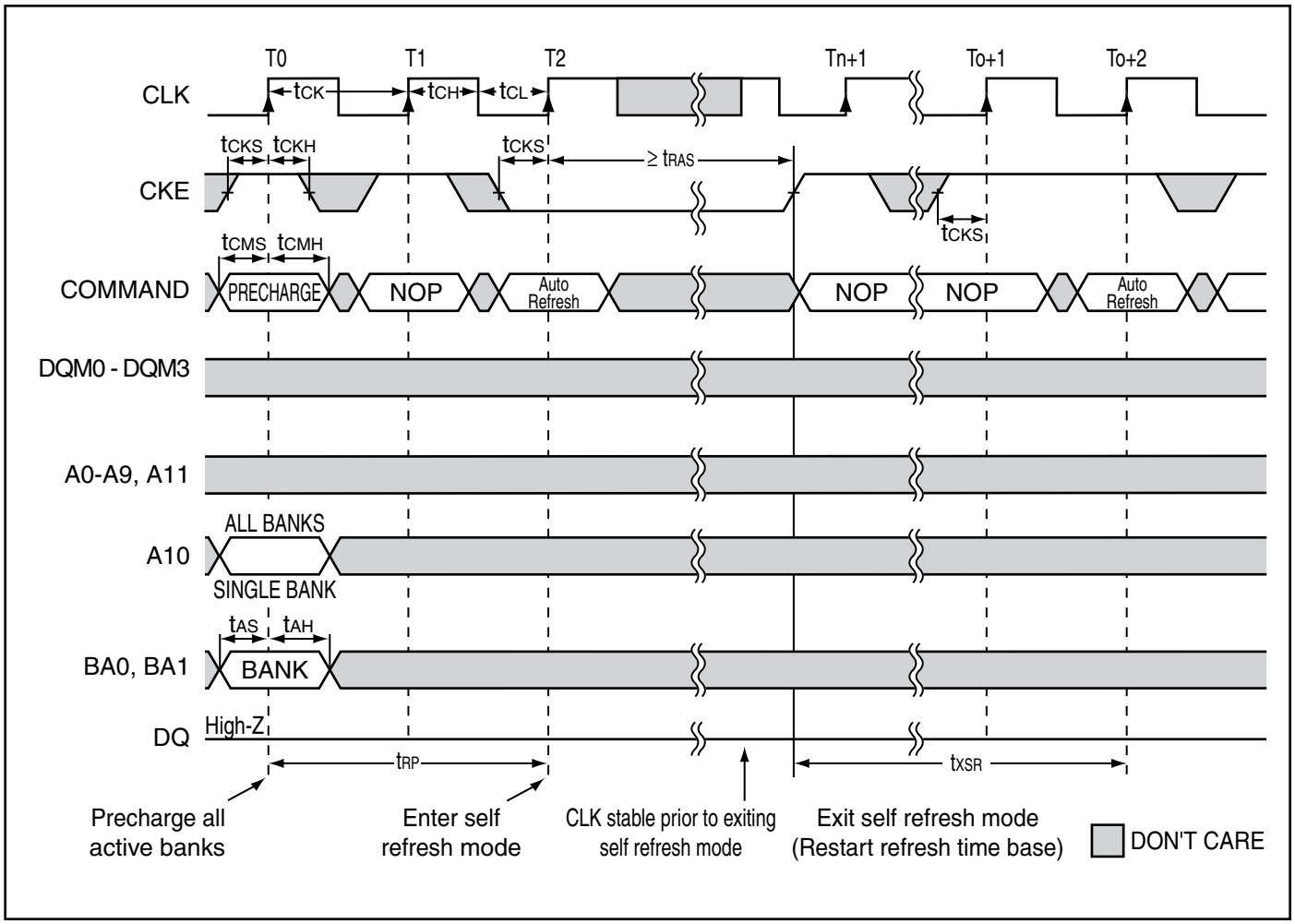
Notes:
1. If $\overline{CS}$ is High at clock High time, all commands applied are NOP.
2. The Mode register may be loaded prior to the Auto-Refresh cycles if desired.
3. JEDEC and PC100 specify three clocks.
4. Outputs are guaranteed High-Z after the command is issued.

AUTO-REFRESH CYCLE



Notes:
1. $\overline{CAS}$ latency = 2, 3

SELF-REFRESH CYCLE



REGISTER DEFINITION

Mode Register

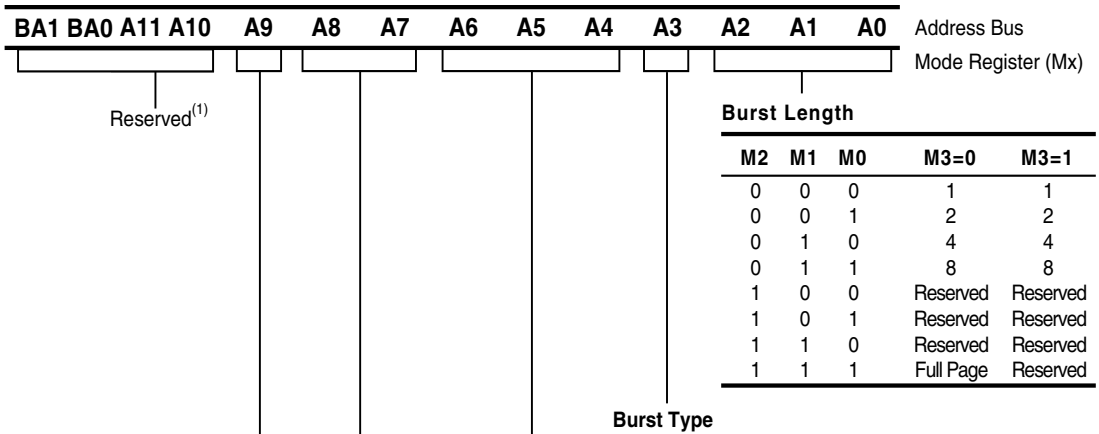
The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in MODE REGISTER DEFINITION.

The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0-M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4- M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the WRITE burst mode, and M10 and M11 are reserved for future use.

The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

MODE REGISTER DEFINITION



Burst Length

M2	M1	M0	M3=0	M3=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

Burst Type

M3	Type
0	Sequential
1	Interleaved

Latency Mode

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Operating Mode

M8	M7	M6-M0	Mode
0	0	Defined	Standard Operation
—	—	—	All Other States Reserved

Write Burst Mode

M9	Mode
0	Programmed Burst Length
1	Single Location Access

1. To ensure compatibility with future devices, should program BA1, BA0, A11, A10 = "0"

BURST LENGTH

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in MODE REGISTER DEFINITION. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4 or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A7 (x32) when the burst length is set to two; by A2-A7 (x32) when the burst length is set to four; and by A3-A7 (x32) when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in BURST DEFINITION table.

BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
			A 0		
2			0	0-1	0-1
			1	1-0	1-0
		A 1	**A 0**		
		0	0	0-1-2-3	0-1-2-3
4		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
	A 2	**A 1**	**A 0**		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
8	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0-A7 (location 0-y)			Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... …Cn - 1, Cn…	Not Supported

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge n, and the latency is *m* clocks, the data will be available by clock edge *n* + m. The DQs will start driving as a result of the clock edge one cycle earlier *(n + m* - 1), and provided that the relevant access times are met, the data will be valid by clock edge *n* + m. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in CAS Latency diagrams. The Allowable Operating Frequency table indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

CAS Latency

Allowable Operating Frequency (MHz)

Speed	CAS Latency = 2	CAS Latency = 3
-6	125	166
-7	100	143

CAS LATENCY