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IS43/46DR86400C
IS43/46DR16320C

64Mx8, 32Mx16 DDR2 DRAM

MARCH 2013

FEATURES

- V_{DD} = 1.8V ±0.1V, V_{DDQ} = 1.8V ±0.1V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Double data rate interface: two data transfers per clock cycle
- Differential data strobe (DQS, $\overline{DQS}$)
- 4-bit prefetch architecture
- On chip DLL to align DQ and DQS transitions with CK
- 4 internal banks for concurrent operation
- Programmable CAS latency (CL) 3, 4, 5, and 6 supported
- Posted CAS and programmable additive latency (AL) 0, 1, 2, 3, 4, and 5 supported
- WRITE latency = READ latency - 1 tCK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength, full and reduced strength options
- On-die termination (ODT)

OPTIONS

- Configuration(s):
  64Mx8 (16Mx8x4 banks) IS43/46DR86400C
  32Mx16 (8Mx16x4 banks) IS43/46DR16320C
- Package:
  x8: 60-ball BGA (8mm x 10.5mm)
  x16: 84-ball WBGA (8mm x 12.5mm)
  Timing – Cycle time
  2.5ns @CL=5 DDR2-800D
  2.5ns @CL=6 DDR2-800E
  3.0ns @CL=5 DDR2-667D
  3.75ns @CL=4 DDR2-533C
  5ns @CL=3 DDR2-400B
- Temperature Range:
  Commercial (0°C ≤ Tc ≤ 85°C)
  Industrial (-40°C ≤ Tc ≤ 95°C; -40°C ≤ TA ≤ 85°C)
  Automotive, A1 (-40°C ≤ Tc ≤ 95°C; -40°C ≤ TA ≤ 85°C)
  Automotive, A2 (-40°C ≤ Tc; TA ≤ 105°C)
  Tc = Case Temp, TA = Ambient Temp

DESCRIPTION

ISSI's 512Mb DDR2 SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double-data rate architecture is essentially a 4n-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls.

ADDRESS TABLE

Parameter	64M x 8	32M x 16
Configuration	16M x 8 x 4 banks	8M x 16 x 4 banks
Refresh Count	8K/64ms	8K/64ms
Row Addressing	16K (A0-A13)	8K (A0-A12)
Column Addressing	1K (A0-A9)	1K (A0-A9)
Bank Addressing	BA0, BA1	BA0, BA1
Precharge Addressing	A10	A10

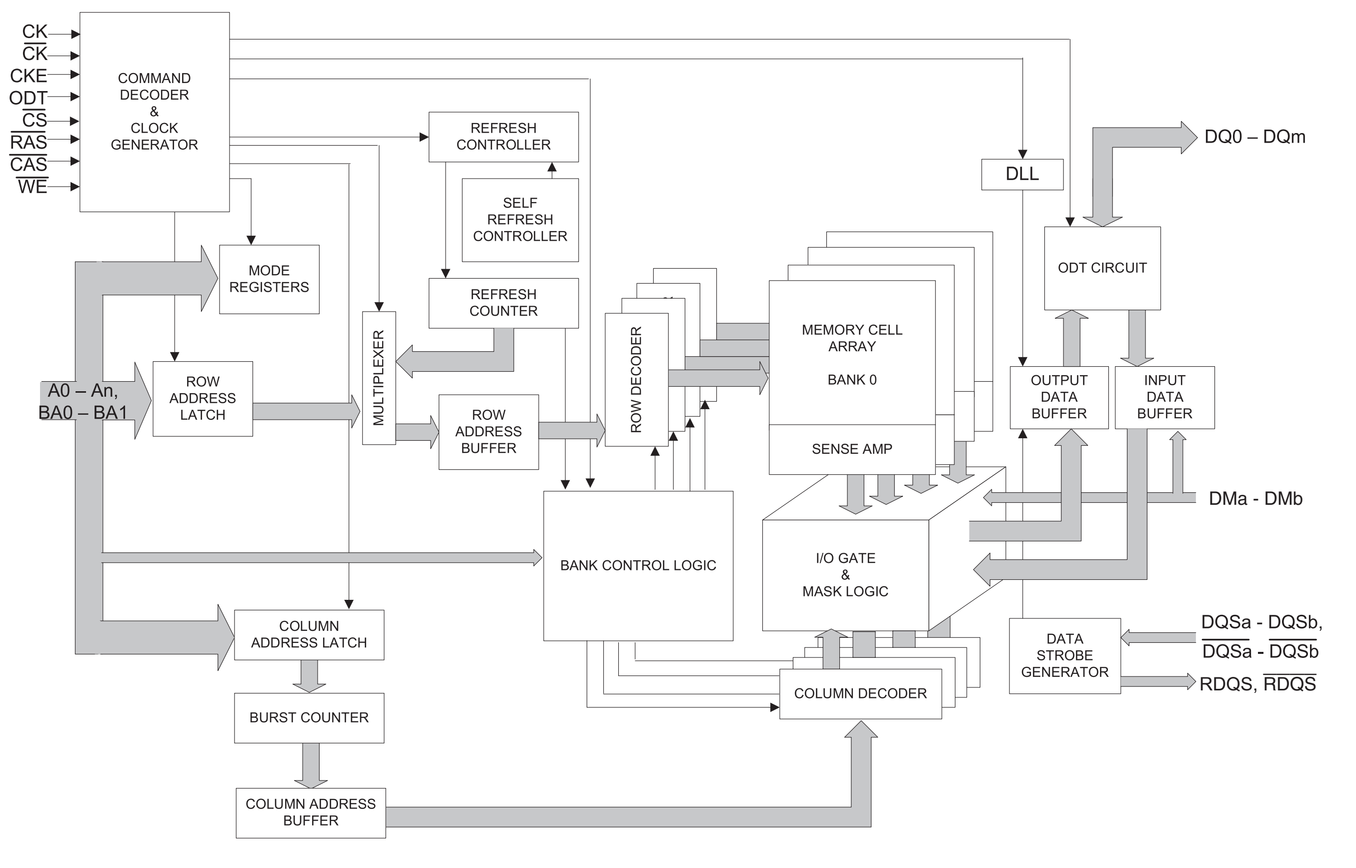
KEY TIMING PARAMETERS

Speed Grade	-25D	-3D
tRCD	12.5	15
tRP	12.5	15
tRC	55	55
tRAS	40	40
tCK @CL=3	5	5
tCK @CL=4	3.75	3.75
tCK @CL=5	2.5	3
tCK @CL=6	2.5	—

GENERAL DESCRIPTION

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the active command are used to select the bank and row to be accessed (BA0-BA1 select the bank; A0-A12(x16) or A0-A13(x8) select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location A0-A9 for the burst access and to determine if the auto precharge A10 command is to be issued. Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

FUNCTIONAL BLOCK DIAGRAM



Notes:
1. An:n = no. of address pins - 1
2. DQm: m = no. of data pins - 1
3. For x8 devices:
DMa - DMb = DM; DQSa - DQSb = DQS; $\overline{\text{DQSa}}$ - $\overline{\text{DQSb}}$ = $\overline{\text{DQS}}$; RDQS, $\overline{\text{RDQS}}$ available only for x8
4. For x16 devices:
DMa - DMb = UDM, LDM; DQSa - DQSb = UDQS, LDQS; $\overline{\text{DQSa}}$ - $\overline{\text{DQSb}}$ = $\overline{\text{UDQS}}$, $\overline{\text{LDQS}}$

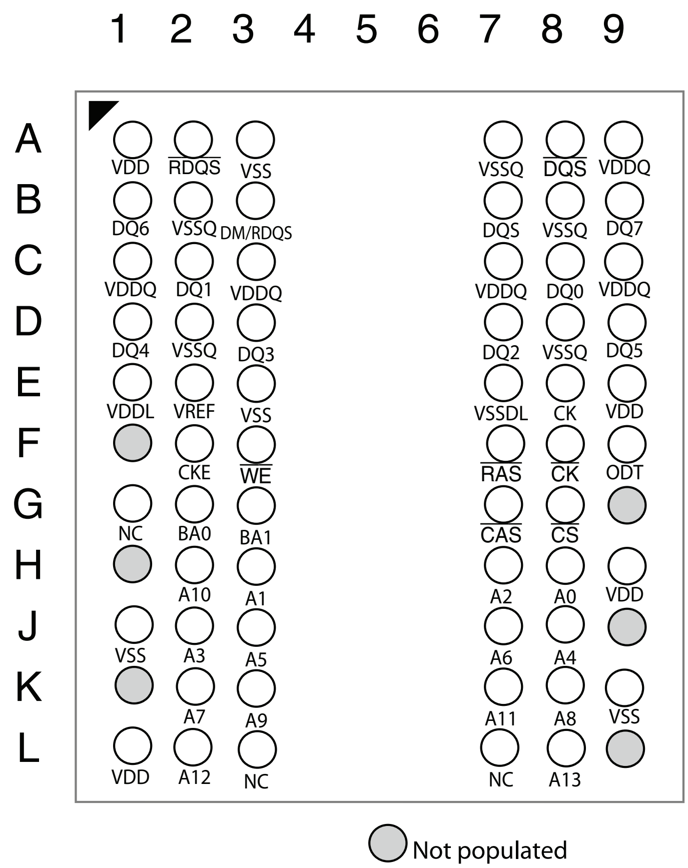
PIN DESCRIPTION TABLE

Symbol	Type	Function
CK, $\overline{CK}$	Input	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates, internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must be maintained to this input. CKE must be maintained HIGH throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	Chip Select: All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is applied to each DQ, DQS, $\overline{DQS}$, DM signals. The ODT pin will be ignored if the EMR(1) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (x8) or UDM, LDM (x16)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8, the function of DM is enabled by EMRS command to EMR(1) [A11].
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or one of the extended mode registers is to be accessed during a MRS or EMRS command cycle.
A0 - A13	Input	Address Inputs: Provide the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0 - BA1. The address inputs also provide the op-code during MRS or EMRS commands.

Symbol	Type	Function
DQ0-7 x8 DQ0-15 x16	Input/ Output	Data Input/Output: Bi-directional data bus.
DQS, ($\overline{DQS}$) RDQS, ($\overline{RDQS}$) x8 UDQS, ($\overline{UDQS}$), LDQS, ($\overline{LDQS}$) x16	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobes DQS(n) may be used in single ended mode or paired with optional complementary signals $\overline{DQS}$(n) to provide differential pair signaling to the system during both reads and writes. A control bit at EMR(1)[A10] enables or disables all complementary data strobe signals. x8 DQS corresponds to the data on DQ0-DQ7 RDQS corresponds to the Read data on DQ0-DQ7, and is enabled by EMRS command to EMR(1) [A11]. x16 LDQS corresponds to the data on DQ0-DQ7 UDQS corresponds to the data on DQ8-DQ15
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.8 V +/- 0.1 V
VSSQ	Supply	DQ Ground
VDDL	Supply	DLL Power Supply: 1.8 V +/- 0.1 V
VSSDL	Supply	DLL Ground
VDD	Supply	Power Supply: 1.8 V +/- 0.1 V
VSS	Supply	Ground
VREF	Supply	Reference voltage

PIN CONFIGURATION

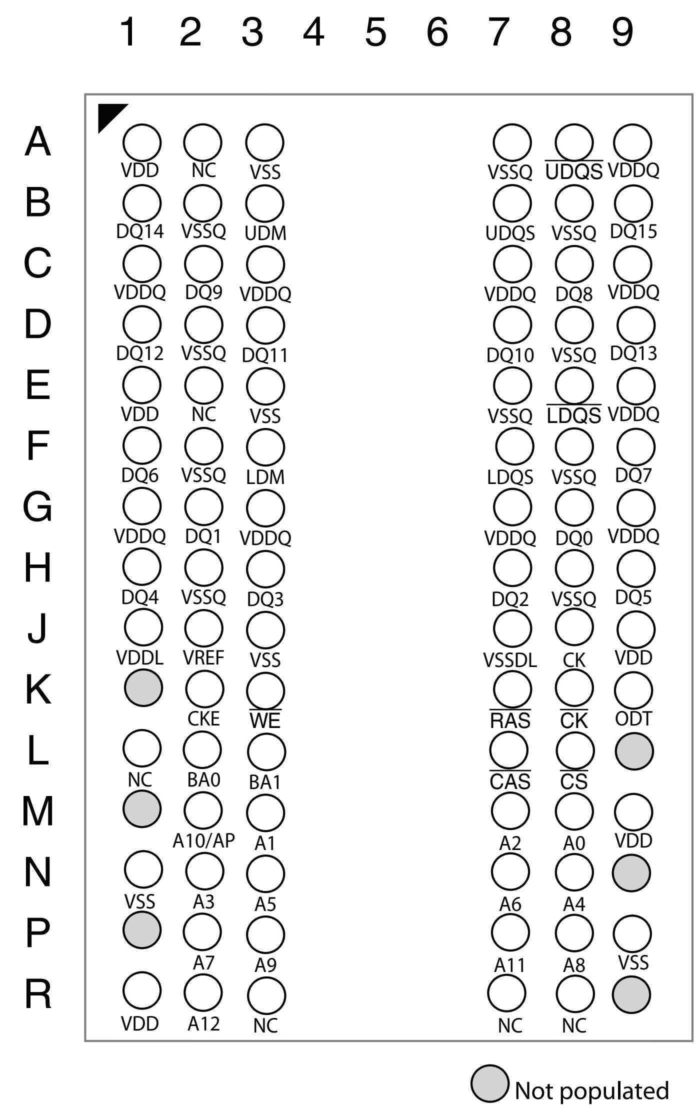
PACKAGE CODE: B 60 BALL FBGA (Top View) (8.00 mm x 10.5 mm Body, 0.8 mm Ball Pitch)



Pin name	Function	Pin name	Function
A0 to A13	Address inputs	ODT	ODT control
BA0, BA1	Bank select	VDD	Supply voltage for internal circuit
DQ0 to DQ7	Data input/output	VSS	Ground for internal circuit
DQS, /DQS	Differential data strobe	VDDQ	Supply voltage for DQ circuit
/CS	Chip select	VSSQ	Ground for DQ circuit
/RAS, /CAS, /WE	Command input	VREF	Input reference voltage
CKE	Clock enable	VDDL	Supply voltage for DLL circuit
CK, /CK	Differential clock input	VSSDL	Ground for DLL circuit
DM	Write data mask	NC	No connection
RDQS, /RDQS	Differential Redundant Data Strobe		

PIN CONFIGURATION

PACKAGE CODE: B 84 BALL FBGA (Top View) (8.00 mm x 12.50 mm Body, 0.8 mm Ball Pitch)



Pin name	Function	Pin name	Function
A0 to A12	Address inputs	ODT	ODT control
BA0, BA1	Bank select	VDD	Supply voltage for internal circuit
DQ0 to DQ15	Data input/output	VSS	Ground for internal circuit
LDQS, UDQS /LDQS, /UDQS	Differential data strobe	VDDQ	Supply voltage for DQ circuit
/CS	Chip select	VSSQ	Ground for DQ circuit
/RAS, /CAS, /WE	Command input	VREF	Input reference voltage
CKE	Clock enable	VDDL	Supply voltage for DLL circuit
CK, /CK	Differential clock input	VSSDL	Ground for DLL circuit
LDM to UDM	Write data mask	NC	No connection

ELECTRICAL SPECIFICATIONS

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on VDD pin relative to Vss	- 1.0 V ~ 2.3 V	V	1,3
V_{DDQ}	Voltage on VDDQ pin relative to Vss	- 0.5 V ~ 2.3 V	V	1,3
V_{DDL}	Voltage on VDDL pin relative to Vss	- 0.5 V ~ 2.3 V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	- 0.5 V ~ 2.3 V	V	1,4
T_{STG}	Storage Temperature	-55 to +150	°C	1, 2

Notes:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be not greater than 0.6 x VDDQ. When VDD and VDDQ and VDDL are less than 500 mV, Vref may be equal to or less than 300 mV.
4. Voltage on any input or I/O may not exceed voltage on VDDQ.

AC & DC Recommended Operating Conditions

Recommended DC Operating Conditions (SSTL-1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	5
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1, 5
VREF	Input Reference Voltage	0.49 x VDDQ	0.50 x VDDQ	0.51 x VDDQ	V	2. 3
VTT	Termination Voltage	VREF - 0.04	VREF	VREF + 0.04	V	4

Notes:
1. There is no specific device VDD supply voltage requirement for SSTL_18 compliance. However under all conditions VDDQ must be less than or equal to VDD.
2. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
3. Peak to peak ac noise on VREF may not exceed +/-2 % VREF(dc).
4. VTT of transmitting device must track VREF of receiving device.
5. VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDL tied together

Operating Temperature Condition

Symbol	Parameter	Rating(1,2,3)	Units
TOPER	Commercial Temperature	T_C = 0 to +85	°C
	Industrial Temperature,	T_C = -40 to +95	°C
	Automotive Temperature (A1)	T_A = -40 to +85	°C
	Automotive Temperature (A2)	T_C = -40 to +105	°C
		T_A = -40 to +105	°C

Notes:
1. T_C = Operating case temperature at center of package
2. T_A = Operating ambient temperature immediately above package center.
3. Both temperature specifications must be met.

Thermal Resistance:

Package	Substrate	Theta-ja (Airflow = 0m/s)	Theta-ja (Airflow = 1m/s)	Theta-ja (Airflow = 2m/s)	Theta-jc	Units
60-ball BGA	4-layer	35.8	32.0	29.8	5.9	C/W
84-ball BGA	4-layer	33.9	30.3	28.3	5.7	C/W

ODT DC Electrical Characteristics

PARAMETER/CONDITION	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
R_{TT} effective impedance value for EMR(1)[A6,A2]=0,1; 75 Ω	R_{TT}1(eff)	60	75	90	Ω	1
R_{TT} effective impedance value for EMR(1)[A6,A2]=1,0; 150 Ω	R_{TT}2(eff)	120	150	180	Ω	1
R_{TT} effective impedance value for EMR(1)[A6,A2]=1,1; 50 Ω	R_{TT}3(eff)	40	50	60	Ω	1
Deviation of VM with respect to VDDQ/2	ΔVM	- 6		+ 6	%	1

Notes:
1. Test condition for R_{TT} measurements

Measurement Definition for R_{TT}(eff): Apply VIH (ac) and VIL (ac) to test pin separately, then measure current I(VIH (ac)) and I(VIL (ac)) respectively. VIH (ac), VIL (ac), and VDDQ values defined in SSTL_18

$$R_{TT}\,(eff) \quad \frac{V_{IH}\,(ac) - V_{IL}\,(ac)}{I(V_{IH}\,(ac)) - I(V_{IL}\,(ac))}$$

Measurement Definition for VM: Measure voltage (VM) at test pin (midpoint) with no load.

ΔVM = [(2 x VM / VDDQ) - 1] x 100%

Input DC logic level

Symbol	Parameter	Min.	Max.	Units	Notes
VIH(dc)	dc input logic HIGH	VREF + 0.125	VDDQ + 0.3	V	
VIL(dc)	dc input logic LOW	- 0.3	VREF - 0.125	V	

Input AC logic level

Symbol	Parameter	DDR2-400, DDR2-533		DDR2-667, DDR2-800		Units	Notes
		Min.	Max.	Min.	Max		
VIH (ac)	ac input logic HIGH	VREF + 0.250	VDDQ + Vpeak	VREF + 0.200	VDDQ + Vpeak	V	1
VIL (ac)	ac input logic LOW	VSSQ - Vpeak	VREF - 0.250	VSSQ - Vpeak	VREF - 0.200	V	1

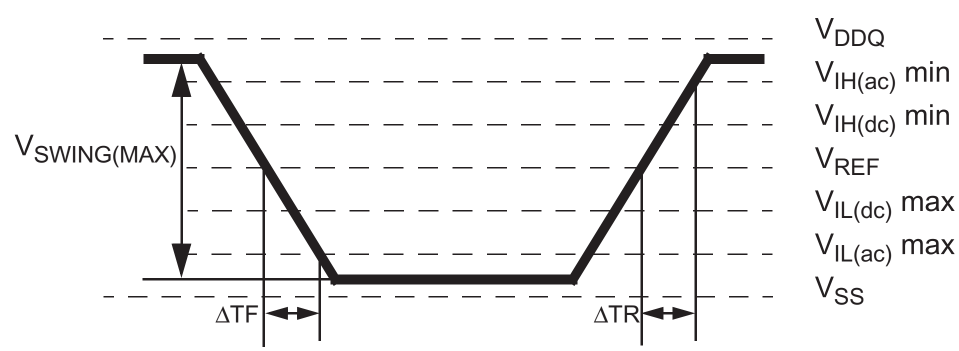
Notes:
1. Refer to Overshoot/undershoot specifications for Vpeak value: maximum peak amplitude allowed for overshoot and undershoot.

AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
VREF	Input reference voltage	0.5 x VDDQ	V	1
VSWING(MAX)	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Notes:
1. Input waveform timing is referenced to the input signal crossing through the VIH/IL(AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from VREF to VIH(ac) min for rising edges and the range from VREF to VIL(ac) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.

AC input test signal waveform



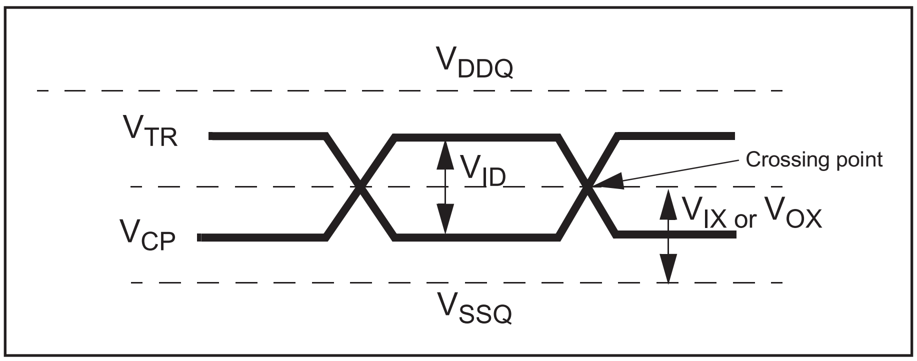
$$\text{Falling Slew} = \frac{V_{REF} - V_{IL(ac)}\ \text{max}}{\Delta TF} \qquad \text{Rising Slew} = \frac{V_{IH(ac)}\ \text{min} - V_{REF}}{\Delta TR}$$

Differential input AC Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
VID (ac)	ac differential input voltage	0.5	VDDQ	V	1,3
VIX (ac)	ac differential crosspoint voltage	0.5 x VDDQ - 0.175	0.5 x VDDQ + 0.175	V	2

Notes:
1. VID(AC) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input signal (such as CK, DQS and VCP is the complementary input signal (such as CK or DQS). The minimum value is equal to VIH(AC) - VIL(AC).
2. The typical value of VIX(AC) is expected to be about 0.5 x VDDQ of the transmitting device and VIX(AC) is expected to track variations in VDDQ. VIX(AC) indicates the voltage at which differential input signals must cross.
3. Refer to Overshoot/undershoot specifications for Vpeak value: maximum peak amplitude allowed for overshoot and undershoot.

Differential signal levels



Differential AC Output Parameters

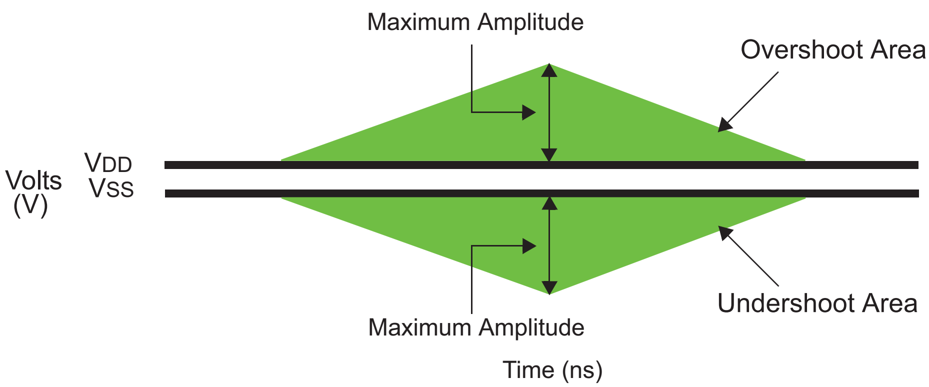
Symbol	Parameter	Min.	Max.	Units	Notes
VOX (ac)	ac differential crosspoint voltage	0.5 x VDDQ - 0.125	0.5 x VDDQ + 0.125	V	1

Note:
1. The typical value of VOX(AC) is expected to be about 0.5 x VDDQ of the transmitting device and VOX(AC) is expected to track variations in VDDQ. VOX(AC) indicates the voltage at which differential output signals must cross.

OVERSHOOT/UNDERSHOOT SPECIFICATION

AC overshoot/undershoot specification for Address and Control pins

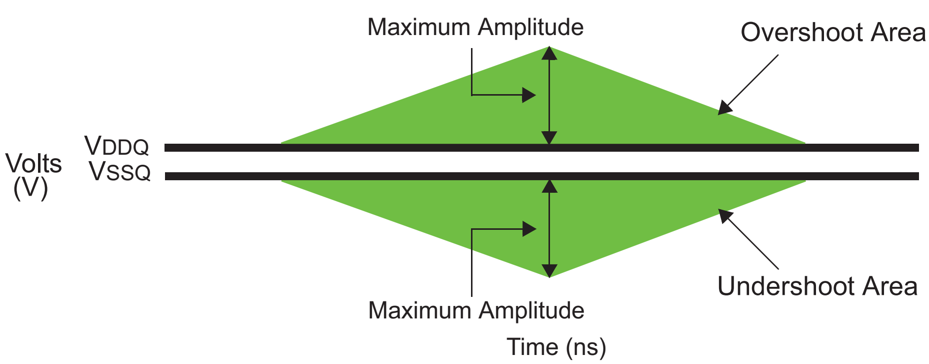
Parameter	Specification			
	DDR2-400	DDR2-533	DDR2-667	DDR2-800
Maximum peak amplitude allowed for overshoot area	0.5V	0.5V	0.5V	0.5V
Maximum peak amplitude allowed for undershoot area	0.5V	0.5V	0.5V	0.5V
Maximum overshoot area above VDD (see figure below)	1.33 V-ns	1.0 V-ns	0.8 V-ns	0.66 V-ns
Maximum undershoot area below VSS (see figure below)	1.33 V-ns	1.0 V-ns	0.8 V-ns	0.66 V-ns



AC overshoot and undershoot definition for address and control pins

AC overshoot/undershoot specification for Clock, Data, Strobe, and Mask pins: DQ, ($\overline{\text{U/L/R}}$) $\overline{\text{DQS}}$, (U/L/R) DQS, DM, CK, $\overline{\text{CK}}$

Parameter	Specification			
	DDR2-400	DDR2-533	DDR2-667	DDR2-800
Maximum peak amplitude allowed for overshoot area	0.5V	0.5V	0.5V	0.5V
Maximum peak amplitude allowed for undershoot area	0.5V	0.5V	0.5V	0.5V
Maximum overshoot area above VDDQ (See Figure below)	0.38 V-ns	0.28 V-ns	0.23 V-ns	0.23 V-ns
Maximum undershoot area below VSSQ (See Figure below)	0.38 V-ns	0.28 V-ns	0.23 V-ns	0.23 V-ns



AC overshoot and undershoot definition for clock, data, strobe, and mask pins

Output Buffer Characteristics

Output AC Test Conditions

Symbol	Parameter	SSTL_18	Units	Notes
VOTR	Output Timing Measurement Reference Level	0.5 x VDDQ	V	1

Output DC Current Drive

Symbol	Parameter	SSTL_18	Units	Notes
IOH(dc)	Output Minimum Source DC Current	- 13.4	mA	1, 3, 4
IOL(dc)	Output Minimum Sink DC Current	13.4	mA	2, 3, 4

Notes:
1. VDDQ = 1.7 V; VOUT = 1420 mV. (VOUT - VDDQ)/IOH must be less than 21 Ω for values of VOUT between VDDQ and VDDQ - 280 mV.
2. VDDQ = 1.7 V; VOUT = 280 mV. VOUT/IOL must be less than 21 Ω for values of VOUT between 0 V and 280 mV.
3. The dc value of VREF applied to the receiving device is set to VTT
4. The values of IOH(dc) and IOL(dc) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure VIH min plus a noise margin and VIL max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see Section 3.3 of JESD8-15A) along a 21 Ω load line to define a convenient driver current for measurement.

OCD Default Characteristics

Description	Parameter	Min	Nom	Max	Unit	Notes
Output impedance		See full strength default driver characteristics			Ω	1
Output impedance step size for OCD calibration		0		1.5	Ω	6
Pull-up and pull-down mismatch		0		4	Ω	1,2,3
Output slew rate	Sout	1.5		5	V/ns	1,4,5,7,8,9

Notes:
1. Absolute Specifications (TOPER; VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V). DRAM I/O specifications for timing, voltage, and slew rate are no longer applicable if OCD is changed from default settings.
2. Impedance measurement condition for output source dc current: VDDQ = 1.7 V; VOUT = 1420 mV; (VOUTVDDQ)/IOH must be less than 23.4 Ω for values of VOUT between VDDQ and VDDQ - 280 mV. Impedance measurement condition for output sink dc current: VDDQ = 1.7 V; VOUT = 280 mV; VOUT/IOL must be less than 23.4 Ω for values of VOUT between 0 V and 280 mV.
3. Mismatch is absolute value between pull-up and pull-down, both are measured at same temperature and voltage.
4. Slew rate measured from VIL(ac) to VIH(ac).
5. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.
6. This represents the step size when the OCD is near 18 Ω at nominal conditions across all process corners/variations and represents only the DRAM uncertainty. A 0 Ω value (no calibration) can only be achieved if the OCD impedance is 18 Ω +/-0.75 Ω under nominal conditions.
7. DRAM output slew rate specification applies to 400 MT/s, 533 MT/s & 667 MT/s speed bins.
8. Timing skew due to DRAM output slew rate mis-match between DQS / DQS and associated DQ's is included in tDQSQ and tQHS specification.
9. DDR2 SDRAM output slew rate test load is defined in General Note 3 of the AC Timing specification Table.

IDD Specifications & Test Conditions

Symbol	Conditions		-25D/-25E DDR2-800D/800E	-3D DDR2-667D	-37C DDR2-533C	-5B DDR2-400B	Units
IDD0	Operating one bank active-precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		135	120	110	110	mA
IDD1	Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		165	150	135	130	mA
IDD2P	Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		13	11	10	10	mA
IDD2Q	Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		80	70	60	50	mA
IDD2N	Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		95	85	75	65	mA
IDD3P	Active power-down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Power Down Fast Exit	40	45	30	35	mA
		Power Down Slow Exit	25	25	25	25	
IDD3N	Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		80	70	60	75	mA
IDD4W	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		360	290	240	210	mA

IDD Specifications & Test Conditions (continued)

Symbol	Conditions	-25D/-25E	-3D	-37C	-5B	Units
		DDR2-800D/800E	DDR2-667D	DDR2-533C	DDR2-400B	
IDD4R	Operating burst read current; All banks open, Continuous burst reads, IOUT = 0 mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	345	275	230	190	mA
IDD5B	Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	230	185	175	170	mA
IDD6	Self refresh current; CK and CK at 0 V; CKE ≤ 0.2 V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	3	3	3	3	mA
IDD7	Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD) - 1 x tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1 x tCK(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R	370	350	340	265	mA

Notes:
1. IDD specifications are tested after the device is properly initialized
2. Input slew rate is specified by AC Parametric Test Condition
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, $\overline{\text{DQS}}$, RDQS, $\overline{\text{RDQS}}$, LDQS, $\overline{\text{LDQS}}$, UDQS, and $\overline{\text{UDQS}}$. IDD values must be met with all combinations of EMR(1) bits 10 and 11.
5. For DDR2-667/800 testing, tCK in the Conditions should be interpreted as tCK(avg)
6. Definitions for IDD

LOW = Vin ≤ VILAC(max)
HIGH = Vin ≥ VIHAC(min)
STABLE = inputs stable at a HIGH or LOW level
FLOATING = inputs at VREF = VDDQ/2
SWITCHING = inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

7. The -25E, -37C, and-5B device specifications are shown for reference only.

IDD testing parameters

Speed	DDR2-800D	DDR2-667D	Units
Bin(CL-tRCD-tRP)	5-5-5	5-5-5	
CL(IDD)	5	5	tCK
tRCD(IDD)	12.5	15	ns
tRC(IDD)	55	55	ns
tRRD(IDD) x8	7.5	7.5	ns
tRRD(IDD) x16	10	10	ns
tCK(IDD)	2.5	3	ns
tRASmin(IDD)	40	40	ns
tRASmax(IDD)	70	70	µs
tRP(IDD)	12.5	15	ns
tRFC(IDD)	105	105	ns

Input/Output Capacitance:

Parameter	Symbol	DDR2-400 DDR2-553		DDR2-667		DDR2-800		Units
		Min.	Max.	Min.	Max	Min.	Max.	
Input capacitance, CK and $\overline{CK}$	CCK	1.0	2.0	1.0	2.0	1.0	2.0	pF
Input capacitance delta, CK and $\overline{CK}$	CDCK	–	0.25	–	0.25	–	0.25	pF
Input capacitance, all other input-only pins	CI	1.0	2.0	1.0	2.0	1.0	1.75	pF
Input capacitance delta, all other input-only pins	CDI	–	0.25	–	0.25	–	0.25	pF
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	2.5	4.0	2.5	3.5	2.5	3.5	pF
Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	CDIO	–	0.5	–	0.5	–	0.5	pF

Electrical Characteristics & AC Timing Specifications

Refresh parameters (TOPER; VDDQ = 1.8 V +/- 0.1 V; VDD = 1.8 V +/- 0.1 V)

Parameter	Symbol			Units	Notes
Refresh to active/Refresh command time	tRFC		105	ns	1
Average periodic refresh interval	tREFI	-40°C ≤ Tc < 0°C	7.8	µs	1,2
		0°C ≤ Tc ≤ 85°C	7.8	µs	1
		85°C < Tc ≤ 95°C	3.9	µs	1,2
		95°C < Tc ≤ 105°C	3.9	µs	1,2,3

Notes:
1. If refresh timing is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
2. Specified for Industrial and Automotive grade only; not applicable for Commercial grade. TOPER may not be violated.
3. Specified for Automotive grade (A2) only; not applicable for any other grade. TOPER may not be violated.

Key Timing Parameters by Speed Grade

	-25D	-25E	-3D	-37C	-5B
Speed bin (JEDEC)	DDR2-800D	DDR2-800E	DDR2-667D	DDR2-533C	DDR2-400B
CL-tRCD-tRP	5-5-5	6-6-6	5-5-5	4-4-4	3-3-3
tRCD	12.5	15	15	15	15
tRP	12.5	15	15	15	15
tRC	55	55	55	55	55
tRAS	40	40	40	40	40
tCK(avg)@CL=3	5	5	5	5	5
tCK(avg)@CL=4	3.75	3.75	3.75	3.75	5
tCK(avg)@CL=5	2.5	3	3	–	–
tCK(avg)@CL=6	2.5	2.5	–	–	–

Note:
Each of the -25D and -3D speed options is individually backward compatible with all the timing specifications for slower options (ie. -25D complies with specifications for -25D, -25E, -3D, -37C, -5B). -25E, -37C, and -5B shown for reference only.

Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)

(For information related to the entries in this table, refer to both the Guidelines and the Specific Notes following this Table.)

Parameter	Symbol	DDR2-400		DDR2-553		Units	Notes
		Min.	Max.	Min.	Max		
Clock cycle time, CL=x	tCK	5	8	3.75	8	ns	15
CK HIGH pulse width	tCH	0.45	0.55	0.45	0.55	tCK	
CK LOW pulse width	tCL	0.45	0.55	0.45	0.55	tCK	
DQS latching rising transitions to associated clock edges	tDQSS	- 0.25	0.25	- 0.25	0.25	tCK	
DQS falling edge to CK setup time	tDSS	0.2	–	0.2	–	tCK	
DQS falling edge hold time from CK	tDSH	0.2	–	0.2	–	tCK	
DQS input HIGH pulse width	tDQSH	0.35	–	0.35	–	tCK	
DQS input LOW pulse width	tDQSL	0.35	–	0.35	–	tCK	
Write preamble	tWPRE	0.35	–	0.35	–	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	10
Address and control input setup time	tIS(base)	350	–	250	–	ps	5, 7, 9, 22
Address and control input hold time	tIH(base)	475	–	375	–	ps	5, 7, 9, 23
Control & Address input pulse width for each input	tIPW	0.6	–	0.6	–	tCK	
DQ and DM input setup time (differential strobe)	tDS(base)	150	–	100	–	ps	6, 7, 8, 20, 28
DQ and DM input hold time (differential strobe)	tDH(base)	275	–	225	–	ps	6, 7, 8, 21, 28
DQ and DM input setup time (single-ended strobe)	tDS1(base)	25	–	- 25	–	ps	6, 7, 8, 25
DQ and DM input hold time (single-ended strobe)	tDH1(base)	25	–	- 25	–	ps	6, 7, 8, 26
DQ and DM input pulse width for each input	tDIPW	0.35	–	0.35	–	tCK	
DQ output access time from CK/$\overline{CK}$	tAC	- 600	+ 600	- 500	+ 500	ps	
DQS output access time from CK/ $\overline{CK}$	tDQSCK	- 500	+ 500	- 450	+ 450	ps	
Data-out high-impedance time from CK/ $\overline{CK}$	tHZ	–	tAC max	–	tAC max	ps	18
DQS($\overline{DQS}$) low-impedance time from CK/ $\overline{CK}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	ps	18
DQ low-impedance time from CK/ $\overline{CK}$	tLZ(DQ)	2 x tAC min	tAC max	2 x tAC min	tAC max	ps	18
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	–	350	–	300	ps	13
CK half pulse width	tHP	min (tCL, tCH)	–	min (tCL, tCH)	–	ps	11,12
DQ hold skew factor	tQHS	–	450	–	400	ps	12
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	–	tHP - tQHS	–	ps	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	19
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	19

Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) cont'd

(For information related to the entries in this table, refer to both the Guidelines and the Specific Notes following this Table.)

Parameter	Symbol		DDR2-400		DDR2-533		Units	Notes
			Min.	Max.	Min.	Max.		
Active to active command period	tRRD	x8	7.5	–	7.5	–	ns	4
		x16	10	–	10	–		
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD		2	–	2	–	tCK	
Write recovery time	tWR		15	–	15	–	ns	
Auto precharge write recovery + precharge time	tDAL		WR + tRP	–	WR + tRP	–	tCK	14
Internal write to read command delay	tWTR		10	–	7.5	–	ns	24
Internal read to precharge command delay	tRTP		7.5	–	7.5	–	ns	3
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE		3	–	3	–	tCK	27
Exit self refresh to a non-read command	tXSNR		tRFC + 10	–	tRFC + 10	–	ns	
Exit self refresh to a read command	tXSRD		200	–	200	–	tCK	
Exit precharge power down to any non-read command	tXP		2	–	2	–	tCK	
Exit active power down to read command	tXARD		2	–	2	–	tCK	1
Exit active power down to read command (slow exit, lower power)	tXARDS		6 - AL	–	6 - AL	–	tCK	1,2
ODT turn-on delay	tAOND		2	2	2	2	tCK	16
ODT turn-on	tAON		tAC(min)	tAC(max)+1	tAC(min)	tAC (max)+1	ns	16
ODT turn-on (Power-Down mode)	tAONPD		tAC(min)+2	2 x tCK + tAC(max)+1	tAC(min) + 2	2 x tCK + tAC(max)+1	ns	
ODT turn-off delay	tAOFD		2.5	2.5	2.5	2.5	tCK	17, 44
ODT turn-off	tAOF		tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	ns	17, 44
ODT turn-off (Power-Down mode)	tAOFPD		tAC(min)+2	2.5 x tCK + tAC(max)+1	tAC(min)+2	2.5 x tCK+ tAC(max)+1	ns	
ODT to power down entry latency	tANPD		3	–	3	–	tCK	
ODT power down exit latency	tAXPD		8	–	8	–	tCK	
Mode register set command cycle time	tMRD		2	–	2	–	tCK	
MRS command to ODT update delay	tMOD		0	12	0	12	ns	
OCD drive mode output delay	tOIT		0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay		tIS+tCK+tIH	–	tIS+tCK+tIH	–	ns	15

Timing Parameters by Speed Grade (DDR2-667 and DDR2-800)

(For information related to the entries in this table, refer to both the Guidelines and the Specific Notes following this Table.)

Parameter	Symbol	DDR2-667		DDR2-800		Units	Notes
		Min.	Max.	Min.	Max		
Average clock period	tCK(avg)	3	8	2.5	8	ns	35,36
Average clock HIGH pulse width	tCH(avg)	0.45	0.55	0.45	0.55	tCK(avg)	35,36
Average clock LOW pulse width	tCL(avg)	0.45	0.55	0.45	0.55	tCK(avg)	35,36
DQS latching rising transitions to associated clock edges	tDQSS	- 0.25	0.25	- 0.25	0.25	tCK(avg)	30
DQS falling edge to CK setup time	tDSS	0.2	–	0.2	–	tCK(avg)	30
DQS falling edge hold time from CK	tDSH	0.2	–	0.2	–	tCK(avg)	30
DQS input HIGH pulse width	tDQSH	0.35	–	0.35	–	tCK(avg)	
DQS input LOW pulse width	tDQSL	0.35	–	0.35	–	tCK(avg)	
Write preamble	tWPRE	0.35	–	0.35	–	tCK(avg)	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK(avg)	10
Address and control input setup time	tIS(base)	200	–	175	–	ps	5, 7, 9, 22, 29
Address and control input hold time	tIH(base)	275	–	250	–	ps	5, 7, 9, 23, 29
Control & Address input pulse width for each input	tIPW	0.6	–	0.6	–	tCK(avg)	
DQ and DM input setup time	tDS(base)	50	–	50	–	ps	6, 7, 8, 20, 28, 31
DQ and DM input hold time	tDH(base)	175	–	125	–	ps	6, 7, 8, 21, 28, 31
DQ and DM input pulse width for each input	tDIPW	0.35	–	0.35	–	tCK(avg)	
DQ output access time from CK/CK	tAC	- 450	450	- 400	400	ps	40
DQS output access time from CK/CK	tDQSCK	- 400	400	- 350	350	ps	40
Data-out high-impedance time from CK/CK	tHZ	–	tAC,max	–	tAC, max	ps	18,40
DQS/DQS low-impedance time from CK/CK	tLZ(DQS)	tAC,min	tAC,max	tAC,min	tAC, max	ps	18,40
DQ low-impedance time from CK/CK	tLZ(DQ)	2 x tAC,min	tAC,max	2 x tAC,min	tAC, max	ps	18,40
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	–	240	–	200	ps	13
CK half pulse width	tHP	Min(tCH(abs), tCL(abs))	–	Min(tCH(abs), tCL(abs))	–	ps	37
DQ hold skew factor	tQHS	–	340	–	300	ps	38
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	–	tHP - tQHS	–	ps	39
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK(avg)	19,41
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK(avg)	19,42

Timing parameters by speed grade (DDR2-667 and DDR2-800) cont'd

(For information related to the entries in this table, refer to both the Guidelines and the Specific Notes following this Table.)

Parameter	Symbol		DDR2-667		DDR2-800		Units	Notes
			Min.	Max	Min.	Max.		
Activate to activate command period	tRRD	x8	7.5	–	7.5	–	ns	4,32
		x16	10	–	10	–		
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD		2	–	2	–	nCK	
Write recovery time	tWR		15	–	15	–	ns	32
Auto precharge write recovery + precharge time	tDAL		WR + tnRP	–	WR + tnRP	–	nCK	33
Internal write to read command delay	tWTR		7.5	–	7.5	–	ns	24, 32
Internal read to precharge command delay	tRTP		7.5	–	7.5	–	ns	3, 32
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE		3	–	3	–	nCK	27
Exit self refresh to a non-read command	tXSNR		tRFC + 10	–	tRFC + 10	–	ns	32
Exit self refresh to a read command	tXSRD		200	–	200	–	nCK	
Exit precharge power down to any command	tXP		2	–	2	–	nCK	
Exit active power down to read command	tXARD		2	–	2	–	nCK	1
Exit active power down to read command (slow exit, lower power)	tXARDS		7 - AL	–	8 - AL	–	nCK	1, 2
ODT turn-on delay	tAOND		2	2	2	2	nCK	16
ODT turn-on	tAON		tAC, min	tAC,max + 0.7	tAC,min	tAC,max + 0.7	ns	6, 16, 40
ODT turn-on (Power-Down mode)	tAONPD		tAC, min + 2	2 x tCK(avg) + tAC,max + 1	tAC,min + 2	2 x tCK(avg) + tAC,max + 1	ns	
ODT turn-off delay	tAOFD		2.5	2.5	2.5	2.5	nCK	17, 45
ODT turn-off	tAOF		tAC, min	tAC,max + 0.6	tAC,min	tAC,max + 0.6	ns	17, 43, 45
ODT turn-off (Power-Down mode)	tAOFPD		tAC, min+2	2.5 x tCK(avg) + tAC,max + 1	tAC,min+2	2.5 x tCK(avg) + tAC,max + 1	ns	
ODT to power down entry latency	tANPD		3	–	3	–	nCK	
ODT Power Down Exit Latency	tAXPD		8	–	8	–	nCK	
Mode register set command cycle time	tMRD		2	–	2	–	nCK	
OCD drive mode output delay	tOIT		0	12	0	12	ns	32
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay		tIS + tCK(avg) + tIH	–	tIS + tCK(avg) + tIH	–	ns	15

Guidelines for AC Parameters

1. DDR2 SDRAM AC Timing Reference Load

Figure "AC Timing Reference Load" represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment or a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

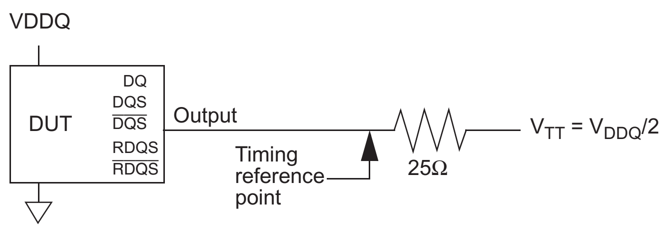


Figure - AC Timing Reference Load

The output timing reference voltage level for single ended signals is the crosspoint with VTT. The output timing reference voltage level for differential signals is the crosspoint of the true (e.g. DQS) and the complement (e.g. DQS) signal.

2. Slew Rate Measurement Levels

a) Output slew rate for falling and rising edges is measured between VTT - 250 mV and VTT + 250 mV for single ended signals. For differential signals (e.g. DQS - $\overline{DQS}$) output slew rate is measured between DQS - $\overline{DQS}$ = - 500 mV and DQS - $\overline{DQS}$ = + 500 mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

b) Input slew rate for single ended signals is measured from Vref(dc) to VIH(ac),min for rising edges and from Vref(dc) to VIL(ac),max for falling edges.

For differential signals (e.g. CK - $\overline{CK}$) slew rate for rising edges is measured from CK - $\overline{CK}$ = - 250 mV to CK - $\overline{CK}$ = + 500 mV (+ 250 mV to - 500 mV for falling edges).

c) VID is the magnitude of the difference between the input voltage on CK and the input voltage on CK, or between DQS and $\overline{DQS}$ for differential strobe.

3. DDR2 SDRAM output slew rate test load

Output slew rate is characterized under the test conditions as shown in Figure "Slew Rate Test Load".

4. Differential data strobe

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing

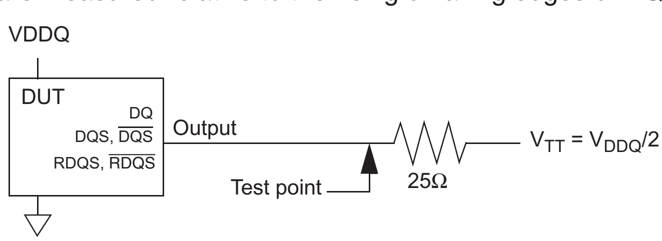
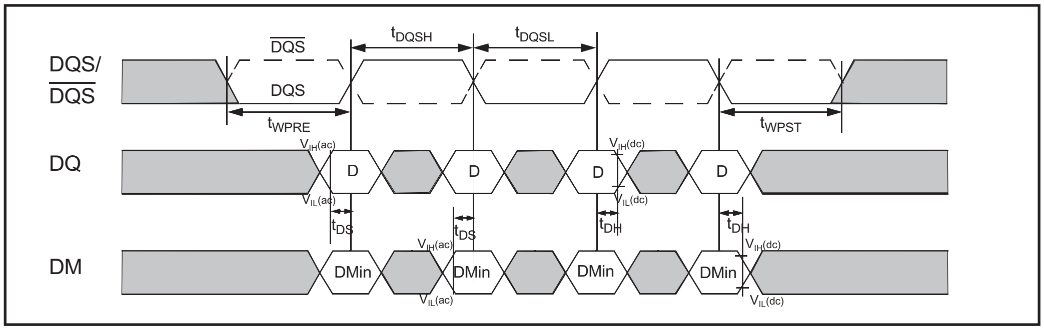
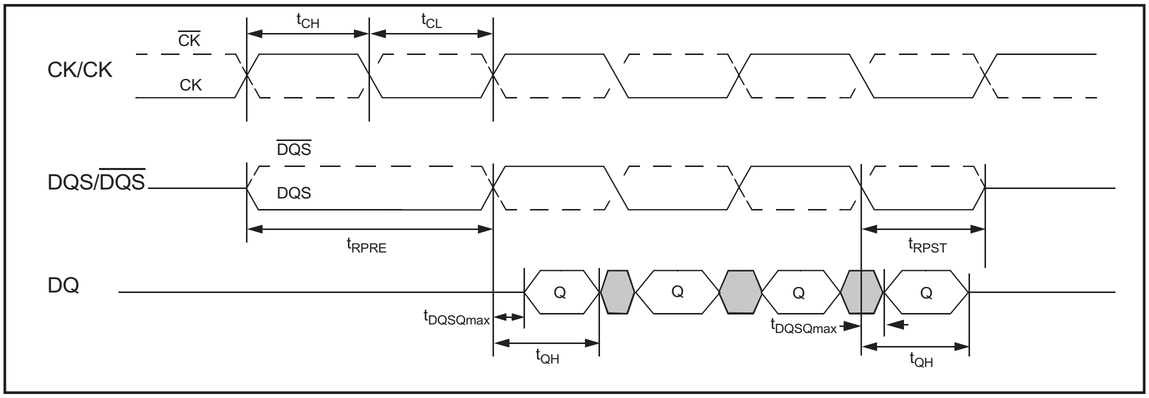


Figure - Slew Rate Test Load

relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 Ω to 10 kΩ resistor to insure proper operation.



Data Input (Write) Timing



Data Output (Read) Timing

5. AC timings are for linear signal transitions. See Specific Notes on derating for other signal transitions.

6. All voltages are referenced to VSS.

7. These parameters guarantee device behavior, but they are not necessarily tested on each device They may be guaranteed by device design or tester correlation.

8. Tests for AC timing, IDD, and electrical (AC and DC) characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

Specific Notes for Dedicated AC Parameters

1. User can choose which active power down exit timing to use via Mode Register Set [A12]. tXARD is expected to be used for fast active power down exit timing. tXARDS is expected to be used for slow active power down exit timing.

2. AL = Additive Latency.

3. This is a minimum requirement. Minimum read to precharge timing is AL + BL / 2 provided that the tRTP and tRAS(min) have been satisfied.

4. A minimum of two clocks (2 x tCK or 2 x nCK) is required irrespective of operating frequency.

5. Timings are specified with command/address input slew rate of 1.0 V/ns. See Specific Notes on derating for other slew rate values.

6. Timings are specified with DQs, DM, and DQS's (DQS/RDQS in single ended mode) input slew rate of 1.0V/ns. See Specific Notes on derating for other slew rate values.

7. Timings are specified with CK/CK differential slew rate of 2.0 V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0 V/ns in differential strobe mode and a slew rate of 1 V/ns in single ended mode. See Specific Notes on derating for other slew rate values.

8. Data setup and hold time derating (tDS, tDH).

ΔtDS, ΔtDH derating values for DDR2-400, DDR2-553 (All units in 'ps'; the note applies to the entire table)																			
		DQS, $\overline{DQS}$ Differential Slew Rate																	
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	125	45	125	45	125	45	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	83	21	83	21	83	21	95	33	-	-	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
	0.9	-	-	-11	-14	-11	-14	1	-2	13	10	25	22	-	-	-	-	-	-
	0.8	-	-	-	-	-25	-31	-13	-19	-1	-7	11	5	23	17	-	-	-	-
	0.7	-	-	-	-	-	-	-31	-42	-19	-30	-7	-18	5	-6	17	6	-	-
	0.6	-	-	-	-	-	-	-	-	-43	-59	-31	-47	-19	-35	-7	-23	5	-11
	0.5	-	-	-	-	-	-	-	-	-	-	-74	-89	-62	-77	-50	-65	-38	-53
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-127	-140	-115	-128	-103	-116

DDR2-400/533 tDS/tDH derating with differential data strobe

ΔtDS, ΔtDH derating values for DDR2-667, DDR2-800 (All units in 'ps'; the note applies to the entire table)																			
		DQS, $\overline{DQS}$ Differential Slew Rate																	
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	100	45	100	45	100	45	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	67	21	67	21	67	21	79	33	-	-	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
	0.9	-	-	-5	-14	-5	-14	7	-2	19	10	31	22	-	-	-	-	-	-
	0.8	-	-	-	-	-13	-31	-1	-19	11	-7	23	5	35	17	-	-	-	-
	0.7	-	-	-	-	-	-	-10	-42	2	-30	14	-18	26	-6	38	6	-	-
	0.6	-	-	-	-	-	-	-	-	-10	-59	2	-47	14	-35	26	-23	38	-11
	0.5	-	-	-	-	-	-	-	-	-	-	-24	-89	-12	-77	0	-65	12	-53
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-52	-140	-40	-128	-28	-116

DDR2-667/800 tDS/tDH derating with differential data strobe

ΔtDS1, ΔtDH1 derating values for DDR2-400, DDR2-533 (All units in 'ps'; the note applies to the entire table)																			
		DQS, Single-ended Slew Rate																	
		2.0 V/ns		1.5 V/ns		1.0 V/ns		0.9 V/ns		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 V/ns		0.4 V/ns	
		ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1
DQ Slew rate V/ns	2.0	188	167	145	125	63	-	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	146	167	125	125	83	42	81	43	-	-	-	-	-	-	-	-	-	-
	1.0	63	125	42	83	0	0	-2	1	-7	-13	-	-	-	-	-	-	-	-
	0.9	-	-	31	69	-11	-14	-13	-13	-18	-27	-29	-45	-	-	-	-	-	-
	0.8	-	-	-	-	-25	-31	-27	-30	-32	-44	-43	-62	-60	-86	-	-	-	-
	0.7	-	-	-	-	-	-	-45	-53	-50	-67	-61	-85	-78	-109	-108	-152	-	-
	0.6	-	-	-	-	-	-	-	-	-74	-96	-85	-114	-102	-138	-132	-181	-183	-246
	0.5	-	-	-	-	-	-	-	-	-	-	-128	-156	-145	-180	-175	-223	-226	-288
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-210	-243	-240	-286	-291	-351

DDR2-400/533 tDS1/tDH1 derating with single-ended data strobe

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value to the ΔtDS and ΔtDH derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of Vih(ac)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of VREF(dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to VREF(dc) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).

For slew rates in between the values listed in the "Data Setup and Hold Time Derating" tables, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

9. Input Setup and Hold Time Derating (tIS, tIH)

tIS, tIH Derating Values for DDR2-400, DDR2-533									
CK, /CK Differential Slew Rate									
		2.0 V/ns		1.5 V/ns		1.0 V/ns		Units	Notes
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH		
Command/ Address Slew rate (V/ns)	4.0	187	94	217	124	247	154	ps	1
	3.5	179	89	209	119	239	149	ps	1
	3	167	83	197	113	227	143	ps	1
	2.5	150	75	180	105	210	135	ps	1
	2.0	125	45	155	75	185	105	ps	1
	1.5	83	21	113	51	143	81	ps	1
	1.0	0	0	30	30	60	60	ps	1
	0.9	-11	-14	19	16	49	46	ps	1
	0.8	-25	-31	5	-1	35	29	ps	1
	0.7	-43	-54	-13	-24	17	6	ps	1
	0.6	-67	-83	-37	-53	-7	-23	ps	1
	0.5	-110	-125	-80	-95	-50	-65	ps	1
	0.4	-175	-188	-145	-158	-115	-128	ps	1
	0.3	-285	-292	-255	-262	-225	-232	ps	1
	0.25	-350	-375	-320	-345	-290	-315	ps	1
	0.2	-525	-500	-495	-470	-465	-440	ps	1
	0.15	-800	-708	-770	-678	-740	-648	ps	1
	0.1	-1450	-1125	-1420	-1095	-1390	-1065	ps	1