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IS43/46LD16640A
IS43/46LD32320A

1Gb (x16, x32) Mobile LPDDR2 S4 SDRAM

AUGUST 2014

FEATURES

- Low-voltage Core and I/O Power Supplies VDD2 = 1.14-1.30V, VDDCA/VDDQ = 1.14-1.30V, VDD1 = 1.70-1.95V
- High Speed Un-terminated Logic(HSUL_12) I/O Interface
- Clock Frequency Range : 10MHz to 400MHz (data rate range : 20Mbps to 800 Mbps per I/O)
- Four-bit Pre-fetch DDR Architecture
- Multiplexed, double data rate, command/address inputs
- Eight internal banks for concurrent operation
- Bidirectional/differential data strobe per byte of data (DQS/DQS#)
- Programmable Read/Write latencies(RL/WL) and burst lengths(4,8 or 16)
- Per-bank refresh for concurrent operation
- ZQ Calibration
- On-chip temperature sensor to control self refresh rate
- Partial –array self refresh(PASR) – Bank & Segment masking
- Deep power-down mode(DPD)
- Operation Temperature
  Commercial (T_C = 0°C to 85°C)
  Industrial (T_C = -40°C to 85°C)
  Automotive, A1 (T_C = -40°C to 85°C)
  Automotive, A2 (T_C = -40°C to 105°C)

OPTIONS

- Configuration:
  – 64Mx16 (8M x 16 x 8 banks)
  – 32Mx32 (4M x 32 x 8 banks)
  Package:
  – 134-ball BGA for x16 / x32
  – 168-ball PoP BGA for x32

DESCRIPTION

The IS43/46LD16640A/32320A is 1,073,741,824 bits CMOS Mobile Double Data Rate Synchronous DRAMs organized as 8 banks (S4). The deviceis organized as 8 banks of 8Meg words of 16bits or 4Meg words of 32bits. This product uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4N prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. This product offers fully synchronous operations referenced to both rising and falling edges of the clock. The data paths are internally pipelined and 4n bits prefetched to achieve very high bandwidth.

ADDRESS TABLE

Parameter	32Mx32	64Mx16
Row Addresses	R0-R12	R0-R12
Column Addresses	C0-C8	C0-C9
Bank Addresses	BA0-BA2	BA0-BA2
Refresh Count	4K	4K

KEY TIMING PARAMETERS

Speed Grade	Data Rate (Mb/s)	Write Latency	Read Latency	tRCD/ tRP
-25	800	3	6	Typical
-3	667	2	5	Typical

Note: Other clock frequencies/data rates supported; please refer to AC timing tables.

BALL ASSIGNMENTS AND DESCRIPTIONS

134-ball FBGA (x32), 0.65mm pitch

	1	2	3	4	5	6	7	8	9	10	
A	DNU	DNU							DNU	DNU	A
B	DNU	NC	NC		VDD2	VDD1	DQ31	DQ29	DQ26	DNU	B
C	VDD1	VSS	RFU		VSS	VSSQ	VDDQ	DQ25	VSSQ	VDDQ	C
D	VSS	VDD2	ZQ		VDDQ	DQ30	DQ27	DQS3_t	DQS3_c	VSSQ	D
E	VSSCA	CA9	CA8		DQ28	DQ24	DM3	DQ15	VDDQ	VSSQ	E
F	VDDCA	CA6	CA7		VSSQ	DQ11	DQ13	DQ14	DQ12	VDDQ	F
G	VDD2	CA5	Vref(CA)		DQS1_c	DQS1_t	DQ10	DQ9	DQ8	VSSQ	G
H	VDDCA	VSS	CK_c		DM1	VDDQ					H
J	VSSCA	NC	CK_t		VSSQ	VDDQ	VDD2	VSS	Vref(DQ)		J
K	CKE	RFU	RFU		DM0	VDDQ					K
L	CS_n	RFU	RFU		DQS0_c	DQS0_t	DQ5	DQ6	DQ7	VSSQ	L
M	CA4	CA3	CA2		VSSQ	DQ4	DQ2	DQ1	DQ3	VDDQ	M
N	VSSCA	VDDCA	CA1		DQ19	DQ23	DM2	DQ0	VDDQ	VSSQ	N
P	VSS	VDD2	CA0		VDDQ	DQ17	DQ20	DQS2_t	DQS2_c	VSSQ	P
R	VDD1	VSS	NC		VSS	VSSQ	VDDQ	DQ22	VSSQ	VDDQ	R
T	DNU	NC	NC		VDD2	VDD1	DQ16	DQ18	DQ21	DNU	T
U	DNU	DNU							DNU	DNU	U
	1	2	3	4	5	6	7	8	9	10	

DQ
CA
Power
Ground
No ball
ZQ
Clock
NC, DNU, RFU

Top View (ball down)

BALL ASSIGNMENTS AND DESCRIPTIONS

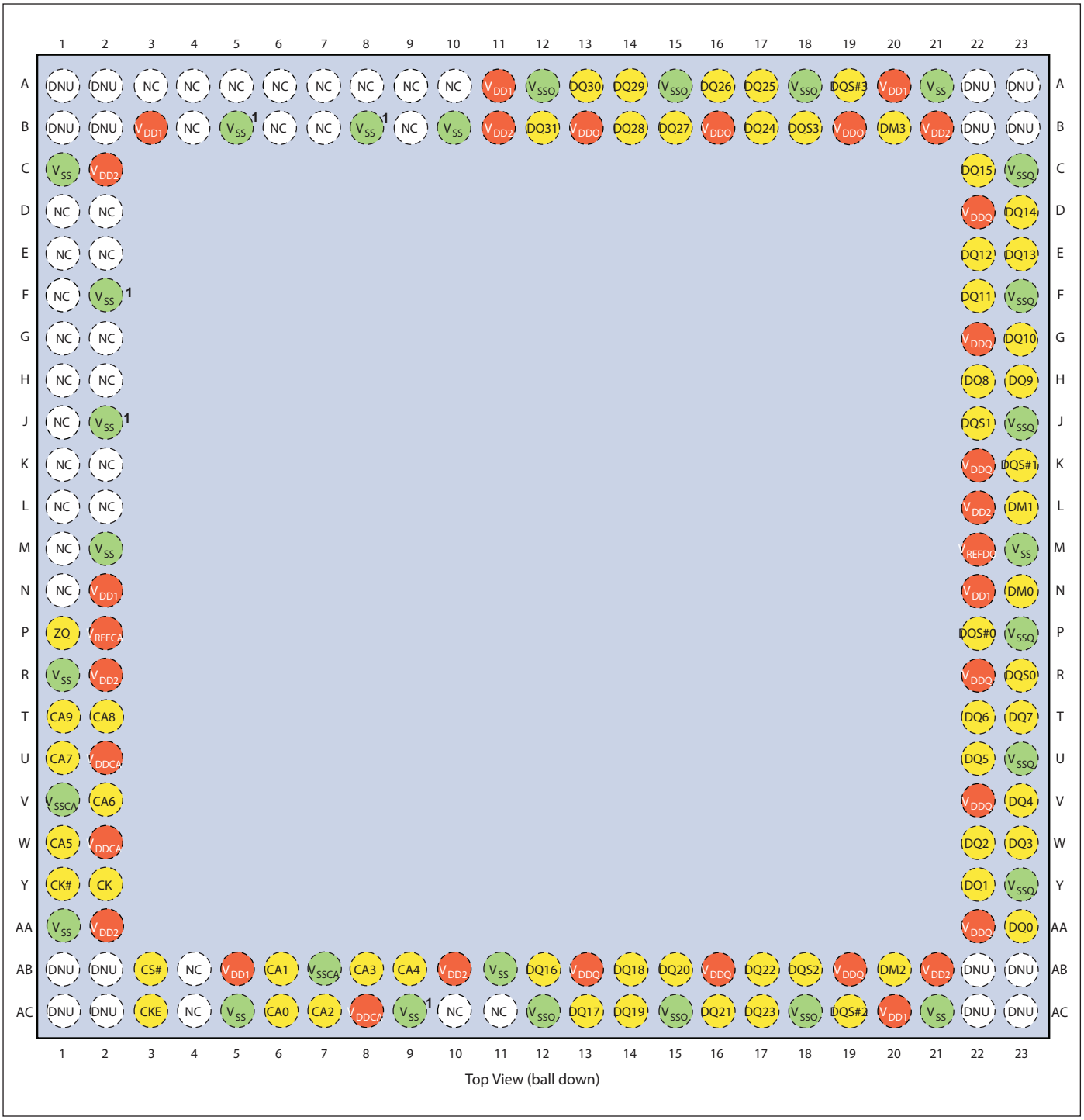
134-ball FBGA (x16), 0.65mm pitch

	1	2	3	4	5	6	7	8	9	10	
A	DNU	DNU							DNU	DNU	A
B	DNU	NC	NC		VDD2	VDD1	NC	NC	NC	DNU	B
C	VDD1	VSS	RFU		VSS	VSSQ	VDDQ	NC	VSSQ	VDDQ	C
D	VSS	VDD2	ZQ		VDDQ	NC	NC	NC	NC	VSSQ	D
E	VSSCA	CA9	CA8		NC	NC	NC	DQ15	VDDQ	VSSQ	E
F	VDDCA	CA6	CA7		VSSQ	DQ11	DQ13	DQ14	DQ12	VDDQ	F
G	VDD2	CA5	Vref(CA)		DQS1_c	DQS1_t	DQ10	DQ9	DQ8	VSSQ	G
H	VDDCA	VSS	CK_c		DM1	VDDQ					H
J	VSSCA	NC	CK_t		VSSQ	VDDQ	VDD2	VSS	Vref(DQ)		J
K	CKE	RFU	RFU		DM0	VDDQ					K
L	CS_n	RFU	RFU		DQS0_c	DQS0_t	DQ5	DQ6	DQ7	VSSQ	L
M	CA4	CA3	CA2		VSSQ	DQ4	DQ2	DQ1	DQ3	VDDQ	M
N	VSSCA	VDDCA	CA1		NC	NC	NC	DQ0	VDDQ	VSSQ	N
P	VSS	VDD2	CA0		VDDQ	NC	NC	NC	NC	VSSQ	P
R	VDD1	VSS	NC		VSS	VSSQ	VDDQ	NC	VSSQ	VDDQ	R
T	DNU	NC	NC		VDD2	VDD1	NC	NC	NC	DNU	T
U	DNU	DNU							DNU	DNU	U
	1	2	3	4	5	6	7	8	9	10	

DQ
CA
Power
Ground
No ball
ZQ
Clock
NC, DNU, RFU

Top View (ball down)

168-ball FBGA - 12mm x 12mm (x32), 0.5mm pitch



Note:
1. Balls labeled Vss[1] (at coordinates B5, B8, F2, J2, AC9) may be connected to Vss or left unconnected.
2. Balls indicated as (NC) are no connects.

INPUT/OUTPUT FUNCTIONAL DESCRIPTION

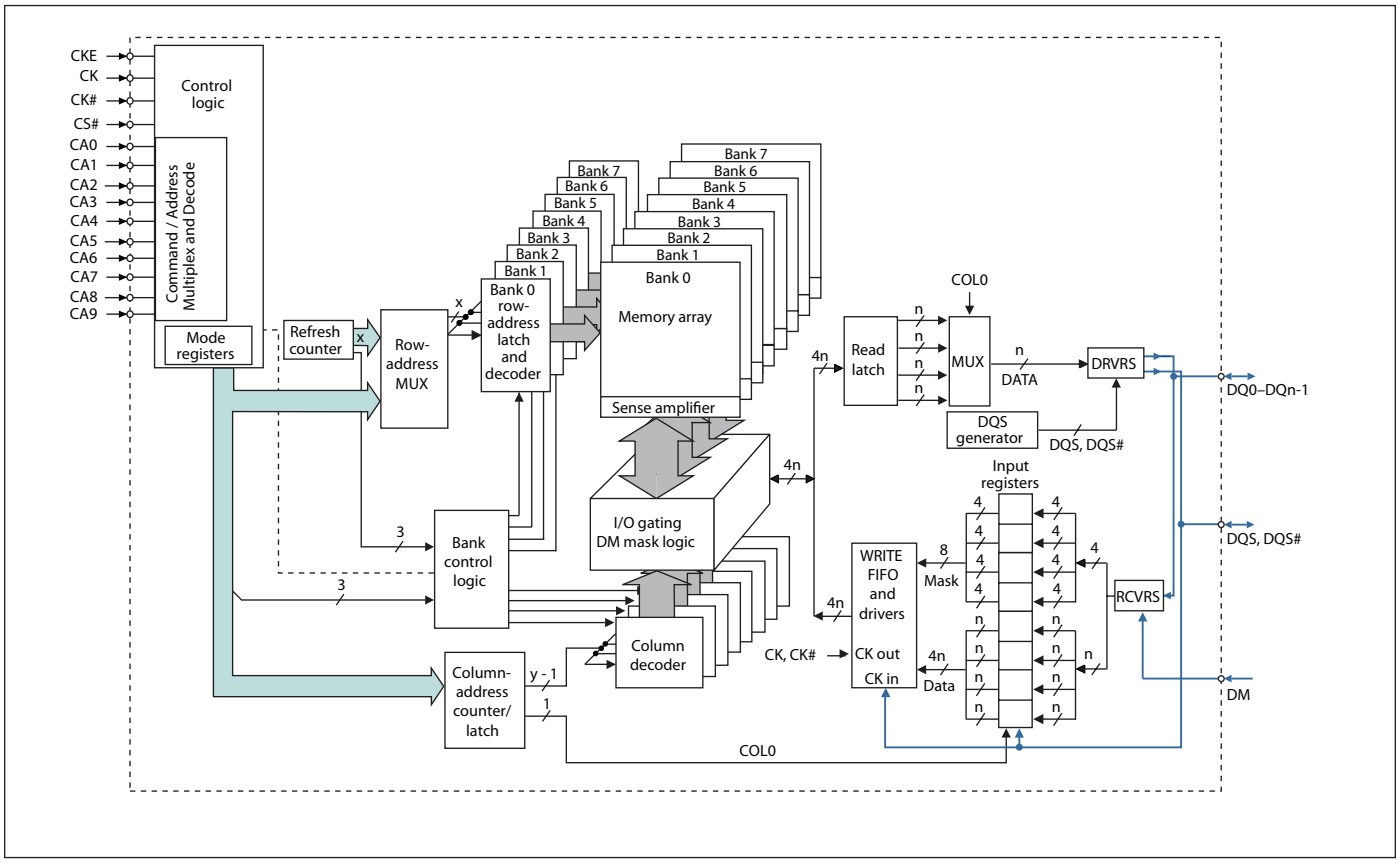
Pad Definition and Description

Name	Type	Description
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c.
CKE	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See Command Truth Table for command code descriptions. CKE is sampled at the positive Clock edge.
CS_n	Input	Chip Select: CS_n is considered part of the command code. See Command Truth Table for command code descriptions. CS_n is sampled at the positive Clock edge.
CA0 - CA9	Input	DDR Command/Address Inputs: Uni-directional command/address bus inputs. CA is considered part of the command code. See Command Truth Table for command code descriptions.
DQ0 - DQ15 (x16) DQ0 - DQ31 (x32)	I/O	Data Inputs/Output: Bi-directional data bus
DQS0_t, DQS0_c, DQS1_t, DQS1_c (x16) DQS0_t - DQS3_t, DQS0_c - DQS3_c (x32)	I/O	Data Strobe (Bi-directional, Differential): The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data. For x16, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7; DQS1_t and DQS1_c to the data on DQ8 - DQ15. For x32 DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7, DQS1_t and DQS1_c to the data on DQ8 - DQ15, DQS2_t and DQS2_c to the data on DQ16 - DQ23, DQS3_t and DQS3_c to the data on DQ24 - DQ31.
DM0-DM1 (x16) DM0 - DM3 (x32)	Input	Input Data Mask: For LPDDR2 devices that do not support the DNV feature, DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS_t. Although DM is for input only, the DM loading shall match the DQ and DQS_t (or DQS_c). DM0 is the input data mask signal for the data on DQ0-7. For x16 and x32 devices, DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.

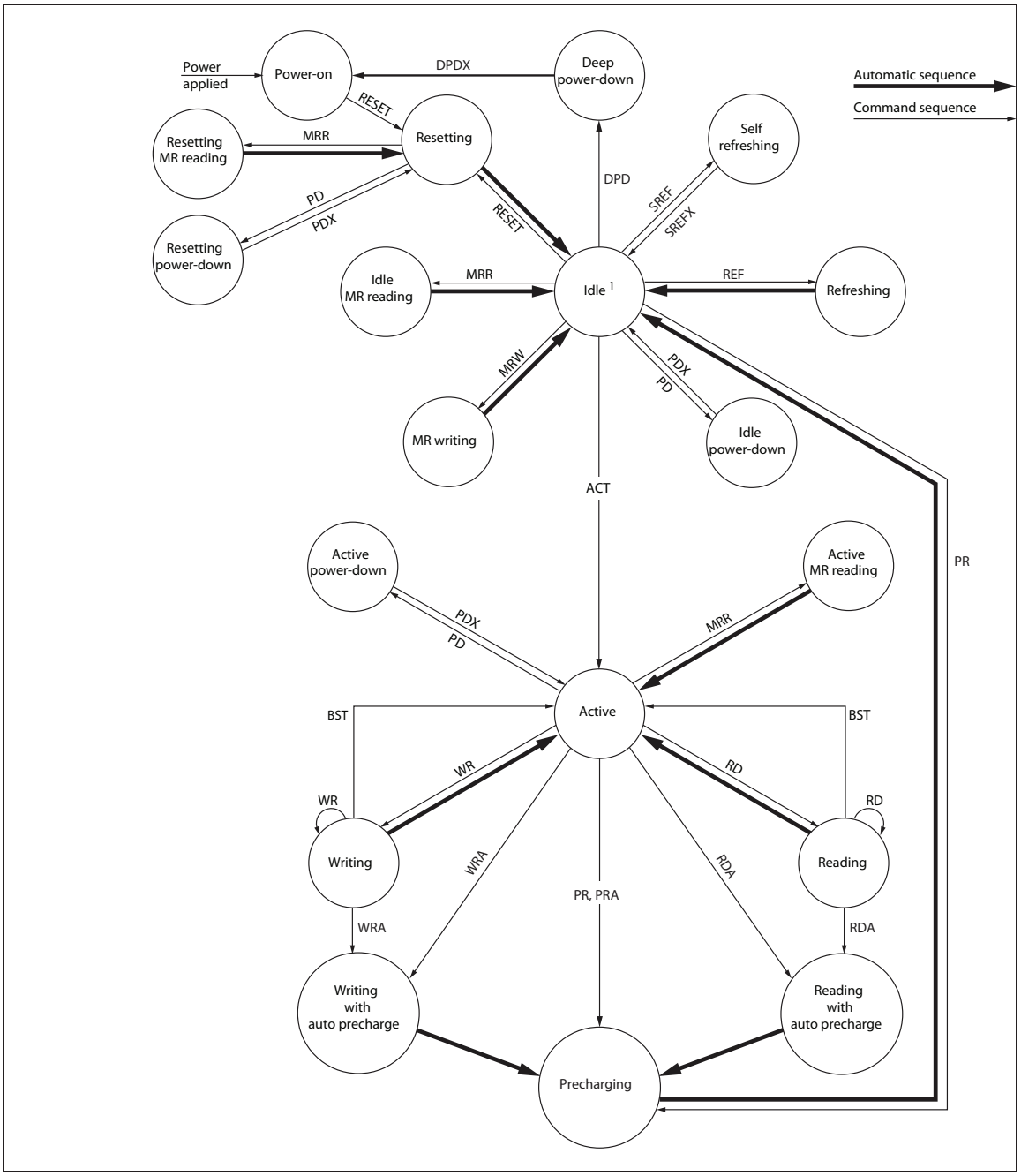
Name	Type	Description
V_{DD1}	Supply	Core Power Supply 1
V_{DD2}	Supply	Core Power Supply 2
V_{DDCA}	Supply	Input Receiver Power Supply: Power supply for CA0-9, CKE, CS_n, CK_t, and CK_c input buffers.
V_{DDQ}	Supply	I/O Power Supply: Power supply for Data input/output buffers.
$V_{REF(CA)}$	Supply	Reference Voltage for CA Command and Control Input Receiver: Reference voltage for all CA0-9, CKE, CS_n, CK_t, and CK_c input buffers.
$V_{REF(DQ)}$	Supply	Reference Voltage for DQ Input Receiver: Reference voltage for all Data input buffers.
V_{SS}	Supply	Ground
V_{SSCA}	Supply	Ground for Input Receivers
V_{SSQ}	Supply	I/O Ground
ZQ	I/O	Reference Pin for Output Drive Strength Calibration

NOTE 1 Data includes DQ and DM.

FUNCTIONAL BLOCK DIAGRAM



SIMPLIFIED STATE DIAGRAM



Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Active	PD	Enter Power Down	REF	Refresh
RD(A)	Read (w/ Autopre-charge)	PDX	Exit Power Down	SREF	Enter self refresh
WR(A)	Write (w/ Autopre-charge)	DPD	Enter Deep Power Down	SREFX	Exit self refresh
PR(A)	Precharge (All)	DPDX	Exit Deep Power Down		
MRW	Mode Register Write	BST	Burst Terminate		
MRR	Mode Register Read	RESET	Reset is achieved through MRW command		

Note: For LPDDR2-S4 SDRAM in the idle state, all banks are precharged.

FUNCTIONAL DESCRIPTION

LPDDR2-S4 is a high-speed SDRAM device internally configured as an 8-Bank memory. This device contains 1,073,741,824 bits (1 Gigabit)

All LPDDR2 devices use a double data rate archiecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

This LPDDR2-S4 device also uses a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the memory device effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM core and four corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR2 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR2 must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

POWER-UP AND INITIALIZATION

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

The following sequence is required for Power-up and Initialization.

1. Voltage ramp up sequence is required :

A. While applying power, attempt to maintain CKE below 0.2 x VDDCA and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW. The voltage ramp time tINIT0 (Tb-Ta) must be no greater than 20 ms from Tb which is point for all supply and reference voltage are within their defined operating ranges , to Ta which is point for any power supply first reaches 300mV.

B. The following conditions apply for voltage ramp after Ta is reached,
− VDD1 must be greater than VDD2-200mV AND
− VDD1 and VDD2 must be greater than VDDCA-200mV AND
− VDD1 and VDD2 must be greater than VDDQ-200mV AND
− VREF must always be less than all other supply voltages
− The voltage difference between any of VSS, VSSQ, and VSSCA pins must not exceed 100mV

2. Start clock and maintain stable condition.

Beginning at Tb, CKE must remain LOW for at least tINIT1 = 100 ns, after which CKE can be asserted HIGH. The clock must be stable at least tINIT2 = 5 × tCK prior to the first CKE LOW-to-HIGH transition (Tc). CKE, /CS, and CA inputs must observe setup and hold requirements (tIS, tIH) with respect to the first rising clock edge (and to subsequent falling and rising edges).

Once the ramping of the supply voltages is complete (Tb), CKE must be maintained LOW. DQ, DM, DQS and DQS# voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latchup. CK, /CK, /CS, and CA input levels must be between VSSCA and VDDCA during voltage ramp to avoid latch-up

If any Mode Register Read (MRRs) are issued, the clock period must be within the range defined for tCKb (18ns to 100ns). Mode Register Write (MRWs) can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters could have relaxed timings before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least tINIT3 = 200µs (Td).

3. RESET Command

After tINIT3 is satisfied, the MRW RESET command must be issued (Td).
An optional PRECHARGE ALL command can be issued prior to the MRW RESET command. Wait at least tINIT4 while keeping CKE asserted and issuing NOP commands

4. Mode Register Reads and Device Auto Initialization (DAI) Polling:

After tINIT4 is satisfied (Te), only MRR commands and power-down entry/exit commands are supported. After Te, CKE can go LOW in alignment with power-down entry and exit specifications.
Use the MRR command to poll the DAI bit and report when device auto initialization is complete; otherwise, the controller must wait a minimum of tINIT5, or until the DAI bit is set before proceeding.
As the memory output buffers are not properly configured by Te, some AC parameters must have relaxed timings before the system is appropriately configured. After the DAI bit (MR0, DAI) is set to zero by the memory device (DAI complete), the device is in the idle state (Tf). DAI status can be determined by issuing the MRR command to MR0. The device sets the DAI bit no later than tINIT5 after the RESET command. The controller must wait at least tINIT5 or until the DAI bit is set before proceeding

5. ZQ Calibration

After tINIT5 (Tf), the MRR initialization calibration (ZQ_CAL) command can be issued to the memory (MR10). This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one LPDDR2 device exists on the same bus, the controller must not overlap MRR ZQ_CAL commands. The device is ready for normal operation after tZQINIT.

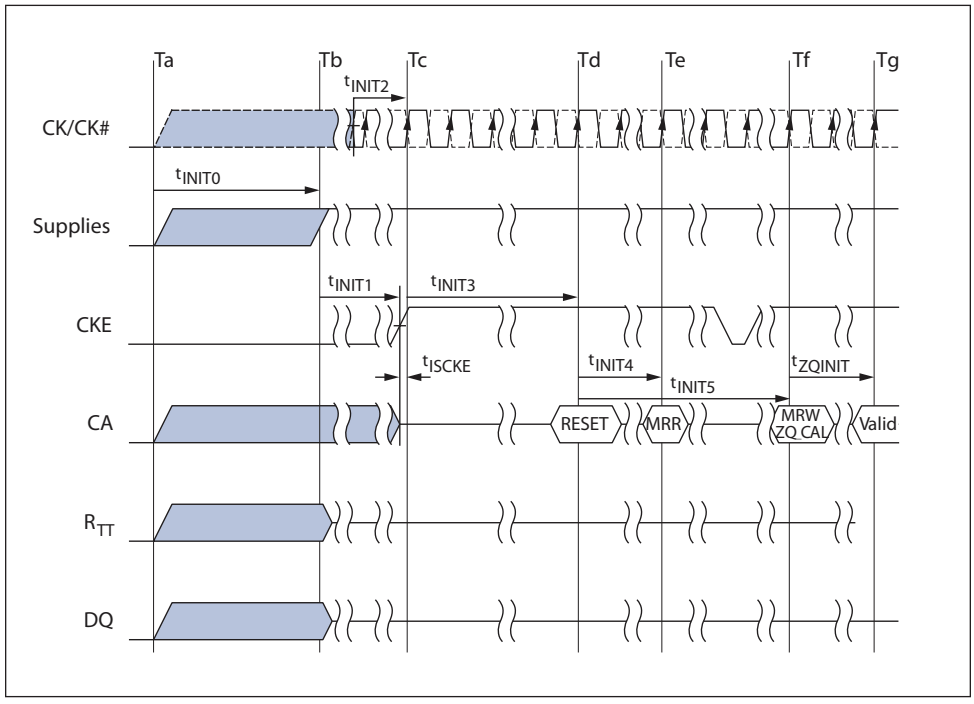
6. Normal Operation

After tZQINIT (Tg), MRW commands must be used to properly configure the memory . Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration
After the initialization sequence is complete, the device is ready for any valid command. After Tg, the clock frequency can be changed using the procedure described in Input Clock Frequency Changes and Clock Stop Eventsll.

INITIALIZATION TIMING

Symbol	Parameter	Value		Unit
		min	max	
tINIT0	Maximum Power Ramp Time	-	20	ms
tINIT1	Minimum CKE low time after completion of power ramp	100	-	ns
tINIT2	Minimum stable clock before first CKE high	5	-	tCK
tINIT3	Minimum idle time after first CKE assertion	200	-	us
tINIT4	Minimum idle time after Reset command, this time will be about 2 x tRFCab + tRPab	1	-	us
tINIT5	Maximum duration of Device Auto-Initialization	-	10	us
tCKb	Clock cycle time during boot	18	100	ns
tZQINIT	ZQ initial calibration	1	-	us

Figure - Power Ramp and Initialization Sequence



Initialization After RESET (without voltage ramp):

If the RESET command is issued before or after the power-up initialization sequence, the re-initialization procedure must begin at Td

Power-Off Sequence

Use the following sequence to power off the device. Unless specified otherwise, this procedure is mandatory and applies to S4 devices.

While powering off, CKE must be held LOW (≤ 0.2 × VDDCA); all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW.

DQ, DM, DQS, and /DQS voltage levels must be between VSSQ and VDDQ during the power-off sequence to avoid latch-up. CK, /CK, /CS, and CA input levels must be between VSSCA and VDDCA during the power-off sequence to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified in the DC operating condition table.

Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off

Required Power Supply Conditions Between Tx and Tz:

• VDD1 must be greater than VDD2 - 200mV

• VDD1 must be greater than VDDCA - 200mV

• VDD1 must be greater than VDDQ - 200mV

• VREF must always be less than all other supply voltages

The voltage difference between VSS, VSSQ, and VSSCA must not exceed 100mV.

For supply and reference voltage operating conditions, see Recommended DC Operating Conditions table.

Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

1.At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.

2.After Tz , the device must power off. The time between Tx and Tz must not exceed 20ms. During this period, the relative voltage between power supplies is uncontrolled. VDD1 and VDD2 must decrease with a slope lower than 0.5 V/µs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device

Mode Register Definition

LPDDR2 devices contain a set of mode registers used for programming device operating parameters, reading device information and status, and for initiating special operations such as DQ calibration, ZQ calibration, and device reset.

Mode Register Assignment

The MRR command is used to read from a register. The MRW command is used to write to a register.

Mode Register Assignment

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00_H	Device Info.	R	(RFU)						DI	DAI
1	01_H	Device Feature1	W	nWR (for AP)			WC	BT	BL		
2	02_H	Device Feature2	W	(RFU)					RL & WL		
3	03_H	I/O Config-1	W	(RFU)					DS		
4	04_H	Refresh Rate	R	TUF	(RFU)				Refresh Rate		
5	05_H	Basic Config-1	R	LPDDR2 Manufacturer ID							
6	06_H	Basic Config-2	R	Revision ID1							
7	07_H	Basic Config-3	R	Revision ID2							
8	08_H	Basic Config-4	R	I/O width		Density				Type	
9	09_H	Test Mode	W	Vendor-Specific Test Mode							
10	$0A_H$	IO Calibration	W	Calibration Code							
11~15	$0B_H$~$0F_H$	(reserved)		(RFU)							

Mode Register Assignment

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
16	10_H	PASR_BANK	W	Bank Mask							
17	11_H	PASR_Seg	W	Segment Mask							
18-19	12_H-13_H	(Reserved)		(RFU)							

Mode Register Assignment

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
20-31	18_H-$1F_H$	Reserved									

Mode Register Assignment (Reset Command & RFU part)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
32	20_H	DQ calibration pattern A	R	See "Data Calibration Pattern Description"							
33-39	21_H-27_H	(Do Not Use)									
40	28_H	DQ calibration pattern B	R	See "Data Calibration Pattern Description"							
41-47	29_H-$2F_H$	(Do Not Use)									
48-62	30_H-$3E_H$	(Reserved)		(RFU)							
63	$3F_H$	Reset	W	X							
64-126	40_H-$7E_H$	(Reserved)		(RFU)							
127	$7F_H$	(Do Not Use)									
128-190	80_H-BE_H	(Reserved for Vendor Use)		(RFU)							
191	BF_H	(Do Not Use)									
192-254	$C0_H$-FE_H	(Reserved for Vendor Use)		(RFU)							
255	FF_H	(Do Not Use)									

Notes:
1. RFU bits shall be set to '0' during Mode Register writes.
2.RFU bits shall be read as '0' during Mode Register reads.
3.All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS shall be toggled.
4.All Mode Registers that are specified as RFU shall not be written.
5.See Vendor Device Datasheets for details on Vendor Specific Mode Registers.
6.Writes to read-only registers shall have no impact on the functionality of the device.

MR0_Device Information (MA<7:0> = 00_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
(RFU)						DI	DAI	

OP1	DI (Device Information)	Read-only	0_B: SDRAM 1_B: Do Not Use
OP0	DAI (Device Auto-Initialization Status)	Read-only	0_B: DAI complete 1_B: DAI still in progress

MR1_Devcie Feature 1 (MA<7:0> = 01_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
nWR (for AP)			WC	BT	BL			

OP<2:0>	BL (Burst Length)	Write-only	010_B: BL4 (default) 011_B: BL8 100_B: BL16 All others: reserved
OP3	BT[*1] (Burst Type)	Write-only	0_B: Sequential (default) 1_B: Interleaved
OP4	WC (Wrap)	Write-only	0_B: Wrap (default) 1_B: No wrap (allowed for SDRAM BL4 only)
OP<7:5>	nWR[*2]	Write-only	001_B: nWR=3 (default) 010_B: nWR=4 011_B: nWR=5 100_B: nWR=6 101_B: nWR=7 110_B: nWR=8 All others: reserved

Notes:
1. BL16, interleaved is not an official combination to be supported.
2. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK)

Burst Sequence by BL, BT, and WC

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence													
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
x	x	0_B	0_B	wrap	any	4	0	1	2	3												
x	x	1_B	0_B				2	3	0	1												
x	x	x	0_B	nw	any		y	y+1	y+2	y+3												

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
x	0_B	0_B	0_B	wrap	seq	8	0	1	2	3	4	5	6	7								
x	0_B	1_B	0_B				2	3	4	5	6	7	0	1								
x	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
x	1_B	1_B	0_B				6	7	0	1	2	3	4	5								
x	0_B	0_B	0_B		int		0	1	2	3	4	5	6	7								
x	0_B	1_B	0_B				2	3	0	1	6	7	4	5								
x	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
x	1_B	1_B	0_B				6	7	4	5	2	3	0	1								
x	x	x	0_B	nw	any		illegal (not allowed)															
0_B	0_B	0_B	0_B	wrap	seq	16	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0_B	0_B	1_B	0_B				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
0_B	1_B	0_B	0_B				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
0_B	1_B	1_B	0_B				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
1_B	0_B	0_B	0_B				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1_B	0_B	1_B	0_B				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
1_B	1_B	0_B	0_B				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
1_B	1_B	1_B	0_B				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
x	x	x	0_B		int		illegal (not allowed)															
x	x	x	0_B	nw	any		illegal (not allowed)															

Notes:
1. C0 input is not present on CA bus. It is implied zero.
2. For BL=4, the burst address represents C1~C0.
3. For BL=8, the burst address represents C2~C0.
4. For BL=16, the burst address represents C3~C0.
5. For no-wrap, BL4, the burst must not cross the page boundary or the sub-page boundary.The variabley can start at any address with C0 equal to 0, but must not start at any address shown below

Non-Wrap Restrictions

Width	64Mb	128Mb/256Mb	512Mb/1Gb/2Gb	4Gb/8Gb
Cannot cross full page boundary				
X16	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001	7FE, 7FF, 000, 001
X32	7E, 7F, 00, 01	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001
Cannot cross sub-page boundary				
X16	7E, 7F, 80, 81	0FE, 0FF, 100, 101	1FE, 1FF, 200, 201	3FE, 3FF, 400, 401
X32	none	none	None	none

Note: Non-wrap BL=4 data orders shown are prohibited.

MR2_Devcie Feature 2 (MA<7:0> = 02_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
(RFU)				RL & WL				
OP<3:0>		RL & WL (Read Latency & Write Latency)				Write-only		0001_B: RL3 / WL1 (default) 0010_B: RL4 / WL2 0011_B: RL5 / WL2 0100_B: RL6 / WL3 0101_B: RL7 / WL4 0110_B: RL8 / WL4 All others: reserved

MR3_I/O Configuration 1 (MA<7:0> = 03_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
(RFU)				DS				
OP<3:0>		DS (Drive Strength)				Write-only		0000_B: reserved 0001_B: 34.3 ohm typical 0010_B: 40.0 ohm typical (default) 0011_B: 48.0 ohm typical 0100_B: 60.0 ohm typical 0101_B: reserved 0110_B: 80.0 ohm typical All others: reserved

MR4_Device Temperature (MA<7:0> = 04_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
TUF	(RFU)				SDRAM Refresh Rate			
OP<2:0>		SDRAM Refresh Rate				Read-only		000_B: 4 x t_{REFI}, SDRAM Low Temp. operating limit exceeded 001_B: 4 × tREFI, 4 × tREFIpb, 4 × tREFW 010_B: 2 × tREFI, 2 × tREFIpb, 2 × tREFW, 011_B: 1 × tREFI, 1 × tREFIpb, 1 × tREFW (<= 85C) 100_B: RFU

			101_B: 0.25 × tREFI, 0.25 × tREFIpb, 0.25 × tREFW, don't re-rate SDRAM AC timing 110_B: 0.25 × tREFI, 0.25 × tREFIpb, 0.25 × tREFW, derate SDRAM AC timing 111_B: SDRAM High temperature operating limit exceeded
OP7	TUF (Temperature Update Flag)	Read-only	0_B: (no used) 1_B: (always)

Notes:
1. A Mode Register Read from MR4 will reset OP7 to "0".
2. OP7 is reset to "0" at power-up.
3. If OP2 equals "1", the device temperature is greater than 85C.
4. OP7 is set to "1", if OP2~OP0 has changed at any time since the last read of MR4.
5. LPDDR2 might not operate properly when OP<2:0> = 000B or 111B.
6. For specified operating temperature range and maximum operating temperature.
7. LPDDR2 devices must be derated by adding 1.875ns to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. The tDQSCK parameter must be derated Prevailing clock frequency specifications and related setup and hold timings remain unchanged.
8. The recommended frequency for reading MR4 is provided in "Temperature Sensor"

MR5_Basic Configuration 1 (MA<7:0> = 05_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
LPDDR2 Manufacturer ID								
OP<7:0>	Manufacturer ID					Read-only		0001 1011B: ISSI All Others : Reserved

MR6_Basic Configuration 2 (MA<7:0> = 06_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Revision ID1								
OP<7:0>	Revision ID1					Read-only		00000000_B: A-version

MR7_Basic Configuration 3 (MA<7:0> = 07_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Revision ID2								
OP<7:0>	Revision ID2					Read-only		00000000_B: A-version

MR8_Basic Configuration 4 (MA<7:0> = 08_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
I/O width		Density				Type		

OP<1:0>	Type	Read-only	00_B: S4 SDRAM 01_B: Reserved 10_B: Reserved 11_B: Reserved
OP<5:2>	Density	Read-only	0000_B: 64Mb (Reserved) 0001_B: 128Mb (Reserved) 0010_B: 256Mb (Reserved) 0011_B: 512Mb (Reserved) 0100_B: **1Gb** 0101_B: 2Gb (Reserved) 0110_B: 4Gb (Reserved) 0111_B: 8Gb (Reserved) 1000_B: 16Gb (Reserved) 1001_B: 32Gb (Reserved) All others: reserved
OP<7:6>	I/O width	Read-only	00_B: x32 01_B: x16 10_B: x8 (Reserved) 11_B: not used

MR9_Test Mode (MA<7:0> = 09_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Vendor-specific Test Mode								

MR10_Calibration (MA<7:0> = $0A_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Calibration Code								
OP<7:0>		Calibration Code				Write-only		0xFF: Calibration command after initialization 0xAB: Long calibration 0x56: Short calibration 0xC3: ZQ Reset All others: Reserved

Notes:
1. Host processor shall not write MR10 with “Reserved” values.
2. LPDDR2 devices shall ignore calibration command, when a “Reserved” values is written into MR10.
3. See AC timing table for the calibration latency.
4. If ZQ is connected to VSSCA through RZQ, either the ZQ calibration function (see “MRW ZQ Calibration Command”) or default
calibration (through the ZQ RESET command) is supported. If ZQ is connected to VDDCA, the device opeates with default calibration,
and ZQ calibration commands are ignored. In both cases, the ZQ connection must not change after power is supplied to the device.
5. Devices that do not support calibration ignore the ZQ calibration command.

MR11:15_(Reserved) (MA<7:0> = $0B_H$- $0F_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR16_PASR_Bank Mask (MA<7:0> = 010_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Bank Mask (4-Bank or 8-Bank)								
OP<7:0>		Bank Mask Code				Write-only		0_B: refresh enable to the bank (=unmasked, default) 1_B: refresh blocked (=masked)

OP	Bank Mask	4 Bank	8 Bank
0	XXXXXXX1	Bank 0	Bank 0
1	XXXXXX1X	Bank 1	Bank 1
2	XXXXX1XX	Bank 2	Bank 2
3	XXXX1XXX	Bank 3	Bank 3
4	XXX1XXXX	-	Bank 4
5	XX1XXXXX	-	Bank 5
6	X1XXXXXX	-	Bank 6
7	1XXXXXXX	-	Bank 7

Note: For 4-bank S4 SDRAM, only OP<3:0> are used.

MR17_PASR_Segment Mask (MA<7:0> = 011_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Segment Mask								
OP<7:0>		Segment Mask Code				Write-only		0_B: refresh enable to the bank (=unmasked, default) 1_B: refresh blocked (=masked)

Segment	OP	Bank Mask	1Gb	2Gb, 4Gb	8Gb
			R12:10	R13:11	R14:12
0	0	XXXXXXX1	000_B		
1	1	XXXXXX1X	001_B		
2	2	XXXXX1XX	010_B		
3	3	XXXX1XXX	011_B		
4	4	XXX1XXXX	100_B		
5	5	XX1XXXXX	101_B		
6	6	X1XXXXXX	110_B		
7	7	1XXXXXXX	111_B		

Note: This table indicates the range of row addresses in each masked segment. X is don't care for a particular segment.

MR18:19_(Reserved) (MA<7:0> = 012_H- 013_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR20:31_(Do Not Use) (MA<7:0> = 014_H- $01F_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Do Not Use								

MR32_(Do Not Use) (MA<7:0> = 020_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Do Not Use								

MR33:39_(Do Not Use) (MA<7:0> = 021_H- 027_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Do Not Use								

MR40_(Do Not Use) (MA<7:0> = 028_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Do Not Use								

MR41:47_(Do Not Use) (MA<7:0> = 029_H- $02F_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Do Not Use								

MR48:62_(Reserved) (MA<7:0> = 030_H- $03E_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR63_Reset (MA<7:0> = $03F_H$): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
X								

Note: For additional information on MRW RESET, see “Mode Register Write Command” on Timing Spec.

MR64:126_(Reserved) (MA<7:0> = 040_H- $07E_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR127_(Do Not Use) (MA<7:0> = $07F_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Do Not Use								

MR128:190_(Reserved for Vendor Use) (MA<7:0> = 080_H- $0BE_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR191_(Do Not Use) (MA<7:0> = $0BF_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Do Not Use								

MR192:254_(Reserved for Vendor Use) (MA<7:0> = $0C0_H$- $0FE_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR255_(Do Not Use) (MA<7:0> = $0FF_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Do Not Use								

Truth Tables

Truth tables provide complementary information to the state diagram. They also clarify device behavior and applicable restrictions when considering the actual state of the banks.

Unspecified operations and timings are illegal. To ensure proper operation after an illegal event, the device must be powered down and then restarted using the specified initialization sequence before normal operation can continue.

Command Truth Table

Table 49: Command Truth Table

Notes 1–11 apply to all parameters conditions

Command	Command Pins			CA Pins										CK Edge
	CKE													
	CK(n-1)	CK(n)	CS#	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
	H	H	X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
	H	H	X	MA6	MA7	X								↓
REFRESH (per bank)	H	H	L	L	L	H	L	X						↑
	H	H	X	X										↓
REFRESH (all banks)	H	H	L	L	L	H	H	X						↑
	H	H	X	X										↓
Enter self refresh	H	L	L	L	L	H	X							↑
	X	L	X	X										↓
ACTIVATE (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	↑
	H	H	X	R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	↓
WRITE (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
	H	H	X	AP	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
READ (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
	H	H	X	AP	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
PRECHARGE (bank)	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	BA2	↑
	H	H	X	X										↓
BST	H	H	L	H	H	L	L	X						↑
	H	H	X	X										↓
Enter DPD	H	L	L	H	H	L	X							↑
	X	L	X	X										↓
NOP	H	H	L	H	H	H	X							↑
	H	H	X	X										↓
Maintain PD, SREF, DPD, (NOP)	L	L	L	H	H	H	X							↑
	L	L	X	X										↓