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IS43/46R86400F
IS43/46R16320F

Long-term Support
World Class Quality

32Mx16, 64Mx8
512Mb DDR SDRAM

DECEMBER 2016

FEATURES

- VDD and VDDQ: 2.5V ± 0.2V (-5, -6)
- VDD and VDDQ: 2.5V ± 0.1V (-4)
- SSTL_2 compatible I/O
- Double-data rate architecture; two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/ received with data, to be used in capturing data at the receiver
- DQS is edge-aligned with data for READs and centre-aligned with data for WRITEs
- Differential clock inputs (CK and $\overline{CK}$)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data Mask for write data. DM masks write data at both rising and falling edges of data strobe
- Burst Length: 2, 4 and 8
- Burst Type: Sequential and Interleave mode
- Programmable CAS latency: 2, 2.5 and 3
- Auto Refresh and Self Refresh Modes
- Auto Precharge

OPTIONS

- Configuration(s): 32Mx16, 64Mx8
- Package(s):
  66-pin TSOP-II
  60-ball BGA
- Lead-free package available
- Temperature Range:
  Commercial (0°C to +70°C)
  Industrial (-40°C to +85°C)
  Automotive, A1 (-40°C to +85°C)
  Automotive, A2 (-40°C to +105°C)

DEVICE OVERVIEW

ISSI's 512-Mbit DDR SDRAM achieves high speed data transfer using pipeline architecture and two data word accesses per clock cycle. The 536,870,912-bit memory array is internally organized as four banks of 128Mb to allow concurrent operations. The pipeline allows Read and Write burst accesses to be virtually continuous, with the option to concatenate or truncate the bursts. The programmable features of burst length, burst sequence and CAS latency enable further advantages. The device is available in 8-bit and 16-bit word size. Input data is registered on the I/O pins on both edges of Data Strobe signal(s), while output data is referenced to both edges of Data Strobe and both edges of CLK. Commands are registered on the positive edges of CLK.

An Auto Refresh mode is provided, along with a Self Refresh mode. All I/Os are SSTL_2 compatible.

ADDRESS TABLE

Parameter	32M x 16	64M x 8
Configuration	8M x 16 x 4 banks	16M x 8 x 4 banks
Bank Address Pins	BA0, BA1	BA0, BA1
Autoprecharge Pins	A10/AP	A10/AP
Row Address	8K(A0 – A12)	8K(A0 – A12)
Column Address	1K(A0 – A9)	2K(A0 – A9, A11)
Refresh Count Com./Ind./A1 A2	 8K / 64ms 8K / 16ms	 8K / 64ms 8K / 16ms

KEY TIMING PARAMETERS

Speed Grade	-4	-5	-6	Units
F_{CK} Max CL = 3	250	200	167	MHz
F_{CK} Max CL = 2.5	167	167	167	MHz
F_{CK} Max CL = 2	133	133	133	MHz

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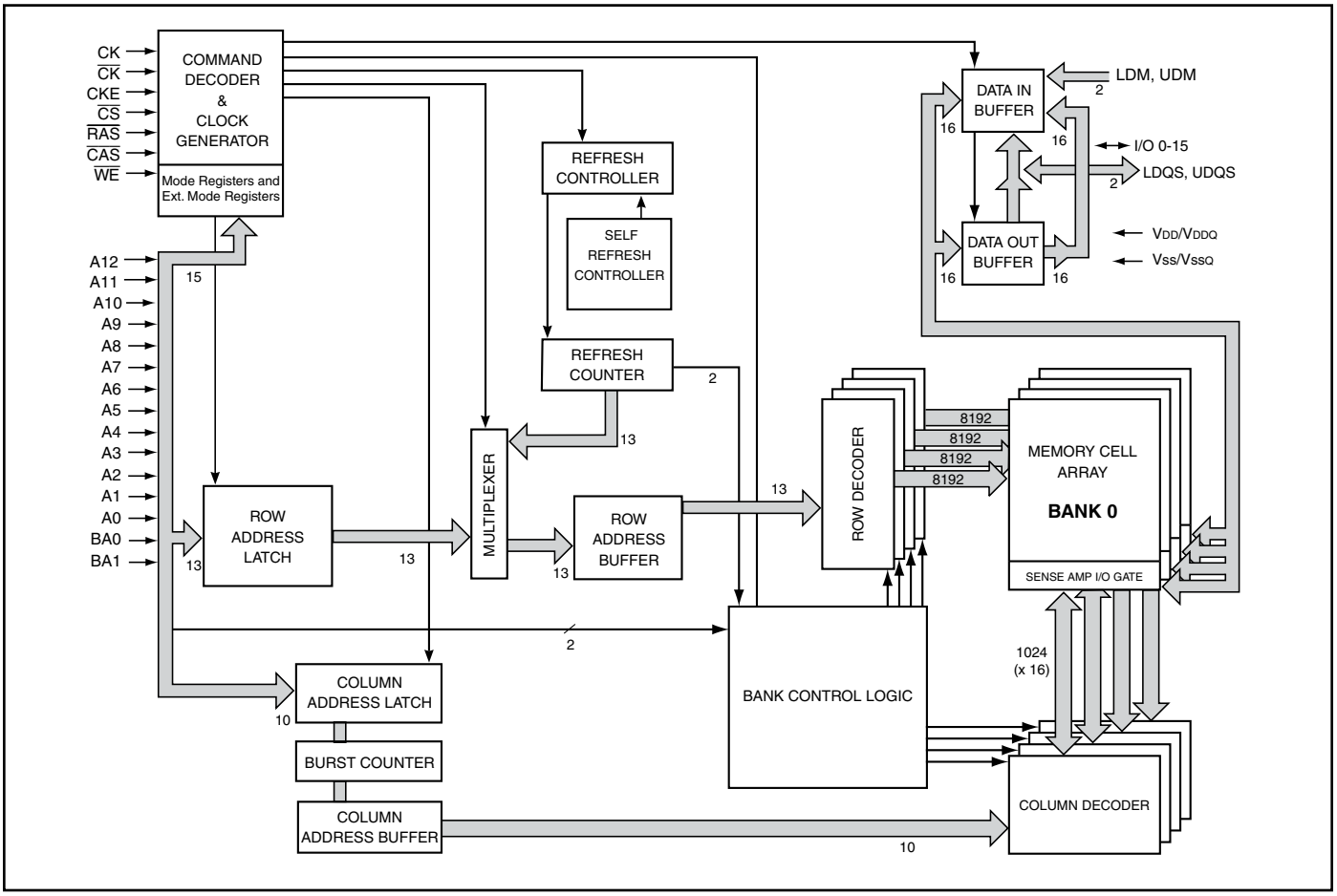
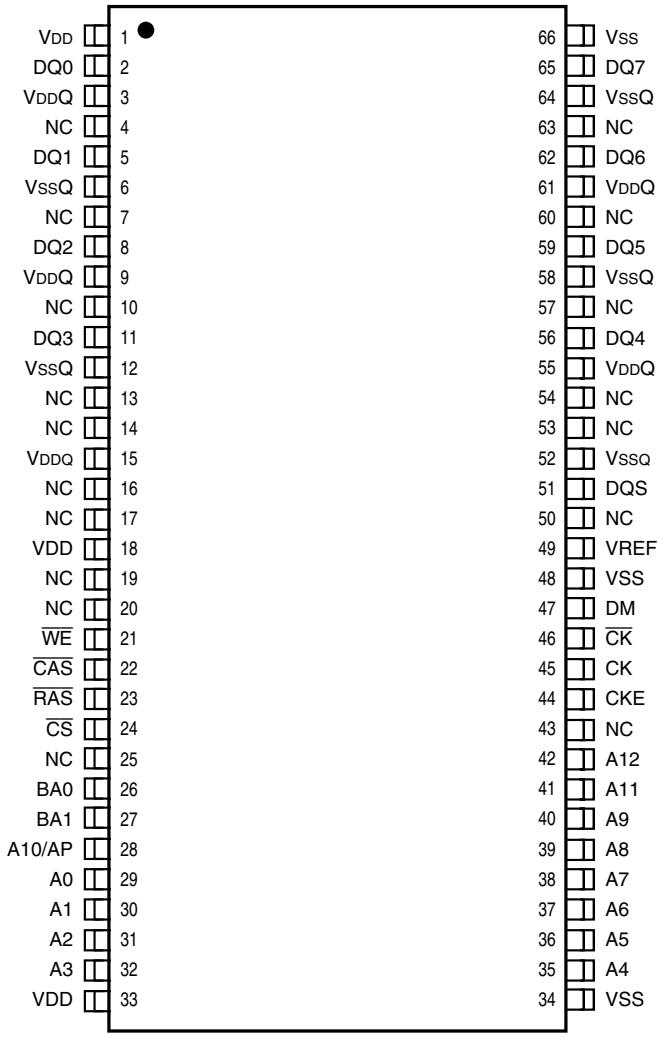
a.) the risk of injury or damage has been minimized;
b.) the user assume all such risks; and
c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

FUNCTIONAL BLOCK DIAGRAM (x16)



PIN CONFIGURATIONS

66 pin TSOP - Type II for x8



PIN DESCRIPTION: x8

A0-A12	Row Address Input
A0-A9, A11	Column Address Input
BA0, BA1	Bank Select Address
DQ0 – DQ7	Data I/O
CK, $\overline{CK}$	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{CAS}$	Column Address Strobe Command
$\overline{RAS}$	Row Address Strobe Command
$\overline{WE}$	Write Enable

DM	Data Write Mask
DQS	Data Strobe
VDD	Power
VDDQ	Power Supply for I/O Pins
VSS	Ground
VSSQ	Ground for I/O Pins
VREF	SSTL_2 reference voltage
NC	No Connection

PIN CONFIGURATION

Package Code B: 60-ball FBGA (top view) for x8

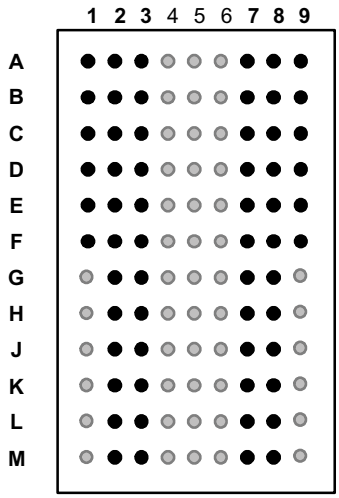
(8mm x 13mm Body, 0.8mm Ball Pitch)

Top View

(Balls seen through the Package)

● : Ball Existing
○ : Depopulated Ball

Top View(See the balls through the Package)



BGA Package Ball Pattern
Top View

1	2	3		7	8	9
VSSQ	DQ7	VSS	A	VDD	DQ0	VDDQ
NC	VDDQ	DQ6	B	DQ1	VSSQ	NC
NC	VSSQ	DQ5	C	DQ2	VDDQ	NC
NC	VDDQ	DQ4	D	DQ3	VSSQ	NC
NC	VSSQ	DQS	E	NC	VDDQ	NC
VREF	VSS	DM	F	NC	VDD	NC
	CK	$\overline{CK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

x8 Device Ball Pattern

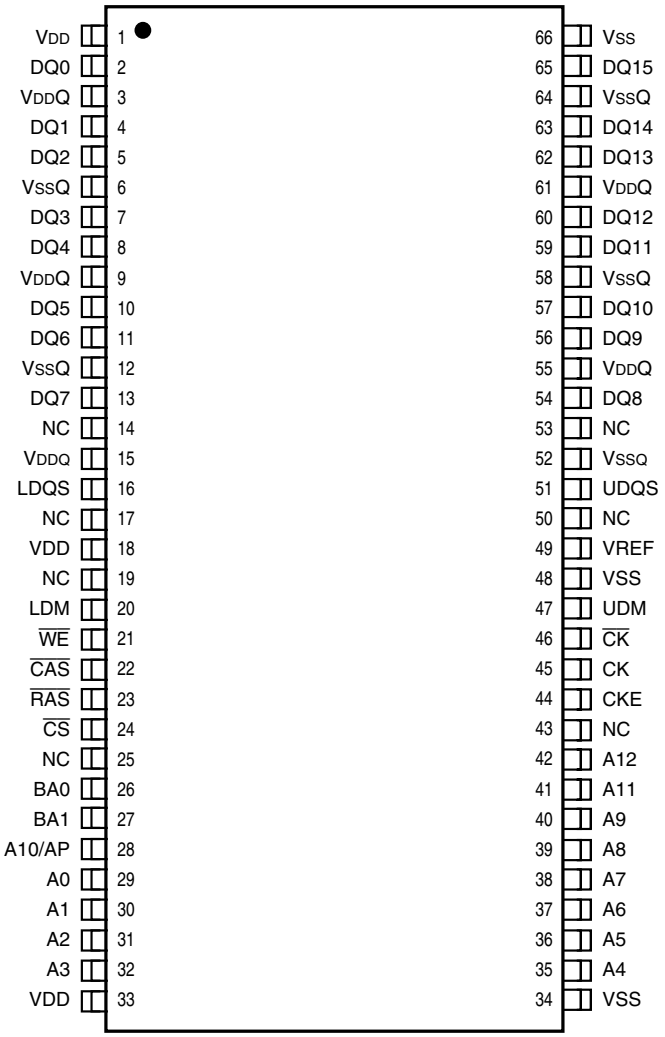
PIN DESCRIPTION: x8

A0-A12	Row Address Input
A0-A9, A11	Column Address Input
BA0, BA1	Bank Select Address
DQ0 – DQ7	Data I/O
CK, $\overline{CK}$	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{CAS}$	Column Address Strobe Command
$\overline{RAS}$	Row Address Strobe Command
$\overline{WE}$	Write Enable
DM	Data Write Mask

DQS	Data Strobe
VDD	Power
VDDQ	Power Supply for I/O Pins
VSS	Ground
VSSQ	Ground for I/O Pins
VREF	SSTL_2 reference voltage
NC	No Connection

PIN CONFIGURATIONS

66 pin TSOP - Type II for x16



PIN DESCRIPTION: x16

A0-A12	Row Address Input
A0-A9	Column Address Input
BA0, BA1	Bank Select Address
DQ0 – DQ15	Data I/O
CK, $\overline{CK}$	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{CAS}$	Column Address Strobe Command
$\overline{RAS}$	Row Address Strobe Command
$\overline{WE}$	Write Enable

LDM, UDM	Data Write Mask
LDQS, UDQS	Data Strobe
VDD	Power
VDDQ	Power Supply for I/O Pins
VSS	Ground
VSSQ	Ground for I/O Pins
VREF	SSTL_2 reference voltage
NC	No Connection

PIN CONFIGURATION

Package Code B: 60-ball FBGA (top view) for x16

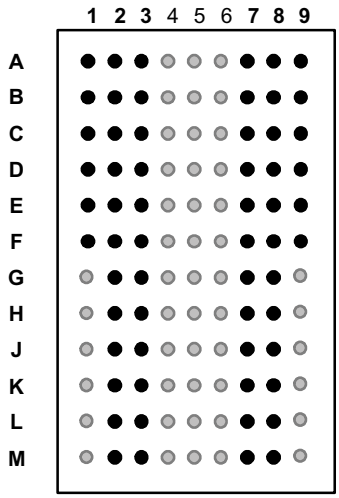
(8mm x 13mm Body, 0.8mm Ball Pitch)

Top View

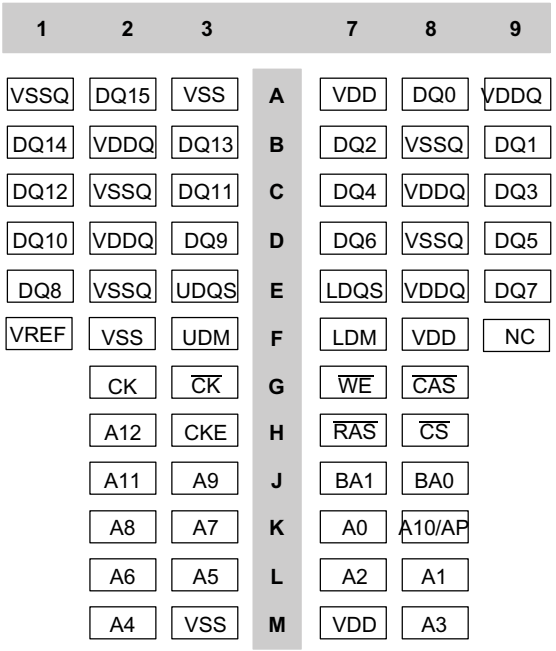
(Balls seen through the Package)

● : Ball Existing
○ : Depopulated Ball

Top View(See the balls through the Package)



BGA Package Ball Pattern
Top View



x16 Device Ball Pattern

PIN DESCRIPTION: x16

A0-A12	Row Address Input
A0-A9	Column Address Input
BA0, BA1	Bank Select Address
DQ0 – DQ15	Data I/O
CK, $\overline{CK}$	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{CAS}$	Column Address Strobe Command
$\overline{RAS}$	Row Address Strobe Command
$\overline{WE}$	Write Enable
LDM, UDM	Data Write Mask

LDQS, UDQS	Data Strobe
VDD	Power
VDDQ	Power Supply for I/O Pins
VSS	Ground
VSSQ	Ground for I/O Pins
VREF	SSTL_2 reference voltage
NC	No Connection

PIN FUNCTIONAL DESCRIPTIONS

Symbol	Type	Description
CK, $\overline{CK}$	Input	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK. Input and output data is referenced to the crossing of CK and $\overline{CK}$ (both directions of crossing). Internal clock signals are derived from CK/ $\overline{CK}$.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWERDOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously. Input buffers, excluding CK, CK and CKE, are disabled during power-down and self refresh mode which are contrived for low standby power consumption.
$\overline{CS}$	Input	Chip Select: CS enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS is registered HIGH. CS provides for external bank selection on systems with multiple banks. CS is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM: x8; LDM, UDM: x16;	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading matches the DQ and DQS loading. For x16 devices, LDM corresponds to the data on DQ0-DQ7, UDM corresponds to the data on DQ8-DQ15.
BA0, BA1	Input	Input Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A [12:0]	Input	Address Inputs: provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ / WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the opcode during a MODE REGISTER SET command.
DQ: DQ0-DQ7: x8; DQ0-DQ15: x16	I/O	Data Bus: Input / Output
DQS: x8: LDQS, UDQS x16:	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered with write data. Used to capture write data. For x16 device, LDQS corresponds to the data on DQ0-DQ7, UDQS corresponds to the data on DQ8-DQ15.
NC	--	No Connect: Should be left unconnected.
VREF	Supply	SSTL_2 reference voltage.
VDDQ	Supply	I/O Power Supply.
VSSQ	Supply	I/O Ground.
VDD	Supply	Power Supply.
VSS	Supply	Ground.

COMMANDS TRUTH TABLES

All commands (address and control signals) are registered on the positive edge of clock (crossing of CK going high and CK going low). Truth Table shows basic timing parameters for all commands.

TRUTH TABLE - COMMANDS

NAME (FUNCTION)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	AP	Address	Notes
DESELECT (NOP)	H	X	X	X	X	X	X	2
NO OPERATION (NOP)	L	H	H	H	X	X	X	2
ACTIVE (select bank and activate row)	L	L	H	H	Valid	X	Row	
READ (select bank and column and start read burst)	L	H	L	H	Valid	L	Column	
READ with AP (read burst with Auto Precharge)	L	H	L	H	Valid	H	Column	3
WRITE (select bank and column and start write burst)	L	H	L	L	Valid	L	Column	
WRITE with AP (write burst with Auto Precharge)	L	H	L	L	Valid	H	Column	3
BURST TERMINATE	L	H	H	L	X	X	X	4
PRECHARGE (deactivate row in selected bank)	L	L	H	L	Valid	L	X	5
PRECHARGE ALL (deactivate rows in all banks)	L	L	H	L	X	H	X	5
AUTO REFRESH or enter SELF REFRESH	L	L	L	H	X	X	X	6,7,8
MODE REGISTER SET	L	L	L	L	Valid	Op-code		9

Notes:
1. All states and sequences not shown are illegal or reserved.
2. DESELECT and NOP are functionally interchangeable.
3. Autoprecharge is non-persistent. AP High enables Auto Precharge, while AP Low disables Autoprecharge.
4. Burst Terminate applies to only Read bursts with Auto Precharge disabled. This command is undefined and should not be used for Read with Auto Precharge enabled, and for Write bursts.
5. If AP is Low, bank address determines which bank is to be precharged. If AP is High, all banks are precharged and BA0-BA1are don't care.
6. This command is AUTO REFRESH if CKE is High, and SELF REFRESH if CKE is low.
7. All address inputs and I/O are 'don't care' except for CKE. Internal refresh counters control bank and row addressing.
8. All banks must be precharged before issuing an AUTO-REFRESH or SELF REFRESH command.
9. BA0 and BA1 value select between MRS and EMRS.
10. CKE is HIGH for all commands shown except SELF REFRESH.

TRUTH TABLE - DM Operations

FUNCTION	DM	DQ
Write Enable	L	Valid
Write Inhibit	H	X

Note: Used to mask write data, provided coincident with the corresponding data.

ADDRESSING

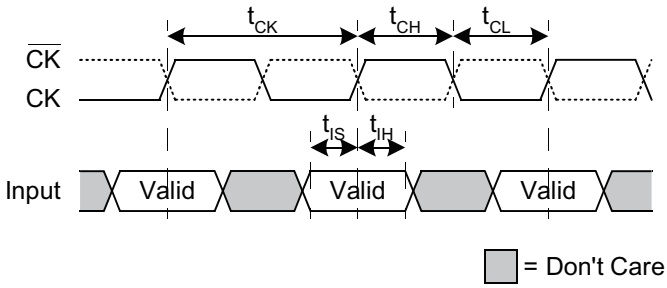
	x16	x8
Auto Precharge (AP)	A10	A10
Row Address (RA)	A0-A12	A0-A12
Column Address (CA)	A0-A9	A0-A9, A11

TRUTH TABLE - CKE

CKE n-1	CKE n	Current State	COMMAND n	ACTION n	NOTES
L	L	Power Down	X	Maintain Power Down	
L	L	Self Refresh	X	Maintain Self Refresh	
L	H	Power Down	NOP or DESELECT	Exit Power Down	6
L	H	Self Refresh	NOP or DESELECT	Exit Self Refresh	6, 7
H	L	All Banks Idle	NOP or DESELECT	Precharge Power Down Entry	6
H	L	Bank(s) Active	NOP or DESELECT	Active Power Down Entry	6
H	L	All Banks Idle	AUTO REFRESH	Self Refresh entry	
H	H	See Truth Tables - Commands			

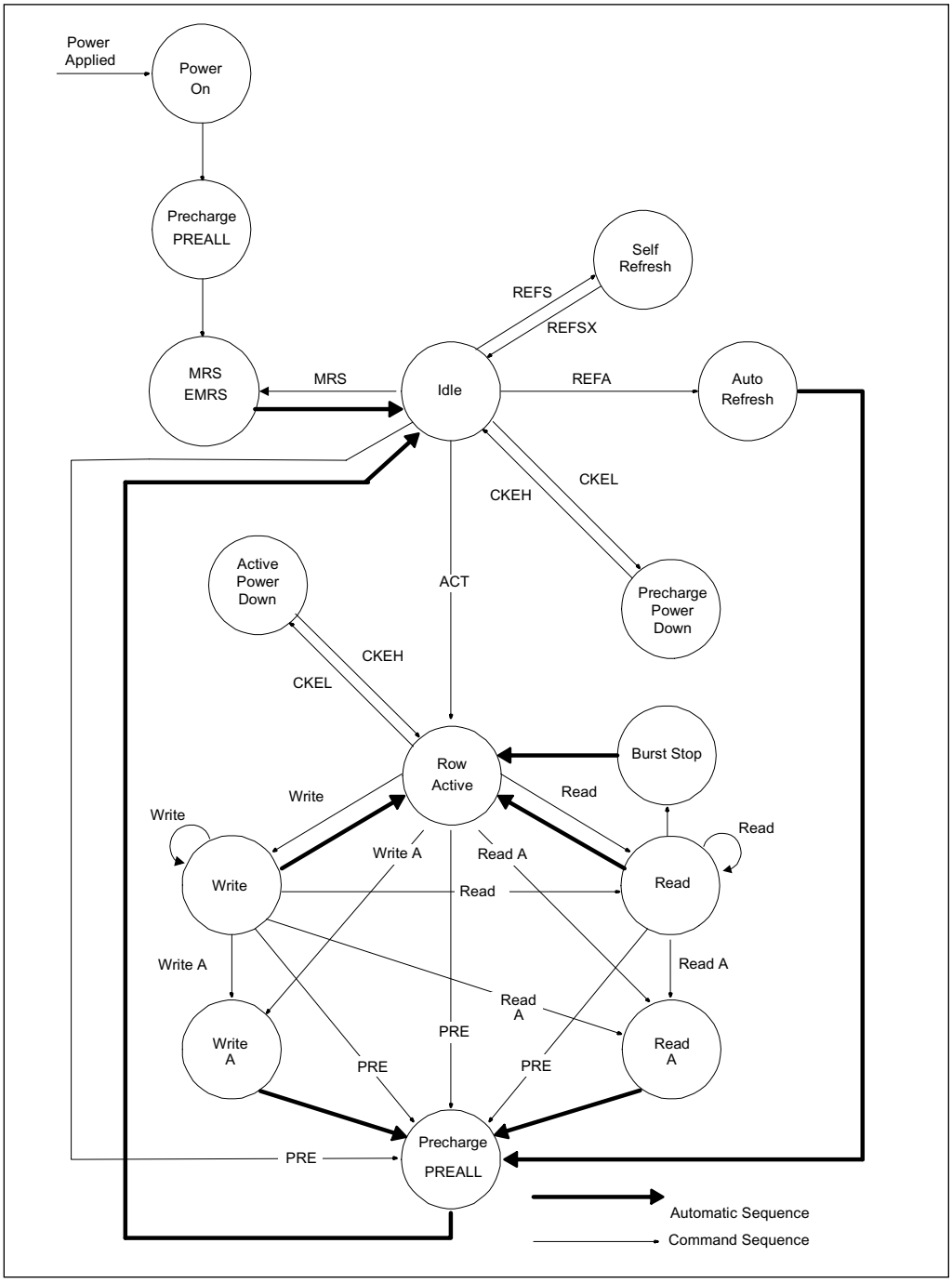
Notes:
1. CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2. Current state is the state of DDR immediately prior to clock edge n.
3. COMMANDn is the command registered at clock edge n, and ACTIONn is the result of COMMANDn.
4. All states and sequences not shown are illegal or reserved.
5. CKE must not go LOW during a Read or Write, and must stay HIGH until after t_{RPST} or t_{WR}, respectively.
6. DESELECT and NOP are functionally interchangeable.
7. NOPs or Deselects must be issued for at least t_{SNR} after Self-Refresh exit before any other command. After DLL Reset, at least t_{XSRD} must elapse before any Read commands occur.

Basic Timing Parameters for Commands



NOTE: Input = A0 - An, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$;
An = Address bus MSB

SIMPLIFIED STATE DIAGRAM



PREALL = Precharge All Banks

CKEL = Enter Power Down

MRS = Mode Register Set

CKEH = Exit Power Down

EMRS = Extended Mode Register Set

ACT = Active

REFS = Enter Self Refresh

Write A = Write with Autoprecharge

REFSX = Exit Self Refresh

Read A = Read with Autoprecharge

REFA = Auto Refresh

PRE = Precharge

FUNCTIONAL DESCRIPTION

The DDR SDRAM is a high speed CMOS, dynamic random-access memory internally configured as a quad-bank DRAM. The 512Mb devices contains: 536,870,912 bits.

The DDR SDRAM uses double data rate architecture to achieve high speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins. Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation

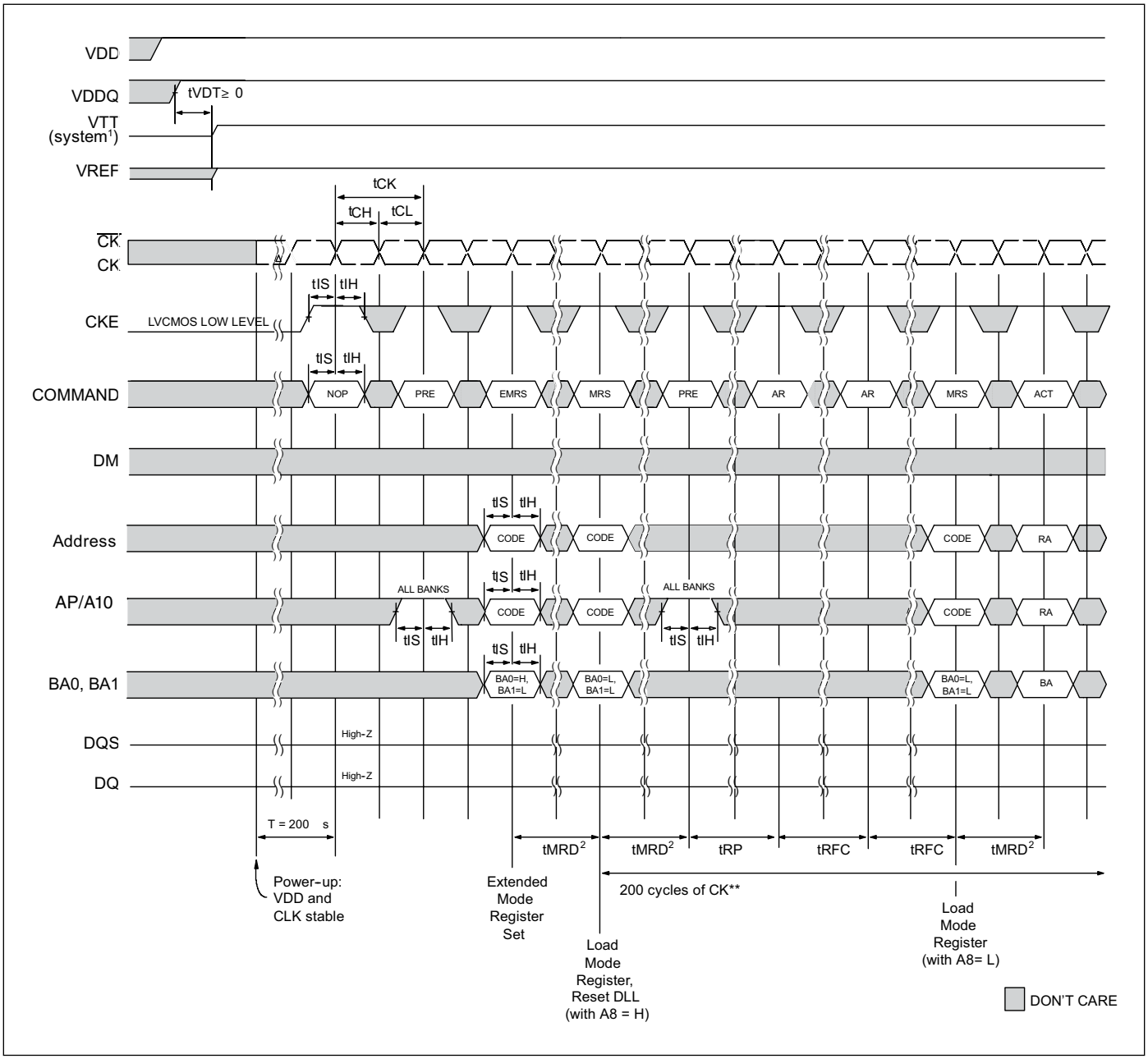
INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operations procedures other than those specified may result in undefined operation. If there is any interruption to the device power, the initialization routine should be followed. The steps to be followed for device initialization are listed below. The Initialization Flow diagram and the Initialization Flow sequence are shown in the following figures.

The Mode Register and Extended Mode Register do not have default values. If they are not programmed during the initialization sequence, it may lead to unspecified operation. The clock stop feature is not available until the device has been properly initialized from Step 1 through 13.

- Step 1: Apply VDD before or at the same time as VDDQ.
- Step 2: CKE must maintain LVCMOS Low until VREF is stable. Apply VDDQ before applying VTT and VREF.
- Step 3: There must be at least 200 µs of valid clocks before any command may be given to the DRAM. During this time NOP or DESELECT commands must be issued on the command bus and CKE should be brought HIGH.
- Step 4: Issue a PRECHARGE ALL command.
- Step 5: Provide NOPs or DESELECT commands for at least tRP time.
- Step 6: Issue EMRS command
- Step 7: Issue MRS command, load the base mode register and to reset the DLL. Set the desired operating modes.
- Step 8: Provide NOPs or DESELECT commands for at least tMRD time.
- Step 9: Issue a PRECHARGE ALL command
- Step 10: Issue 2 or more AUTO REFRESH cycles
- Step 11: Issue MRS command with the reset DLL bit deactivated to program operating parameters without resetting the DLL
- Step 12: Provide NOP or DESELECT commands for at least tMRD time.
- Step 13: The DRAM has been properly initialized and is ready for any valid command.

Initialization Waveform Sequence

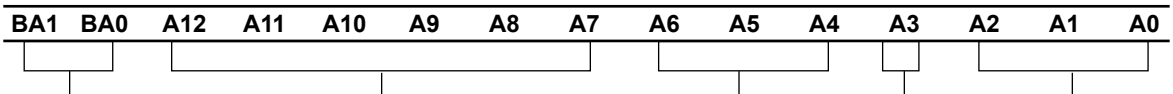


Notes:
1. VTT is not applied directly to the device, however tVTD must be greater than or equal to zero to avoid device latch--up.
2. tMRD is required before any command can be applied, and 200 cycles of CK are required before any executable command can be applied
3. The two Auto Refresh commands may be moved to follow the first MRS but precede the second PRECHARGE ALL command.

MODE REGISTER (MR) DEFINITION

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the definition of a burst length, a burst type, and a CAS latency. The Mode Register is programmed via the MODE REGISTER SET command (with BA0=0 and BA1=0) and will retain the stored information until it is reprogrammed, or the device loses power. Mode Register bits A0-A2 specify the burst length, A3 the type of burst (sequential or interleave), A4-A6 the CAS latency, and A8 DLL reset. A logic 0 should be programmed to all the undefined addresses bits to ensure future compatibility. The Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation. Reserved states should not be used, as unknown operation or incompatibility with future versions may result

MODE REGISTER



A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A3	Burst Type
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

A12	A11	A10	A9	A8	A7	DLL
0	0	0	0	0	0	Normal operation
0	0	0	0	1	0	Reset DLL

BA1	BA0	Mode Register Definition
0	0	Program Mode Register
0	1	Program Extended Mode Register
1	0	Reserved
1	1	Reserved

Notes:
1. A logic 0 should be programmed to all unused / undefined address bits to ensure future compatibility.

BURST LENGTH

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being set and the burst order as in Burst Definition. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			**A 0**		
			0	0-1	0-1
			1	1-0	1-0
4		**A 1**	**A 0**		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	**A 2**	**A 1**	**A 0**		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Notes:
1. For a burst length of two, A1-An selects the two data element block; A0 selects the first access within the block.
2. For a burst length of four, A2-An selects the four data element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-An selects the eight data element block; A0-A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence, the following access wraps within the block.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within the block, meaning that the burst will wrap within the block if a boundary is reached.

The block is uniquely selected by A1-An when the burst length is set to two, by A2-An when the burst length is set to 4, by A3-An when the burst length is set to 8. An is the most significant column address bit, which depends if the device is x8 or x16. The programmed burst length applies to both read and write bursts.

BURST TYPE

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address.

READ LATENCY

The READ latency, or CAS latency, is the delay between the registration of a READ command and the availability of the first piece of output data.

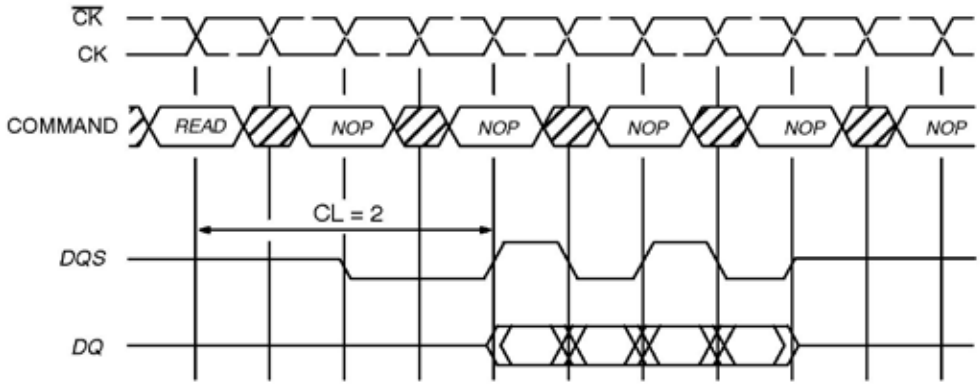
If a READ command is registered at a clock edge n and the latency is 3 clocks, the first data element will be valid at n + 2tCK + tAC. If a READ command is registered at a clock edge n and the latency is 2 clocks, the first data element will be valid at n + tCK + tAC.

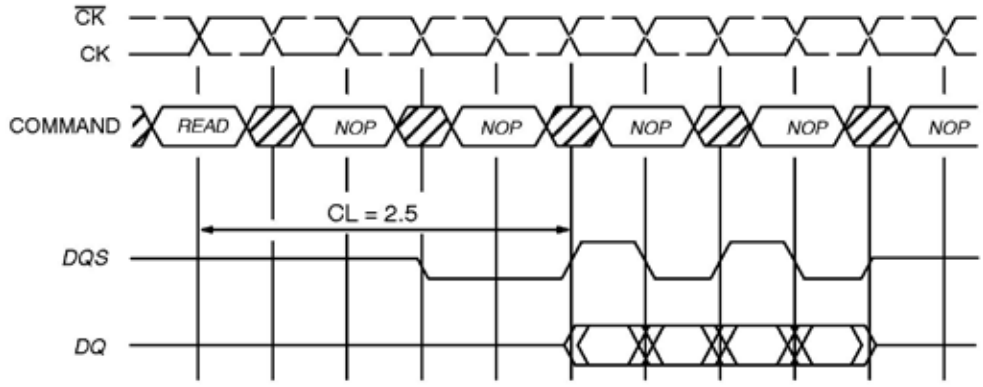
OPERATING MODE

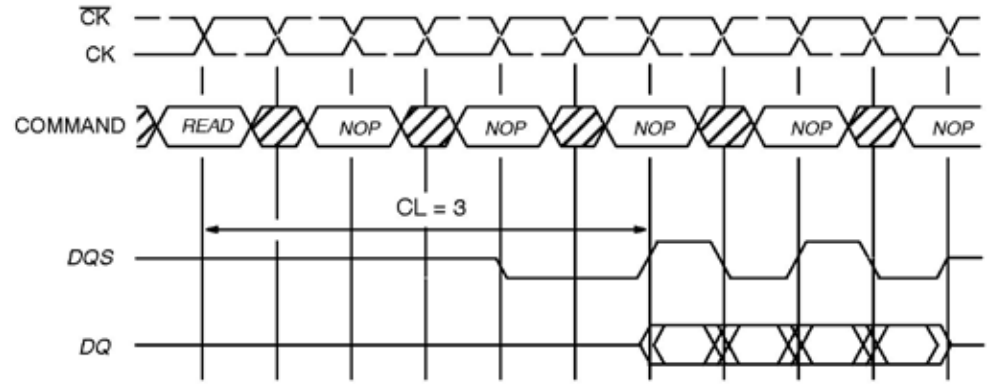
The normal operating mode is selected by issuing a Mode Register Set command with bits A7 to A12 each set to zero, and bits A0 to A6 set to the desired values. A DLL reset is initiated by issuing a Mode Register Set command with bits A7 and A9 to A12 each set to zero, bit A8 set to one, and bits A0 to A6 set to the desired values. A Mode Register Set command issued to reset the DLL must always be followed by a Mode Register Set command to select normal operating mode (A8=0).

All other combinations of values for A7 to A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

CAS LATENCIES







Burst Length = 4 in the cases shown
Shown with nominal tDQSCK

DON'T CARE

EXTENDED MODE REGISTER (EMR) DEFINITION

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, and output drive strength selection. The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA1=0 and BA0=1) and will retain the stored information until it is reprogrammed, or the device loses power. The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

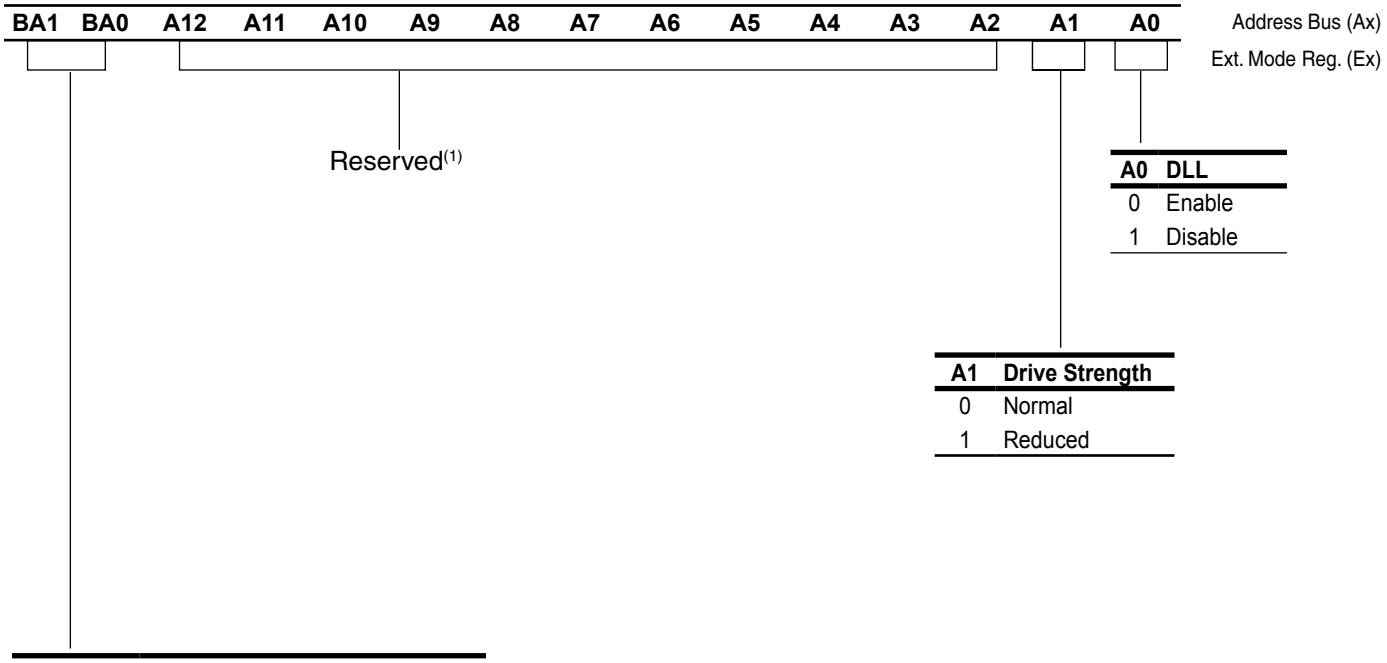
DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation (upon exiting Self Refresh Mode, the DLL is enabled automatically). Any time the DLL is enabled a DLL Reset must follow and 200 clock cycles must occur before any executable command can be issued.

OUTPUT DRIVE STRENGTH (DS)

The normal drive strength for all outputs is specified to be SSTL_2, Class II. This DRAM also supports a reduced driver strength option, intended for lighter load and/or point-to-point environments. I--V curves for the normal drive strength and weak drive strength are included in this datasheet.

EXTENDED MODE REGISTER



BA1	BA0	Mode Register Definition
0	0	Program Mode Register
0	1	Program Extended Mode Register
1	0	Reserved
1	1	Reserved

NOTES:
1. A logic 0 should be programmed to all unused/undefined address bits to ensure future compatibility

Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Voltage on any pin relative to VSS	V_{IN}, V_{OUT}	-1.0 ~ 3.6	V
Voltage on VDD & VDDQ supply relative to VSS	V_{DD}, V_{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.5	W
Short circuit current	I_{OS}	50	mA

Note:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommend operation condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability

AC/DC Electrical Characteristics and Operating Conditions

Recommended operating conditions (Voltage referenced to VSS=0V; TA=0 to 70°C for Commercial, TA = -40°C to +85°C for Industrial and A1, TA = -40°C to +105°C for A2)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage (with a nominal VDD of 2.5V for -5, -6)	V_{DD}	2.3	2.7	V	
Supply voltage (with a nominal VDD of 2.5V for -4)	V_{DD}	2.4	2.6	V	
I/O Supply voltage (with a nominal VDD of 2.5V for -5, -6)	V_{DDQ}	2.3	2.7	V	
I/O Supply voltage (with a nominal VDD of 2.5V for -4)	V_{DDQ}	2.4	2.6	V	
I/O Reference voltage	V_{REF}	0.49*VDDQ	0.51*VDDQ	V	1
I/O Termination voltage (system)	V_{TT}	VREF-0.04	VREF+0.04	V	2
Input logic high voltage	$V_{IH(DC)}$	VREF+0.15	VDDQ+0.3	V	
Input logic low voltage	$V_{IL(DC)}$	-0.3	VREF-0.15	V	
Input Voltage Level, CLK and CLK inputs	$V_{IN(DC)}$	-0.3	VDDQ+0.3	V	
Input Differential Voltage, CLK and CLK inputs	$V_{ID(DC)}$	0.36	VDDQ+0.6	V	3
V-I Matching: Pullup to Pulldown Current Ratio	V_I(Ratio)	0.71	1.4	–	4
Input leakage current	I_L	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current (Normal strength driver) ; VOUT = VTT + 0.84V	I_{OH}	-16.8	–	mA	
Output High Current (Normal strength driver) ; VOUT = VTT - 0.84V	I_{OL}	16.8	–	mA	
Output High Current (Half strength driver); VOUT = VTT + 0.45V	I_{OHR}	-9	–	mA	
Output High Current (Half strength driver); VOUT = VTT - 0.45V	I_{OLR}	9	–	mA	
Ambient Operating Temperature					
Commercial	T_A	0	+70	°C	
Industrial	T_A	-40	+85	°C	
A1	T_A	-40	+85	°C	
A2	T_A	-40	+105	°C	

Note :
1. VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the dc level of same. Peak-to peak noise on VREF may not exceed +/-2% of the dc value.
2. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
3. VID is the magnitude of the difference between the input level on CLK and the input level on CLK.
4. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25V to 1.0V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7 for device drain to source voltages from 0.1 to 1.0.

CAPACITANCE CHARACTERISTICS

(V_{DD} = V_{DDQ} = 2.5V + 0.2V, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits		Units
			Min	Max	
CI(A)	Input Capacitance, address pin	VI=1.25v	1.3	3	pF
CI(C)	Input Capacitance, control pin	f=100MHz	1.3	3	pF
CI(K)	Input Capacitance, CLK pin	VI=25mVrms	1.3	3	pF
CI/O	I/O Capacitance, I/O, DQS, DM pin		2	5	pF

Notes:
1. This parameter is characterized.
2. Conditions: Frequency = 100MHz; V_{OUT}(DC) = V_{DD}/2; V_{OUT}(peak-to-peak) = 0.2V; V_{REF} = Vss.

THERMAL RESISTANCE

Package	Subtrate	Theta-ja (Airflow = 0m/s)	Theta-ja (Airflow = 1m/s)	Theta-ja (Airflow = 2m/s)	Theta-jc	Units
TSOP2(66)	4-layer	88.1	80.8	76.8	18.9	C/W
BGA(60)	4-layer	54.8	49.2	47.6	11.6	C/W

IDD Specification Parameters and Test Conditions:

(V_{DD} = V_{DDQ} = 2.5V ± 0.2V (-5, -6), V_{DD} = V_{DDQ} = 2.5V ± 0.1V (-4), Vss = VssQ = 0V, Output Open, unless otherwise noted)

Symbol	Parameter/ Test Condition	-4	-5	-6	Units
IDD0	Operating current for one bank active-precharge; tRC = tRC(min); tCK = tCK(min); DQ, DM and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles; CS = high between valid commands.	100	90	80	mA
IDD1	Operating current for one bank operation; one bank open, BL = 4, tRC = tRC(min), tCK = tCK(min), Iout=0mA, Address and control inputs changing once per clock cycle.	100	90	80	mA
IDD2P	Precharge power-down standby current; all banks idle; power-down mode; CKE VIL(max); tCK = tCK(min); VIN = VREF for DQ, DQS and DM	35	35	35	mA
IDD2F	Precharge floating standby current; CS VIH(min); all banks idle; CKE VIH(min); tCK = tCK(min); address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DQS and DM	70	65	60	mA
IDD3P	Active power-down standby current; one bank active; power-down mode; CKE VIL(max); tCK = tCK(min); VIN = VREF for DQ, DQS and DM	35	35	35	mA
IDD3N	Active standby current; CS VIH(min); CKE VIH(min); one bank active; tRC = tRAS(max); tCK = tCK(min); DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	80	75	70	mA
IDD4R	Operating current for burst read; burst length = 2; reads; continuous burst; one bank active; address and control inputs changing once per clock cycle; tCK = tCK(min); 50% of data changing on every transfer; IOUT = 0mA	160	150	140	mA
IDD4W	Operating current for burst write; burst length = 2; writes; continuous burst; one bank active address and control inputs changing once per clock cycle; tCK = tCK(min); DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every transfer	160	150	140	mA
IDD5	Auto refresh current; tRC = tRFC(min);	170	160	150	mA
IDD6	Self refresh current; CKE 0.2V;	8	8	8	mA
IDD7	Operating current for four bank operation; four bank interleaving READs (BL=4) with auto precharge; tRC = tRC(min), tCK = tCK(min); Address and control inputs change only during ACTIVE, READ, or WRITE commands	260	240	220	mA

AC TIMING REQUIREMENTS

Absolute Specifications (VDD, VDDQ = +2.5 V ±0.1 V)

PARAMETER	SYMBOL	-4		UNITS
		MIN	MAX	
DQ output access time for CLK,/CLK	tAC	-0.7	0.7	ns
DQS output access time for CLK,/CLK	tDQSCK	-0.6	0.6	ns
CLK high-level width	tCH	0.45	0.55	tCK
CLK low-level width	tCL	0.45	0.55	tCK
CLK half period	tHP	min (tCL,tCH)	–	ns
CLK cycle time CL=3	tCK(3)	4	8	ns
CL=2.5	tCK(2.5)	6	12	ns
CL=2	tCK(2)	7.5	12	ns
DQ and DM input hold time	tDH	0.4	–	ns
DQ and DM input setup time	tDS	0.4	–	ns
Control & Address input pulse width (for each input)	tIPW	2.2	–	ns
DQ and DM input pulse width (for each input)	tDIPW	1.75	–	ns
DQ & DQS high-impedance time from CLK,/CLK	tHZ	–	0.7	ns
DQ & DQS low--impedance time from CLK,/CLK	tLZ	-0.7	–	ns
DQS--DQ Skew, DQS to last DQ valid, per group, per access	tDQSQ	–	0.4	ns
DQ/DQS output hold time from DQS	tQH	tHP-tQHS	–	ns
Data Hold Skew Factor	tQHS	–	0.5	ns
Write command to first DQS latching transition	tDQSS	0.72	1.28	tCK
DQS input high pulse width	tDQSH	0.35	–	tCK
DQS input low pulse width	tDQSL	0.35	–	tCK
DQS falling edge to CLK setup time	tDSS	0.2	–	tCK
DQS falling edge hold time from CLK	tDSH	0.2	–	tCK
MODE REGISTER SET command cycle time	tMRD	2	–	tCK
Write preamble setup time	tWPRES	0.25	–	tCK
Write postamble	tWPST	0.4	0.6	tCK
Write preamble	tWPRE	0.25	–	tCK
Address and Control input hold time (fast slew rate)	tIHF	0.6	–	ns
Address and Control input setup time (fast slew rate)	tISF	0.6	–	ns
Address and Control input hold time (slow slew rate)	tIH	0.7	-–	ns
Address and Control input setup time (slow slew rate)	tIS	0.7	–	ns
Read preamble	tRPRE	0.9	1.1	tCK
Read postamble	tRPST	0.4	0.6	tCK
ACTIVE to PRECHARGE command	tRAS	40	70,000	ns

AC TIMING REQUIREMENTS

Absolute Specifications (VDD, VDDQ = +2.5 V ±0.1 V)

PARAMETER		SYMBOL	-4		UNITS
			MIN	MAX	
ACTIVE to ACTIVE/Auto Refresh command period		tRC	55	–	ns
Auto Refresh to Active/Auto		tRFC	70	–	ns
ACTIVE to READ or WRITE delay		tRCD	15	–	ns
PRECHARGE command period		tRP	15	–	ns
Active to Autoprecharge Delay		tRAP	15	–	ns
ACTIVE bank A to ACTIVE bank B command		tRRD	10	–	ns
Write recovery time		tWR	15	–	ns
Auto Precharge write recovery + precharge time		tDAL	tWR+tRP	–	tCK
Internal Write to Read Command Delay		tWTR	2	–	tCK
Exit self refresh to non-READ		tXSNR	70	–	ns
Exit self refresh to READ command		tXSRD	200	–	tCK
Average Periodic Refresh Interval	$T_A \leq 85^oC$	tREFI	–	7.8	µs

AC TIMING REQUIREMENTS

Absolute Specifications (VDD, VDDQ = +2.5 V ±0.2 V)

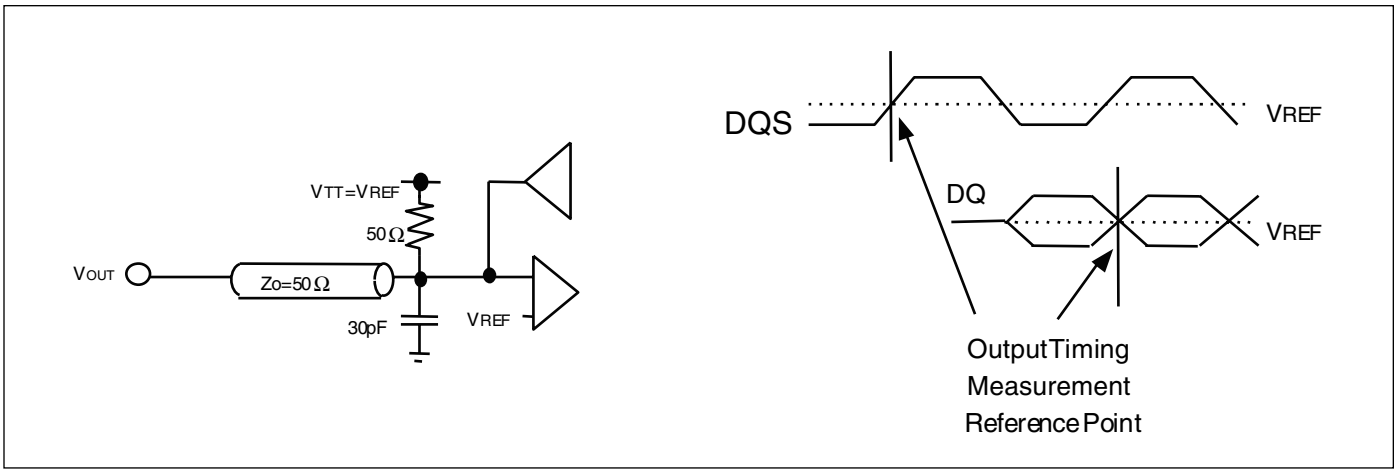
PARAMETER	SYMBOL	-5		-6		UNITS
		MIN	MAX	MIN	MAX	
DQ output access time for CLK,/CLK	tAC	-0.7	0.7	-0.7	0.7	ns
DQS output access time for CLK,/CLK	tDQSCK	-0.6	0.6	-0.6	0.6	ns
CLK high-level width	tCH	0.45	0.55	0.45	0.55	tCK
CLK low-level width	tCL	0.45	0.55	0.45	0.55	tCK
CLK half period	tHP	min (tCL,tCH)	–	min (tCL,tCH)	–	ns
CLK cycle time CL=3	tCK(3)	5	8	6	12	ns
CL=2.5	tCK(2.5)	6	12	6	12	ns
CL=2	tCK(2)	7.5	12	7.5	12	ns
DQ and DM input hold time	tDH	0.4	–	0.45	–	ns
DQ and DM input setup time	tDS	0.4	–	0.45	–	ns
Control & Address input pulse width (for each input)	tIPW	2.2	–	2.2	–	ns
DQ and DM input pulse width (for each input)	tDIPW	1.75	–	1.75	–	ns
DQ & DQS high-impedance time from CLK,/CLK	tHZ	–	0.7	–	0.7	ns
DQ & DQS low--impedance time from CLK,/CLK	tLZ	-0.7	–	-0.7	–	ns
DQS--DQ Skew, DQS to last DQ valid, per group, per access	tDQSQ	–	0.4	–	0.45	ns
DQ/DQS output hold time from DQS	tQH	tHP-tQHS	–	tHP-tQHS	–	ns
Data Hold Skew Factor	tQHS	–	0.5	–	0.55	ns
Write command to first DQS latching transition	tDQSS	0.72	1.28	0.75	1.28	tCK
DQS input high pulse width	tDQSH	0.35	–	0.35	–	tCK
DQS input low pulse width	tDQSL	0.35	–	0.35	–	tCK
DQS falling edge to CLK setup time	tDSS	0.2	–	0.2	–	tCK
DQS falling edge hold time from CLK	tDSH	0.2	–	0.2	–	tCK
MODE REGISTER SET command cycle time	tMRD	2	–	2	–	tCK
Write preamble setup time	tWPRES	0.25	–	0.25	–	tCK
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK
Write preamble	tWPRE	0.25	–	0.25	–	tCK
Address and Control input hold time (fast slew rate)	tIHF	0.6	–	0.75	–	ns
Address and Control input setup time (fast slew rate)	tISF	0.6	–	0.75	–	ns
Address and Control input hold time (slow slew rate)	tIH	0.7	–	0.8	––	ns
Address and Control input setup time (slow slew rate)	tIS	0.7	–	0.8	–	ns
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK
ACTIVE to PRECHARGE command	tRAS	40	70,000	42	120,000	ns

AC TIMING REQUIREMENTS

Absolute Specifications (VDD, VDDQ = +2.5 V ±0.2 V)

PARAMETER		SYMBOL	-5		-6		UNITS
			MIN	MAX	MIN	MAX	
ACTIVE to ACTIVE/Auto Refresh command period		tRC	55	–	60	–	ns
Auto Refresh to Active/Auto		tRFC	70	–	72	–	ns
ACTIVE to READ or WRITE delay		tRCD	15	–	18	–	ns
PRECHARGE command period		tRP	15	–	18	–	ns
Active to Autoprecharge Delay		tRAP	0.5	–	18	–	ns
ACTIVE bank A to ACTIVE bank B command		tRRD	10	–	12	–	ns
Write recovery time		tWR	15	–	15	–	ns
Auto Precharge write recovery + precharge time		tDAL	tWR+tRP	–	tWR+tRP	–	tCK
Internal Write to Read Command Delay		tWTR	2	–	2	–	tCK
Exit self refresh to non-READ		tXSNR	70	–	70	–	ns
Exit self refresh to READ command		tXSRD	200	–	200	–	tCK
Average Periodic Refresh Interval	$T_A \leq 85$ °C	tREFI	–	7.8	–	7.8	µs
Average Periodic Refresh Interval	$T_A > 85$ °C, A2 only	tREFI	–	1.9	–	1.9	µs

Output Load Condition



AC Input Operating Conditions

(VDD = VDDQ = 2.5 ± 0.2V, VSS= VSSQ= 0V, output open, unless otherwise noted.)

Parameter/Condition	Symbol	Min	Max	Units
Input high (logic 1) voltage	VIH(AC)	VREF+0.310	-	V
Input low (logic 0) voltage	VIL(AC)	-	VREF-0.310	V
I/O reference voltage	VREF(AC)	0.49 x VDDQ	0.51 x VDDQ	V

Notes

1. All voltages referenced to Vss.
2. Tests for AC timing, IDD, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. AC timing and IDD tests may use a VIL to VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK//CK), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between VIL(AC) and VIH(AC).
4. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.
5. VREF is expected to be equal to 0.5*VddQ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed +2% of the DC value.
6. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF.
7. VID is the magnitude of the difference between the input level on CLK and the input level on /CLK.
8. The value of VIX is expected to equal 0.5*VddQ of the transmitting device and must track variations in the DC level of the same.
9. IDD specifications are tested after the device is properly initialized.
10. The CLK//CLK input reference level (for timing referenced to CLK//CLK) is the point at which CLK and /CLK cross; the input reference level for signals other than CLK//CLK, is VREF.
11. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE< 0.3VddQ is recognized as LOW.
12. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ), or begins driving (LZ).
13. The maximum limit for tWPRES is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
14. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CLK edge. A valid transition is defined as monotonic, and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
15. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
16. tXPRD should be 200 tCLK in the condition of the unstable CLK operation during the power down mode.
17. For command/address and CK & /CK slew rate > 1.0V/ns.
18. For slew rates less than 1V/ns and greater than or equal to 0.5V/ns. If the slew rate is less than 0.5V/ns, timing must be derated: tIS has an additional 50ps per each 100mV/ns reduction in slew rate from the 500 mV/ns. tIH has nothing added. If the slew rate exceeds 4.5V/ns, functionality is uncertain. For operation at 166mHz or faster, slew rates must be greater than or equal to 0.5 V/ns.
19. To maintain a valid level, the transitioning edge of the input must:
    a. Sustain a constant slew rate from the current AC level through to the target AC level, VIL(AC) or VIH(AC).
    b. Reach at least the target AC level.
    c. After the AC target level is reached, continue to maintain at least the target DC level, VIL(DC) or VIH(DC)
20. VIH overshoot: VIHmax = VDDQ + 1.5V for a pulse width ≤ 3ns, and the pulse width can not be greater than 1/3 of the cycle rate. VIL undershoot: VIL undershoot: VIL, min = -1.5V for a pulse width ≤ 3ns, and the pulse width can not be greater than 1/3 of the cycle rate.
21. Min (tCL,tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device.
22. For A2 temperature grade with TA > 85°C: IDD2F, IDD3N and IDD7 are derated to 10% above these values; IDD2P and IDD6 are derated to 20% above these values.