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# IS42S32400E IS45S32400E



## 4M x 32 128Mb SYNCHRONOUS DRAM

NOVEMBER 2010

### FEATURES

- Clock frequency: 166, 143, 133 MHz
- Fully synchronous; all signals referenced to a positive clock edge
- Internal bank for hiding row access/precharge
- Single Power supply: 3.3V  $\pm$  0.3V
- LVTTTL interface
- Programmable burst length  
– (1, 2, 4, 8, full page)
- Programmable burst sequence:  
Sequential/Interleave
- Auto Refresh (CBR)
- Self Refresh
- 4096 refresh cycles every 16ms (A2 grade) or 64 ms (Commercial, Industrial, A1 grade)
- Random column address every clock cycle
- Programmable  $\overline{\text{CAS}}$  latency (2, 3 clocks)
- Burst read/write and burst read/single write operations capability
- Burst termination by burst stop and precharge command

### OPTIONS

- Package:  
86-pin TSOP-II  
90-ball TF-BGA
- Operating Temperature Range:  
Commercial (0°C to +70°C)  
Industrial (-40°C to +85°C)  
Automotive Grade, A1 (-40°C to +85°C)  
Automotive Grade, A2 (-40°C to +105°C)

### OVERVIEW

ISSI's 128Mb Synchronous DRAM achieves high-speed data transfer using pipeline architecture. All inputs and outputs signals refer to the rising edge of the clock input. The 128Mb SDRAM is organized in 1Meg x 32 bit x 4 Banks.

### KEY TIMING PARAMETERS

Parameter	-6	-7	-75E	Unit
Clk Cycle Time				
$\overline{\text{CAS}}$ Latency = 3	6	7	–	ns
$\overline{\text{CAS}}$ Latency = 2	10	10	7.5	ns
Clk Frequency				
$\overline{\text{CAS}}$ Latency = 3	166	143	–	Mhz
$\overline{\text{CAS}}$ Latency = 2	100	100	133	Mhz
Access Time from Clock				
$\overline{\text{CAS}}$ Latency = 3	5.4	5.4	–	ns
$\overline{\text{CAS}}$ Latency = 2	6.5	6.5	5.5	ns

### ADDRESS TABLE

Parameter	4M x 32
Configuration	1M x 32 x 4 banks
Refresh Count	Com./Ind. 4K / 64ms
	A1 4K / 64ms
	A2 4K / 16ms
Row Addresses	A0 – A11
Column Addresses	A0 – A7
Bank Address Pins	BA0, BA1
Autoprecharge Pins	A10/AP

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- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances



## DEVICE OVERVIEW

The 128Mb SDRAM is a high speed CMOS, dynamic random-access memory designed to operate in 3.3V V<sub>DD</sub> and 3.3V V<sub>DDQ</sub> memory systems containing 134,217,728 bits. Internally configured as a quad-bank DRAM with a synchronous interface. Each 33,554,432-bit bank is organized as 4,096 rows by 256 columns by 32 bits.

The 128Mb SDRAM includes an AUTO REFRESH MODE, and a power-saving, power-down mode. All signals are registered on the positive edge of the clock signal, CLK. All inputs and outputs are LVTTTL compatible.

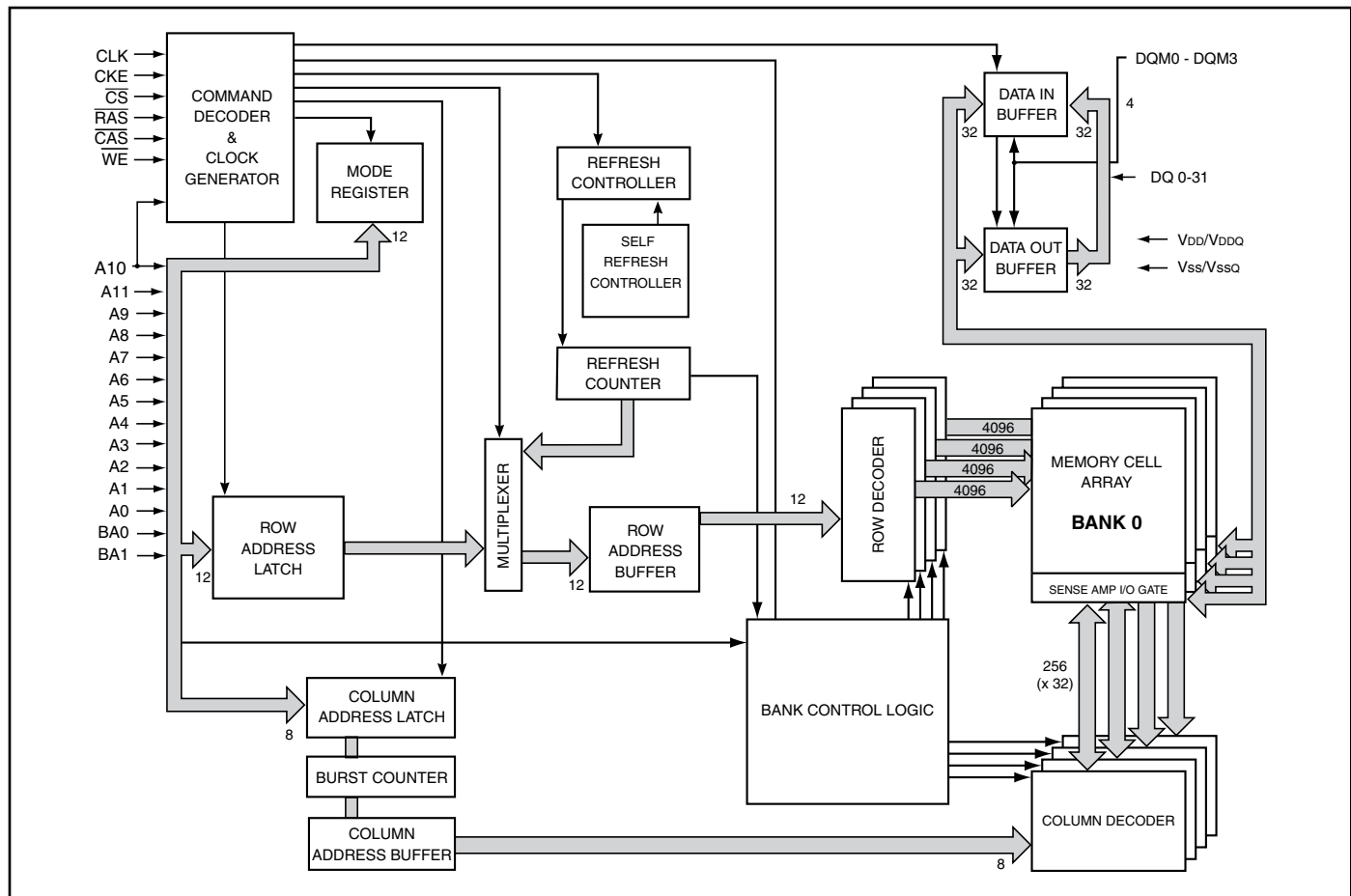
The 128Mb SDRAM has the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time and the capability to randomly change column addresses on each clock cycle during burst access.

A self-timed row precharge initiated at the end of the burst sequence is available with the AUTO PRECHARGE function enabled. Precharge one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

SDRAM read and write accesses are burst oriented starting at a selected location and continuing for a programmed number of locations in a programmed sequence. The registration of an ACTIVE command begins accesses, followed by a READ or WRITE command. The ACTIVE command in conjunction with address bits registered are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11 select the row). The READ or WRITE commands in conjunction with address bits registered are used to select the starting column location for the burst access.

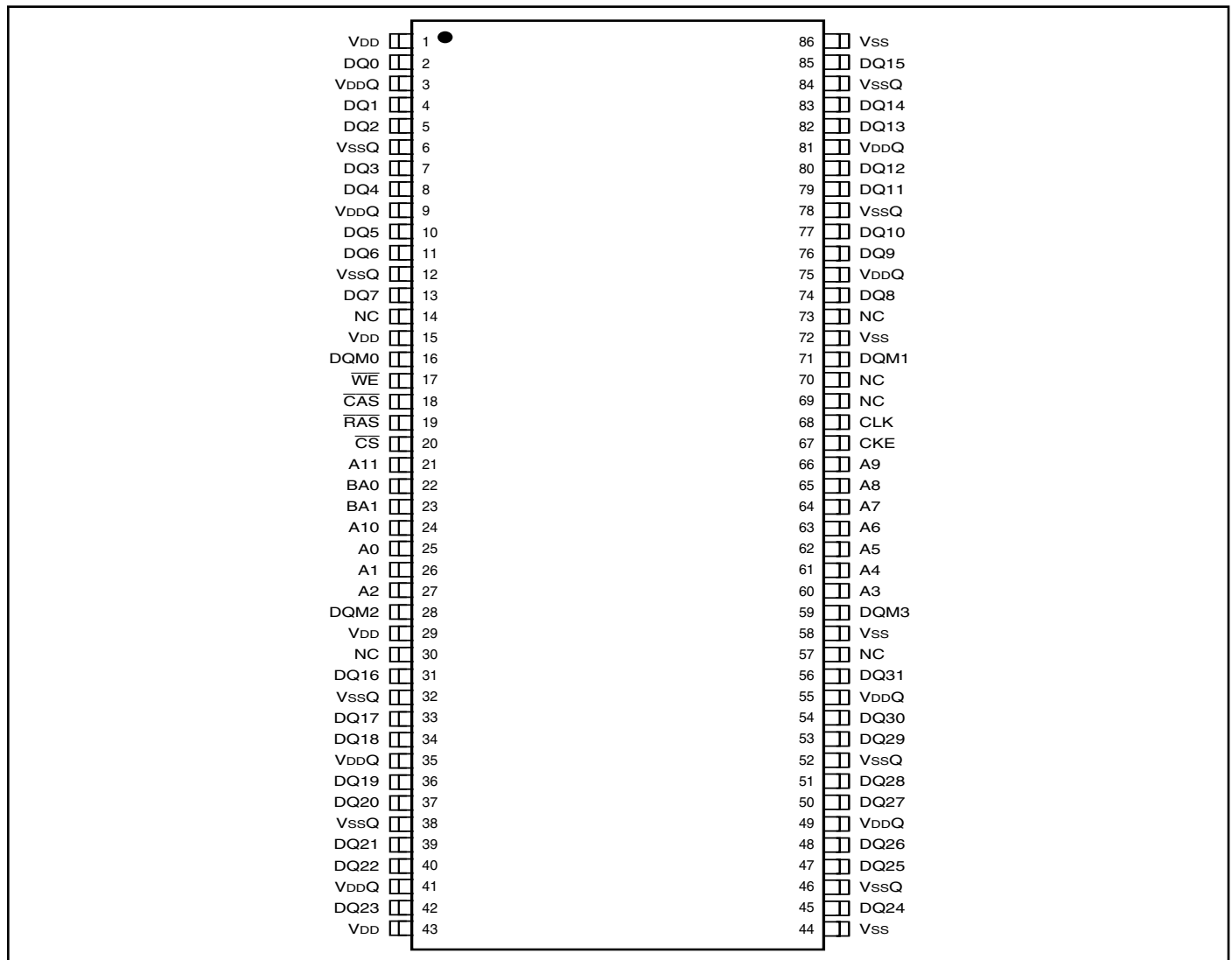
Programmable READ or WRITE burst lengths consist of 1, 2, 4 and 8 locations or full page, with a burst terminate option.

## FUNCTIONAL BLOCK DIAGRAM (FOR 1MX32X4 BANKS)



## PIN CONFIGURATIONS

86 pin TSOP - Type II for x32



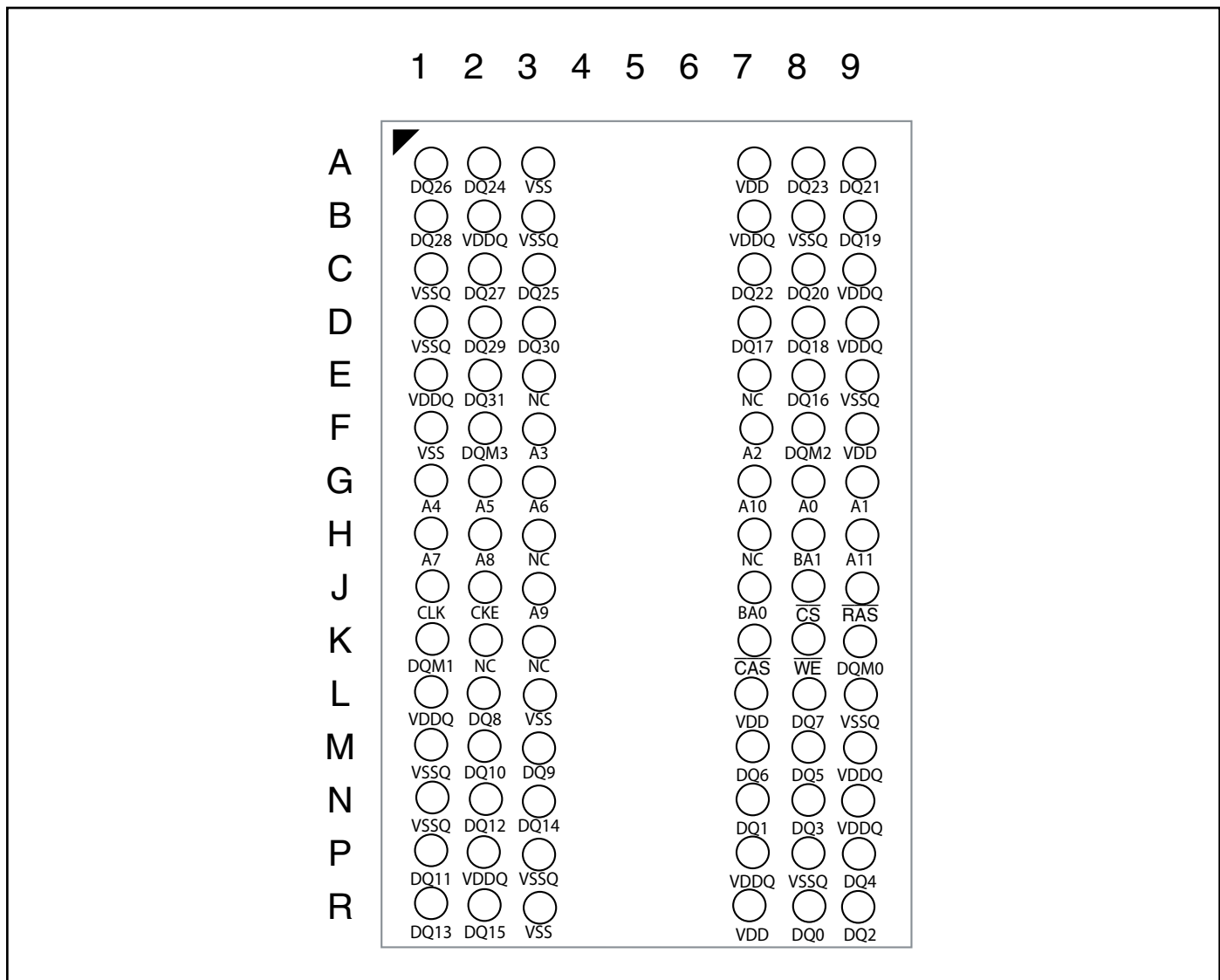
## PIN DESCRIPTIONS

A0-A11	Row Address Input
A0-A7	Column Address Input
BA0, BA1	Bank Select Address
DQ0 to DQ31	Data I/O
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command

$\overline{WE}$	Write Enable
DQM0-DQM3	x32 Input/Output Mask
VDD	Power
Vss	Ground
VDDQ	Power Supply for I/O Pin
VSSQ	Ground for I/O Pin
NC	No Connection

**PIN CONFIGURATION**

PACKAGE CODE: B 90 BALL TF-BGA (Top View) (8.00 mm x 13.00 mm Body, 0.8 mm Ball Pitch)


**PIN DESCRIPTIONS**

A0-A11	Row Address Input
A0-A7	Column Address Input
BA0, BA1	Bank Select Address
DQ0 to DQ31	Data I/O
CLK	System Clock Input
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$\overline{\text{CS}}$	Chip Select
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VDD	Power
VSS	Ground
VDDQ	Power Supply for I/O Pin
VSSQ	Ground for I/O Pin
NC	No Connection

**PIN FUNCTIONS**

Symbol	Type	Function (In Detail)
A0-A11	Input Pin	Address Inputs: A0-A11 are sampled during the ACTIVE command (row-address A0-A11) and READ/WRITE command (column address A0-A7), with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
BA0, BA1	Input Pin	Bank Select Address: BA0 and BA1 defines which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
$\overline{\text{CAS}}$	Input Pin	$\overline{\text{CAS}}$ , in conjunction with the $\overline{\text{RAS}}$ and $\overline{\text{WE}}$ , forms the device command. See the "Command Truth Table" for details on device commands.
CKE	Input Pin	The CKE input determines whether the CLK input is enabled. The next rising edge of the CLK signal will be valid when is CKE HIGH and invalid when LOW. When CKE is LOW, the device will be in either power-down mode, clock suspend mode, or self refresh mode. CKE is an asynchronous input.
CLK	Input Pin	CLK is the master clock input for this device. Except for CKE, all inputs to this device are acquired in synchronization with the rising edge of this pin.
$\overline{\text{CS}}$	Input Pin	The $\overline{\text{CS}}$ input determines whether command input is enabled within the device. Command input is enabled when $\overline{\text{CS}}$ is LOW, and disabled with $\overline{\text{CS}}$ is HIGH. The device remains in the previous state when $\overline{\text{CS}}$ is HIGH.
DQM0-DQM3	Input Pin	DQM0 - DQM3 control the four bytes of the I/O buffers (DQ0-DQ31). In read mode, DQMn control the output buffer. When DQMn is LOW, the corresponding buffer byte is enabled, and when HIGH, disabled. The outputs go to the HIGH impedance state when DQMn is HIGH. This function corresponds to $\overline{\text{OE}}$ in conventional DRAMs. In write mode, DQMn control the input buffer. When DQMn is LOW, the corresponding buffer byte is enabled, and data can be written to the device. When DQMn is HIGH, input data is masked and cannot be written to the device.
DQ0-DQ31	Input/Output Pin	Data on the Data Bus is latched on these pins during Write commands, and buffered after Read commands.
$\overline{\text{RAS}}$	Input Pin	$\overline{\text{RAS}}$ , in conjunction with $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ , forms the device command. See the "Command Truth Table" item for details on device commands.
$\overline{\text{WE}}$	Input Pin	$\overline{\text{WE}}$ , in conjunction with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ , forms the device command. See the "Command Truth Table" item for details on device commands.
V <sub>DDQ</sub>	Power Supply Pin	V <sub>DDQ</sub> is the output buffer power supply.
V <sub>DD</sub>	Power Supply Pin	V <sub>DD</sub> is the device internal power supply.
V <sub>SSQ</sub>	Power Supply Pin	V <sub>SSQ</sub> is the output buffer ground.
V <sub>SS</sub>	Power Supply Pin	V <sub>SS</sub> is the device internal ground.

## GENERAL DESCRIPTION

### READ

The READ command selects the bank from BA0, BA1 inputs and starts a burst read access to an active row. Inputs A0-A7 provides the starting column location. When A10 is HIGH, this command functions as an AUTO PRECHARGE command. When the auto precharge is selected, the row being accessed will be precharged at the end of the READ burst. The row will remain open for subsequent accesses when AUTO PRECHARGE is not selected. DQ's read data is subject to the logic level on the DQM inputs two clocks earlier. When a given DQM signal was registered HIGH, the corresponding DQ's will be High-Z two clocks later. DQ's will provide valid data when the DQM signal was registered LOW.

### WRITE

A burst write access to an active row is initiated with the WRITE command. BA0, BA1 inputs selects the bank, and the starting column location is provided by inputs A0-A7. Whether or not AUTO-PRECHARGE is used is determined by A10.

The row being accessed will be precharged at the end of the WRITE burst, if AUTO PRECHARGE is selected. If AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses.

A memory array is written with corresponding input data on DQ's and DQM input logic level appearing at the same time. Data will be written to memory when DQM signal is LOW. When DQM is HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

### PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. BA0, BA1 can be used to select which bank is precharged or they are treated as "Don't Care". A10 determined whether one or all banks are precharged. After executing this command, the next command for the selected bank(s) is executed after passage of the period  $t_{RP}$  which is the period required for bank precharging. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

### AUTO PRECHARGE

The AUTO PRECHARGE function ensures that the precharge is initiated at the earliest valid stage within a burst. This function allows for individual-bank precharge without requiring an explicit command. A10 to enable the AUTO

PRECHARGE function in conjunction with a specific READ or WRITE command. For each individual READ or WRITE command, auto precharge is either enabled or disabled. AUTO PRECHARGE does not apply except in full-page burst mode. Upon completion of the READ or WRITE burst, a precharge of the bank/row that is addressed is automatically performed.

### AUTO REFRESH COMMAND

This command executes the AUTO REFRESH operation. The row address and bank to be refreshed are automatically generated during this operation. The stipulated period ( $t_{RC}$ ) is required for a single refresh operation, and no other commands can be executed during this period. This command is executed at least 4096 times for every  $T_{REF}$ . During an AUTO REFRESH command, address bits are "Don't Care". This command corresponds to CBR Auto-refresh.

### BURST TERMINATE

The BURST TERMINATE command forcibly terminates the burst read and write operations by truncating either fixed-length or full-page bursts and the most recently registered READ or WRITE command prior to the BURST TERMINATE.

### COMMAND INHIBIT

COMMAND INHIBIT prevents new commands from being executed. Operations in progress are not affected, apart from whether the CLK signal is enabled

### NO OPERATION

When  $\overline{CS}$  is low, the NOP command prevents unwanted commands from being registered during idle or wait states.

### LOAD MODE REGISTER

During the LOAD MODE REGISTER command the mode register is loaded from A0-A11. This command can only be issued when all banks are idle.

### ACTIVE COMMAND

When the ACTIVE COMMAND is activated, BA0, BA1 inputs selects a bank to be accessed, and the address inputs on A0-A11 selects the row. Until a PRECHARGE command is issued to the bank, the row remains open for accesses.

**COMMAND TRUTH TABLE**

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA1	BA0	A11	
	n - 1	n							A10	A9 - A0
Device deselect (DESL)	H	x	H	x	x	x	x	x	x	x
No operation (NOP)	H	x	L	H	H	H	x	x	x	x
Burst stop (BST)	H	x	L	H	H	L	x	x	x	x
Read	H	x	L	H	L	H	V	V	L	V
Read with auto precharge	H	x	L	H	L	H	V	V	H	V
Write	H	x	L	H	L	L	V	V	L	V
Write with auto precharge	H	x	L	H	L	L	V	V	H	V
Bank activate (ACT)	H	x	L	L	H	H	V	V	V	V
Precharge select bank (PRE)	H	x	L	L	H	L	V	V	L	x
Precharge all banks (PALL)	H	x	L	L	H	L	x	x	H	x
CBR Auto-Refresh (REF)	H	H	L	L	L	H	x	x	x	x
Self-Refresh (SELF)	H	L	L	L	L	H	x	x	x	x
Mode register set (MRS)	H	x	L	L	L	L	L	L	L	V

Note: H=V<sub>IH</sub>, L=V<sub>IL</sub> x= V<sub>IH</sub> or V<sub>IL</sub>, V = Valid Data.

**DQM TRUTH TABLE**

Function	CKE		DQM	
	n-1	n	U	L
Data write / output enable	H	x	L	L
Data mask / output disable	H	x	H	H
Upper byte write enable / output enable	H	x	L	x
Lower byte write enable / output enable	H	x	x	L
Upper byte write inhibit / output disable	H	x	H	x
Lower byte write inhibit / output disable	H	x	x	H

Note: H=V<sub>IH</sub>, L=V<sub>IL</sub> x= V<sub>IH</sub> or V<sub>IL</sub>, V = Valid Data.



**CKE TRUTH TABLE**

Current State /Function	CKE		$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Address
	n - 1	n					
Activating Clock suspend mode entry	H	L	x	x	x	x	x
Any Clock suspend mode	L	L	x	x	x	x	x
Clock suspend mode exit	L	H	x	x	x	x	x
Auto refresh command Idle (REF)	H	H	L	L	L	H	x
Self refresh entry Idle (SELF)	H	L	L	L	L	H	x
Power down entry Idle	H	L	x	x	x	x	x
Self refresh exit	L	H	L	H	H	H	x
	L	H	H	x	x	x	x
Power down exit	L	H	x	x	x	x	x

Note: H= $V_{IH}$ , L= $V_{IL}$  x=  $V_{IH}$  or  $V_{IL}$ , V = Valid Data.

**FUNCTIONAL TRUTH TABLE**

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
Idle	H	X	X	X	X	DESL	Nop or Power Down <sup>(2)</sup>
	L	H	H	H	X	NOP	Nop or Power Down <sup>(2)</sup>
	L	H	H	L	X	BST	Nop or Power Down
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL <sup>(3)</sup>
	L	H	L	L	A, CA, A10	WRIT/ WRITA	ILLEGAL <sup>(3)</sup>
	L	L	H	H	BA, RA	ACT	Row activating
	L	L	H	L	BA, A10	PRE/PALL	Nop
	L	L	L	H	X	REF/SELF	Auto refresh or Self-refresh <sup>(4)</sup>
	L	L	L	L	OC, BA1=L	MRS	Mode register set
Row Active	H	X	X	X	X	DESL	Nop
	L	H	H	H	X	NOP	Nop
	L	H	H	L	X	BST	Nop
	L	H	L	H	BA, CA, A10	READ/READA	Begin read <sup>(5)</sup>
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	Begin write <sup>(5)</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>(3)</sup>
	L	L	H	L	BA, A10	PRE/PALL	Precharge Precharge all banks <sup>(6)</sup>
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Read	H	X	X	X	X	DESL	Continue burst to end to Row active
	L	H	H	H	X	NOP	Continue burst to end Row Row active
	L	H	H	L	X	BST	Burst stop, Row active
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, begin new read <sup>(7)</sup>
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, begin write <sup>(7,8)</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>(3)</sup>
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst Precharging
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Write	H	X	X	X	X	DESL	Continue burst to end Write recovering
	L	H	H	H	X	NOP	Continue burst to end Write recovering
	L	H	H	L	X	BST	Burst stop, Row active
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, start read : Determine AP <sup>(7,8)</sup>
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, new write : Determine AP <sup>(7)</sup>
	L	L	H	H	BA, RA	RA ACT	ILLEGAL <sup>(3)</sup>
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst Precharging <sup>(9)</sup>
	L	L	L	H	X	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL

Note: H=V<sub>IH</sub>, L=V<sub>IL</sub> x= V<sub>IH</sub> or V<sub>IL</sub>, V = Valid Data, BA= Bank Address, CA+Column Address, RA=Row Address, OC= Op-Code

**FUNCTIONAL TRUTH TABLE Continued:**

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
Read with auto Precharging	H	x	x	x	x	DESL	Continue burst to end, Precharge
	L	H	H	H	x	NOP	Continue burst to end, Precharge
	L	H	H	L	x	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL <sup>(11)</sup>
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL <sup>(11)</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>(3)</sup>
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL <sup>(11)</sup>
	L	L	L	H	x	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Write with Auto Precharge	H	x	x	x	x	DESL	Continue burst to end, Write recovering with auto precharge
	L	H	H	H	x	NOP	Continue burst to end, Write recovering with auto precharge
	L	H	H	L	x	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL <sup>(11)</sup>
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL <sup>(11)</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>(3,11)</sup>
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL <sup>(3,11)</sup>
	L	L	L	H	x	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Precharging	H	x	x	x	x	DESL	Nop, Enter idle after tRP
	L	H	H	H	x	NOP	Nop, Enter idle after tRP
	L	H	H	L	x	BST	Nop, Enter idle after tRP
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL <sup>(3)</sup>
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL <sup>(3)</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>(3)</sup>
	L	L	H	L	BA, A10	PRE/PALL	Nop Enter idle after tRP
	L	L	L	H	x	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
Row Activating	H	x	x	x	x	DESL	Nop, Enter bank active after tRCD
	L	H	H	H	x	NOP	Nop, Enter bank active after tRCD
	L	H	H	L	x	BST	Nop, Enter bank active after tRCD
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL <sup>(3)</sup>
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL <sup>(3)</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>(3,9)</sup>
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL <sup>(3)</sup>
	L	L	L	H	x	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL

Note: H=V<sub>IH</sub>, L=V<sub>IL</sub> x= V<sub>IH</sub> or V<sub>IL</sub>, V = Valid Data, BA= Bank Address, CA+Column Address, RA=Row Address, OC= Op-Code

**FUNCTIONAL TRUTH TABLE Continued:**

Current State	CS	RAS	CAS	WE	Address	Command	Action
Write Recovering	H	x	x	x	x	DESL	Nop, Enter row active after tDPL
	L	H	H	H	x	NOP	Nop, Enter row active after tDPL
	L	H	H	L	x	BST	Nop, Enter row active after tDPL
	L	H	L	H	BA, CA, A10	READ/READA	Begin read <sup>(8)</sup>
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Begin new write
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>(3)</sup>
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL <sup>(3)</sup>
	L	L	L	H	x	REF/SELF	ILLEGAL
Write Recovering with Auto Precharge	L	L	L	L	OC, BA	MRS	ILLEGAL
	H	x	x	x	x	DESL	Nop, Enter precharge after tDPL
	L	H	H	H	x	NOP	Nop, Enter precharge after tDPL
	L	H	H	L	x	BST	Nop, Enter row active after tDPL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL <sup>(3,8,11)</sup>
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL <sup>(3,11)</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>(3,11)</sup>
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL <sup>(3,11)</sup>
Refresh	L	L	L	H	x	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
	H	x	x	x	x	DESL	Nop, Enter idle after tRC
	L	H	H	x	x	NOP/BST	Nop, Enter idle after tRC
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL
Mode Register Accessing	L	L	L	H	x	REF/SELF	ILLEGAL
	L	L	L	L	OC, BA	MRS	ILLEGAL
	H	x	x	x	x	DESL	Nop, Enter idle after 2 clocks
	L	H	H	H	x	NOP	Nop, Enter idle after 2 clocks
	L	H	H	L	x	BST	ILLEGAL
	L	H	L	x	BA, CA, A10	READ/WRITE	ILLEGAL
	L	L	x	x	BA, RA	ACT/PRE/PALL REF/MRS	ILLEGAL

Note: H=V<sub>IH</sub>, L=V<sub>IL</sub>, x= V<sub>IH</sub> or V<sub>IL</sub>, V = Valid Data, BA= Bank Address, CA+Column Address, RA=Row Address, OC= Op-Code

**Notes:**

- All entries assume that CKE is active (CKEn-1=CKEn=H).
- If both banks are idle, and CKE is inactive (Low), the device will enter Power Down mode. All input buffers except CKE will be disabled.
- Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
- If both banks are idle, and CKE is inactive (Low), the device will enter Self-Refresh mode. All input buffers except CKE will be disabled.
- Illegal if tRCD is not satisfied.
- Illegal if tRAS is not satisfied.
- Must satisfy burst interrupt condition.
- Must satisfy bus contention, bus turn around, and/or write recovery requirements.
- Must mask preceding data which don't satisfy tDPL.
- Illegal if tRRD is not satisfied.
- Illegal for single bank, but legal for other banks.



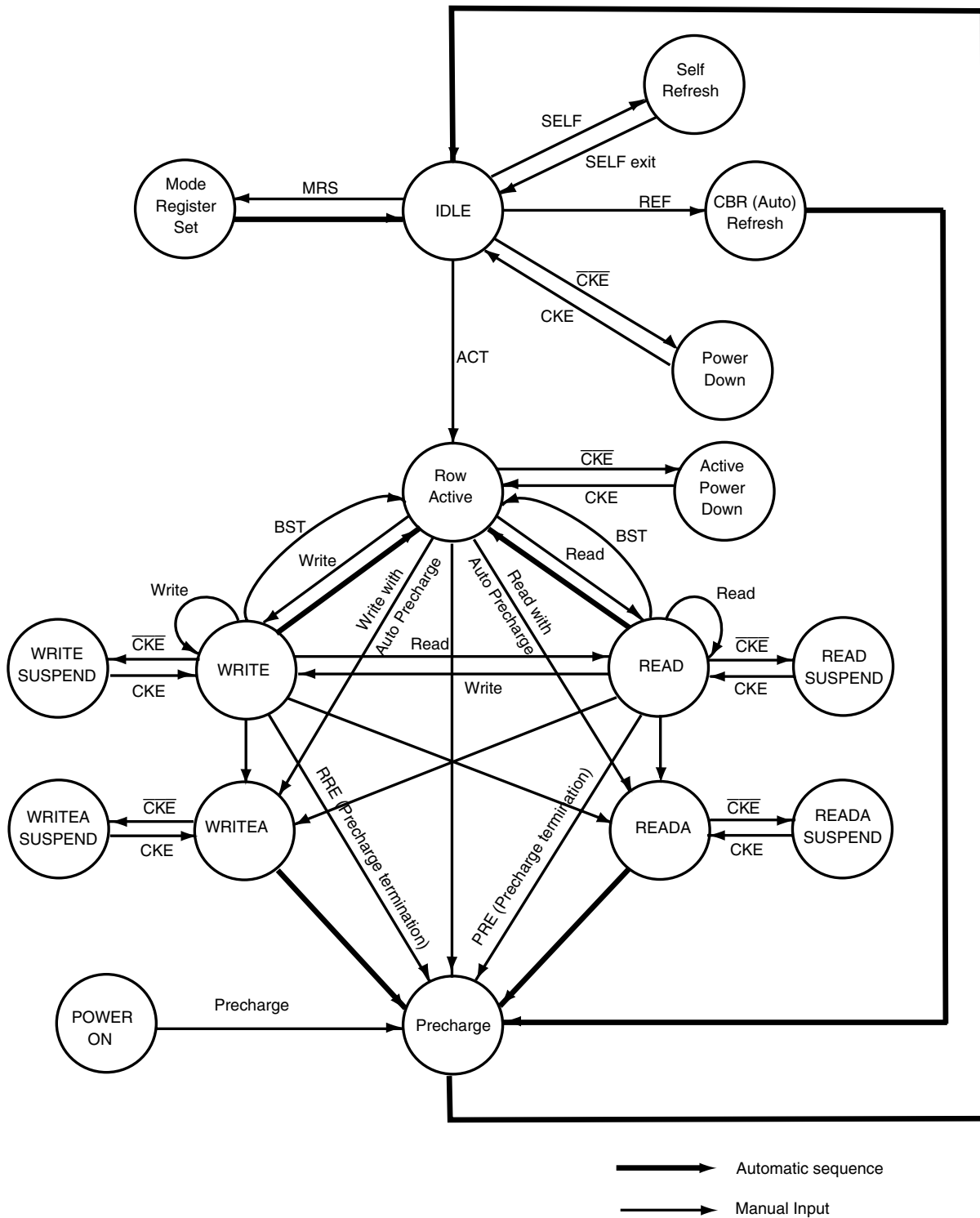
**CKE RELATED COMMAND TRUTH TABLE<sup>(1)</sup>**

Current State	Operation	CKE						Address
		n-1	n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	
Self-Refresh (S.R.)	INVALID, CLK (n - 1) would exit S.R.	H	X	X	X	X	X	X
	Self-Refresh Recovery <sup>(2)</sup>	L	H	H	X	X	X	X
	Self-Refresh Recovery <sup>(2)</sup>	L	H	L	H	H	X	X
	Illegal	L	H	L	H	L	X	X
	Illegal	L	H	L	L	X	X	X
	Maintain S.R.	L	L	X	X	X	X	X
Self-Refresh Recovery Idle After $t_{RC}$	Idle After $t_{RC}$	H	H	H	X	X	X	X
	Idle After $t_{RC}$	H	H	L	H	H	X	X
	Illegal	H	H	L	H	L	X	X
	Illegal	H	H	L	L	X	X	X
	Begin clock suspend next cycle <sup>(5)</sup>	H	L	H	X	X	X	X
	Begin clock suspend next cycle <sup>(5)</sup>	H	L	L	H	H	X	X
	Illegal	H	L	L	H	L	X	X
	Illegal	H	L	L	L	X	X	X
	Exit clock suspend next cycle <sup>(2)</sup>	L	H	X	X	X	X	X
	Maintain clock suspend	L	L	X	X	X	X	X
Power-Down (P.D.)	INVALID, CLK (n - 1) would exit P.D.	H	X	X	X	X	X	—
	EXIT P.D. --> Idle <sup>(2)</sup>	L	H	X	X	X	X	X
	Maintain power down mode	L	L	X	X	X	X	X
Both Banks Idle	Refer to operations in Operative Command Table	H	H	H	X	X	X	—
	Refer to operations in Operative Command Table	H	H	L	H	X	X	—
	Refer to operations in Operative Command Table	H	H	L	L	H	X	—
	Auto-Refresh	H	H	L	L	L	H	X
	Refer to operations in Operative Command Table	H	H	L	L	L	L	Op - Code
	Refer to operations in Operative Command Table	H	L	H	X	X	X	—
	Refer to operations in Operative Command Table	H	L	L	H	X	X	—
	Refer to operations in Operative Command Table	H	L	L	L	H	X	—
	Self-Refresh <sup>(3)</sup>	H	L	L	L	L	H	X
	Refer to operations in Operative Command Table	H	L	L	L	L	L	Op - Code
Power-Down <sup>(3)</sup>	L	X	X	X	X	X	X	
Any state other than listed above	Refer to operations in Operative Command Table	H	H	X	X	X	X	X
	Begin clock suspend next cycle <sup>(4)</sup>	H	L	X	X	X	X	X
	Exit clock suspend next cycle	L	H	X	X	X	X	X
	Maintain clock suspend	L	L	X	X	X	X	X

**Notes:**

1. H : High level, L : low level, X : High or low level (Don't care).
2. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
3. Power down and Self refresh can be entered only from the both banks idle state.
4. Must be legal command as defined in Operative Command Table.
5. Illegal if  $t_{XSR}$  is not satisfied.

STATE DIAGRAM



**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameters	Rating	Unit
V <sub>DD MAX</sub>	Maximum Supply Voltage	-0.5 to +4.6	V
V <sub>DDQ MAX</sub>	Maximum Supply Voltage for Output Buffer	-0.5 to +4.6	V
V <sub>IN</sub>	Input Voltage	-0.5 to V <sub>DD</sub> + 0.5	V
V <sub>OUT</sub>	Output Voltage	-1.0 to V <sub>DDQ</sub> + 0.5	V
P <sub>D MAX</sub>	Allowable Power Dissipation	1	W
I <sub>CS</sub>	Output Shorted Current	50	mA
T <sub>OPR</sub>	Operating Temperature	Com. 0 to +70 Ind. -40 to +85 A1 -40 to +85 A2 -40 to +105	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C

**Notes:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are referenced to V<sub>SS</sub>.

**DC RECOMMENDED OPERATING CONDITIONS**

(T<sub>A</sub> = 0°C to +70°C for Com. grade. T<sub>A</sub> = -40°C to +85°C for Ind. and A1 grade. T<sub>A</sub> = -40°C to +105°C for A2 grade.)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply Voltage	3.0	3.3	3.6	V
V <sub>DDQ</sub>	I/O Supply Voltage	3.0	3.3	3.6	V
V <sub>IH</sub> <sup>(1)</sup>	Input High Voltage	2.0	—	V <sub>DDQ</sub> + 0.3	V
V <sub>IL</sub> <sup>(2)</sup>	Input Low Voltage	-0.3	—	+0.8	V

**Note:**

1. V<sub>IH</sub> (max) = V<sub>DDQ</sub> + 1.2V (PULSE WIDTH ≤ 3NS).
2. V<sub>IL</sub> (min) = -1.2V (PULSE WIDTH ≤ 3NS).
3. All voltages are referenced to V<sub>SS</sub>.

**CAPACITANCE CHARACTERISTICS** (At T<sub>A</sub> = 0 to +25°C, V<sub>DD</sub> = V<sub>DDQ</sub> = 3.3 ± 0.3V)

Symbol	Parameter	Min.	Max.		Unit
			-6	-7/-75E	
C <sub>IN1</sub>	Input Capacitance: CLK	2.5	3.5	4.0	pF
C <sub>IN2</sub>	Input Capacitance: All other input pins	2.5	3.8	5.0	pF
C <sub>I/O</sub>	Data Input/Output Capacitance: I/Os	4.0	6.5	6.5	pF

**DC ELECTRICAL CHARACTERISTICS 1** (Recommended Operation Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	-6	-7	-75E	Unit
I <sub>DD1</sub> <sup>(1)</sup>	Operating Current	One bank active, CL = 3, BL = 1, t <sub>CLK</sub> = t <sub>CLK</sub> (min), t <sub>RC</sub> = t <sub>RC</sub> (min)	140	120	140	mA
I <sub>DD2P</sub>	Precharge Standby Current (In Power-Down Mode)	CKE ≤ V <sub>IL</sub> (MAX), t <sub>CK</sub> = 15ns	2	2	2	mA
I <sub>DD2PS</sub>	Precharge Standby Current (In Power-Down Mode)	CKE ≤ V <sub>IL</sub> (MAX), CLK ≤ V <sub>IL</sub> (MAX)	1	1	1	mA
I <sub>DD2N</sub> <sup>(2)</sup>	Precharge Standby Current (In Non Power-Down Mode)	$\overline{CS} \geq V_{DD} - 0.2V$ , CKE ≥ V <sub>IH</sub> (MIN) t <sub>CK</sub> = 15ns	25	25	25	mA
I <sub>DD2NS</sub>	Precharge Standby Current (In Non Power-Down Mode)	$\overline{CS} \geq V_{DD} - 0.2V$ , CKE ≥ V <sub>IH</sub> (MIN) or CKE ≤ V <sub>IL</sub> (MAX), All inputs stable	15	15	15	mA
I <sub>DD3N</sub> <sup>(2)</sup>	Active Standby Current (In Non Power-Down Mode)	$\overline{CS} \geq V_{DD} - 0.2V$ , CKE ≥ V <sub>IH</sub> (MIN) t <sub>CK</sub> = 15ns	30	30	30	mA
I <sub>DD3NS</sub>	Active Standby Current (In Non Power-Down Mode)	$\overline{CS} \geq V_{DD} - 0.2V$ , CKE ≥ V <sub>IH</sub> (MIN) or CKE ≤ V <sub>IL</sub> (MAX), All inputs stable	20	20	20	mA
I <sub>DD3P</sub>	Active Standby Current (Power-Down Mode)	CKE ≤ V <sub>IL</sub> (MAX), t <sub>CK</sub> = 15ns	2	2	2	mA
I <sub>DD3PS</sub>	Active Standby Current (Power-Down Mode)	CKE ≤ V <sub>IL</sub> (MAX), CLK ≤ V <sub>IL</sub> (MAX)	2	2	2	mA
I <sub>DD4</sub>	Operating Current	All banks active, BL = 4, CL = 3, t <sub>CK</sub> = t <sub>CK</sub> (min)	180	130	180	mA
I <sub>DD5</sub>	Auto-Refresh Current	t <sub>RC</sub> = t <sub>RC</sub> (min), t <sub>CLK</sub> = t <sub>CLK</sub> (min)	180	160	180	mA
I <sub>DD6</sub>	Self-Refresh Current	CKE ≤ 0.2V	2	2	2	mA

**Notes:**

- I<sub>DD</sub> (MAX) is specified at the output open condition.
- Input signals are changed one time during 30ns.

**DC ELECTRICAL CHARACTERISTICS 2** (Recommended Operation Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	Min	Max	Unit
I <sub>IL</sub>	Input Leakage Current	0V ≤ V <sub>in</sub> ≤ V <sub>DD</sub> , with pins other than the tested pin at 0V	-10	10	μA
I <sub>OL</sub>	Output Leakage Current	Output is disabled, 0V ≤ V <sub>out</sub> ≤ V <sub>DD</sub> ,	-10	10	μA
V <sub>OH</sub>	Output High Voltage Level	I <sub>OH</sub> = -2mA	2.4	—	V
V <sub>OL</sub>	Output Low Voltage Level	I <sub>OL</sub> = 2mA	—	0.4	V





# IS42S32400E, IS45S32400E

## AC ELECTRICAL CHARACTERISTICS <sup>(1,2,3)</sup>

Symbol	Parameter		-6		-7		-75E		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
tCK3	Clock Cycle Time	CAS Latency = 3	6	—	7	—	—	—	ns
tCK2		CAS Latency = 2	10	—	10	—	7.5	—	ns
tAC3	Access Time From CLK	CAS Latency = 3	—	5.4	—	5.4	—	—	ns
tAC2		CAS Latency = 2	—	6.5	—	6.5	—	5.5	ns
tCH	CLK HIGH Level Width		2.5	—	2.5	—	2.5	—	ns
tCL	CLK LOW Level Width		2.5	—	2.5	—	2.5	—	ns
tOH3	Output Data Hold Time	CAS Latency = 3	2.7	—	2.7	—	2.7	—	ns
tOH2		CAS Latency = 2	2.7	—	2.7	—	2.7	—	ns
tLZ	Output LOW Impedance Time		0	—	0	—	0	—	ns
tHZ3	Output HIGH Impedance Time	CAS Latency = 3	2.7	5.4	2.7	5.4	—	—	ns
tHZ2		CAS Latency = 2	2.7	6.5	2.7	6.5	2.7	5.5	ns
tDS	Input Data Setup Time <sup>(2)</sup>		1.5	—	1.5	—	1.5	—	ns
tDH	Input Data Hold Time <sup>(2)</sup>		0.8	—	0.8	—	0.8	—	ns
tAS	Address Setup Time <sup>(2)</sup>		1.5	—	1.5	—	1.5	—	ns
tAH	Address Hold Time <sup>(2)</sup>		0.8	—	0.8	—	0.8	—	ns
tCKS	CKE Setup Time <sup>(2)</sup>		1.5	—	1.5	—	1.5	—	ns
tCKH	CKE Hold Time <sup>(2)</sup>		0.8	—	0.8	—	0.8	—	ns
tCMS	Command Setup Time (CS, RAS, CAS, WE, DQM) <sup>(2)</sup>		1.5	—	1.5	—	1.5	—	ns
tCMH	Command Hold Time (CS, RAS, CAS, WE, DQM) <sup>(2)</sup>		0.8	—	0.8	—	0.8	—	ns
tRC	Command Period (REF to REF / ACT to ACT)		60	—	67.5	—	67.5	—	ns
tRAS	Command Period (ACT to PRE)		42	100K	45	100K	45	100K	ns
tRP	Command Period (PRE to ACT)		18	—	20	—	15	—	ns
tRCD	Active Command To Read / Write Command Delay Time		18	—	20	—	15	—	ns
tRRD	Command Period (ACT [0] to ACT[1])		12	—	14	—	15	—	ns
tDPL	Input Data To Precharge Command Delay time		12	—	14	—	15	—	ns
tDAL	Input Data To Active / Refresh Command Delay time (During Auto-Precharge)		30	—	35	—	30	—	ns
tMRD	Mode Register Program Time		12	—	14	—	15	—	ns
tDDE	Power Down Exit Setup Time		6	—	7	—	7.5	—	ns
tXSR	Exit Self-Refresh to Active Time <sup>(4)</sup>		70	—	70	—	70	—	ns
t <sub>r</sub>	Transition Time		0.3	1.2	0.3	1.2	0.3	1.2	ns
tREF	Refresh Cycle Time (4096)								
		T <sub>A</sub> ≤ 70°C Com., Ind., A1, A2	—	64	—	64	—	64	ms
		T <sub>A</sub> ≤ 85°C Ind., A1, A2	—	64	—	64	—	64	ms
		T <sub>A</sub> > 85°C A2	—	16	—	16	—	—	ms

### Notes:

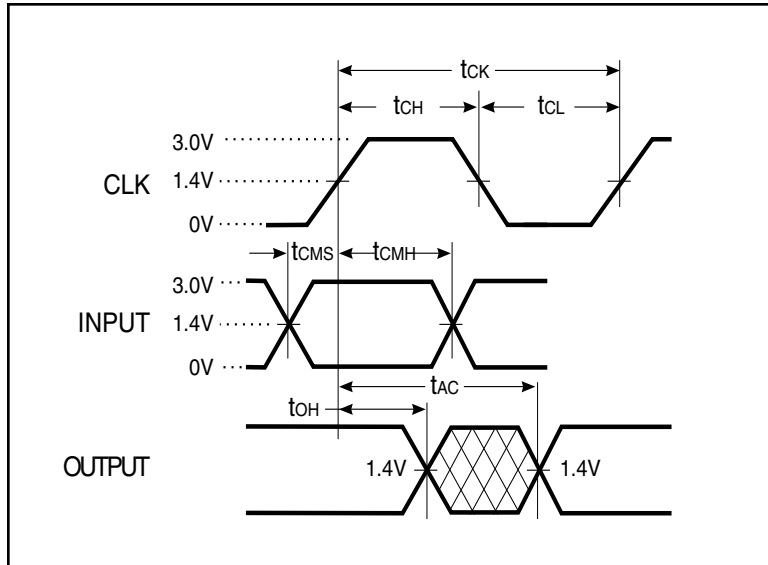
1. The power-on sequence must be executed before starting memory operation.
2. Measured with t<sub>r</sub> = 1 ns. If clock rising time is longer than 1ns, (t<sub>r</sub> / 2 - 0.5) ns should be added to the parameter.
3. The reference level is 1.4V when measuring input signal timing. Rise and fall times are measured between V<sub>IH</sub>(min.) and V<sub>IL</sub>(max).
4. Self-Refresh Mode is not supported for A2 grade with T<sub>A</sub> > 85°C.

**OPERATING FREQUENCY / LATENCY RELATIONSHIPS**

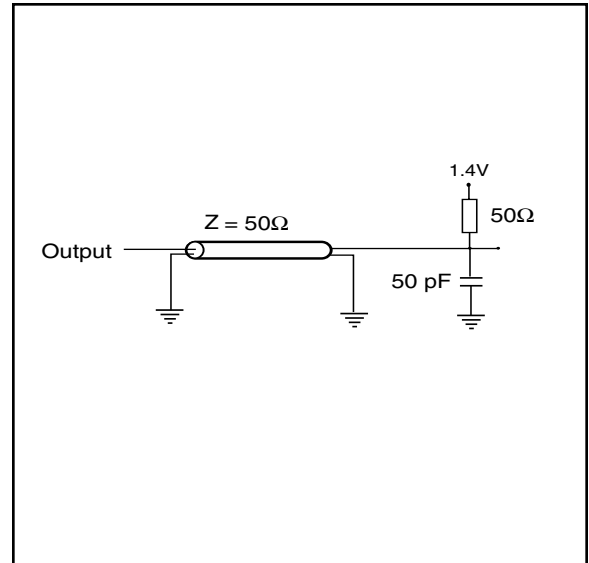
SYMBOL	PARAMETER	-6	-7	-75E	UNITS
—	Clock Cycle Time	6	7	7.5	ns
—	Operating Frequency	166	143	133	MHz
t <sub>CAC</sub>	$\overline{\text{CAS}}$ Latency	3	3	2	cycle
t <sub>RC</sub>	Active Command To Read/Write Command Delay Time	3	3	2	cycle
t <sub>RAC</sub>	$\overline{\text{RAS}}$ Latency (t <sub>RC</sub> + t <sub>CAC</sub> )	$\overline{\text{CAS}}$ Latency = 3 $\overline{\text{CAS}}$ Latency = 2	6 —	— 4	cycle
t <sub>RC</sub>	Command Period (REF to REF / ACT to ACT)	10	10	9	cycle
t <sub>RA</sub>	Command Period (ACT to PRE)	7	7	6	cycle
t <sub>RP</sub>	Command Period (PRE to ACT)	3	3	2	cycle
t <sub>RRD</sub>	Command Period (ACT[0] to ACT [1])	2	2	2	cycle
t <sub>CCD</sub>	Column Command Delay Time (READ, READA, WRIT, WRITA)	1	1	1	cycle
t <sub>DPL</sub>	Input Data To Precharge Command Delay Time	2	2	2	cycle
t <sub>DAL</sub>	Input Data To Active/Refresh Command Delay Time (During Auto-Precharge)	5	5	4	cycle
t <sub>RBD</sub>	Burst Stop Command To Output in HIGH-Z Delay Time (Read)	$\overline{\text{CAS}}$ Latency = 3 $\overline{\text{CAS}}$ Latency = 2	3 —	— 3	cycle
t <sub>WBD</sub>	Burst Stop Command To Input in Invalid Delay Time (Write)	0	0	0	cycle
t <sub>RQL</sub>	Precharge Command To Output in HIGH-Z Delay Time (Read)	$\overline{\text{CAS}}$ Latency = 3 $\overline{\text{CAS}}$ Latency = 2	3 —	— 2	cycle
t <sub>WDL</sub>	Precharge Command To Input in Invalid Delay Time (Write)	0	0	0	cycle
t <sub>PQL</sub>	Last Output To Auto-Precharge Start Time (Read)	$\overline{\text{CAS}}$ Latency = 3 $\overline{\text{CAS}}$ Latency = 2	-2 —	— -1	cycle
t <sub>QMD</sub>	DQM To Output Delay Time (Read)	2	2	2	cycle
t <sub>DMD</sub>	DQM To Input Delay Time (Write)	0	0	0	cycle
t <sub>M</sub>	Mode Register Set To Command Delay Time	2	2	2	cycle

**AC TEST CONDITIONS**

**Input Load**



**Output Load**



**AC TEST CONDITIONS**

Parameter	Rating
AC Input Levels	0V to 3.0V
Input Rise and Fall Times	1 ns
Input Timing Reference Level	1.4V
Output Timing Measurement Reference Level	1.4V

## FUNCTIONAL DESCRIPTION

The 128Mb SDRAMs are quad-bank DRAMs which operate at 3.3V and include a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 33,554,432-bit banks is organized as 4,096 rows by 256 columns by 32 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0-A11 select the row). The address bits A0-A7 registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

## Initialization

SDRAMs must be powered up and initialized in a predefined manner.

The 128M SDRAM is initialized after the power is applied to V<sub>DD</sub> and V<sub>DDQ</sub> (simultaneously) and the clock is stable with DQM High and CKE High.

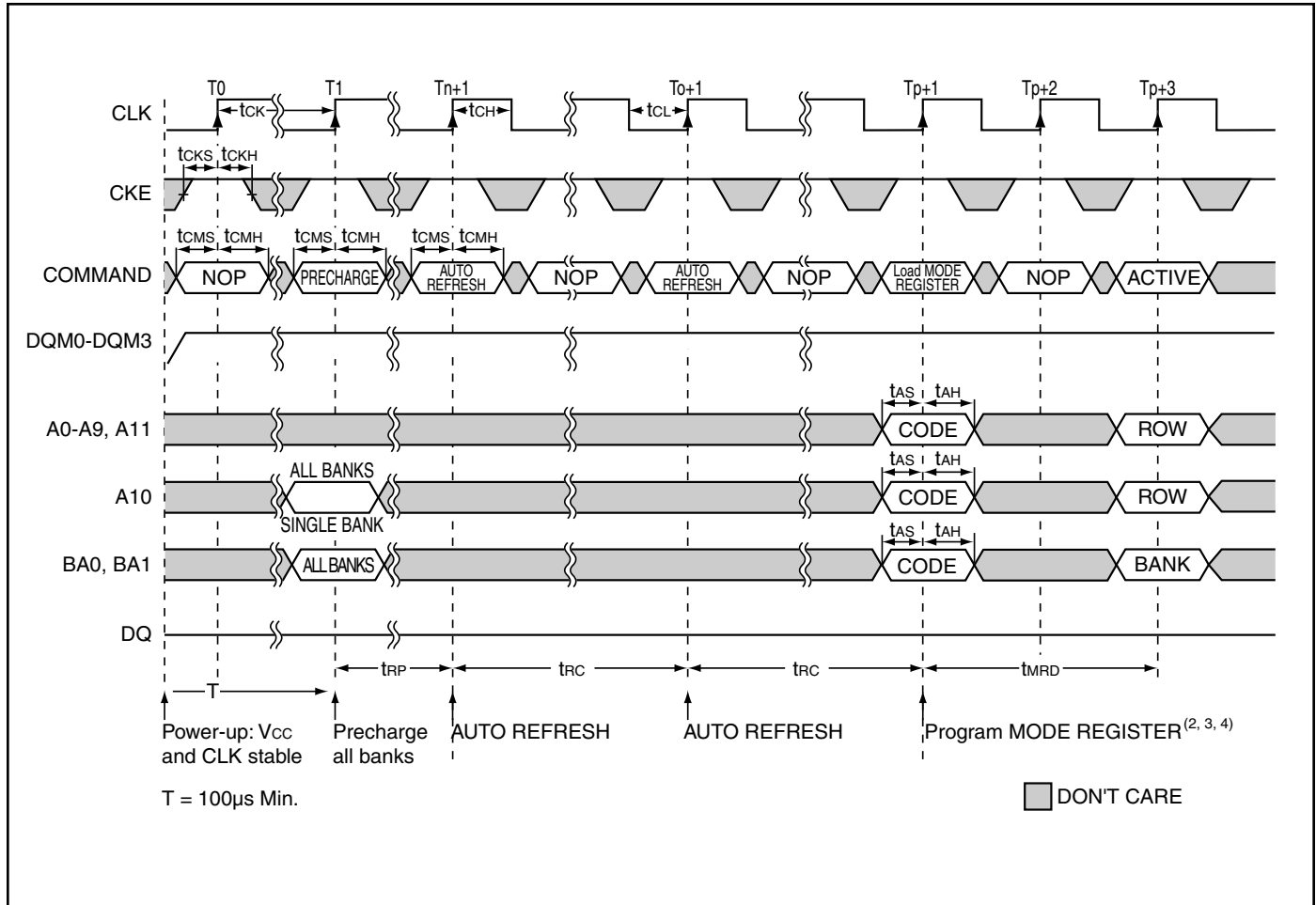
A 100 $\mu$ s delay is required prior to issuing any command other than a COMMAND INHIBIT or a NOP. The COMMAND INHIBIT or NOP may be applied during the 100 $\mu$ s period and should continue at least through the end of the period.

With at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied once the 100 $\mu$ s delay has been satisfied. All banks must be precharged. This will leave all banks in an idle state after which at least two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is then ready for mode register programming.

The mode register should be loaded prior to applying any operational command because it will power up in an unknown state.



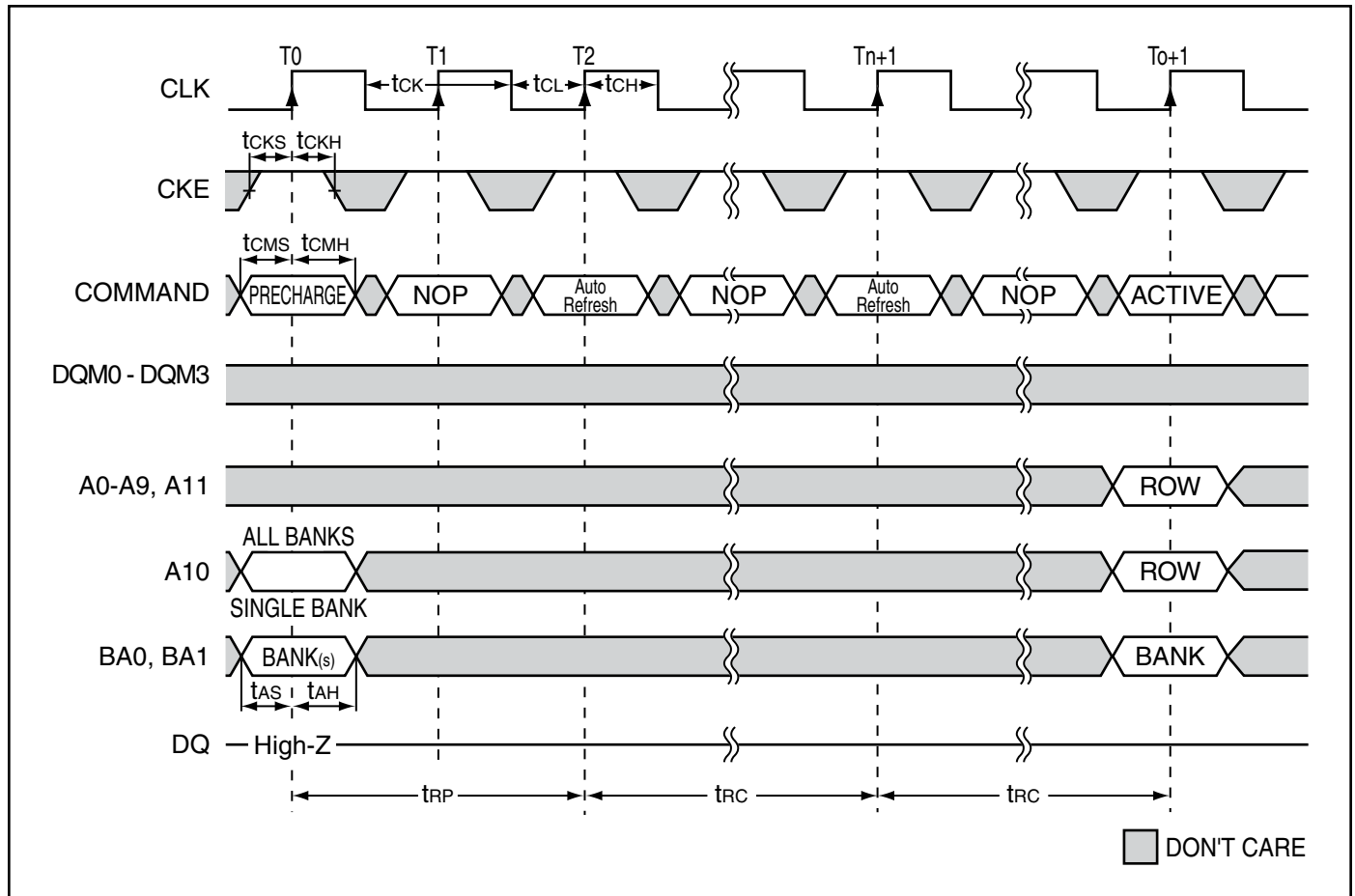
**INITIALIZE AND LOAD MODE REGISTER<sup>(1)</sup>**



**Notes:**

1. If CS is High at clock High time, all commands applied are NOP.
2. The Mode register may be loaded prior to the Auto-Refresh cycles if desired.
3. JEDEC and PC100 specify three clocks.
4. Outputs are guaranteed High-Z after the command is issued.

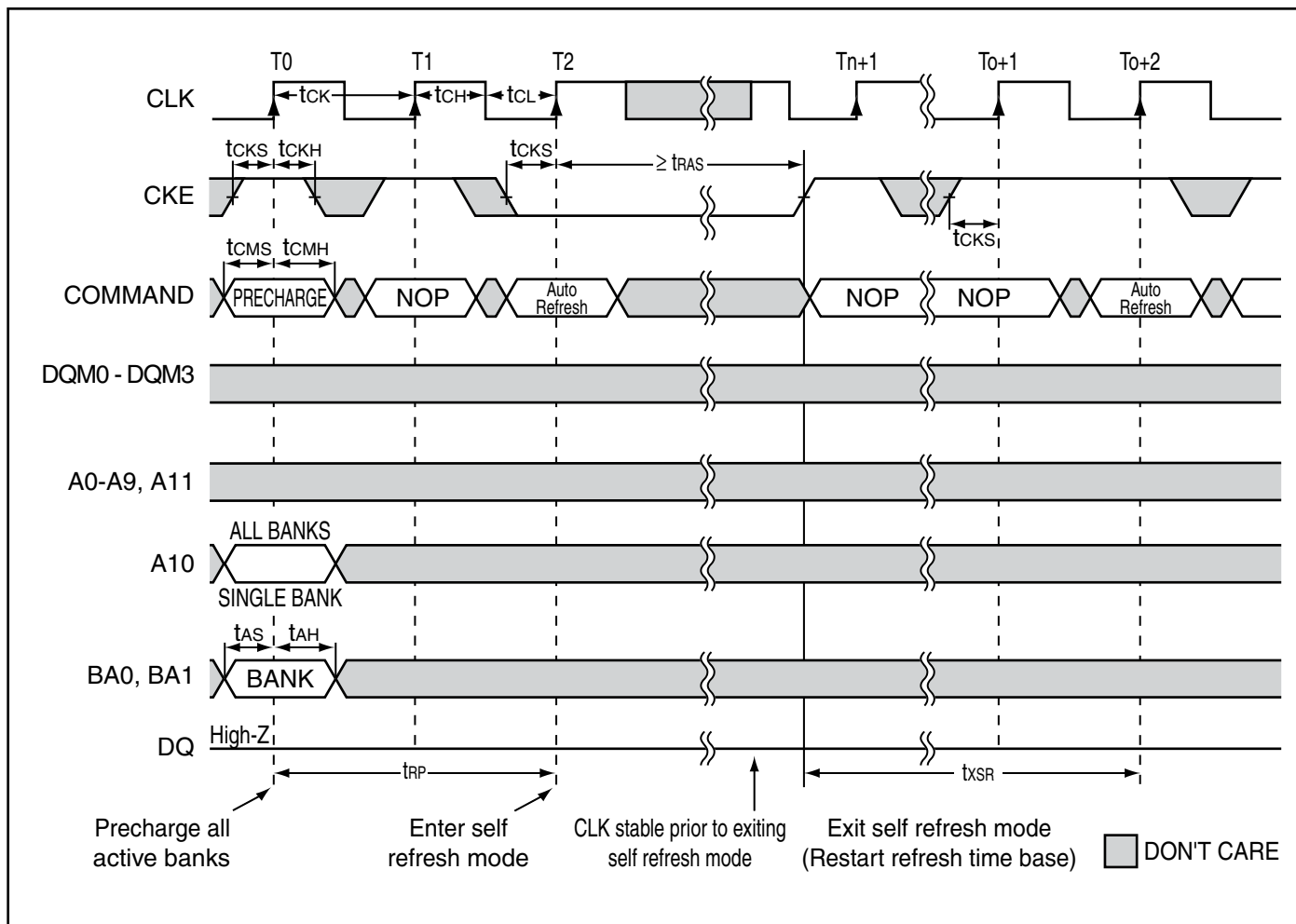
**AUTO-REFRESH CYCLE**



**Notes:**

1.  $\overline{CAS}$  latency = 2, 3

**SELF-REFRESH CYCLE**



**Note:**  
 1. Self-Refresh Mode is not supported for A2 grade with  $T_A > 85^\circ\text{C}$ .

## REGISTER DEFINITION

### Mode Register

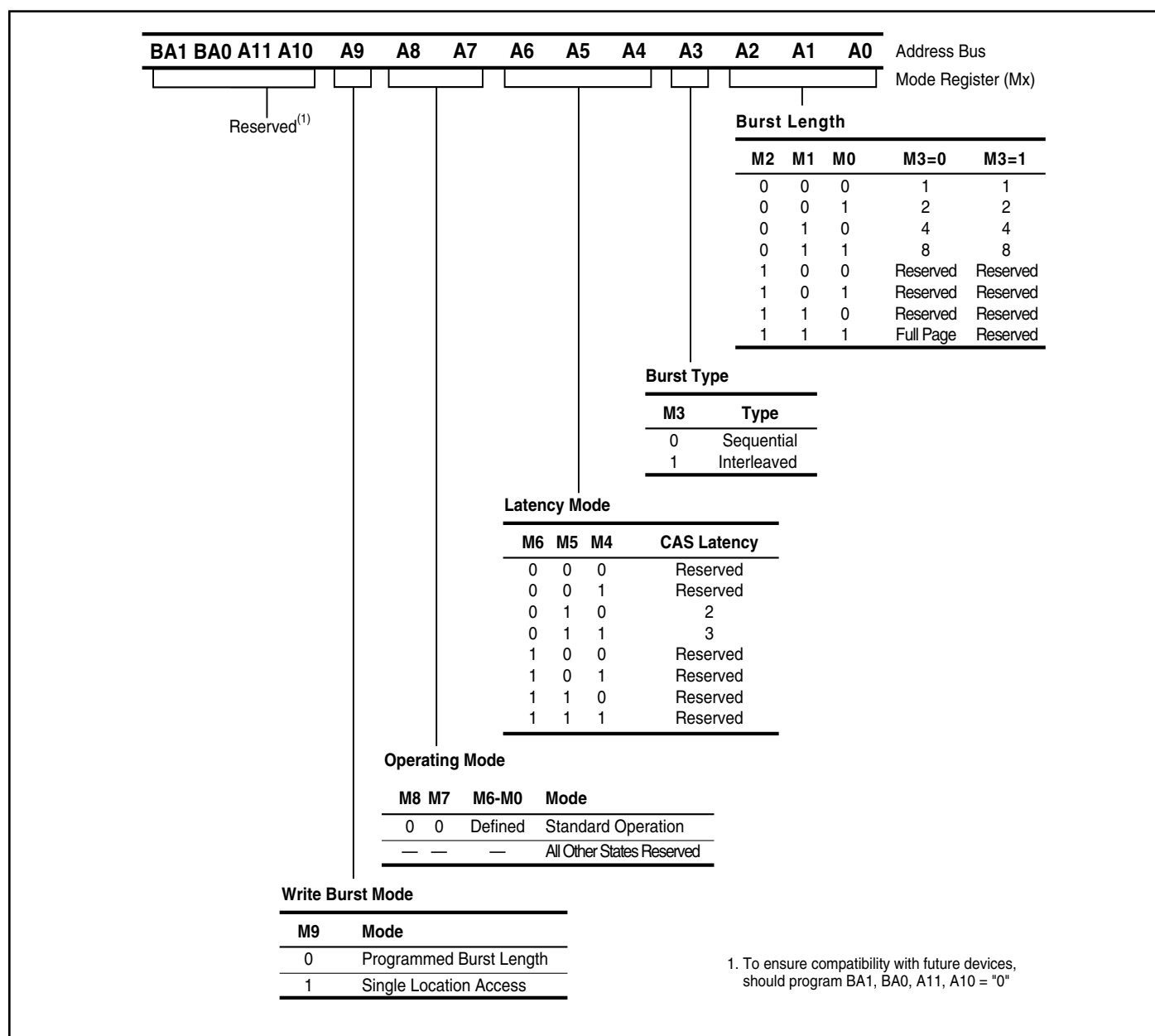
The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in MODE REGISTER DEFINITION.

The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0-M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4- M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the WRITE burst mode, and M10 and M11 are reserved for future use.

The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

### MODE REGISTER DEFINITION





## BURST LENGTH

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in MODE REGISTER DEFINITION. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4 or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, mean-

ing that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A7 (x32) when the burst length is set to two; by A2-A7 (x32) when the burst length is set to four; and by A3-A7 (x32) when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

### Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in BURST DEFINITION table.

## BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
	<b>A 0</b>				
2	0			0-1	0-1
	1			1-0	1-0
	<b>A 1</b>		<b>A 0</b>		
4	0	0		0-1-2-3	0-1-2-3
	0	0	1	1-2-3-0	1-0-3-2
	1	0	0	2-3-0-1	2-3-0-1
	1	1	1	3-0-1-2	3-2-1-0
	<b>A 2</b>		<b>A 1</b>		
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0-A7 (location 0-y)			Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... ...Cn - 1, Cn...	Not Supported

### CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge  $n$ , and the latency is  $m$  clocks, the data will be available by clock edge  $n + m$ . The DQs will start driving as a result of the clock edge one cycle earlier ( $n + m - 1$ ), and provided that the relevant access times are met, the data will be valid by clock edge  $n + m$ . For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at  $T_0$  and the latency is programmed to two clocks, the DQs will start driving after  $T_1$  and the data will be valid by  $T_2$ , as shown in CAS Latency diagrams. The Allowable Operating Frequency table indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

### Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

### Write Burst Mode

When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

### CAS Latency

#### Allowable Operating Frequency (MHz)

Speed	CAS Latency = 2	CAS Latency = 3
-6	100	166
-7	100	143
-75E	133	-

### CAS LATENCY

