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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



## 512K x36 and 1024K x18 18Mb, SYNCHRONOUS FLOW-THROUGH SRAM

OCTOBER 2015

### FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Burst sequence control using MODE input
- Three chip enable option for simple depth expansion and address pipelining
- Common data inputs and data outputs
- Auto Power-down during deselect
- Single cycle deselect
- Snooze MODE for reduced-power standby
- JEDEC 100-pin QFP, 165-ball BGA and 119-ball BGA packages
- Power supply:  
 LF:  $V_{DD}$  3.3V ( $\pm 5\%$ ),  $V_{DDQ}$  3.3V/2.5V ( $\pm 5\%$ )  
 VF:  $V_{DD}$  2.5V ( $\pm 5\%$ ),  $V_{DDQ}$  2.5V ( $\pm 5\%$ )  
 VVF:  $V_{DD}$  1.8V ( $\pm 5\%$ ),  $V_{DDQ}$  1.8V ( $\pm 5\%$ )
- JTAG Boundary Scan for BGA packages
- Commercial, Industrial and Automotive temperature support
- Lead-free available
- For leaded options, please contact ISSI

### FAST ACCESS TIME

Symbol	Parameter	-6.5	-7.5	Units
$t_{kQ}$	Clock Access Time	6.5	7.5	ns
$t_{kC}$	Cycle time	7.5	8.5	ns
	Frequency	133	117	MHz

### DESCRIPTION

The 18Mb product family features high-speed, low-power synchronous static RAMs designed to provide burstable, high-performance memory for communication and networking applications. The IS61(64)LF/VF/VVF51236(32)B organized as 524,288 words by 36(32)bits. The IS61(64)LF/VF/VVF102418B are organized as 1,048,576 words by 18 bits. Fabricated with ISSI's advanced CMOS technology, the device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. The byte write operation is performed by using the byte write enable (/BWE) input combined with one or more individual byte write signals (/BWx). In addition, Global Write (/GW) is available for writing all bytes at one time, regardless of the byte write controls.

Bursts can be initiated with either /ADSP (Address Status Processor) or /ADSC (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the /ADV (burst address advance) input pin.

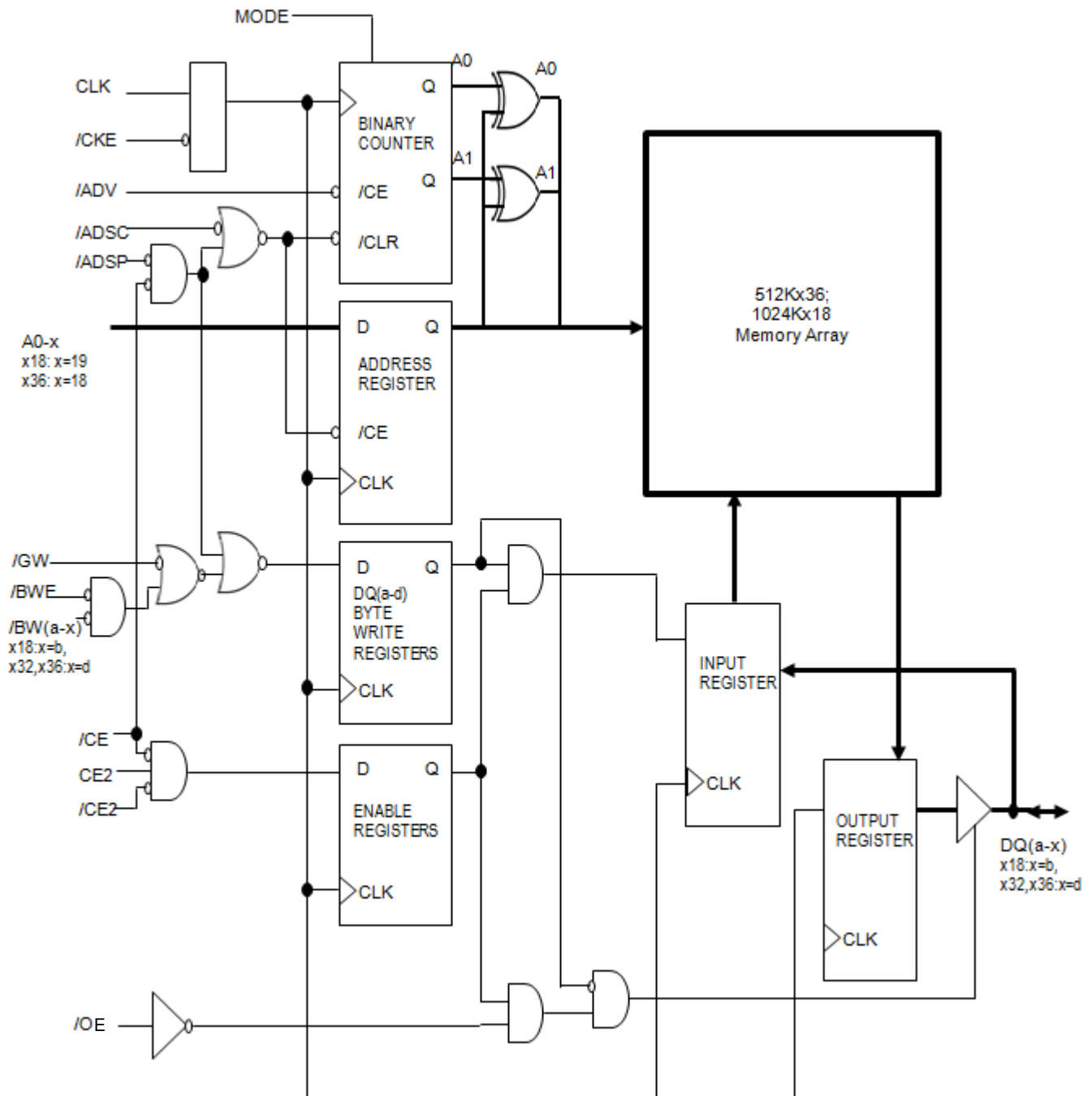
The mode pin is used to select the burst sequence order. Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating

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- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

## BLOCK DIAGRAM



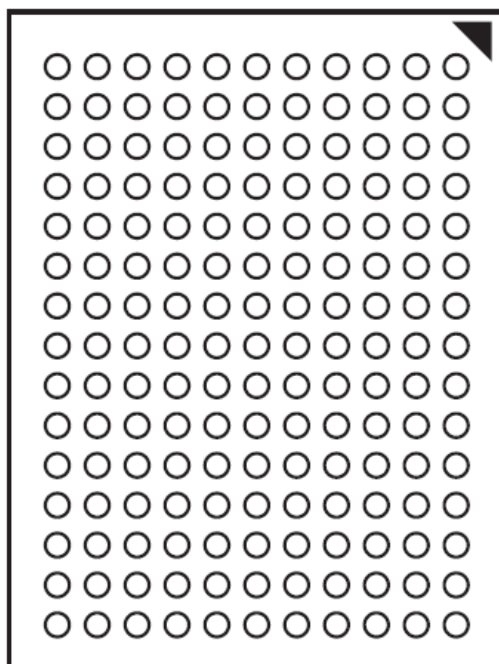


## PIN CONFIGURATION

### 512K x 36, 165-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	/CE	/BWc	/BWb	/CE2	/BWE	/ADSC	/ADV	A	NC
B	NC	A	CE2	/BWd	/BWa	CLK	/GW	/OE	/ADSP	A	NC
C	DQPc	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	DQPb
D	DQc	DQc	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQb	DQb
E	DQc	DQc	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQb	DQb
F	DQc	DQc	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQb	DQb
G	DQc	DQc	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQb	DQb
H	NC	V <sub>SS</sub>	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	NC	ZZ
J	DQd	DQd	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQa	DQa
K	DQd	DQd	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQa	DQa
L	DQd	DQd	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQa	DQa
M	DQd	DQd	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQa	DQa
N	DQPd	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	NC	A	NC	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	DQPa
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	A
R	MODE	NC	A	A	TMS	A0*	TCK	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View  
 165-Ball, 13 mm x 15mm BGA

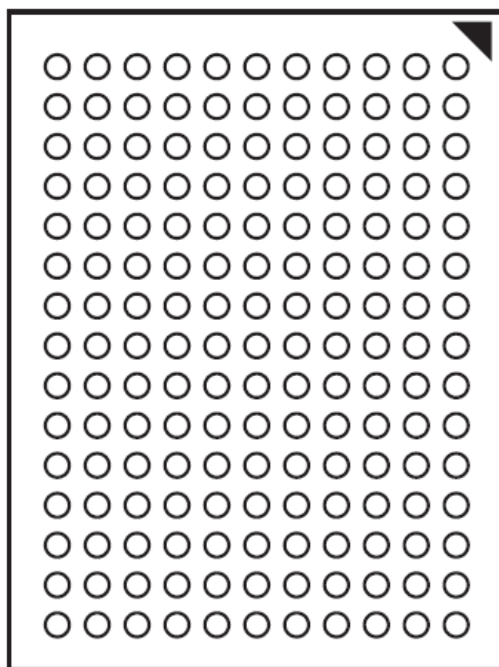
### PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
A0,A1	Synchronous Burst Address Inputs
A	Address Inputs
/ADV	Synchronous Burst Address Advance
/ADSP	Address Status Processor
/ADSC	Address Status Controller
MODE	Burst Sequence Selection
/CE,CE2,/CE2	Synchronous Chip Enable
/BWE	Byte Write Enable
/BWx (x=a-d)	Synchronous Byte Write Inputs
/GW	Global Write Enable
/OE	Output Enable
DQx	Data Inputs/Outputs
DQP <sub>x</sub>	Parity Data I/O
TCK,TDI, TDO,TMS	JTAG Pins
ZZ	Power Sleep Mode
NC	No Connect
V <sub>DD</sub>	Power Supply
V <sub>DDQ</sub>	I/O Power Supply
V <sub>SS</sub>	Ground

512K x 32, 165-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	/CE	/BWc	/BWb	/CE2	/BWE	/ADSC	/ADV	A	NC
B	NC	A	CE2	/BWd	/BWa	CLK	/GW	/OE	/ADSP	A	NC
C	NC	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	NC
D	DQc	DQc	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQb	DQb
E	DQc	DQc	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQb	DQb
F	DQc	DQc	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQb	DQb
G	DQc	DQc	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQb	DQb
H	NC	V <sub>SS</sub>	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	NC	ZZ
J	DQd	DQd	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQa	DQa
K	DQd	DQd	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQa	DQa
L	DQd	DQd	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQa	DQa
M	DQd	DQd	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQa	DQa
N	NC	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	NC	A	NC	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	NC
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	A
R	MODE	NC	A	A	TMS	A0*	TCK	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View  
 165-Ball, 13 mm x 15mm BGA

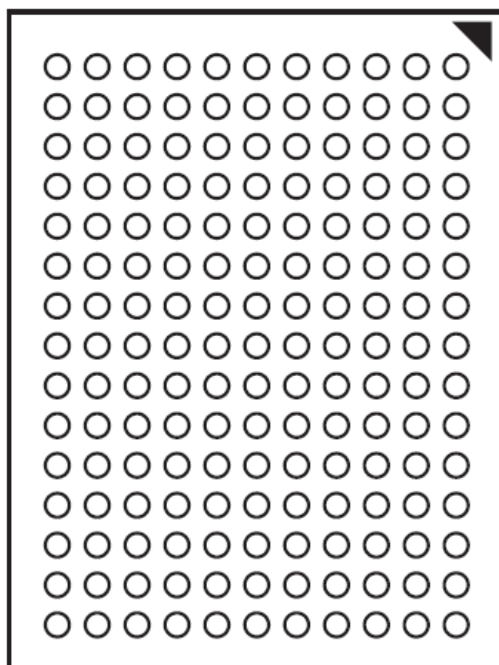
PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
A0,A1	Synchronous Burst Address Inputs
A	Address Inputs
/ADV	Synchronous Burst Address Advance
/ADSP	Address Status Processor
/ADSC	Address Status Controller
MODE	Burst Sequence Selection
/CE,CE2,/CE2	Synchronous Chip Enable
/BWE	Byte Write Enable
/BWx (x=a-d)	Synchronous Byte Write Inputs
/GW	Global Write Enable
/OE	Output Enable
DQx	Data Inputs/Outputs
DQP <sub>x</sub>	Parity Data I/O
TCK,TDI, TDO,TMS	JTAG Pins
ZZ	Power Sleep Mode
NC	No Connect
V <sub>DD</sub>	Power Supply
V <sub>DDQ</sub>	I/O Power Supply
V <sub>SS</sub>	Ground

1024K x 18, 165-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	/CE	/BWb	NC	/CE2	/BWE	/ADSC	/ADV	A	A
B	NC	A	CE2	NC	/BWa	CLK	/GW	/OE	/ADSP	A	NC
C	NC	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	DQP <sub>a</sub>
D	NC	DQb	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>a</sub>
E	NC	DQb	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>a</sub>
F	NC	DQb	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>a</sub>
G	NC	DQb	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>a</sub>
H	NC	V <sub>SS</sub>	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	NC	ZZ
J	DQb	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>a</sub>	NC
K	DQb	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>a</sub>	NC
L	DQb	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>a</sub>	NC
M	DQb	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>a</sub>	NC
N	DQP <sub>b</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	NC	A	NC	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	NC
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	A
R	MODE	NC	A	A	TMS	A0*	TCK	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View  
 165-Ball, 13 mm x 15mm BGA

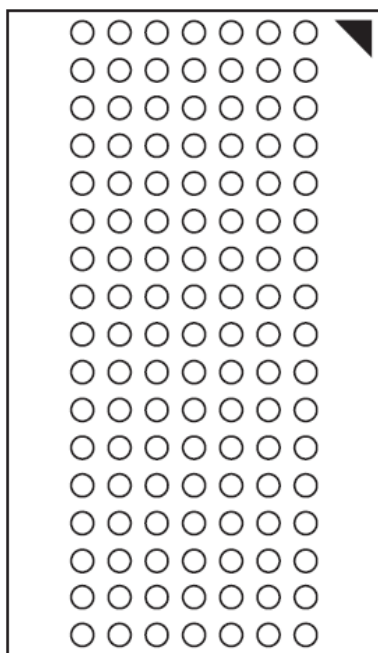
PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
A0,A1	Synchronous Burst Address Inputs
A	Address Inputs
/ADV	Synchronous Burst Address Advance
/ADSP	Address Status Processor
/ADSC	Address Status Controller
MODE	Burst Sequence Selection
/CE,CE2,/CE2	Synchronous Chip Enable
/BWE	Byte Write Enable
/BW <sub>x</sub> (x=a-b)	Synchronous Byte Write Inputs
/GW	Global Write Enable
/OE	Output Enable
DQ <sub>x</sub>	Data Inputs/Outputs
DQP <sub>x</sub>	Parity Data I/O
TCK,TDI, TDO,TMS	JTAG Pins
ZZ	Power Sleep Mode
NC	No Connect
V <sub>DD</sub>	Power Supply
V <sub>DDQ</sub>	I/O Power Supply
V <sub>SS</sub>	Ground

512K x 36, 119-Ball BGA (Top View)

	1	2	3	4	5	6	7
A	V <sub>DDQ</sub>	A	A	/ADSP	A	A	V <sub>DDQ</sub>
B	NC	A	A	/ADSC	A	A	NC
C	NC	A	A	V <sub>DD</sub>	A	A	NC
D	DQc	DQPc	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQPb	DQb
E	DQc	DQc	V <sub>SS</sub>	/CE	V <sub>SS</sub>	DQb	DQb
F	V <sub>DDQ</sub>	DQc	V <sub>SS</sub>	/OE	V <sub>SS</sub>	DQb	V <sub>DDQ</sub>
G	DQc	DQc	/BWc	/ADV	/BWb	DQb	DQb
H	DQc	DQc	V <sub>SS</sub>	/GW	V <sub>SS</sub>	DQb	DQb
J	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
K	DQd	DQd	V <sub>SS</sub>	CLK	V <sub>SS</sub>	DQa	DQa
L	DQd	DQd	/BWd	NC	/BWA	DQa	DQa
M	V <sub>DDQ</sub>	DQd	V <sub>SS</sub>	/BWE	V <sub>SS</sub>	DQa	V <sub>DDQ</sub>
N	DQd	DQd	V <sub>SS</sub>	A1*	V <sub>SS</sub>	DQa	DQa
P	DQd	DQPd	V <sub>SS</sub>	A0*	V <sub>SS</sub>	DQPa	DQa
R	NC	A	MODE	V <sub>DD</sub>	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View  
 119-Ball, 14 mm x 22 mm BGA

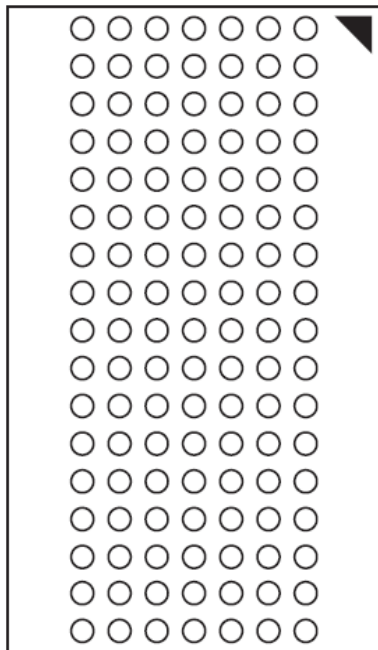
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Symbol	Pin Name
CLK	Synchronous Clock
A0,A1	Synchronous Burst Address Inputs
A	Address Inputs
/ADV	Synchronous Burst Address Advance
/ADSP	Address Status Processor
/ADSC	Address Status Controller
MODE	Burst Sequence Selection
/CE	Synchronous Chip Enable
/BWE	Byte Write Enable
/BWx (x=a-d)	Synchronous Byte Write Inputs
/GW	Global Write Enable
/OE	Output Enable
DQx	Data Inputs/Outputs
DQP <sub>x</sub>	Parity Data I/O
TCK,TDI, TDO,TMS	JTAG Pins
ZZ	Power Sleep Mode
NC	No Connect
V <sub>DD</sub>	Power Supply
V <sub>DDQ</sub>	I/O Power Supply
V <sub>SS</sub>	Ground

512K x 32, 119-Ball BGA (Top View)

	1	2	3	4	5	6	7
A	V <sub>DDQ</sub>	A	A	/ADSP	A	A	V <sub>DDQ</sub>
B	NC	A	A	/ADSC	A	A	NC
C	NC	A	A	V <sub>DD</sub>	A	A	NC
D	DQc	NC	V <sub>SS</sub>	NC	V <sub>SS</sub>	NC	DQb
E	DQc	DQc	V <sub>SS</sub>	/CE	V <sub>SS</sub>	DQb	DQb
F	V <sub>DDQ</sub>	DQc	V <sub>SS</sub>	/OE	V <sub>SS</sub>	DQb	V <sub>DDQ</sub>
G	DQc	DQc	/BWc	/ADV	/BWb	DQb	DQb
H	DQc	DQc	V <sub>SS</sub>	/GW	V <sub>SS</sub>	DQb	DQb
J	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
K	DQd	DQd	V <sub>SS</sub>	CLK	V <sub>SS</sub>	DQa	DQa
L	DQd	DQd	/BWd	NC	/BWa	DQa	DQa
M	V <sub>DDQ</sub>	DQd	V <sub>SS</sub>	/BWE	V <sub>SS</sub>	DQa	V <sub>DDQ</sub>
N	DQd	DQd	V <sub>SS</sub>	A1*	V <sub>SS</sub>	DQa	DQa
P	DQd	NC	V <sub>SS</sub>	A0*	V <sub>SS</sub>	NC	DQa
R	NC	A	MODE	V <sub>DD</sub>	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View  
 119-Ball, 14 mm x 22 mm BGA

PIN DESCRIPTIONS

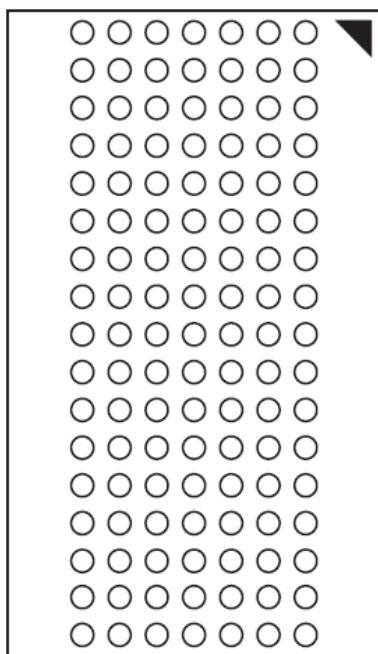
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CLK	Synchronous Clock
A0,A1	Synchronous Burst Address Inputs
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/ADV	Synchronous Burst Address Advance
/ADSP	Address Status Processor
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MODE	Burst Sequence Selection
/CE	Synchronous Chip Enable
/BWE	Byte Write Enable
/BWx (x=a-d)	Synchronous Byte Write Inputs
/GW	Global Write Enable
/OE	Output Enable
DQx	Data Inputs/Outputs
TCK,TDI, TDO,TMS	JTAG Pins
ZZ	Power Sleep Mode
NC	No Connect
V <sub>DD</sub>	Power Supply
V <sub>DDQ</sub>	I/O Power Supply
V <sub>SS</sub>	Ground



1024K x 18, 119-Ball BGA (Top View)

	1	2	3	4	5	6	7
A	V <sub>DDQ</sub>	A	A	/ADSP	A	A	V <sub>DDQ</sub>
B	NC	A	A	/ADSC	A	A	NC
C	NC	A	A	V <sub>DD</sub>	A	A	NC
D	DQb	NC	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQP <sub>a</sub>	NC
E	NC	DQb	V <sub>SS</sub>	/CE	V <sub>SS</sub>	NC	DQ <sub>a</sub>
F	V <sub>DDQ</sub>	NC	V <sub>SS</sub>	/OE	V <sub>SS</sub>	DQ <sub>a</sub>	V <sub>DDQ</sub>
G	NC	DQb	/BW <sub>b</sub>	/ADV	V <sub>SS</sub>	NC	DQ <sub>a</sub>
H	DQb	NC	V <sub>SS</sub>	/GW	V <sub>SS</sub>	DQ <sub>a</sub>	NC
J	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
K	NC	DQb	V <sub>SS</sub>	CLK	V <sub>SS</sub>	NC	DQ <sub>a</sub>
L	DQb	NC	V <sub>SS</sub>	NC	/BW <sub>a</sub>	DQ <sub>a</sub>	NC
M	V <sub>DDQ</sub>	DQb	V <sub>SS</sub>	/BWE	V <sub>SS</sub>	NC	V <sub>DDQ</sub>
N	DQb	NC	V <sub>SS</sub>	A1*	V <sub>SS</sub>	DQ <sub>a</sub>	NC
P	NC	DQP <sub>b</sub>	V <sub>SS</sub>	A0*	V <sub>SS</sub>	NC	DQ <sub>a</sub>
R	NC	A	MODE	V <sub>DD</sub>	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View  
 119-Ball, 14 mm x 22 mm BGA

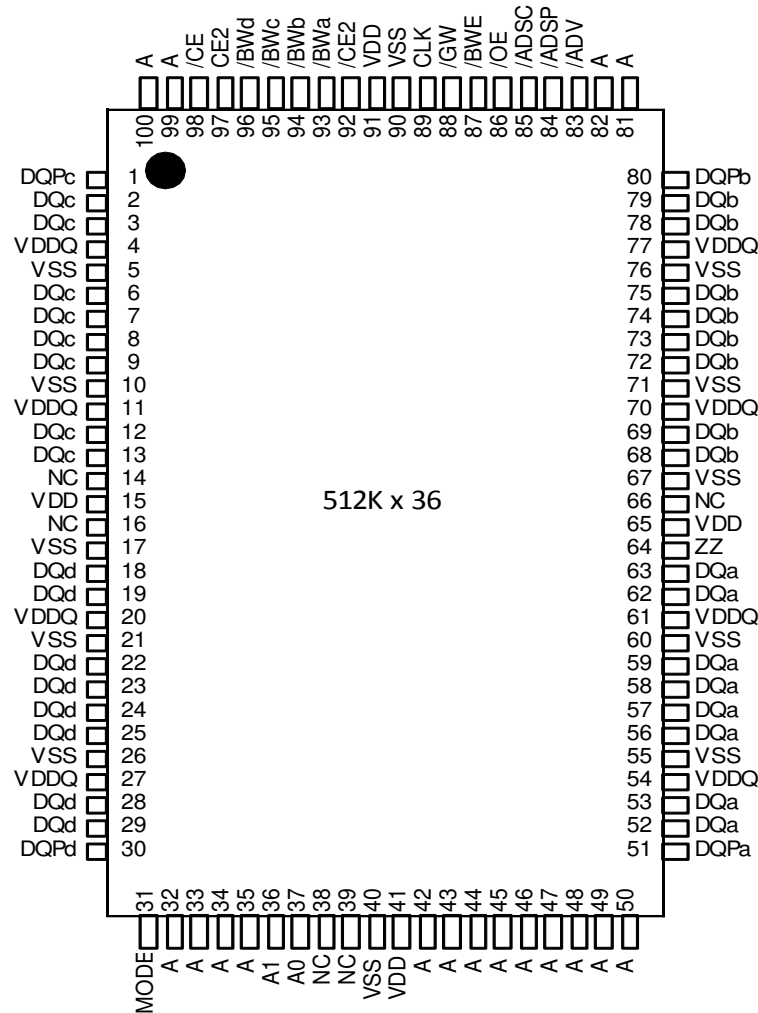
PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
A0,A1	Synchronous Burst Address Inputs
A	Address Inputs
/ADV	Synchronous Burst Address Advance
/ADSP	Address Status Processor
/ADSC	Address Status Controller
MODE	Burst Sequence Selection
/CE	Synchronous Chip Enable
/BWE	Byte Write Enable
/BW <sub>x</sub> (x=a-b)	Synchronous Byte Write Inputs
/GW	Global Write Enable
/OE	Output Enable
DQ <sub>x</sub>	Data Inputs/Outputs
DQP <sub>x</sub>	Parity Data I/O
TCK,TDI, TDO,TMS	JTAG Pins
ZZ	Power Sleep Mode
NC	No Connect
V <sub>DD</sub>	Power Supply
V <sub>DDQ</sub>	I/O Power Supply
V <sub>SS</sub>	Ground

IS61LF51236(32)B/IS61VF51236(32)B/IS61VVF51236(32)B  
 IS61LF102418B/IS61VF102436B/IS61VVF102418B



512K x 36, 100PIN QFP (Top View)

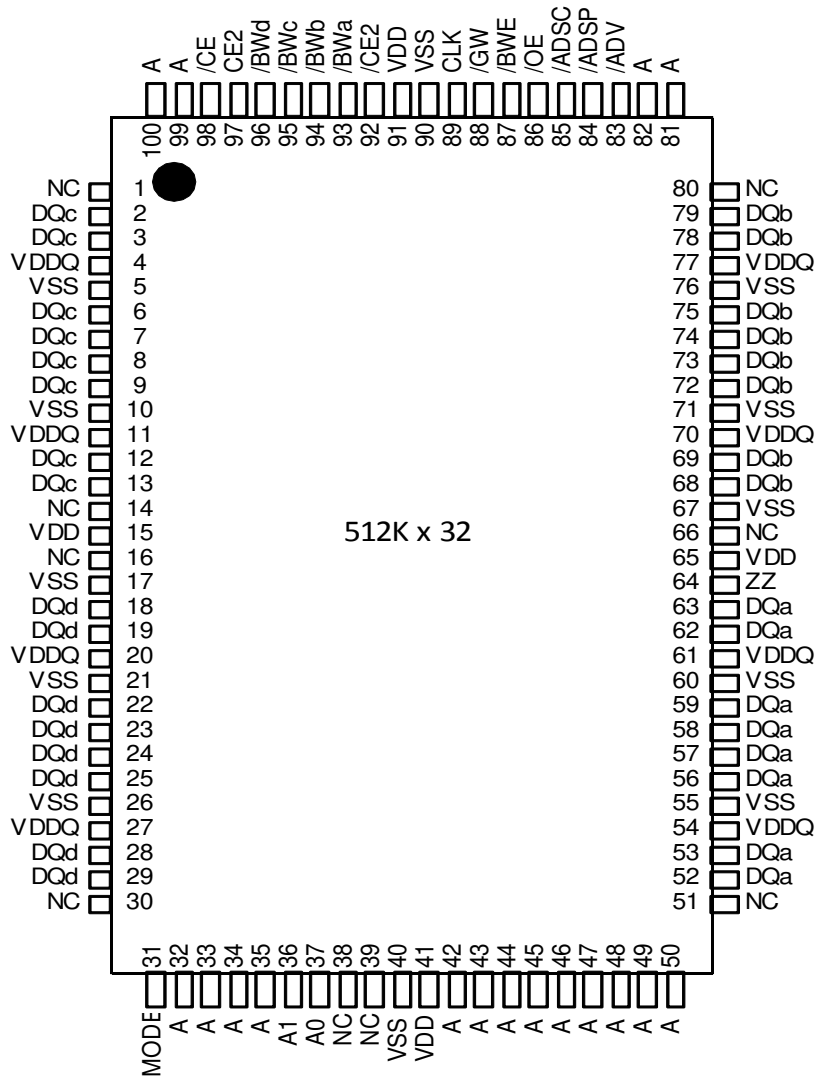


Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

**PIN DESCRIPTIONS**

Symbol	Pin Name	Symbol	Pin Name
CLK	Synchronous Clock	/GW	Global Write Enable
A0,A1	Synchronous Burst Address Inputs	/OE	Output Enable
A	Address Inputs	DQx	Data Inputs/Outputs
/ADV	Synchronous Burst Address Advance	DQPx	Parity Data I/O
/ADSP	Address Status Processor	ZZ	Power Sleep Mode
/ADSC	Address Status Controller	NC	No Connect
MODE	Burst Sequence Selection	V <sub>DD</sub>	Power Supply
/CE,CE2,/CE2	Synchronous Chip Enable	V <sub>DDQ</sub>	I/O Power Supply
/BWE	Byte Write Enable	V <sub>SS</sub>	Ground
/BWx (x=a-d)	Synchronous Byte Write Inputs		

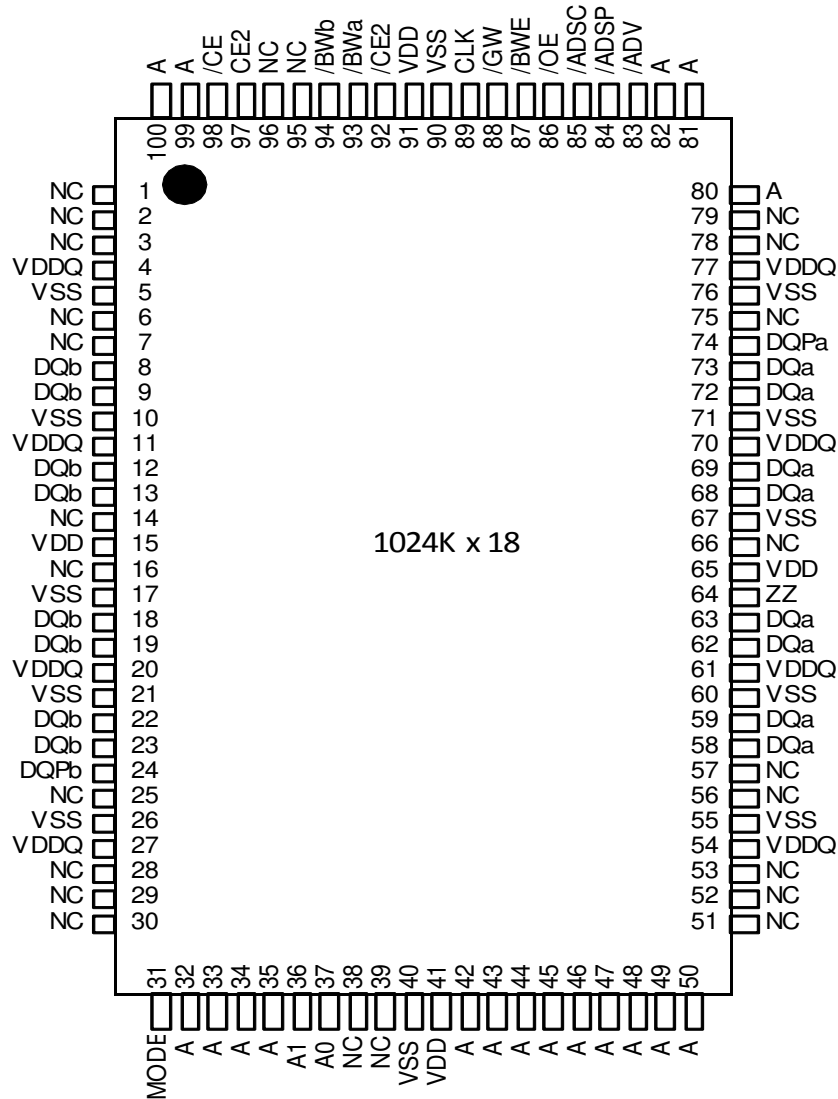
512K x 32, 100PIN QFP (Top View)



Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

**PIN DESCRIPTIONS**

Symbol	Pin Name	Symbol	Pin Name
CLK	Synchronous Clock	/GW	Global Write Enable
A0,A1	Synchronous Burst Address Inputs	/OE	Output Enable
A	Address Inputs	DQx	Data Inputs/Outputs
/ADV	Synchronous Burst Address Advance	ZZ	Power Sleep Mode
/ADSP	Address Status Processor	NC	No Connect
/ADSC	Address Status Controller	V <sub>DD</sub>	Power Supply
MODE	Burst Sequence Selection	V <sub>DDQ</sub>	I/O Power Supply
/CE,CE2,/CE2	Synchronous Chip Enable	V <sub>SS</sub>	Ground
/BWE	Byte Write Enable		
/BWx (x=a-d)	Synchronous Byte Write Inputs		



Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

### PIN DESCRIPTIONS

Symbol	Pin Name	Symbol	Pin Name
CLK	Synchronous Clock	/GW	Global Write Enable
A0,A1	Synchronous Burst Address Inputs	/OE	Output Enable
A	Address Inputs	DQx	Data Inputs/Outputs
/ADV	Synchronous Burst Address Advance	DQP <sub>x</sub>	Parity Data I/O
/ADSP	Address Status Processor	ZZ	Power Sleep Mode
/ADSC	Address Status Controller	NC	No Connect
MODE	Burst Sequence Selection	V <sub>DD</sub>	Power Supply
/CE,CE2,/CE2	Synchronous Chip Enable	V <sub>DDQ</sub>	I/O Power Supply
/BWE	Byte Write Enable	V <sub>SS</sub>	Ground
/BW <sub>x</sub> (x=a-b)	Synchronous Byte Write Inputs		



## TRUTH TABLE

### SYNCHRONOUS TRUTH TABLE

OPERATION	ADDRESS	/CE	/CE2	CE2	ZZ	/ADSP	/ADSC	/ADV	/WRITE	/OE	CLK	DQ
Deselect Cycle, Power-Down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
Snooze Mode, Power-Down	None	X	X	X	H	X	X	X	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
Write Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

NOTE:

1. X means "Don't Care." H means logic HIGH. L means logic LOW.
2. For WRITE, L means one or more byte write enable signals (/BWA-d) and /BWE are LOW or /GW is LOW. /WRITE = H for all /BWx, /BWE, /GW HIGH.
3. /BWA enables WRITES to DQa's and DQPa. /BWB enables WRITES to DQb's and DQPb. /BWC enables WRITES to DQc's and DQPC. /BWD enables WRITES to DQd's and DQPD. DQPa and DQPb are available on the x18 version. DQPa-DQPd are available on the x36 version.
4. All inputs except /OE and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, /OE must be HIGH before the input data setup time and held HIGH during the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. /ADSP LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and /BWE LOW or /GW LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

**PARTIAL TRUTH TABLE**

Operation	/GW	/BWE	/BWa	/BWb	/BWc	/BWd
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE BYTE a	H	L	L	H	H	H
WRITE BYTE b	H	L	H	L	H	H
WRITE BYTE c	H	L	H	H	L	H
WRITE BYTE d	H	L	H	H	H	L
WRITE ALL BYTEs	H	L	L	L	L	L
WRITE ALL BYTEs	L	X	X	X	X	X

Notes:

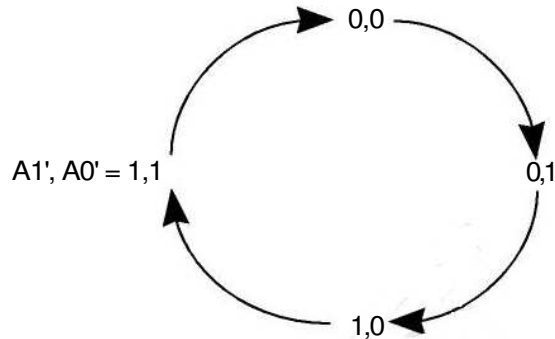
1. X means "Don't Care".
2. All inputs in this table must be set up and hold time around the rising edge of CLK.

**ADDRESS SEQUENCE IN BURST MODE**

**INTERLEAVED BURST ADDRESS TABLE (MODE = V<sub>DD</sub> or NC)**

External Address	1st Burst Address	2nd Burst Address	3rd Burst Address
A1 A0	A1 A0	A1 A0	A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

**LINEAR BURST ADDRESS TABLE (MODE = V<sub>SS</sub>)**



**Power Up Sequence**

V<sub>DDQ</sub> → V<sub>DD</sub><sup>1</sup> → I/O Pins<sup>2</sup>

Notes:

1. V<sub>DD</sub> can be applied at the same time as V<sub>DDQ</sub>
2. Applying I/O inputs is recommended after V<sub>DDQ</sub> is stable. The inputs of the I/O pins can be applied at the same time as V<sub>DDQ</sub> as long as V<sub>Ih</sub> (level of I/O pins) is lower than V<sub>DDQ</sub>.

## ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LPS Value	VPS/VVPS Value	Unit
T <sub>STG</sub>	Storage Temperature	-65 to +150	-65 to +150	°C
P <sub>D</sub>	Power Dissipation	1.6	1.6	W
I <sub>OUT</sub>	Output Current (per I/O)	100	20	mA
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage Relative to V <sub>SS</sub> for I/O Pins	-0.5 to V <sub>DDQ</sub> +0.5	-0.5 to V <sub>DDQ</sub> + 0.3	V
V <sub>IN</sub>	Voltage Relative to V <sub>SS</sub> for Address and Control Inputs	-0.5 to V <sub>DD</sub> +0.5	-0.5 to V <sub>DD</sub> + 0.3	V
V <sub>DD</sub>	Voltage on V <sub>DD</sub> Supply Relative to V <sub>SS</sub>	-0.5 to V <sub>DD</sub> +0.5	-0.5 to V <sub>DD</sub> +0.3	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

### OPERATING RANGE (IS61LFx)

Range	Ambient Temperature	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0°C to +70°C	3.3V ± 5%	3.3V / 2.5V ± 5%
Industrial	-40°C to +85°C	3.3V ± 5%	3.3V / 2.5V ± 5%
Automotive	-40°C to +125°C	3.3V ± 5%	3.3V / 2.5V ± 5%

### OPERATING RANGE (IS61VFx)

Range	Ambient Temperature	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0°C to +70°C	2.5V ± 5%	2.5V ± 5%
Industrial	-40°C to +85°C	2.5V ± 5%	2.5V ± 5%
Automotive	*Please contact ISSI		

### OPERATING RANGE (IS61VVFx)

Range	Ambient Temperature	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0°C to +70°C	1.8V ± 5%	1.8V ± 5%
Industrial	-40°C to +85°C	1.8V ± 5%	1.8V ± 5%
Automotive	*Please contact ISSI		

## CHARACTERISTICS

### DC ELECTRICAL CHARACTERISTICS (Over operating temperature range)

Symbol	Parameter	Test Conditions	3.3V		2.5V		1.8V		Unit	
			Min.	Max.	Min	Max.	Min.	Max.		
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> =-4.0 mA(3.3V)	2.4	—	2.0	—	V <sub>DDQ</sub>	-0.4	—	V
		I <sub>OH</sub> =-1.0 mA(2.5V,1.8V)								
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> =8.0 mA(3.3V)	—	0.4	—	0.4	—	0.4	—	V
		I <sub>OL</sub> =1.0 mA(2.5V,1.8V)								
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>DD</sub> +0.3	1.7	V <sub>DD</sub> +0.3	0.7* V <sub>DD</sub>	V <sub>DD</sub> +0.3		V
V <sub>IL</sub>	Input LOW Voltage		-0.3	0.8	-0.3	0.7	-0.3	0.3* V <sub>DD</sub>		V
I <sub>LI</sub>	Input Leakage Current	V <sub>SS</sub> ≤V <sub>IN</sub> ≤ V <sub>DD</sub>	-1	1	-1	1	-1	1		μA
I <sub>LO</sub>	Output Leakage Current	V <sub>SS</sub> ≤V <sub>OUT</sub> ≤ V <sub>DD</sub> ,/OE=V <sub>IH</sub>	-1	1	-1	1	-1	1		μA

Notes:

- All voltages referenced to ground.
- Overshoot:  
 3.3V and 2.5V: V<sub>IH</sub> (AC) ≤ V<sub>DD</sub> + 1.5V (Pulse width less than t<sub>KC</sub> /2)  
 1.8V: V<sub>IH</sub> (AC) ≤ V<sub>DD</sub> + 0.5V (Pulse width less than t<sub>KC</sub> /2)
- Undershoot:  
 3.3V and 2.5V: V<sub>IL</sub> (AC) ≥ -1.5V (Pulse width less than t<sub>KC</sub> /2)  
 1.8V: V<sub>IL</sub> (AC) ≥ -0.5V (Pulse width less than t<sub>KC</sub> /2)
- MODE pin has an internal pull-up and should be tied to V<sub>DD</sub> or V<sub>SS</sub> . It exhibits ±100μA maximum leakage current when tied to ≤V<sub>SS</sub>+0.2V or ≥ V<sub>DDQ</sub>-0.2V.
- ZZ pin has an internal pull-down and should be tied to V<sub>DD</sub> or V<sub>SS</sub> . It exhibits ±100μA maximum leakage current when tied to ≤V<sub>SS</sub>+0.2V or ≥ V<sub>DD</sub>-0.2V.

### POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Temp. range	-6.5		-7.5		Unit
				Max		Max		
				x18	x36	x18	x36	
I <sub>CC</sub>	AC Operating, Supply Current	Device Selected, /OE = V <sub>IH</sub> , ZZ ≤ V <sub>IL</sub> , All Inputs ≤ 0.2V or ≥ V <sub>DD</sub> - 0.2V, Cycle Time ≥ t <sub>KC</sub> min.	Com.	240	240	190	190	mA
			Ind.	260	260	210	210	
			Auto.	-	-	230	230	
I <sub>SB</sub>	Standby Current TTL Input	Device Deselected, V <sub>DD</sub> = Max. All Inputs ≤ V <sub>IL</sub> or ≥ V <sub>IH</sub> , ZZ ≤ V <sub>IL</sub> , f = Max.	Com.	80	80	70	70	mA
			Ind.	90	90	80	80	
			Auto.	-	-	90	90	
I <sub>SB1</sub>	Standby Current CMOS Input	Device Deselected, V <sub>DD</sub> = Max., V <sub>IN</sub> ≤ V <sub>SS</sub> + 0.2V or ≥ V <sub>DD</sub> - 0.2V, f = 0	Com.	60	60	60	60	mA
			Ind.	70	70	70	70	
			Auto.	-	-	80	80	

Note:

- Power-up assumes a linear ramp from 0V to V<sub>DD</sub> (min) within 200ms. During this time V<sub>IH</sub> < V<sub>DD</sub> and V<sub>DDQ</sub> < V<sub>DD</sub>



## CAPACITANCE

Symbol	Parameter	Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	6	pF
$C_{OUT}$	Input/Output Capacitance	$V_{OUT} = 0V$	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions:  $T_a = 25^\circ C$ ,  $f = 1\text{ MHz}$ ,  $V_{DD} = 3.3V$ .

## READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-6.5		-7.5		Unit
		Min.	Max.	Min.	Max.	
$f_{MAX}$	Clock Frequency	—	133	—	117	MHz
$t_{KC}$	Cycle Time	7.5	—	8.5	—	ns
$t_{KH}$	Clock High Time	2.2	—	2.5	—	ns
$t_{KL}$	Clock Low Time	2.2	—	2.5	—	ns
$t_{KQ}$	Clock Access Time	—	6.5	—	7.5	ns
$t_{KQX}^{(2)}$	Clock High to Output Invalid	2.5	—	2.5	—	ns
$t_{KQLZ}^{(2,3)}$	Clock High to Output Low-Z	2.5	—	2.5	—	ns
$t_{KQHZ}^{(2,3)}$	Clock High to Output High-Z	—	3.8	—	4.0	ns
$t_{OEQ}$	Output Enable to Output Valid	—	3.2	—	3.4	ns
$t_{OELZ}^{(2,3)}$	Output Enable to Output Low-Z	0	—	0	—	ns
$t_{OEZH}^{(2,3)}$	Output Disable to Output High-Z	—	3.5	—	3.5	ns
$t_{AS}$	Address Setup Time	1.5	—	1.5	—	ns
$t_{SS}$	Address Status Setup Time	1.5	—	1.5	—	ns
$t_{ws}$	Read/Write Setup Time	1.5	—	1.5	—	ns
$t_{CES}$	Chip Enable Setup Time	1.5	—	1.5	—	ns
$t_{ADVS}$	Address Advance Setup Time	1.5	—	1.5	—	ns
$t_{DS}$	Data Setup Time	1.5	—	1.5	—	ns
$t_{AH}$	Address Hold Time	0.5	—	0.5	—	ns
$t_{SH}$	Address Status Hold Time	0.5	—	0.5	—	ns
$t_{WH}$	Write Hold Time	0.5	—	0.5	—	ns
$t_{CEH}$	Chip Enable Hold Time	0.5	—	0.5	—	ns
$t_{ADVH}$	Address Advance Hold Time	0.5	—	0.5	—	ns
$t_{DH}$	Data Hold Time	0.5	—	0.5	—	ns

Notes:

1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

**3.3V I/O AC TEST CONDITIONS**

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
$V_{TT}$	1.5V
$V_{LOAD}$	3.3V
R1, R2	317 $\Omega$ , 351 $\Omega$
Output Load	See Figures 1 and 2

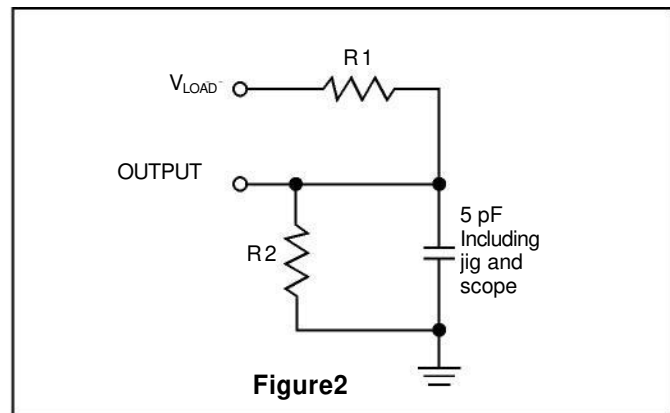
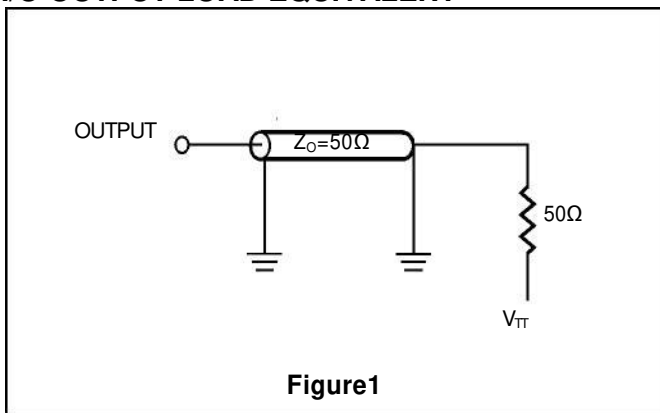
**2.5V I/O AC TEST CONDITIONS**

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.25V
$V_{TT}$	1.25V
$V_{LOAD}$	2.5V
R1, R2	1667 $\Omega$ , 1538 $\Omega$
Output Load	See Figures 1 and 2

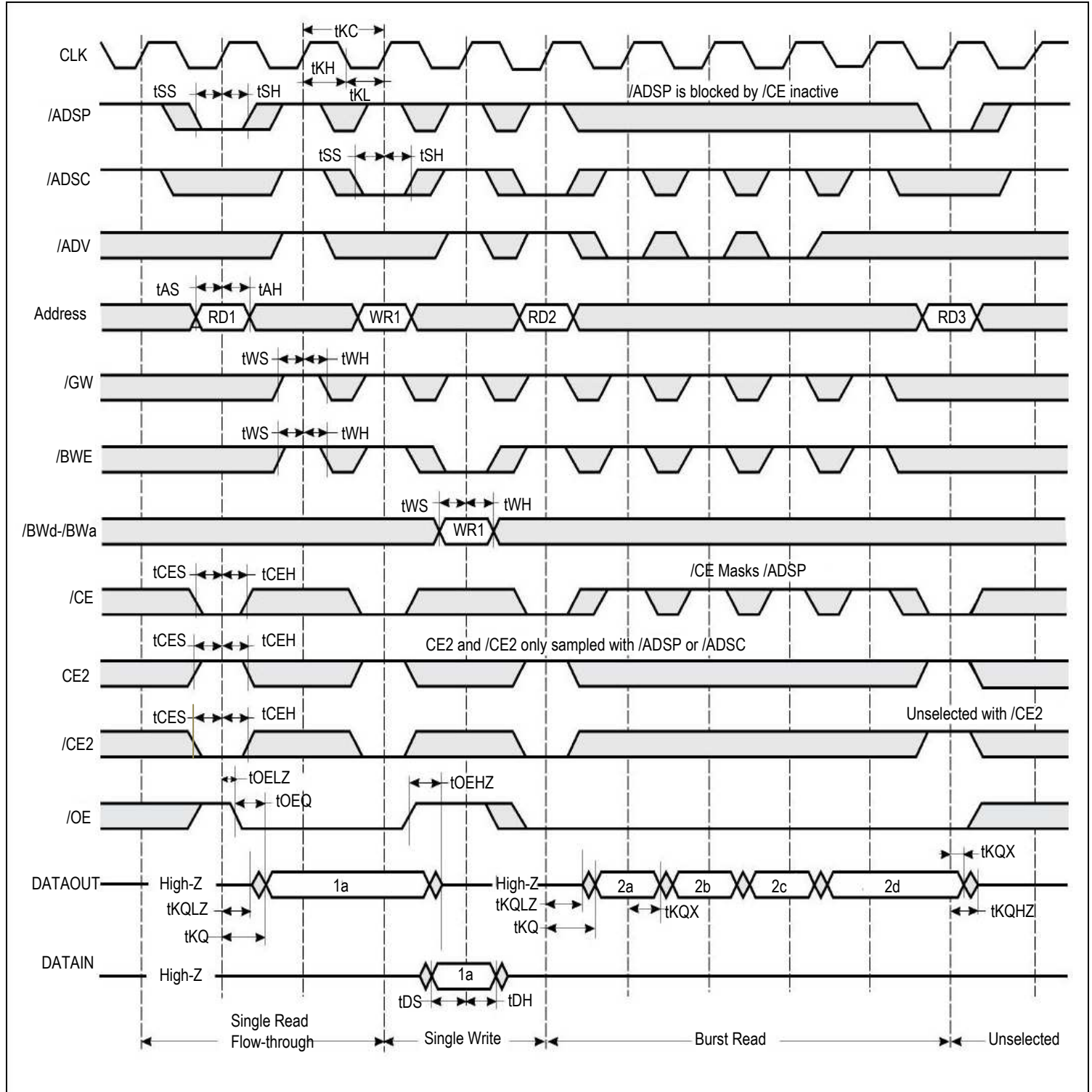
**1.8V I/O AC TEST CONDITIONS**

Parameter	Unit
Input Pulse Level	0V to 1.8V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	0.9V
$V_{TT}$	0.9V
$V_{LOAD}$	1.8V
R1, R2	1K $\Omega$ , 1K $\Omega$
Output Load	See Figures 1 and 2

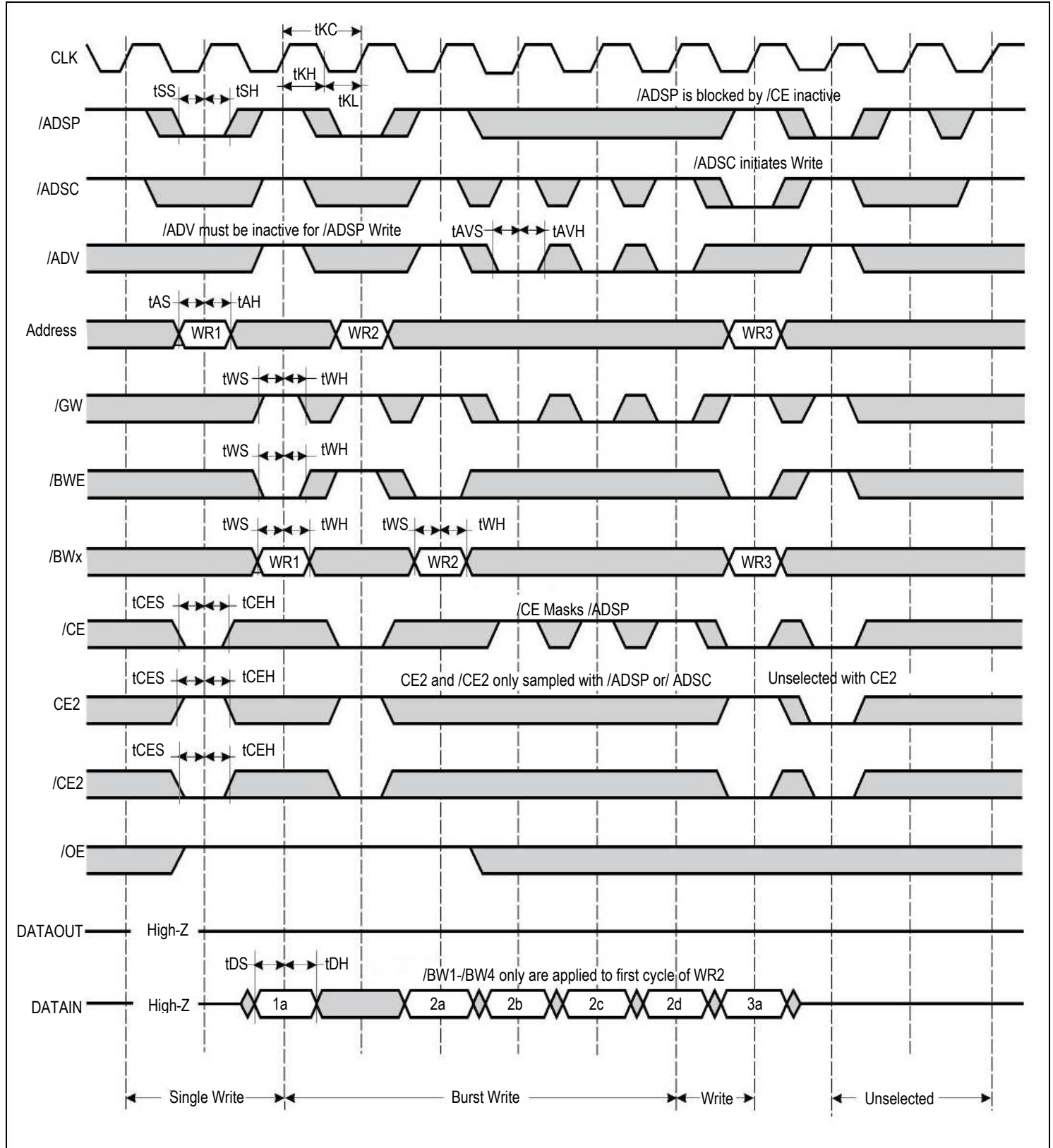
**I/O OUTPUT LOAD EQUIVALENT**



READ/WRITE CYCLE TIMING



**WRITE CYCLE TIMING**

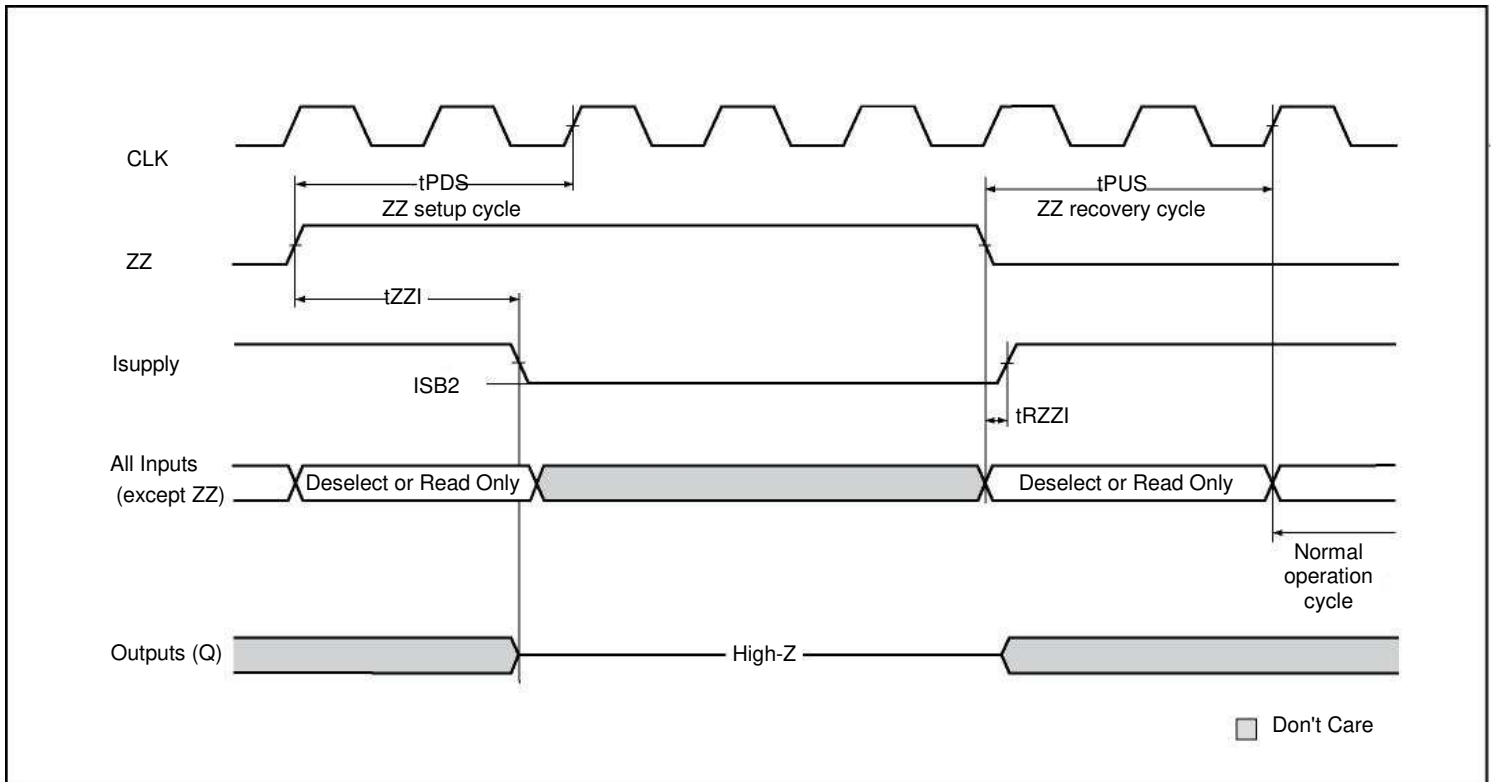




**SNOOZE MODE ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Conditions	Temperature Range	Min.	Max.	Unit
$I_{SB2}$	Current during SNOOZE MODE	$ZZ \geq V_{IH}$	Com.	—	40	mA
			Ind.	—	50	mA
			Auto.	—	60	mA
$t_{PDS}$	ZZ active to input ignored		—	—	2	cycle
$t_{PUS}$	ZZ inactive to input sampled		—	2	—	cycle
$t_{ZZI}$	ZZ active to SNOOZE current		—	—	2	cycle
$t_{RZZI}$	ZZ inactive to exit SNOOZE current		—	0	—	ns

**SLEEP MODE TIMING**



## IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE Standard 1149.1, the SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

The TAP controller has a standard 16-state machine that resets internally on power-up. Therefore, a TRST signal is not required

### Disabling the JTAG feature

The SRAM can operate without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (VSS) to prevent clocking of the device. TDI and TMS are internally pulled up and may be left disconnected. They may alternately be connected to  $V_{DD}$  through a pull-up resistor. TDO should be left disconnected. On power-up, the device will come up in a reset state, which will not interfere with device operation.

### Test Access Port Signal List:

#### 1. Test Clock (TCK)

This signal uses  $V_{DD}$  as a power supply. The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

#### 2. Test Mode Select (TMS)

This signal uses  $V_{DD}$  as a power supply. The TMS input is used to send commands to the TAP controller and is sampled on the rising edge of TCK.

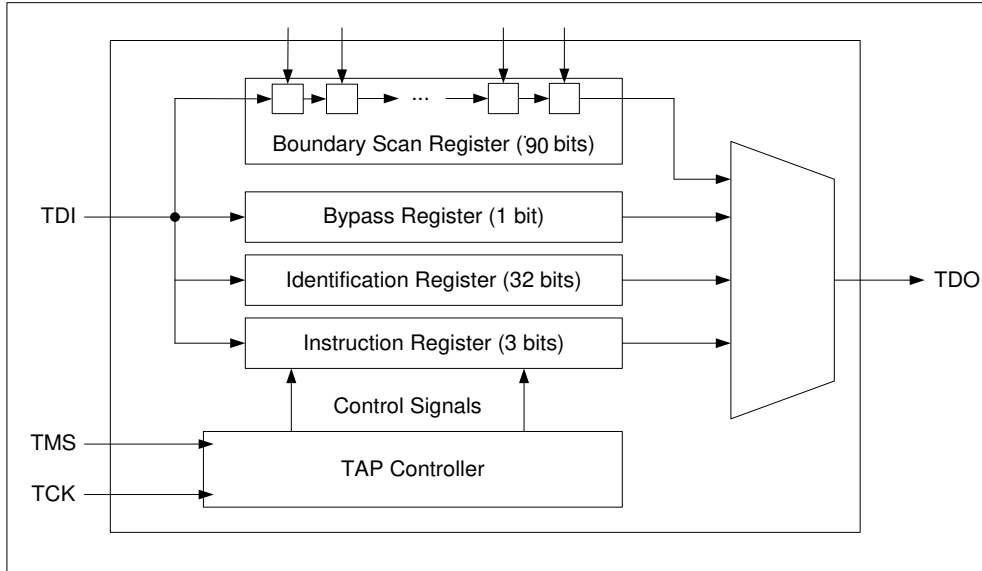
#### 3. Test Data-In (TDI)

This signal uses  $V_{DD}$  as a power supply. The TDI input is used to serially input test instructions and information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is connected to the most significant bit (MSB) of any register. For more information regarding instruction register loading, please see the TAP Controller State Diagram.

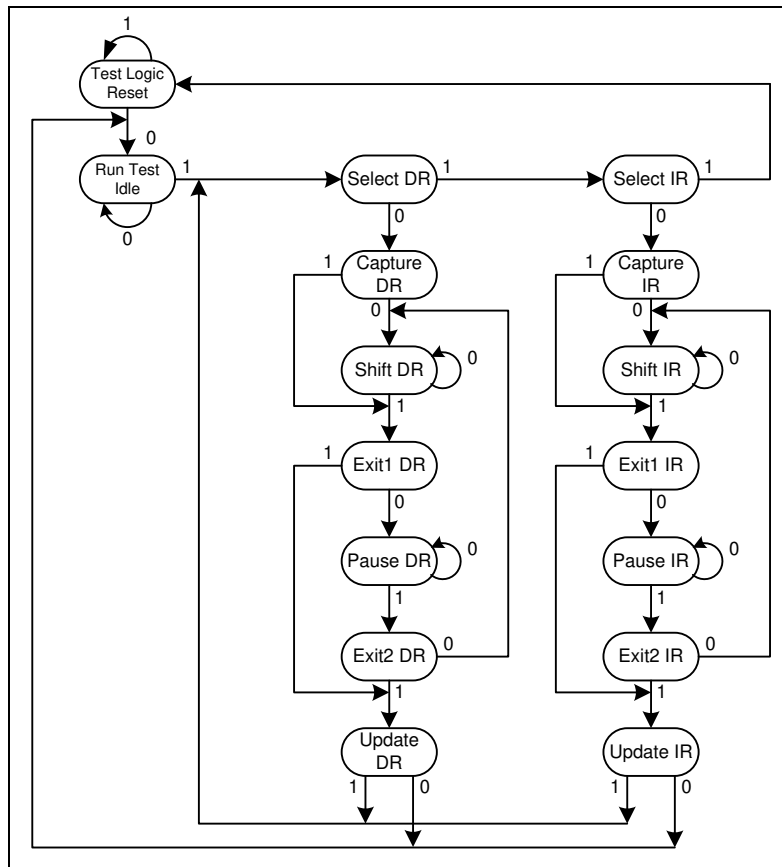
#### 4. Test Data-Out (TDO)

This signal uses  $V_{DDQ}$  as a power supply. The TDO output ball is used to serially clock test instructions and data out from the registers. The TDO output driver is only active during the Shift-IR and Shift-DR TAP controller states. In all other states, the TDO pin is in a High-Z state. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. For more information, please see the TAP Controller State Diagram.

### TAP Controller State and Block Diagram



### TAP Controller State Machine



## Performing a TAP Reset

A Reset is performed by forcing TMS HIGH ( $V_{DD}$ ) for five rising edges of TCK. RESET may be performed while the SRAM is operating and does not affect its operation. At power-up, the TAP is internally reset to ensure that TDO comes up in a high-Z state.

## TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK and output on the TDO pin on the falling edge of TCK.

### 1. Instruction Register

This register is loaded during the update-IR state of the TAP controller. At power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section. When the TAP controller is in the capture-IR state, the two LSBs are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

### 2. Bypass Register

The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW ( $V_{SS}$ ) when the BYPASS instruction is executed.

### 3. Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. Several balls are also included in the scan register to reserved balls. The boundary scan register is loaded with the contents of the SRAM Input and Output ring when the TAP controller is in the capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the shift-DR state. Each bit corresponds to one of the balls on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

### 4. Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the shift-DR state.

## Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	90

## TAP Instruction Set

Many instructions are possible with an eight-bit instruction register and all valid combinations are listed in the TAP Instruction Code Table. All other instruction codes that are not listed on this table are reserved and should not be used. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted from the instruction register through the TDI and TDO pins. To execute an instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.



## **1. EXTEST**

The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output balls are used to apply a test vector, while those at input balls capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the update-IR state of EXTEST, the output driver is turned on, and the PRELOAD data is driven onto the output balls.

## **2. IDCODE**

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

## **3. SAMPLE Z**

If the SAMPLE-Z instruction is loaded in the instruction register, all SRAM outputs are forced to an inactive drive state (high-Z), moving the TAP controller into the capture-DR state loads the data in the SRAMs input into the boundary scan register, and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.

## **4. SAMPLE/PRELOAD**

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register. The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates significantly faster. Because there is a large difference between the clock frequencies, it is possible that during the capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition. This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible. To ensure that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time. The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/ PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register. Once the data is captured, it is possible to shift out the data by putting the TAP into the shift-DR state. This places the boundary scan register between the TDI and TDO balls.

## **6. BYPASS**

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

## **7. PRIVATE**

Do not use these instructions. They are reserved for future use and engineering mode.

### JTAG DC Operating Characteristics

(Over the Operating Temperature Range, 2.5V and 3.3V Option)

Parameter	Symbol	Min	Max	Units	Notes
JTAG Input High Voltage	$V_{IH1}$	2.0	$V_{DD}+0.3$	V	
JTAG Input Low Voltage	$V_{IL1}$	-0.3	0.7	V	
JTAG Output High Voltage	$V_{OH1}$	1.7	-	V	$ I_{OH1} =2\text{mA}$
JTAG Output Low Voltage	$V_{OL1}$	-	0.7	V	$I_{OL1}=2\text{mA}$
JTAG Output High Voltage	$V_{OH2}$	2.1	-	V	$ I_{OH2} =100\mu\text{A}$
JTAG Output Low Voltage	$V_{OL2}$	-	0.2	V	$I_{OL2}=100\mu\text{A}$
JTAG Input Leakage Current	$I_{L1JTAG}$	-10	+10	$\mu\text{A}$	$0 \leq V_{in} \leq V_{DD}$
JTAG Output Leakage Current	$I_{LOJTAG}$	-10	+10	$\mu\text{A}$	$0 \leq V_{out} \leq V_{DD}$

Notes:

- All voltages referenced to VSS (GND); All JTAG inputs and outputs are LVTTTL-compatible.

### JTAG DC Operating Characteristics

(Over the Operating Temperature Range, 1.8V Option)

Parameter	Symbol	Min	Max	Units	Notes
JTAG Input High Voltage	$V_{IH1}$	TBD	TBD	V	
JTAG Input Low Voltage	$V_{IL1}$	TBD	TBD	V	
JTAG Output High Voltage	$V_{OH1}$	TBD	TBD	V	
JTAG Output Low Voltage	$V_{OL1}$	TBD	TBD	V	
JTAG Input Leakage Current	$I_{L1JTAG}$	TBD	TBD	$\mu\text{A}$	
JTAG Output Leakage Current	$I_{LOJTAG}$	TBD	TBD	$\mu\text{A}$	

Notes:

- All voltages referenced to VSS (GND); All JTAG inputs and outputs are LVTTTL-compatible.

### JTAG AC Test Conditions

(Over the Operating Temperature Range)

Parameter	Symbol	1.8V Option	2.5V Option	3.3V Option	Units
Input Pulse High Level	$V_{IH1}$	TBD	2.5	3.0	V
Input Pulse Low Level	$V_{IL1}$	TBD	0	0	V
Input rise and fall time	$T_{R1}$	TBD	1.5	1.5	ns
Test load termination supply voltage	$V_{REF}$	TBD	1.25	1.5	V
Input and Output Timing Reference Level	$V_{REF}$	TBD	1.25	1.5	V

### TAP Output Load Equivalent

