Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

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128K x36/32 and 256K x18 4Mb, ECC, SYNCHRONOUS FLOW-THROUGH SRAM

APRIL 2017

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Burst sequence control using MODE input
- Three chip enable option for simple depth expansion and address pipelining
- Common data inputs and data outputs
- Auto Power-down during deselect
- Single cycle deselect
- Snooze MODE for reduced-power standby
- JEDEC 100-pin QFP, 165-ball BGA and 119-ball BGA packages
- Power supply:
- LF: V_{DD} 3.3V (± 5%), V_{DDQ} 3.3V/2.5V (± 5%)
- VF: V_{DD} 2.5V (± 5%), V_{DDQ} 2.5V (± 5%)
- JTAG Boundary Scan for BGA packages
- Industrial and Automotive temperature support
- Lead-free available
- Error Detection and Error Correction

DESCRIPTION

The 4Mb product family features high-speed, low-power synchronous static RAMs designed to provide burstable, high-performance memory for communication and networking applications. The IS61(64)LF/VF12836EC are organized as 131,072 words by 36bits. The IS61(64)LF/VF12832EC are organized as 131,072 words by 32bits. The IS61(64)LF/VF25618EC are organized as 262,144 words by 18 bits. Fabricated with ISSI's advanced CMOS technology, the device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. The byte write operation is performed by using the byte write enable (/BWE) input combined with one or more individual byte write signals (/BWx). In addition, Global Write (/GW) is available for writing all bytes at one time, regardless of the byte write controls.

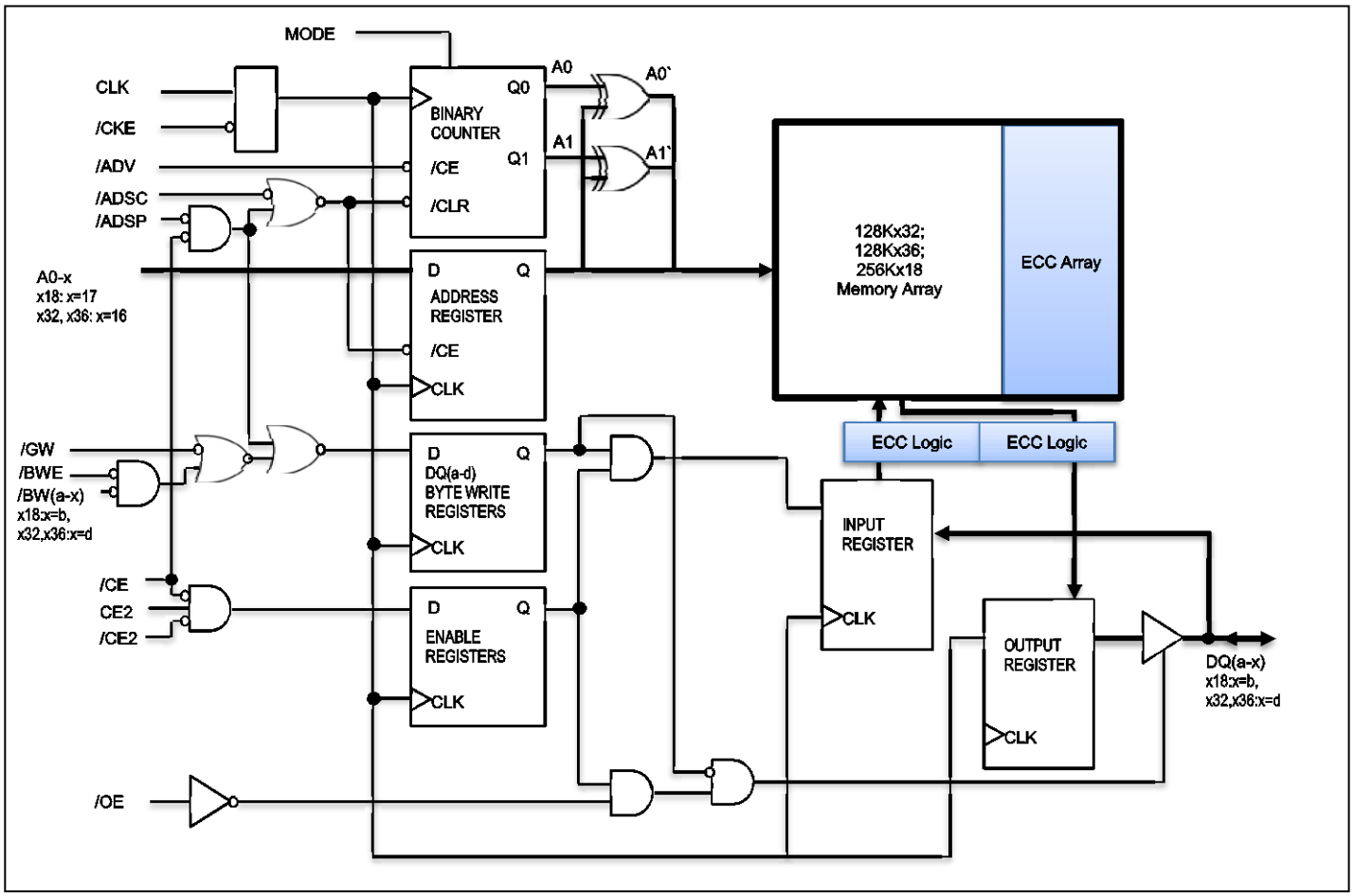
Bursts can be initiated with either /ADSP (Address Status Processor) or /ADSC (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the /ADV (burst address advance) input pin.

The mode pin is used to select the burst sequence order. Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

FAST ACCESS TIME

Symbol	Parameter	-6.5	-7.5	Units
tKQ	Clock Access Time	6.5	7.5	ns
tKC	Cycle time	7.5	8.5	ns
	Frequency	133	117	MHz

BLOCK DIAGRAM

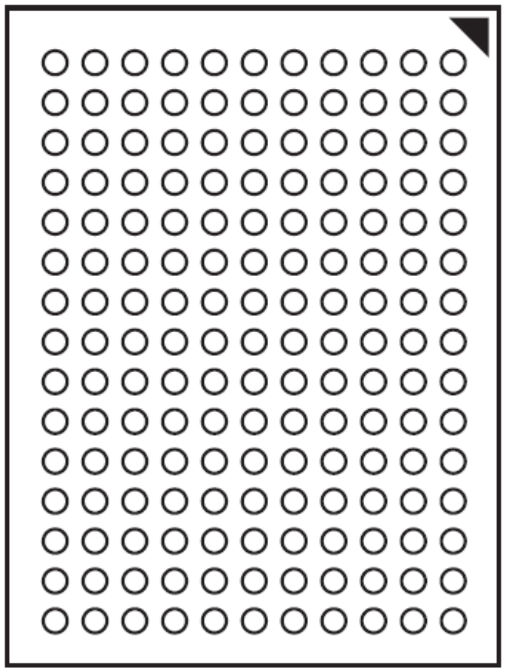


PIN CONFIGURATION

128K x 36, 165-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	/CE	/BWc	/BWb	/CE2	/BWE	/ADSC	/ADV	A	NC
B	NC	A	CE2	/BWd	/BWa	CLK	/GW	/OE	/ADSP	A	NC
C	DQPc	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQPb
D	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
E	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
F	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
G	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
H	NC	V_{SS}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
K	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
L	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
M	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
N	DQPd	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DQPa
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	NC
R	MODE	NC	A	A	TMS	A0*	TCK	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired



Bottom View
165-Ball, 13 mm x 15mm BGA
11 x 15 Ball Array

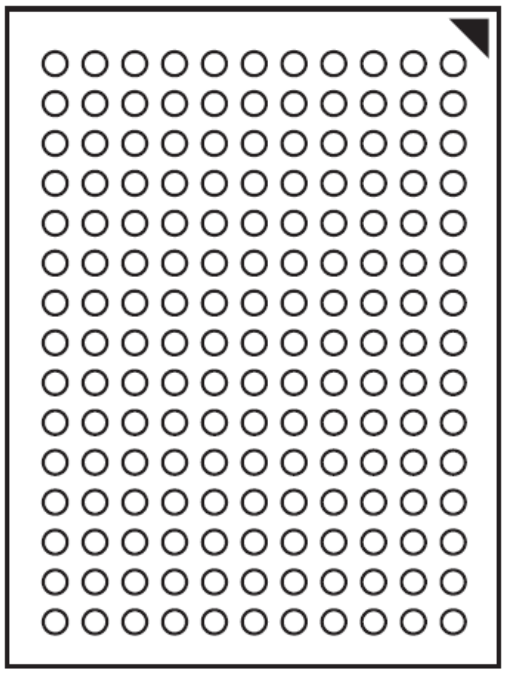
PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
A0,A1	Synchronous Burst Address Inputs
A	Synchronous Address Inputs
/ADV	Synchronous Burst Address Advance
/ADSP	Synchronous Address Status Processor
/ADSC	Synchronous Address Status Controller
MODE	Burst Sequence Selection
/CE,CE2,/CE2	Synchronous Chip Enable
/BWE	Synchronous Byte Write Enable
/BWx (x=a-d)	Synchronous Byte Write Inputs
/GW	Synchronous Global Write Enable
/OE	Asynchronous Output Enable
DQx	Synchronous Data Inputs/Outputs
DQPx	Synchronous Parity Data I/O
TCK,TDI,TDO,TMS	JTAG Pins
ZZ	Asynchronous Power Sleep Mode
NC	No Connect
VDD	Power Supply
VDDQ	I/O Power Supply
VSS	Ground

128K x 32, 165-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	/CE	/BWc	/BWb	/CE2	/BWE	/ADSC	/ADV	A	NC
B	NC	A	CE2	/BWd	/BWa	CLK	/GW	/OE	/ADSP	A	NC
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC
D	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
E	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
F	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
G	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
H	NC	V_{SS}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
K	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
L	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
M	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
N	NC	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	NC
R	MODE	NC	A	A	TMS	A0*	TCK	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
165-Ball, 13 mm x 15mm BGA
11 x 15 Ball Array

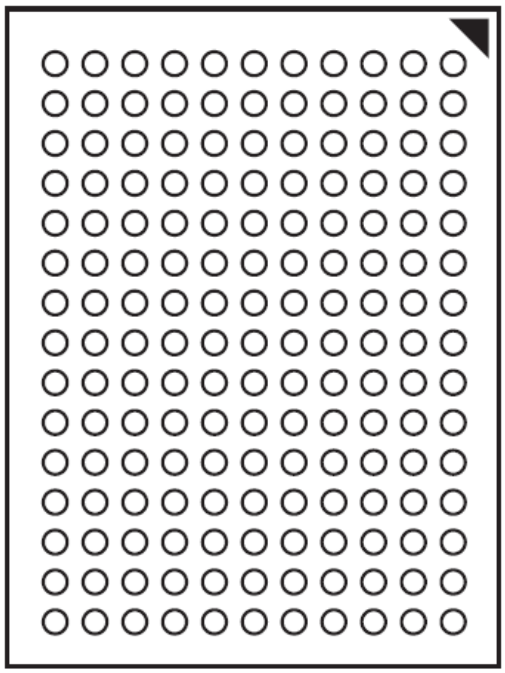
PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
A0,A1	Synchronous Burst Address Inputs
A	Synchronous Address Inputs
/ADV	Synchronous Burst Address Advance
/ADSP	Synchronous Address Status Processor
/ADSC	Synchronous Address Status Controller
MODE	Burst Sequence Selection
/CE,CE2,/CE2	Synchronous Chip Enable
/BWE	Synchronous Byte Write Enable
/BWx (x=a-d)	Synchronous Byte Write Inputs
/GW	Synchronous Global Write Enable
/OE	Asynchronous Output Enable
DQx	Synchronous Data Inputs/Outputs
TCK,TDI,TDO,TMS	JTAG Pins
ZZ	Asynchronous Power Sleep Mode
NC	No Connect
VDD	Power Supply
VDDQ	I/O Power Supply
VSS	Ground

256K x 18, 165-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	/CE	/BWb	NC	/CE2	/BWE	/ADSC	/ADV	A	A
B	NC	A	CE2	NC	/BWa	CLK	/GW	/OE	/ADSP	A	NC
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQPa
D	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
E	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
F	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
G	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
H	NC	V_{SS}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
K	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
L	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
M	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
N	DQPb	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	NC
R	MODE	NC	A	A	TMS	A0*	TCK	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
165-Ball, 13 mm x 15mm BGA
11 x 15 Ball Array

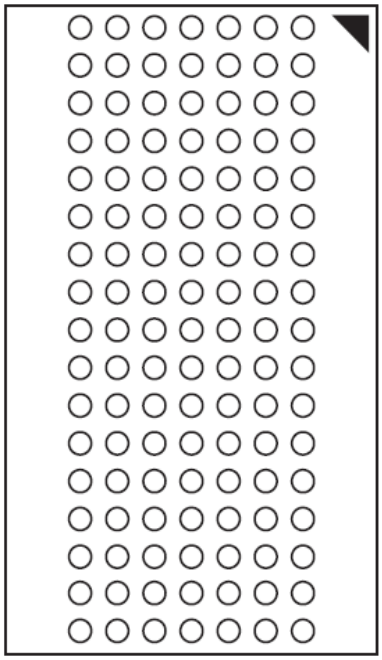
PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
A0,A1	Synchronous Burst Address Inputs
A	Synchronous Address Inputs
/ADV	Synchronous Burst Address Advance
/ADSP	Synchronous Address Status Processor
/ADSC	Synchronous Address Status Controller
MODE	Burst Sequence Selection
/CE,CE2,/CE2	Synchronous Chip Enable
/BWE	Synchronous Byte Write Enable
/BWx (x=a-b)	Synchronous Byte Write Inputs
/GW	Synchronous Global Write Enable
/OE	Asynchronous Output Enable
DQx	Synchronous Data Inputs/Outputs
DQPx	Synchronous Parity Data I/O
TCK,TDI,TDO,TMS	JTAG Pins
ZZ	Asynchronous Power Sleep Mode
NC	No Connect
VDD	Power Supply
VDDQ	I/O Power Supply
VSS	Ground

128K x 36, 119-Ball BGA (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	/ADSP	A	A	V_{DDQ}
B	NC	CE2	A	/ADSC	A	/CE2	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	DQPc	V_{SS}	NC	V_{SS}	DQPb	DQb
E	DQc	DQc	V_{SS}	/CE	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	/OE	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	/BWc	/ADV	/BWb	DQb	DQb
H	DQc	DQc	V_{SS}	/GW	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	V_{SS}	DQa	DQa
L	DQd	DQd	/BWd	NC	/BWa	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	/BWE	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A1*	V_{SS}	DQa	DQa
P	DQd	DQPd	V_{SS}	A0*	V_{SS}	DQPa	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
119-Ball, 14 mm x 22 mm BGA
7 x 17 Ball Array

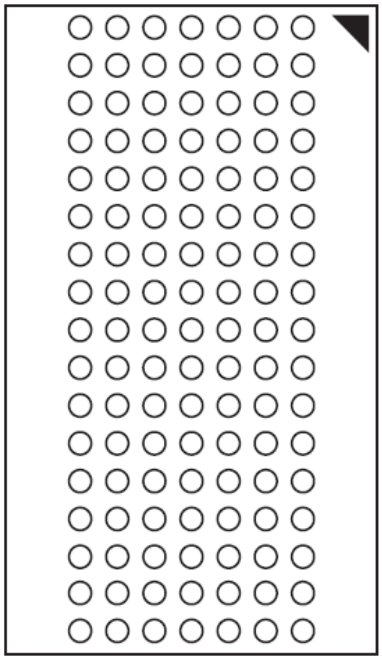
PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
A0,A1	Synchronous Burst Address Inputs
A	Synchronous Address Inputs
/ADV	Synchronous Burst Address Advance
/ADSP	Synchronous Address Status Processor
/ADSC	Synchronous Address Status Controller
MODE	Burst Sequence Selection
/CE,CE2,/CE2	Synchronous Chip Enable
/BWE	Synchronous Byte Write Enable
/BWx (x=a-d)	Synchronous Byte Write Inputs
/GW	Synchronous Global Write Enable
/OE	Asynchronous Output Enable
DQx	Synchronous Data Inputs/Outputs
DQPx	Synchronous Parity Data I/O
TCK,TDI,TDO,TMS	JTAG Pins
ZZ	Asynchronous Power Sleep Mode
NC	No Connect
VDD	Power Supply
VDDQ	I/O Power Supply
VSS	Ground

128K x 32, 119-Ball BGA (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	/ADSP	A	A	V_{DDQ}
B	NC	CE2	A	/ADSC	A	/CE2	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	NC	V_{SS}	NC	V_{SS}	NC	DQb
E	DQc	DQc	V_{SS}	/CE	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	/OE	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	/BWc	/ADV	/BWb	DQb	DQb
H	DQc	DQc	V_{SS}	/GW	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	V_{SS}	DQa	DQa
L	DQd	DQd	/BWd	NC	/BWa	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	/BWE	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A1*	V_{SS}	DQa	DQa
P	DQd	NC	V_{SS}	A0*	V_{SS}	NC	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
119-Ball, 14 mm x 22 mm BGA
7 x 17 Ball Array

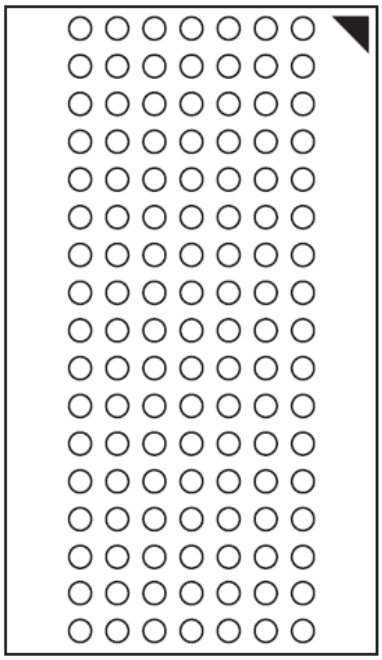
PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
A0,A1	Synchronous Burst Address Inputs
A	Synchronous Address Inputs
/ADV	Synchronous Burst Address Advance
/ADSP	Synchronous Address Status Processor
/ADSC	Synchronous Address Status Controller
MODE	Burst Sequence Selection
/CE,CE2,/CE2	Synchronous Chip Enable
/BWE	Synchronous Byte Write Enable
/BWx (x=a-b)	Synchronous Byte Write Inputs
/GW	Synchronous Global Write Enable
/OE	Asynchronous Output Enable
DQx	Synchronous Data Inputs/Outputs
TCK,TDI,TDO,TMS	JTAG Pins
ZZ	Asynchronous Power Sleep Mode
NC	No Connect
VDD	Power Supply
VDDQ	I/O Power Supply
VSS	Ground

256K x 18, 119-Ball BGA (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	/ADSP	A	A	V_{DDQ}
B	NC	CE2	A	/ADSC	A	/CE2	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQPa	NC
E	NC	DQb	V_{SS}	/CE	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	/OE	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	/BWb	/ADV	V_{SS}	NC	DQa
H	DQb	NC	VSS	/GW	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	VSS	CLK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	NC	/BWa	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	/BWE	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	A1*	V_{SS}	DQa	NC
P	NC	DQPb	V_{SS}	A0*	V_{SS}	NC	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
119-Ball, 14 mm x 22 mm BGA
7 x 17 Ball Array

PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
A0,A1	Synchronous Burst Address Inputs
A	Synchronous Address Inputs
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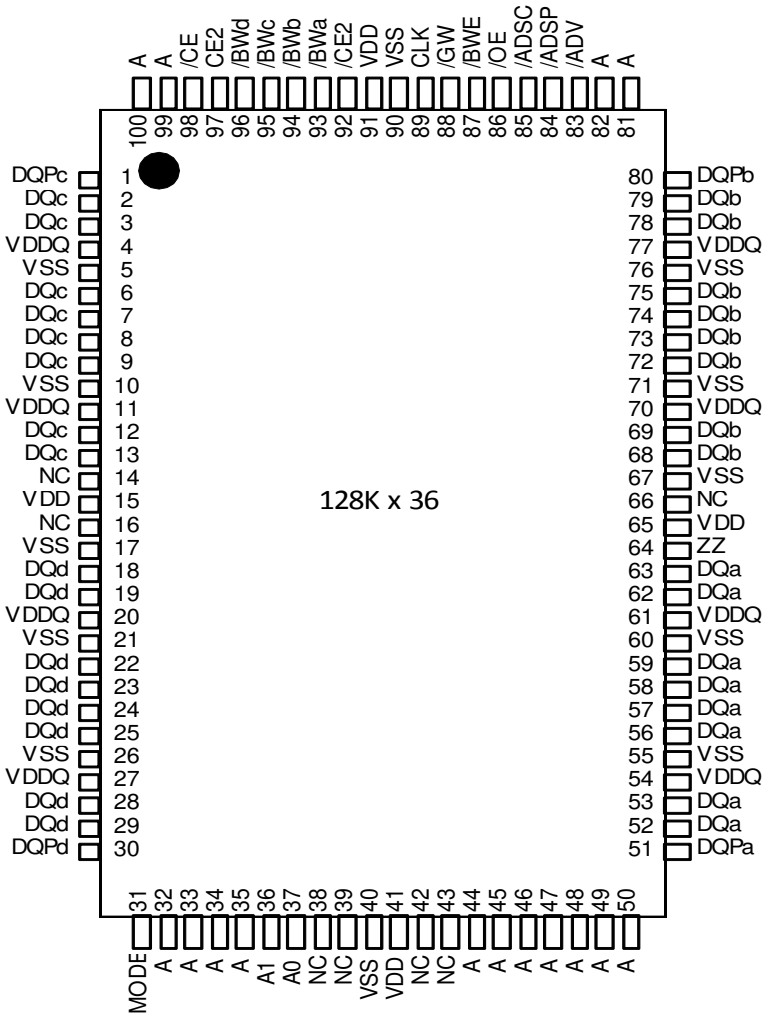
MODE	Burst Sequence Selection
/CE,CE2,/CE2	Synchronous Chip Enable
/BWE	Synchronous Byte Write Enable
/BWx (x=a-b)	Synchronous Byte Write Inputs
/GW	Synchronous Global Write Enable
/OE	Asynchronous Output Enable
DQx	Synchronous Data Inputs/Outputs
DQPx	Synchronous Parity Data I/O
TCK,TDI,TDO,TMS	JTAG Pins
ZZ	Asynchronous Power Sleep Mode
NC	No Connect
VDD	Power Supply
VDDQ	I/O Power Supply
VSS	Ground

128K x 36, 100PIN QFP (Top View)

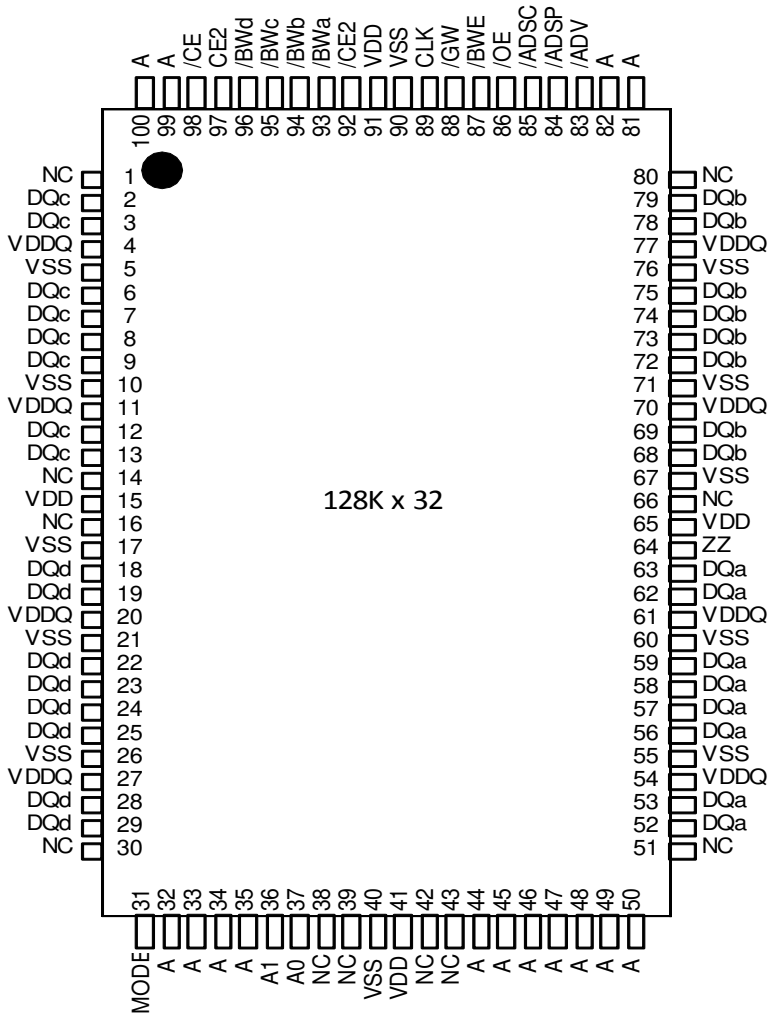


Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name	Symbol	Pin Name
CLK	Synchronous Clock	/GW	Synchronous Global Write Enable
A0,A1	Synchronous Burst Address Inputs	/OE	Asynchronous Output Enable
A	Synchronous Address Inputs	DQx	Synchronous Data Inputs/Outputs
/ADV	Synchronous Burst Address Advance	DQPx	Synchronous Parity Data I/O
/ADSP	Synchronous Address Status Processor	ZZ	Asynchronous Power Sleep Mode
/ADSC	Synchronous Address Status Controller	NC	No Connect
MODE	Burst Sequence Selection	VDD	Power Supply
/CE,CE2,/CE2	Synchronous Chip Enable	VDDQ	I/O Power Supply
/BWE	Synchronous Byte Write Enable	VSS	Ground
/BWx (x=a-d)	Synchronous Byte Write Inputs		

128K x 32, 100PIN QFP (Top View)

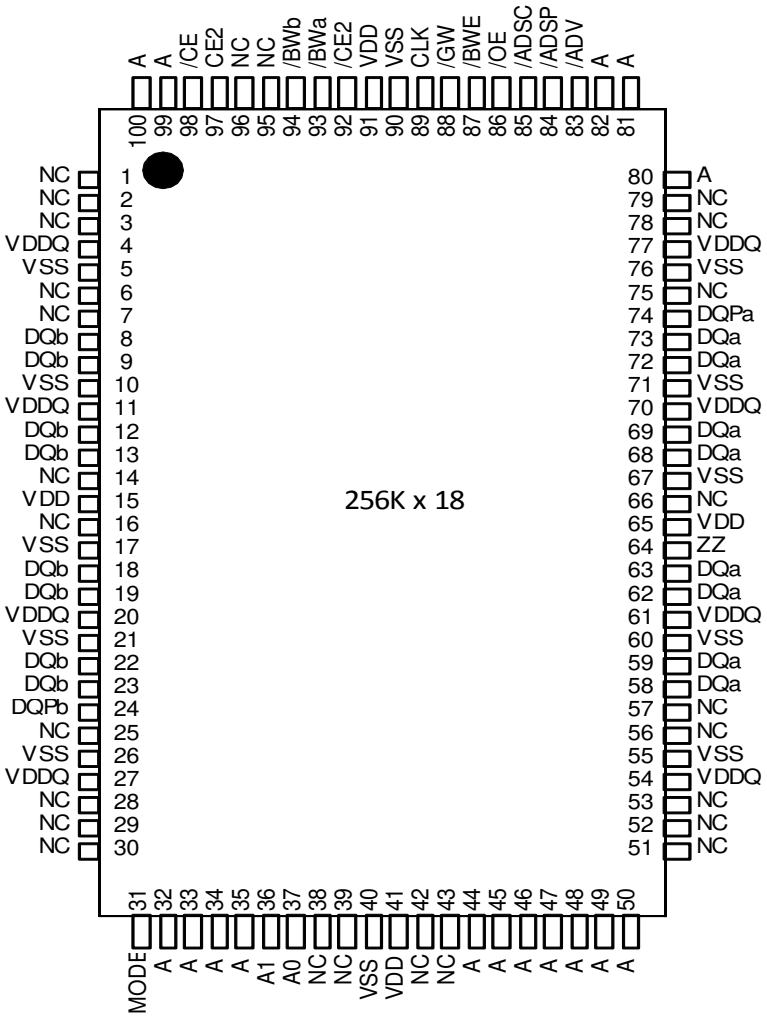


Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name	Symbol	Pin Name
CLK	Synchronous Clock	/BWx (x=a-d)	Synchronous Byte Write Inputs
A0,A1	Synchronous Burst Address Inputs	/GW	Synchronous Global Write Enable
A	Synchronous Address Inputs	/OE	Asynchronous Output Enable
/ADV	Synchronous Burst Address Advance	DQx	Synchronous Data Inputs/Outputs
/ADSP	Synchronous Address Status Processor	ZZ	Asynchronous Power Sleep Mode
/ADSC	Synchronous Address Status Controller	NC	No Connect
MODE	Burst Sequence Selection	VDD	Power Supply
/CE,CE2,/CE2	Synchronous Chip Enable	VDDQ	I/O Power Supply
/BWE	Synchronous Byte Write Enable	VSS	Ground

256K x 18, 100PIN QFP (Top View)



Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name	Symbol	Pin Name
CLK	Synchronous Clock	**/GW**	Synchronous Global Write Enable
A0,A1	Synchronous Burst Address Inputs	**/OE**	Asynchronous Output Enable
A	Synchronous Address Inputs	**DQx**	Synchronous Data Inputs/Outputs
/ADV	Synchronous Burst Address Advance	**DQPx**	Synchronous Parity Data I/O
/ADSP	Synchronous Address Status Processor	**ZZ**	Asynchronous Power Sleep Mode
/ADSC	Synchronous Address Status Controller	**NC**	No Connect
MODE	Burst Sequence Selection	**VDD**	Power Supply
/CE,CE2,/CE2	Synchronous Chip Enable	**VDDQ**	I/O Power Supply
/BWE	Synchronous Byte Write Enable	**VSS**	Ground
/BWx (x=a-b)	Synchronous Byte Write Inputs		

TRUTH TABLE

SYNCHRONOUS TRUTH TABLE

OPERATION	ADDRESS	/CE	/CE2	CE2	ZZ	ADSP	ADSC	ADV	WRITE	/OE	CLK	DQ
Deselect Cycle, Power-Down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
Snooze Mode, Power-Down	None	X	X	X	H	X	X	X	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
Write Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

NOTE:
1. X means “Don’t Care.” H means logic HIGH. L means logic LOW.
2. For WRITE, L means one or more byte write enable signals (/BWa-d) and /BWE are LOW or /GW is LOW. /WRITE = H for all /BWx, /BWE, /GW HIGH.
3. /BWa enables WRITEs to DQa’s and DQPa. /BWb enables WRITEs to DQb’s and DQPb. /BWc enables WRITEs to DQc’s and DQPc. /BWd enables WRITEs to DQd’s and DQPd. DQPa and DQPb are available on the x18 version. DQPa-DQPd are available on the x36 version.
4. All inputs except /OE and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, /OE must be HIGH before the input data setup time and held HIGH during the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. /ADSP LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and /BWE LOW or /GW LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

PARTIAL TRUTH TABLE

Operation	/GW	/BWE	/BWa	/BWb	/BWc	/BWd
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE BYTE a	H	L	L	H	H	H
WRITE BYTE b	H	L	H	L	H	H
WRITE BYTE c	H	L	H	H	L	H
WRITE BYTE d	H	L	H	H	H	L
WRITE ALL BYTEs	H	L	L	L	L	L
WRITE ALL BYTEs	L	X	X	X	X	X

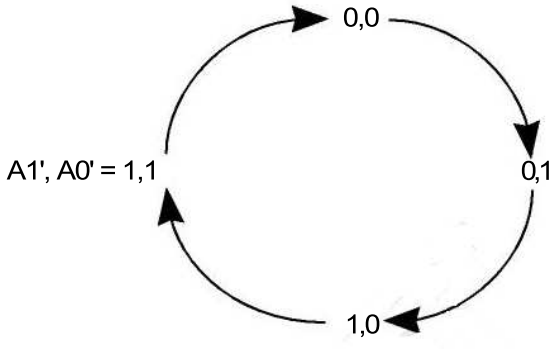
Notes:
1. X means "Don't Care".
2. All inputs in this table must beet setup and hold time around the rising edge of CLK.

ADDRESS SEQUENCE IN BURST MODE

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{dd} or NC)

External Address	1st Burst Address	2nd Burst Address	3rd Burst Address
A1 A0	A1 A0	A1 A0	A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = V_{ss})



Power Up Sequence

Vddq → Vdd[1] → I/O Pins[2]

Notes:
1. Vdd can be applied at the same time as Vddq
2. Applying I/O inputs is recommended after Vddq is stable. The inputs of the I/O pins can be applied at the same time as Vddq as long as Vih (level of I/O pins) is lower than Vddq.

ERROR DETECTION AND CORRECTION

- Independent ECC with Hamming code for each byte.
- Detect and correct one bit error per byte.
- Better reliability than parity code schemes that could detect error bit but NOT correct it.
- Backward compatible : Drop in replacement to current in industry standard devices without ECC.

ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LF Value	VF Value	Unit
T_{STG}	Storage Temperature	–65 to +150	–65 to +150	°C
P_D	Power Dissipation	1.6	1.6	W
I_{OUT}	Output Current (per I/O)	100	100	mA
V_{IN}, V_{OUT}	Voltage Relative to Vss for I/O Pins	–0.5 to V_{DDQ}+0.5	–0.3 to V_{DDQ} + 0.3	V
V_{IN}	Voltage Relative to Vss for Address and Control Inputs	–0.5 to V_{DD}+0.5	–0.3 to V_{DD} + 0.3	V
V_{DDQ}	Voltage on V_{DDQ} Supply Relative to Vss	–0.5 to V_{DD}	–0.3 to V_{DD}	V
V_{DD}	Voltage on V_{DD} Supply Relative to Vss	–0.5 to 4.6	–0.3 to 3.6	V

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Option	Range	VDD	VDDQ	Ambient Temperature
IS61LFXXXXX	Commercial	3.3V ± 5%	3.3V / 2.5V ± 5%	0°C to +70°C
	Industrial	3.3V ± 5%	3.3V / 2.5V ± 5%	-40°C to +85°C
IS61VFXXXXX	Commercial	2.5V ± 5%	2.5V ± 5%	0°C to +70°C
	Industrial	2.5V ± 5%	2.5V ± 5%	-40°C to +85°C
IS64LFXXXXX	Automotive	3.3V ± 5%	3.3V / 2.5V ± 5%	-40°C to +125°C
IS64VFXXXXX	Automotive	2.5V ± 5%	2.5V ± 5%	-40°C to +125°C

CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS (Over operating temperature range)

Symbol	Parameter	Test Conditions	3.3V		2.5V		Unit
			Min.	Max.	Min.	Max.	
Voh	Output HIGH Voltage	Ioh=-4.0 mA(3.3V)	2.4	—	2.0	—	V
		Ioh=–1.0 mA(2.5V)					
Vol	Output LOW Voltage	Iol=8.0 mA(3.3V)	—	0.4	—	0.4	V
		Iol=1.0 mA(2.5V)					
Vih	Input HIGH Voltage		2.0	Vdd+0.3	1.7	Vdd+0.3	V
Vil	Input LOW Voltage		–0.3	0.8	–0.3	0.7	V
Ili	Input Leakage Current	Vss≤Vin≤Vdd	–5	5	–5	5	µA
Ilo	Output Leakage Current	Vss≤Vout≤Vddq,/OE=Vih	–5	5	–5	5	µA

Notes:
1. All voltages referenced to ground.
2. Overshoot:
   3.3V and 2.5V: Vih (AC) ≤ Vdd + 1.5V (Pulse width less than tkc /2)
   1.8V: Vih (AC) ≤ Vdd + 0.5V (Pulse width less than tkc /2)
3. Undershoot:
   3.3V and 2.5V: Vil (AC) ≥ -1.5V (Pulse width less than tkc /2)
   1.8V: Vil (AC) ≥ -0.5V (Pulse width less than tkc /2)

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Temp. range	-6.5		-7.5		Unit
				MAX		MAX		
				x18	x36/32	x18	x36/32	
Icc	AC Operating, Supply Current	Device Selected, OE = Vih, ZZ ≤ Vil,All Inputs ≤ 0.2V or ≥ Vdd – 0.2V,Cycle Time ≥ tkc min.	Com.	175	175	155	155	mA
			Ind.	180	180	160	160	
			Auto	190	190	175	175	
Isb	Standby Current TTL Input	Device Deselected,Vdd = Max.,All Inputs ≤ Vil or ≥ Vih,ZZ ≤ Vil, f = Max.	Com.	100	100	100	100	mA
			Ind.	110	110	110	110	
			Auto	130	130	130	130	
Isb1	Standby Current CMOS Input	Device Deselected,Vdd = Max.,Vin ≤ Vss + 0.2V or ≥Vdd – 0.2V,f = 0	Com.	80	80	80	80	mA
			Ind.	85	85	85	85	
			Auto	100	100	100	100	

Note:
1. MODE pin has an internal pullup and should be tied to Vdd or Vss . It exhibits ±100µA maximum leakage current when tied to ≤Vss+0.2V or ≥Vdd–0.2V.

CAPACITANCE

Symbol	Parameter	Conditions	Max.	Unit
Cin	Input Capacitance	Vin = 0V	6	pF
Cout	Input/Output Capacitance	Vout = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: Ta = 25°C, f = 1 MHz, Vdd = 3.3V.

READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-6.5		-7.5		Unit
		Min.	Max.	Min.	Max.	
f_{MAX}	Clock Frequency	—	133	—	117	MHz
t_{KC}	Cycle Time	7.5	—	8.5	—	ns
t_{KH}	Clock High Time	2.2	—	2.5	—	ns
t_{KL}	Clock Low Time	2.2	—	2.5	—	ns
t_{KQ}	Clock Access Time	—	6.5	—	7.5	ns
t_{KQX}(2)	Clock High to Output Invalid	2.5	—	2.5	—	ns
t_{KQLZ}(2,3)	Clock High to Output Low-Z	2.5	—	2.5	—	ns
t_{KQHZ}(2,3)	Clock High to Output High-Z	—	3.8	—	4.0	ns
t_{OEQ}	Output Enable to Output Valid	—	3.2	—	3.4	ns
t_{OELZ}(2,3)	Output Enable to Output Low-Z	0	—	0	—	ns
t_{OEHZ}(2,3)	Output Disable to Output High-Z	—	3.5	—	3.5	ns
t_{AS}	Address Setup Time	1.5	—	1.5	—	ns
t_{SS}	Address Status Setup Time	1.5	—	1.5	—	ns
t_{WS}	Read/Write Setup Time	1.5	—	1.5	—	ns
t_{CES}	Chip Enable Setup Time	1.5	—	1.5	—	ns
t_{SE}	Clock Enable Setup Time	1.5	—	1.5	—	ns
t_{ADVS}	Address Advance Setup Time	1.5	—	1.5	—	ns
t_{DS}	Data Setup Time	1.5	—	1.5	—	ns
t_{AH}	Address Hold Time	0.5	—	0.5	—	ns
t_{SH}	Address Status Hold Time	0.5	—	0.5	—	ns
t_{HE}	Clock Enable Hold Time	0.5	—	0.5	—	ns
t_{WH}	Write Hold Time	0.5	—	0.5	—	ns
t_{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	ns
t_{ADVH}	Address Advance Hold Time	0.5	—	0.5	—	ns
t_{DH}	Data Hold Time	0.5	—	0.5	—	ns
t_{POWER}(4)	V_{DD} (typical) to First Access	1	—	1	—	ms

Notes:
1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.
4. t_{POWER} is the time that the power needs to be supplied above V_{DD} (min) initially before READ or WRITE operation can be initiated.

3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
V_{TT}	1.5V
V_{LOAD}	3.3V
R1, R2	317Ω, 351Ω
Output Load	See Figures 1 and 2

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.25V
V_{TT}	1.25V
V_{LOAD}	2.5V
R1, R2	1667Ω, 1538Ω
Output Load	See Figures 1 and 2

I/O OUTPUT LOAD EQUIVALENT

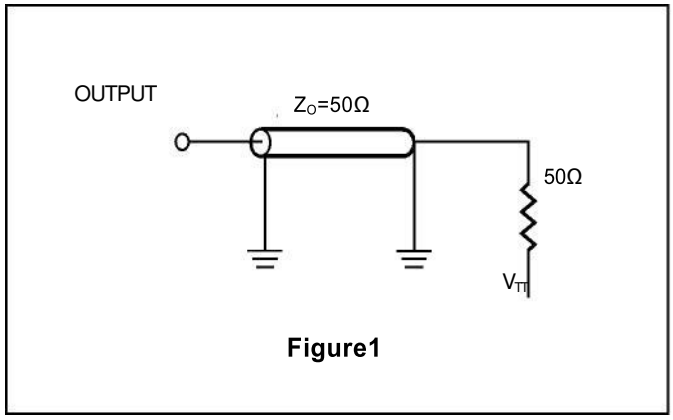


Figure1

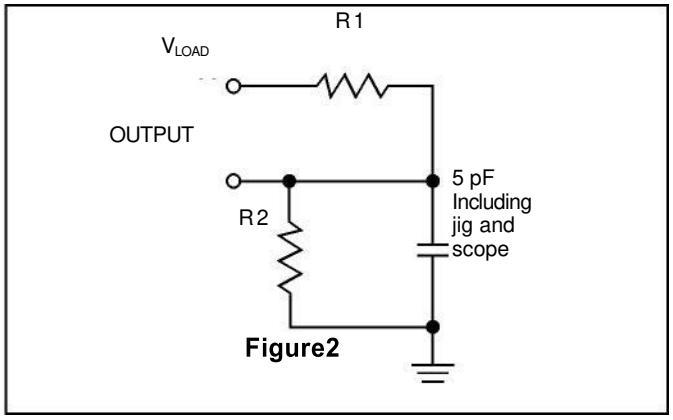
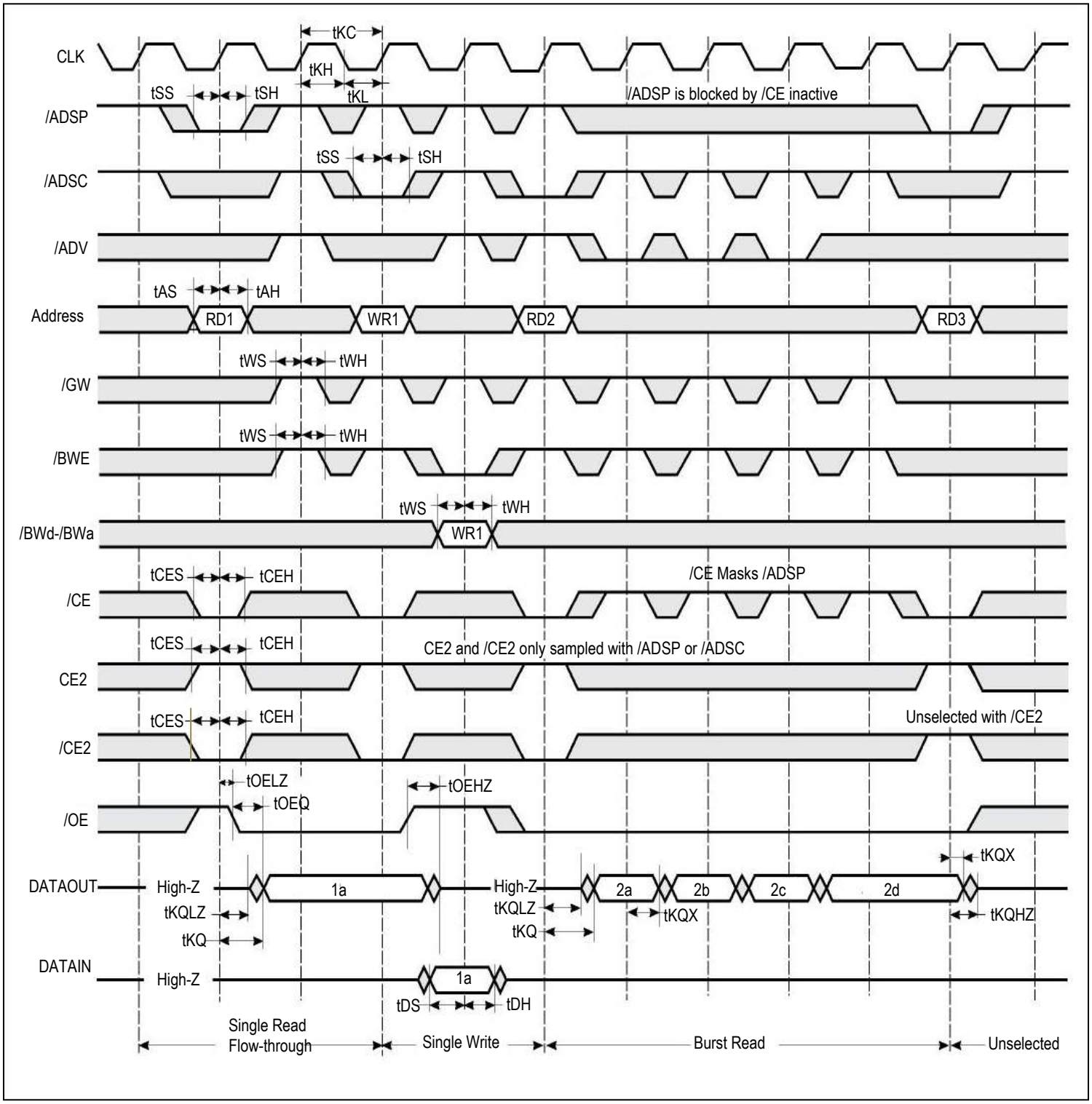
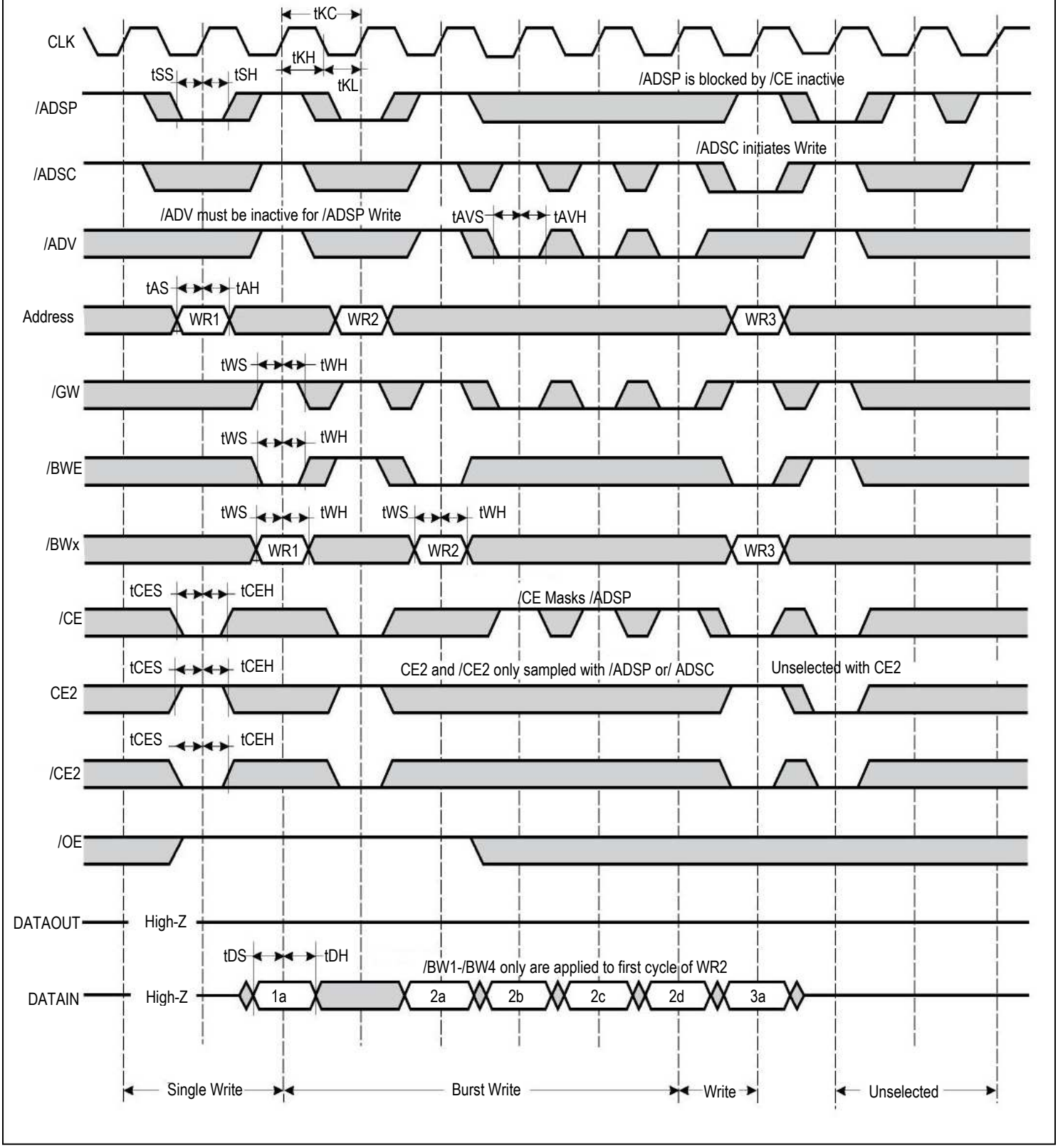


Figure2

READ/WRITE CYCLE TIMING



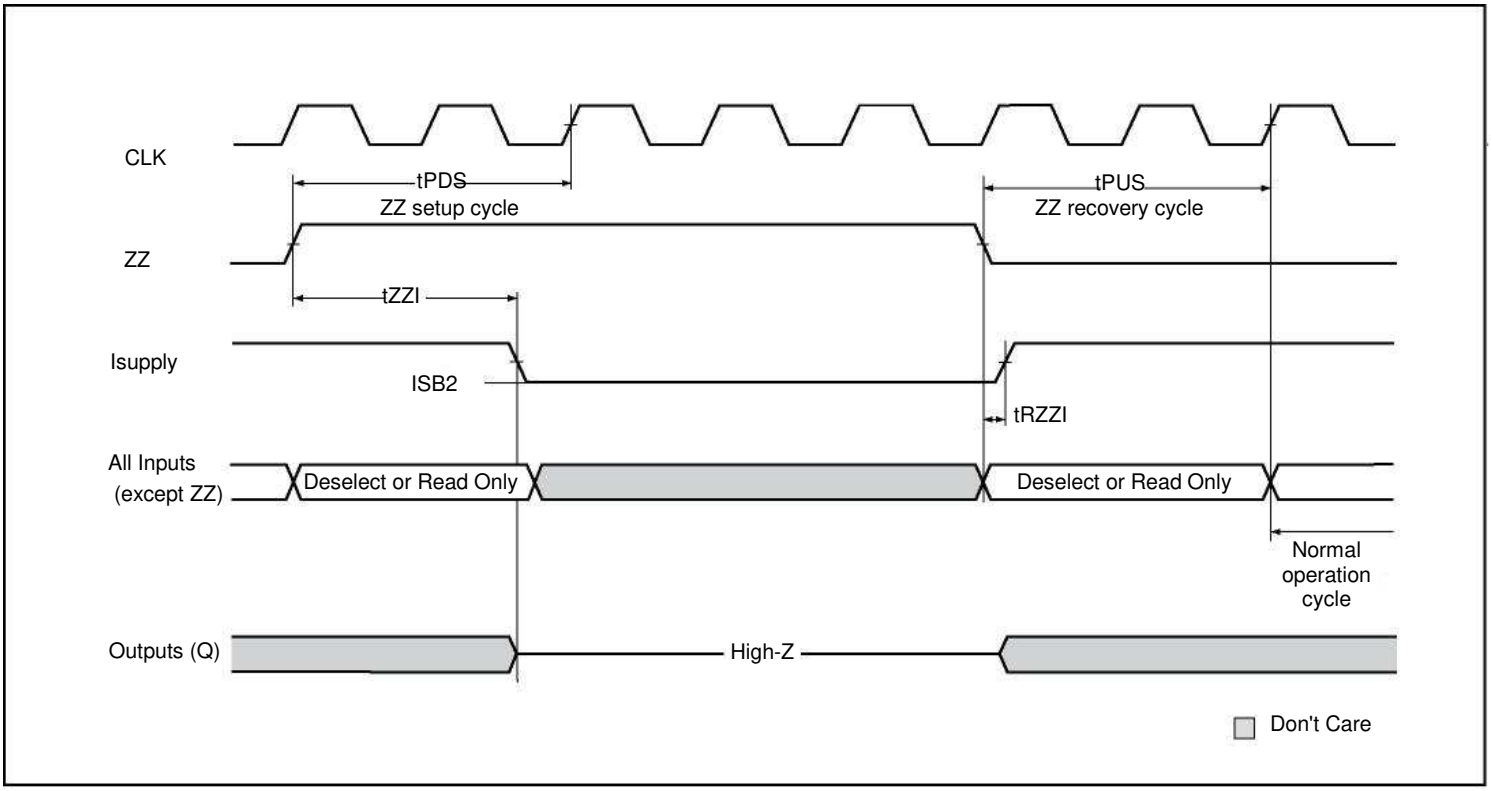
WRITE CYCLE TIMING



SNOOZE MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Temperature Range	Min.	Max.	Unit
Isb2	Current during SNOOZE MODE	ZZ ≥ Vih	Com.	—	35	mA
			Ind.	—	40	
			Auto.	—	60	
tpds	ZZ active to input ignored		—	—	2	cycle
tpus	ZZ inactive to input sampled		—	2	—	cycle
tzzi	ZZ active to SNOOZE current		—	—	2	cycle
trzzi	ZZ inactive to exit SNOOZE current		—	0	—	ns

SLEEP MODE TIMING



IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE Standard 1149.1, the SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

The TAP controller has a standard 16-state machine that resets internally on power-up. Therefore, a TRST signal is not required

Disabling the JTAG feature

The SRAM can operate without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (VSS) to prevent clocking of the device. TDI and TMS are internally pulled up and may be left disconnected. They may alternately be connected to VDD through a pull-up resistor. TDO should be left disconnected. On power-up, the device will come up in a reset state, which will not interfere with device operation.

Test Access Port Signal List:

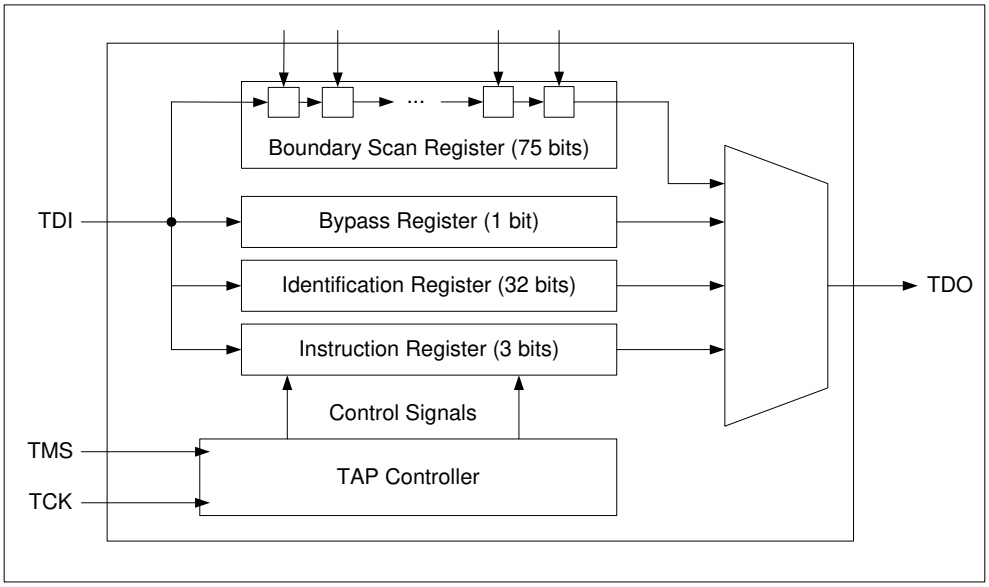
1. Test Clock (TCK)
This signal uses VDD as a power supply. The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

2. Test Mode Select (TMS)
This signal uses VDD as a power supply. The TMS input is used to send commands to the TAP controller and is sampled on the rising edge of TCK.

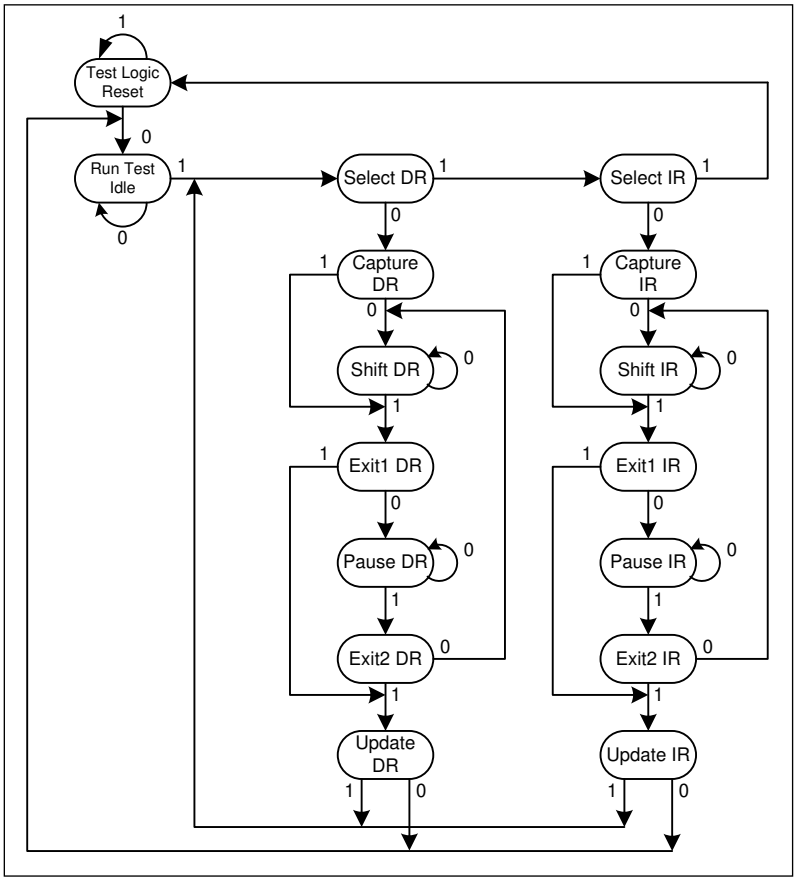
3. Test Data-In (TDI)
This signal uses VDD as a power supply. The TDI input is used to serially input test instructions and information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is connected to the most significant bit (MSB) of any register. For more information regarding instruction register loading, please see the TAP Controller State Diagram.

4. Test Data-Out (TDO)
This signal uses VDDQ as a power supply. The TDO output ball is used to serially clock test instructions and data out from the registers. The TDO output driver is only active during the Shift-IR and Shift-DR TAP controller states. In all other states, the TDO pin is in a High-Z state. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. For more information, please see the TAP Controller State Diagram.

TAP Controller State and Block Diagram



TAP Controller State Machine



Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. RESET may be performed while the SRAM is operating and does not affect its operation. At power-up, the TAP is internally reset to ensure that TDO comes up in a high-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK and output on the TDO pin on the falling edge of TCK.

1. Instruction Register

This register is loaded during the update-IR state of the TAP controller. At power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section. When the TAP controller is in the capture-IR state, the two LSBs are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

2. Bypass Register

The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

3. Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. Several balls are also included in the scan register to reserved balls. The boundary scan register is loaded with the contents of the SRAM Input and Output ring when the TAP controller is in the capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the shift-DR state. Each bit corresponds to one of the balls on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

4. Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the shift-DR state.

Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	75

TAP Instruction Set

Many instructions are possible with an eight-bit instruction register and all valid combinations are listed in the TAP Instruction Code Table. All other instruction codes that are not listed on this table are reserved and should not be used. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted from the instruction register through the TDI and TDO pins. To execute an instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

1. EXTEST
The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output balls are used to apply a test vector, while those at input balls capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the update-IR state of EXTEST, the output driver is turned on, and the PRELOAD data is driven onto the output balls.

2. IDCODE
The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

3. SAMPLE Z
If the SAMPLE-Z instruction is loaded in the instruction register, all SRAM outputs are forced to an inactive drive state (high-Z), moving the TAP controller into the capture-DR state loads the data in the SRAMs input into the boundary scan register, and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.

4. SAMPLE/PRELOAD
When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register. The user must be aware that the TAP controller clock can only operate at a frequency up to 50 MHz, while the SRAM clock operates significantly faster. Because there is a large difference between the clock frequencies, it is possible that during the capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition. This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible. To ensure that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time. The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/ PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register. Once the data is captured, it is possible to shift out the data by putting the TAP into the shift-DR state. This places the boundary scan register between the TDI and TDO balls.

6. BYPASS
When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

7. PRIVATE
Do not use these instructions. They are reserved for future use and engineering mode.

JTAG TAP DC ELECTRICAL CHARACTERISTICS (V_{DDQ}=3.3V Operating Range)

Parameter	Symbol	Min	Max	Units	Notes
JTAG Input High Voltage	V_{IH1}	2.0	V_{DD}+0.3	V	
JTAG Input Low Voltage	V_{IL1}	–0.3	0.8	V	
JTAG Output High Voltage	V_{OH1}	2.4	-	V	$\|I_{OH1}\|$=2mA
JTAG Output Low Voltage	V_{OL1}	-	0.4	V	I_{OL1}=2mA
JTAG Output High Voltage	V_{OH2}	2.9	-	V	$\|I_{OH2}\|$=100uA
JTAG Output Low Voltage	V_{OL2}	-	0.2	V	I_{OL2}=100uA
JTAG Input Load Current	I_X	-10	+10	uA	0 ≤ Vin ≤ V_{DD}

Notes:
1. All voltages referenced to VSS (GND); All JTAG inputs and outputs are LVTTL-compatible.

JTAG TAP DC ELECTRICAL CHARACTERISTICS (V_{DDQ}=2.5V Operating Range)

Parameter	Symbol	Min	Max	Units	Notes
JTAG Input High Voltage	V_{IH1}	1.7	V_{DD}+0.3	V	
JTAG Input Low Voltage	V_{IL1}	–0.3	0.7	V	
JTAG Output High Voltage	V_{OH1}	2.0	-	V	$\|I_{OH1}\|$=2mA
JTAG Output Low Voltage	V_{OL1}	-	0.4	V	I_{OL1}=2mA
JTAG Output High Voltage	V_{OH2}	2.1	-	V	$\|I_{OH2}\|$=100uA
JTAG Output Low Voltage	V_{OL2}	-	0.2	V	I_{OL2}=100uA
JTAG Input Load Current	I_X	-10	+10	uA	0 ≤ Vin ≤ V_{DD}

Notes:
2. All voltages referenced to VSS (GND); All JTAG inputs and outputs are LVTTL-compatible.

JTAG AC Test Conditions

(Over the Operating Temperature Range)

Parameter	Symbol	2.5V Option	3.3V Option	Units
Input Pulse High Level	V_{IH1}	2.5	3.0	V
Input Pulse Low Level	V_{IL1}	0	0	V
Input rise and fall time	T_{R1}	1.5	1.5	ns
Test load termination supply voltage	V_{REF}	1.25	1.5	V
Input and Output Timing Reference Level	V_{REF}	1.25	1.5	V

TAP Output Load Equivalent