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IS61(64)LPS102436B/IS61(64)VPS/VVPS102436B
IS61(64)LPS204818B/IS61(64)VPS/VVPS204818B

1M x 36, 1M x 32, 2M x 18
36 Mb SYNCHRONOUS PIPELINED, SINGLE CYCLE DESELECT STATIC RAM

SEPTEMBER 2015

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Burst sequence control using MODE input
- Three chip enable option for simple depth expansion and address pipelining
- Common data inputs and data outputs
- Auto Power-down during deselect
- Single cycle deselect
- Snooze MODE for reduced-power standby
- JTAG Boundary Scan for BGA package
- Power Supply

  LPS: V_{DD} 3.3V ($\pm$ 5%), V_{DDQ} 3.3V/2.5V ($\pm$ 5%)

  VPS: V_{DD} 2.5V ($\pm$ 5%), V_{DDQ} 2.5V ($\pm$ 5%)

  VVPS: V_{DD} 1.8V ($\pm$ 5%), V_{DDQ} 1.8V ($\pm$ 5%)
- JEDEC 100-Pin QFP, 119-ball BGA, and 165-ball BGA packages
- Lead-free available

DESCRIPTION

The 36Mb product family features high-speed, low-power synchronous static RAMs designed to provide burstable, high-performance memory for communication and networking applications. The IS61LPS/VPS102436B and IS64LPS102436B are organized as 1,048,476 words by 36 bits. The IS61LPS102432B is organized as 1,048,476 words by 32 bits. The IS61LPS/VPS204818B is organized as 2,096,952 words by 18 bits. Fabricated with *ISSI*'s advanced CMOS technology, the device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. The byte write operation is performed by using the byte write enable ($\overline{\text{BWE}}$) input combined with one or more individual byte write signals ($\overline{\text{BWx}}$). In addition, Global Write ($\overline{\text{GW}}$) is available for writing all bytes at one time, regardless of the byte write controls.

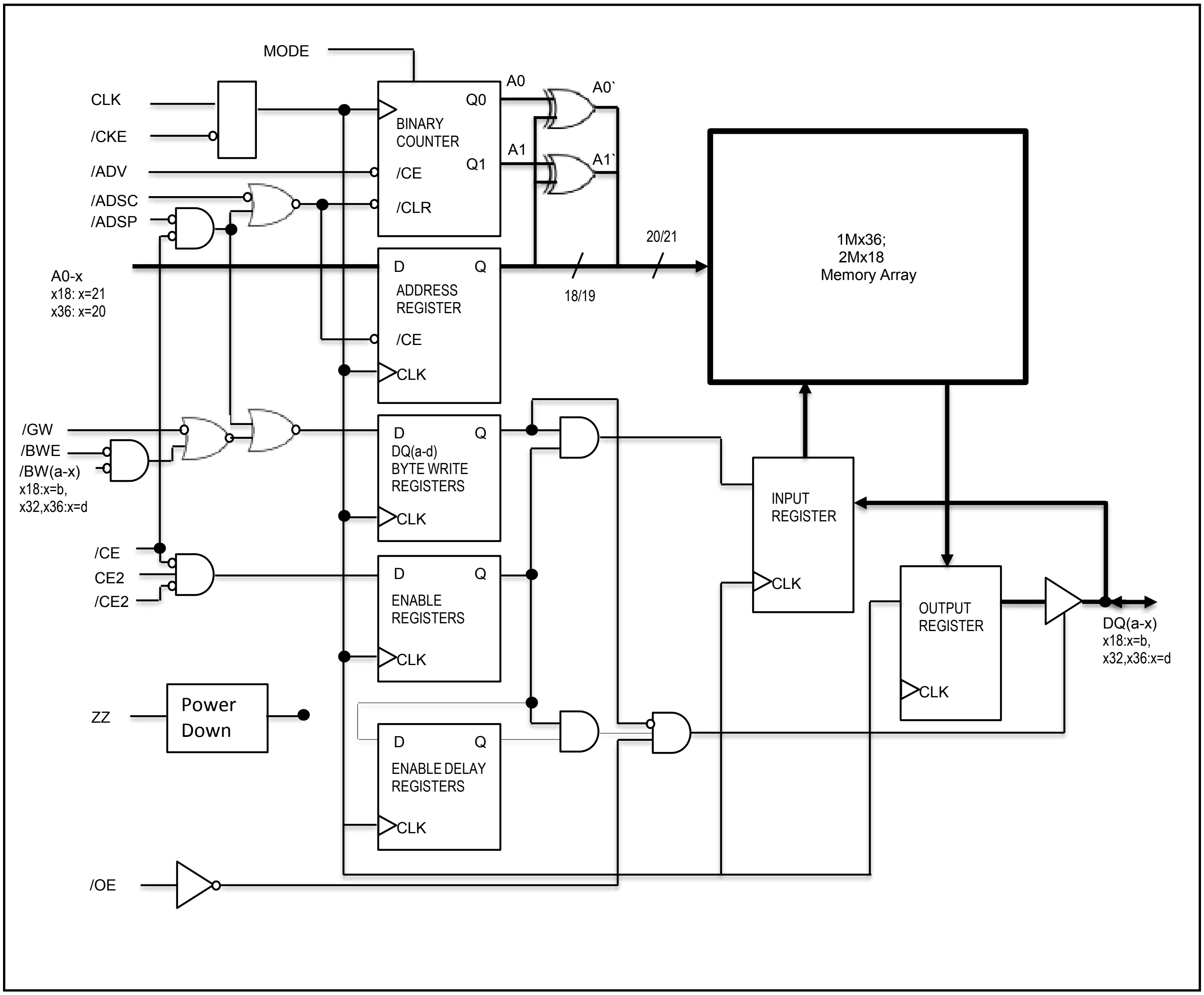
Bursts can be initiated with either $\overline{\text{ADSP}}$ (Address Status Processor) or $\overline{\text{ADSC}}$ (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the $\overline{\text{ADV}}$ (burst address advance) input pin.

The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

FAST ACCESS TIME

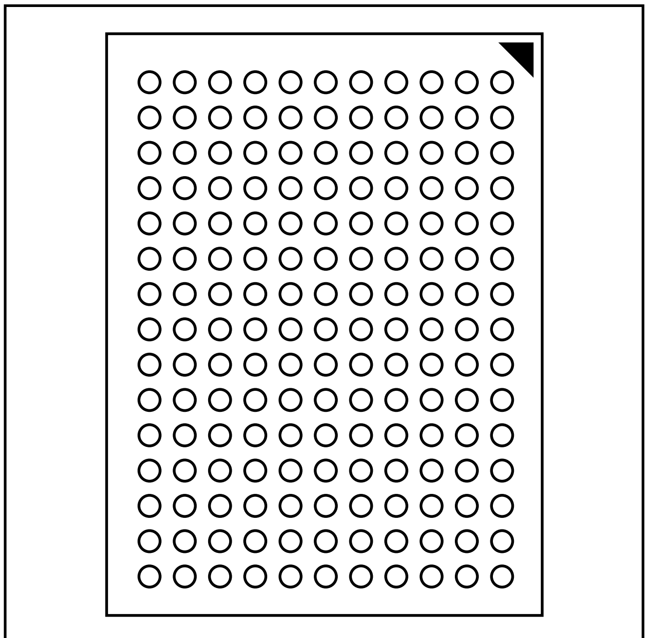
Symbol	Parameter	250	200	166	Units
t_{KQ}	Clock Access Time	2.8	3.1	3.8	ns
t_{KC}	Cycle Time	4	5	6	ns
	Frequency	250	200	166	MHz

BLOCK DIAGRAM



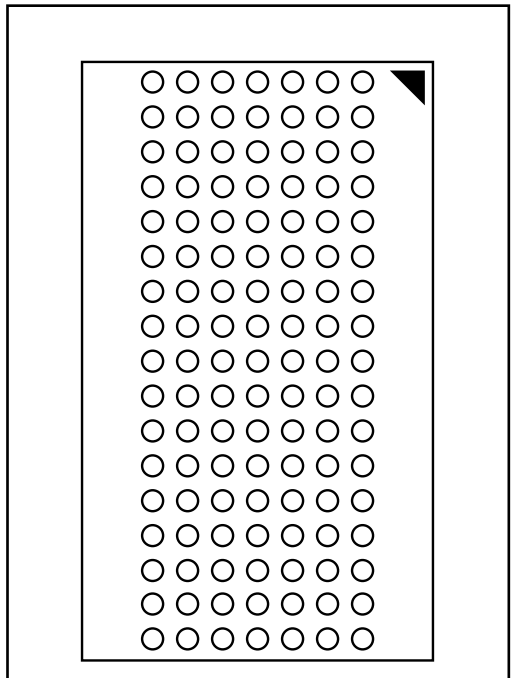
165-PIN BGA

165-Ball, 13x15 mm BGA



119-PIN BGA

119-Ball, 14x22 mm BGA



119 BGA PACKAGE PIN CONFIGURATION-1M x 36 (TOP VIEW)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	A	A	$\overline{ADSC}$	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	DQPc	Vss	NC	Vss	DQPb	DQb
E	DQc	DQc	Vss	$\overline{CE}$	Vss	DQb	DQb
F	V_{DDQ}	DQc	Vss	$\overline{OE}$	Vss	DQb	V_{DDQ}
G	DQc	DQc	$\overline{BWc}$	$\overline{ADV}$	$\overline{BWb}$	DQb	DQb
H	DQc	DQc	Vss	$\overline{GW}$	Vss	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	Vss	CLK	Vss	DQa	DQa
L	DQd	DQd	$\overline{BWd}$	NC	$\overline{BWa}$	DQa	DQa
M	V_{DDQ}	DQd	Vss	$\overline{BWE}$	Vss	DQa	V_{DDQ}
N	DQd	DQd	Vss	A_1*	Vss	DQa	DQa
P	DQd	DQPd	Vss	A_0*	Vss	DQPa	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	NC	A	A	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: * A_0 and A_1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name
A	Synchronous Address Inputs
A0, A1	Synchronous Burst Address Inputs
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{ADSP}$	Synchronous Address Status Processor
$\overline{ADSC}$	Synchronous Address Status Controller
$\overline{GW}$	Synchronous Global Write Enable
CLK	Synchronous Clock
$\overline{CE}$, CE2	Synchronous Chip Select
$\overline{BWa}$-$\overline{BWd}$	Synchronous Byte Write Controls
$\overline{BWE}$	Synchronous Byte Write Enable

Symbol	Pin Name
$\overline{OE}$	Asynchronous Output Enable
ZZ	Asynchronous Power Sleep Mode
MODE	Burst Sequence Selection
TCK, TDO TMS, TDI	JTAG Pins
NC	No Connect
DQa-DQd	Synchronous Data Inputs/Outputs
DQPa-DQPd	Synchronous Parity Data Inputs/Outputs
V_{DD}	Power Supply
V_{DDQ}	I/O Power Supply
Vss	Ground

119 BGA PACKAGE PIN CONFIGURATION

2Mx18 (TOP VIEW)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{\text{ADSP}}$	A	A	V_{DDQ}
B	NC	A	A	$\overline{\text{ADSC}}$	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQb	NC	Vss	NC	Vss	DQPa	NC
E	NC	DQb	Vss	$\overline{\text{CE}}$	Vss	NC	DQa
F	V_{DDQ}	NC	Vss	$\overline{\text{OE}}$	Vss	DQa	V_{DDQ}
G	NC	DQb	$\overline{\text{BWb}}$	$\overline{\text{ADV}}$	Vss	NC	DQa
H	DQb	NC	Vss	$\overline{\text{GW}}$	Vss	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	Vss	CLK	Vss	NC	DQa
L	DQb	NC	Vss	NC	$\overline{\text{BWa}}$	DQa	NC
M	V_{DDQ}	DQb	Vss	$\overline{\text{BWE}}$	Vss	NC	V_{DDQ}
N	DQb	NC	Vss	A_1*	Vss	DQa	NC
P	NC	DQPb	Vss	A_0*	Vss	NC	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	A	A	A	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: * A_0 and A_1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name
A	Synchronous Address Inputs
A0, A1	Synchronous Burst Address Inputs
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$\overline{\text{GW}}$	Synchronous Global Write Enable
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$\overline{\text{CE}}$, CE2	Synchronous Chip Select
$\overline{\text{BWa}}$-$\overline{\text{BWb}}$	Synchronous Byte Write Controls
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TCK, TDO TMS, TDI	JTAG Pins
NC	No Connect
DQa-DQb	Synchronous Data Inputs/Outputs
DQPa-DQPb	Synchronous Parity Data Inputs/Outputs
V_{DD}	Power Supply
V_{DDQ}	I/O Power Supply
Vss	Ground

165 BGA PACKAGE PIN CONFIGURATION

1M x 36 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}$	$\overline{BWc}$	$\overline{BWb}$	$\overline{CE2}$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC	A	CE2	$\overline{BWd}$	$\overline{BWa}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC
C	DQPc	NC	V_{DDQ}	Vss	Vss	Vss	Vss	Vss	V_{DDQ}	NC	DQPb
D	DQc	DQc	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQb	DQb
E	DQc	DQc	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQb	DQb
F	DQc	DQc	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQb	DQb
G	DQc	DQc	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQb	DQb
H	NC	NC	NC	V_{DD}	Vss	Vss	Vss	V_{DD}	NC	NC	ZZ
J	DQd	DQd	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	DQa
K	DQd	DQd	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	DQa
L	DQd	DQd	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	DQa
M	DQd	DQd	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	DQa
N	DQPd	NC	V_{DDQ}	Vss	NC	A	NC	Vss	V_{DDQ}	NC	DQPa
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	A
R	MODE	A	A	A	TMS	A0*	TCK	A	A	A	A

Note: * A_0 and A_1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name
A	Synchronous Address Inputs
A0, A1	Synchronous Burst Address Inputs
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$\overline{ADSC}$	Synchronous Address Status Controller
$\overline{GW}$	Synchronous Global Write Enable
CLK	Synchronous Clock
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Select
$\overline{BWa}$-$\overline{BWd}$	Synchronous Byte Write Controls

Symbol	Pin Name
$\overline{BWE}$	Synchronous Byte Write Enable
$\overline{OE}$	Asynchronous Output Enable
ZZ	Asynchronous Power Sleep Mode
MODE	Burst Sequence Selection
TCK, TDO TMS, TDI	JTAG Pins
NC	No Connect
DQa-DQd	Synchronous Data Inputs/Outputs
DQPa-DQPd	Synchronous Parity Data Inputs/Outputs
V_{DD}	Power Supply
V_{DDQ}	I/O Power Supply
Vss	Ground

165 BGA PACKAGE PIN CONFIGURATION

2M x 18 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}$	$\overline{BWb}$	NC	$\overline{CE2}$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	A
B	NC	A	CE2	NC	$\overline{BWa}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC
C	NC	NC	V_{DDQ}	Vss	Vss	Vss	Vss	Vss	V_{DDQ}	NC	DQPa
D	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
E	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
F	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
G	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
H	NC	NC	NC	V_{DD}	Vss	Vss	Vss	V_{DD}	NC	NC	ZZ
J	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
K	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
L	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
M	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
N	DQPb	NC	V_{DDQ}	Vss	NC	A	NC	Vss	V_{DDQ}	NC	NC
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	A
R	MODE	A	A	A	TMS	A0*	TCK	A	A	A	A

Note: * A_0 and A_1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

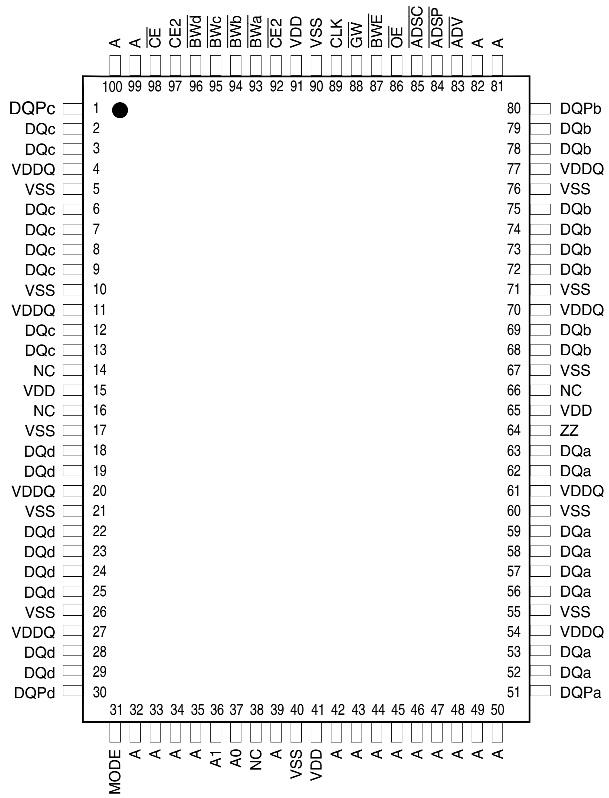
PIN DESCRIPTIONS

Symbol	Pin Name
A	Synchronous Address Inputs
A0, A1	Synchronous Burst Address Inputs
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{ADSP}$	Synchronous Address Status Processor
$\overline{ADSC}$	Synchronous Address Status Controller
$\overline{GW}$	Synchronous Global Write Enable
CLK	Synchronous Clock
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Select
$\overline{BWa}$-$\overline{BWb}$	Synchronous Byte Write Controls

Symbol	Pin Name
$\overline{BWE}$	Synchronous Byte Write Enable
$\overline{OE}$	Asynchronous Output Enable
ZZ	Asynchronous Power Sleep Mode
MODE	Burst Sequence Selection
TCK, TDO TMS, TDI	JTAG Pins
NC	No Connect
DQa-DQb	Synchronous Data Inputs/Outputs
DQPa-DQPb	Synchronous Parity Data Inputs/Outputs
V_{DD}	3.3V/2.5V Power Supply
V_{DDQ}	I/O Power Supply
Vss	Ground

PIN CONFIGURATION

100-PIN QFP (1M x 36)



(3 Chip-Enable option)

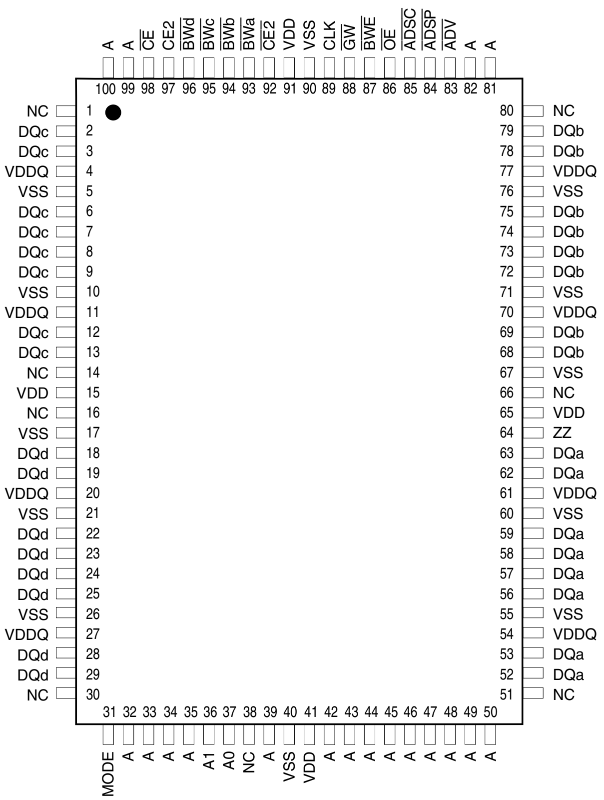
PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWd}$	Synchronous Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
CLK	Synchronous Clock

DQa-DQd	Synchronous Data Inputs/Outputs
DQPa-DQPd	Synchronous Parity Data Inputs/Outputs
$\overline{GW}$	Synchronous Global Write Enable
MODE	Burst Sequence Mode Selection
$\overline{OE}$	Asynchronous Output Enable
V_{DD}	Power Supply
V_{DDQ}	I/O Power Supply
Vss	Ground
ZZ	Asynchronous Snooze Enable

PIN CONFIGURATION

100-PIN QFP (1M x 32)



(3 Chip-Enable option)

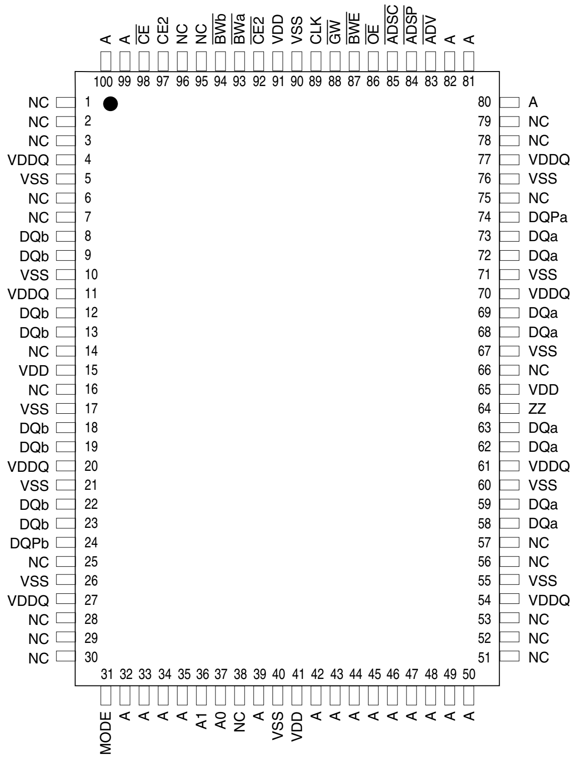
PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWd}$	Synchronous Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
CLK	Synchronous Clock

DQa-DQd	Synchronous Data Inputs/Outputs
$\overline{GW}$	Synchronous Global Write Enable
MODE	Burst Sequence Mode Selection
$\overline{OE}$	Asynchronous Output Enable
V_{DD}	Power Supply
V_{DDQ}	I/O Power Supply
Vss	Ground
ZZ	Asynchronous Snooze Enable

PIN CONFIGURATION

100-PIN QFP (2M x 18)



(3 Chip-Enable Option)

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
$\overline{\text{ADSC}}$	Synchronous Controller Address Status
$\overline{\text{ADSP}}$	Synchronous Processor Address Status
$\overline{\text{ADV}}$	Synchronous Burst Address Advance
$\overline{\text{BWa}}$-$\overline{\text{BWb}}$	Synchronous Byte Write Enable
$\overline{\text{BWE}}$	Synchronous Byte Write Enable
$\overline{\text{CE}}$, CE2, $\overline{\text{CE2}}$	Synchronous Chip Enable
CLK	Synchronous Clock
DQa-DQb	Synchronous Data Inputs/Outputs
DQPa-DQPb	Synchronous Parity Data Inputs/Outputs
$\overline{\text{GW}}$	Synchronous Global Write Enable
MODE	Burst Sequence Mode Selection
$\overline{\text{OE}}$	Asynchronous Output Enable
V_{DD}	Power Supply
V_{DDQ}	I/O Power Supply
Vss	Ground
ZZ	Asynchronous Snooze Enable

TRUTH TABLE(1-8)

OPERATION	ADDRESS	$\overline{CE}$	$\overline{CE2}$	CE2	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect Cycle, Power-Down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
Snooze Mode, Power-Down	None	X	X	X	H	X	X	X	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
Write Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

NOTE:
1. X means "Don't Care." H means logic HIGH. L means logic LOW.
2. For $\overline{WRITE}$, L means one or more byte write enable signals ($\overline{BWa\text{-}d}$) and $\overline{BWE}$ are LOW or $\overline{GW}$ is LOW. $\overline{WRITE}$ = H for all $\overline{BWx}$, $\overline{BWE}$, $\overline{GW}$ HIGH.
3. $\overline{BWa}$ enables WRITEs to DQa's and DQPa. $\overline{BWb}$ enables WRITEs to DQb's and DQPb. $\overline{BWc}$ enables WRITEs to DQc's and DQPc. $\overline{BWd}$ enables WRITEs to DQd's and DQPd. DQPa and DQPb are available on the x18 version. DQPa-DQPd are available on the x36 version.
4. All inputs except $\overline{OE}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, $\overline{OE}$ must be HIGH before the input data setup time and held HIGH during the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

PARTIAL TRUTH TABLE

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte 1	H	L	L	H	H	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

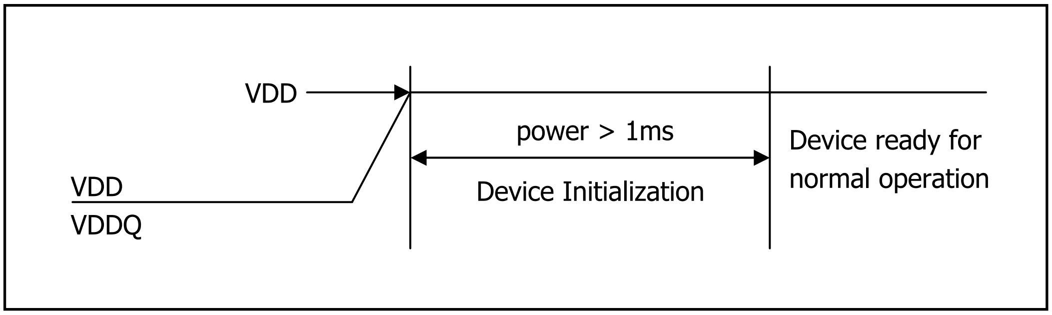
POWER UP SEQUENCE

$V_{DDQ} \rightarrow V_{DD}$[1] $\rightarrow$ I/O Pins[2]

Notes:

1. V_{DD} can be applied at the same time as V_{DDQ}
2. Applying I/O inputs is recommended after V_{DDQ} is ready. The inputs of the I/O pins can be applied at the same time as V_{DDQ} provided V_{IH} (level of I/O pins) is lower than V_{DDQ}.

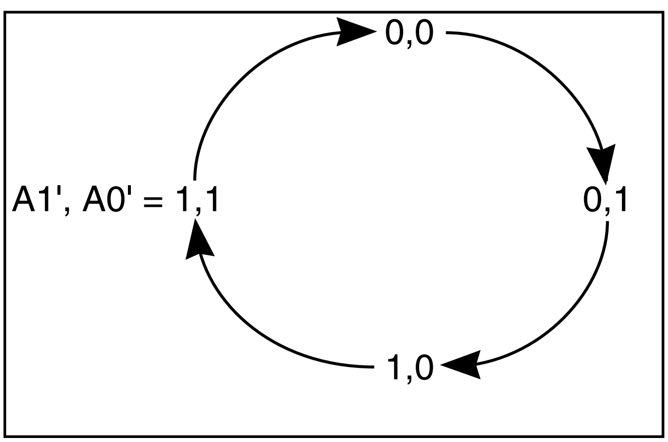
POWER-UP INITIALIZATION TIMING



INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = VSS)



ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	LPS Value	VPS/VVPS Value	Unit
T_{STG}	Storage Temperature	–55 to +150	–55 to +150	°C
P_D	Power Dissipation	1.6	1.6	W
I_{OUT}	Output Current (per I/O)	100	100	mA
V_{IN}, V_{OUT}	Voltage Relative to Vss for I/O Pins	–0.5 to V_{DDQ} + 0.5	–0.5 to V_{DDQ} + 0.3	V
V_{IN}	Voltage Relative to Vss for for Address and Control Inputs	–0.5 to V_{DD} + 0.5	–0.5 to V_{DD} + 0.3	V
V_{DD}	Voltage on V_{DD} Supply Relative to Vss	–0.5 to V_{DD} + 0.5	–0.3 to V_{DD} + 0.3	V

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE (IS61/64LPSXXXXX)

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V ± 5%	3.3V / 2.5V ± 5%
Industrial	–40°C to +85°C	3.3V ± 5%	3.3V / 2.5V ± 5%
Automotive	–40°C to +125°C	3.3V ± 5%	3.3V / 2.5V ± 5%

OPERATING RANGE (IS61/64VPSXXXXX)

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	2.5V ± 5%	2.5V ± 5%
Industrial	–40°C to +85°C	2.5V ± 5%	2.5V ± 5%
Automotive	–40°C to +125°C	2.5V ± 5%	2.5V ± 5%

OPERATING RANGE (IS61/64VVPSXXXXX)

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	1.8V ± 5%	1.8V ± 5%
Industrial	–40°C to +85°C	1.8V ± 5%	1.8V ± 5%
Automotive	–40°C to +125°C	1.8V ± 5%	1.8V ± 5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range) [1, 2, 3]

Symbol	Parameter	Test Conditions	3.3V Min.	3.3V Max.	2.5V Min.	2.5V Max.	1.8V Min.	1.8V Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –4.0 mA (3.3V) I_{OH} = –1.0 mA (2.5V, 1.8V)	2.4	—	2.0	—	V_{DDQ} - 0.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA (3.3V) I_{OL} = 1.0 mA (2.5V, 1.8V)	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{DD} + 0.3	1.7	V_{DD} + 0.3	0.6V_{DD}	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		-0.3	0.8	-0.3	0.7	-0.3	0.3V_{DD}	V
I_{LI}	Input Leakage Current Input Current of MODE Input Current of ZZ	$V_{SS} \leq V_{IN} \leq V_{DD}$(1,4) $V_{SS} \leq V_{IN} \leq V_{DD}$(5) $V_{SS} \leq V_{IN} \leq V_{DD}$(6)	-5 -30 -5	5 5 30	-5 -30 -5	5 5 30	-5 -30 -5	5 5 30	μA
I_{LO}	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{DDQ}$, $\overline{OE}$ = V_{IH}	-5	5	-5	5	-5	5	μA

Notes:
1. All voltages referenced to ground.
2. Overshoot:
   3.3V and 2.5V: V_{IH} (AC) ≤ V_{DD} + 1.5V (Pulse width less than t_{KC} /2)
   1.8V: V_{IH} (AC) ≤ V_{DD} + 0.5V (Pulse width less than t_{KC} /2)
3. Undershoot:
   3.3V and 2.5V: V_{IL} (AC) ≥ -1.5V (Pulse width less than t_{KC} /2)
   1.8V: V_{IL} (AC) ≥ -0.5V (Pulse width less than t_{KC} /2)
4. Except MODE and ZZ
5. MODE is connected to pull-up resister internally.
6. ZZ is connected to pull-down resister internally.

POWER SUPPLY CHARACTERISTICS(1) (Over Operating Range)

Symbol	Parameter	Test Conditions	Temp. range	-250 MAX x18	-250 MAX x36	-200 MAX x18	-200 MAX x36	-166 MAX x18	-166 MAX x36	Unit
I_{CC}	AC Operating Supply Current	Device Selected, $\overline{OE}$ = V_{IH}, ZZ ≤ V_{IL}, All Inputs ≤ 0.2V or ≥ V_{DD} – 0.2V, Cycle Time ≥ t_{KC} min.	Com. Ind. Auto	400 450 -	400 450 -	350 400 500	350 400 500	320 350 450	320 350 450	mA
I_{SB}	Standby Current TTL Input	Device Deselected, V_{DD} = Max., All Inputs ≤ V_{IL} or ≥ V_{IH}, ZZ ≤ V_{IL}, f = Max.	Com. Ind. Auto	200 220 -	200 220 -	200 220 350	200 220 350	200 220 350	200 220 350	mA
I_{SBI}	Standby Current CMOS Input	Device Deselected, V_{DD} = Max., $V_{IN} \leq V_{SS}$ + 0.2V or ≥V_{DD} – 0.2V f = 0	Com. Ind. Auto	180 200 -	180 200 -	180 200 320	180 200 320	180 200 320	180 200 320	mA

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Refe rence Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

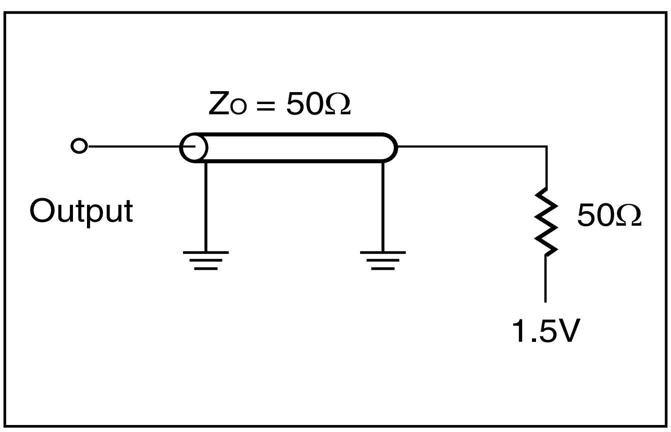


Figure 1

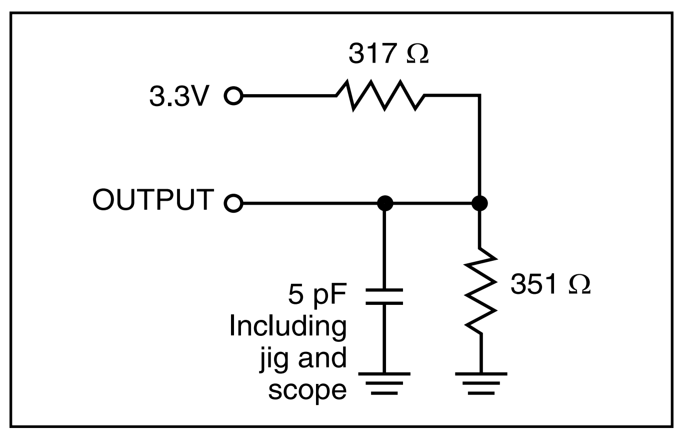


Figure 2

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.25V
Output Load	See Figures 3 and 4

2.5 I/O OUTPUT LOAD EQUIVALENT

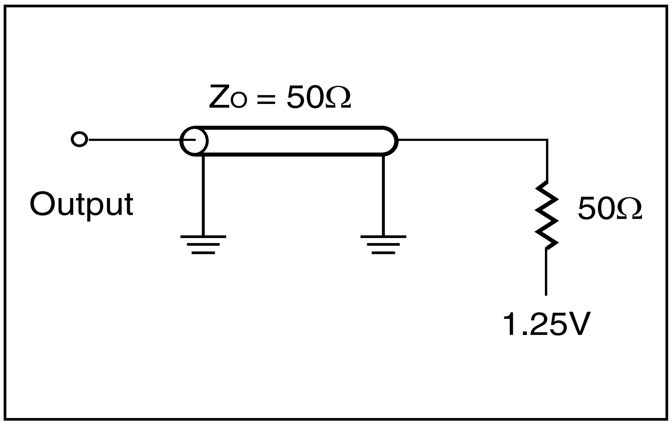


Figure 3

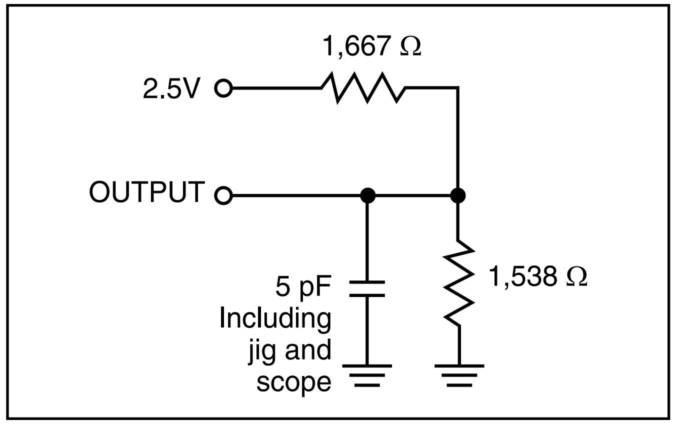


Figure 4

1.8V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 1.8V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	0.9V
Output Load	See Figures 5 and 6

1.8 I/O OUTPUT LOAD EQUIVALENT

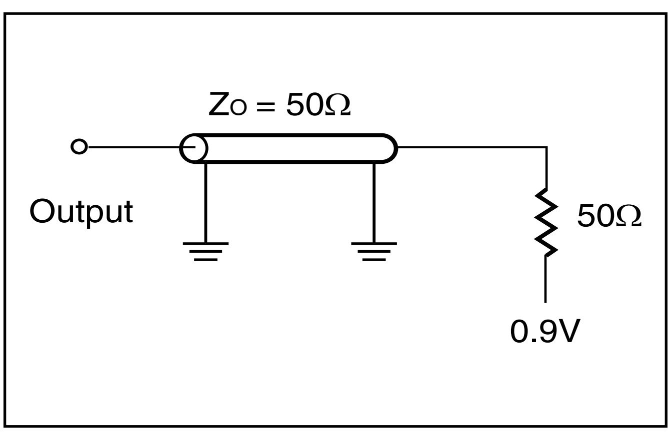


Figure 5

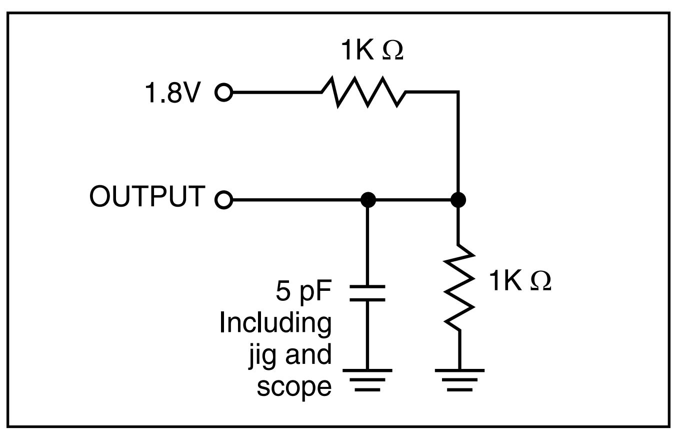


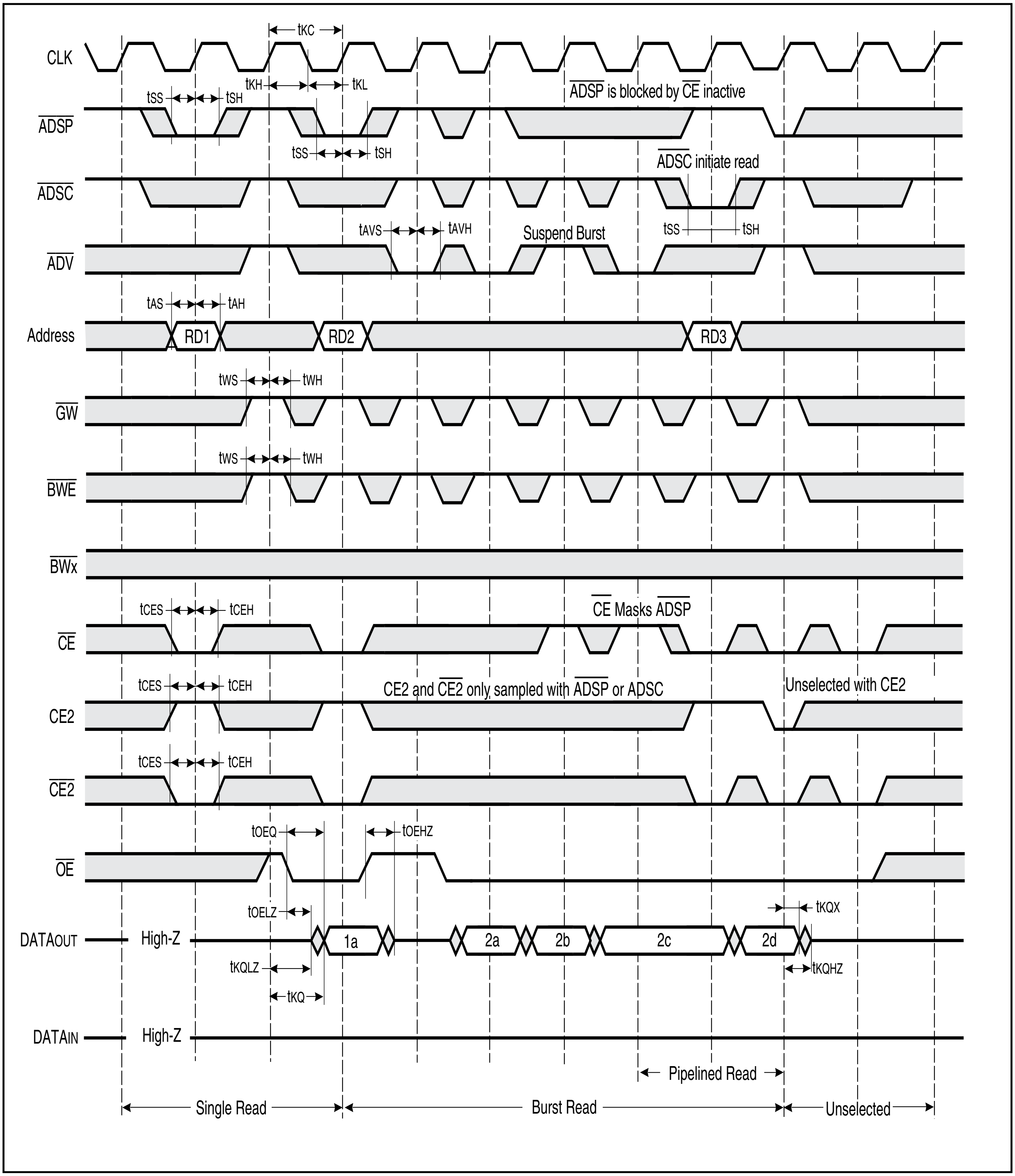
Figure 6

READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

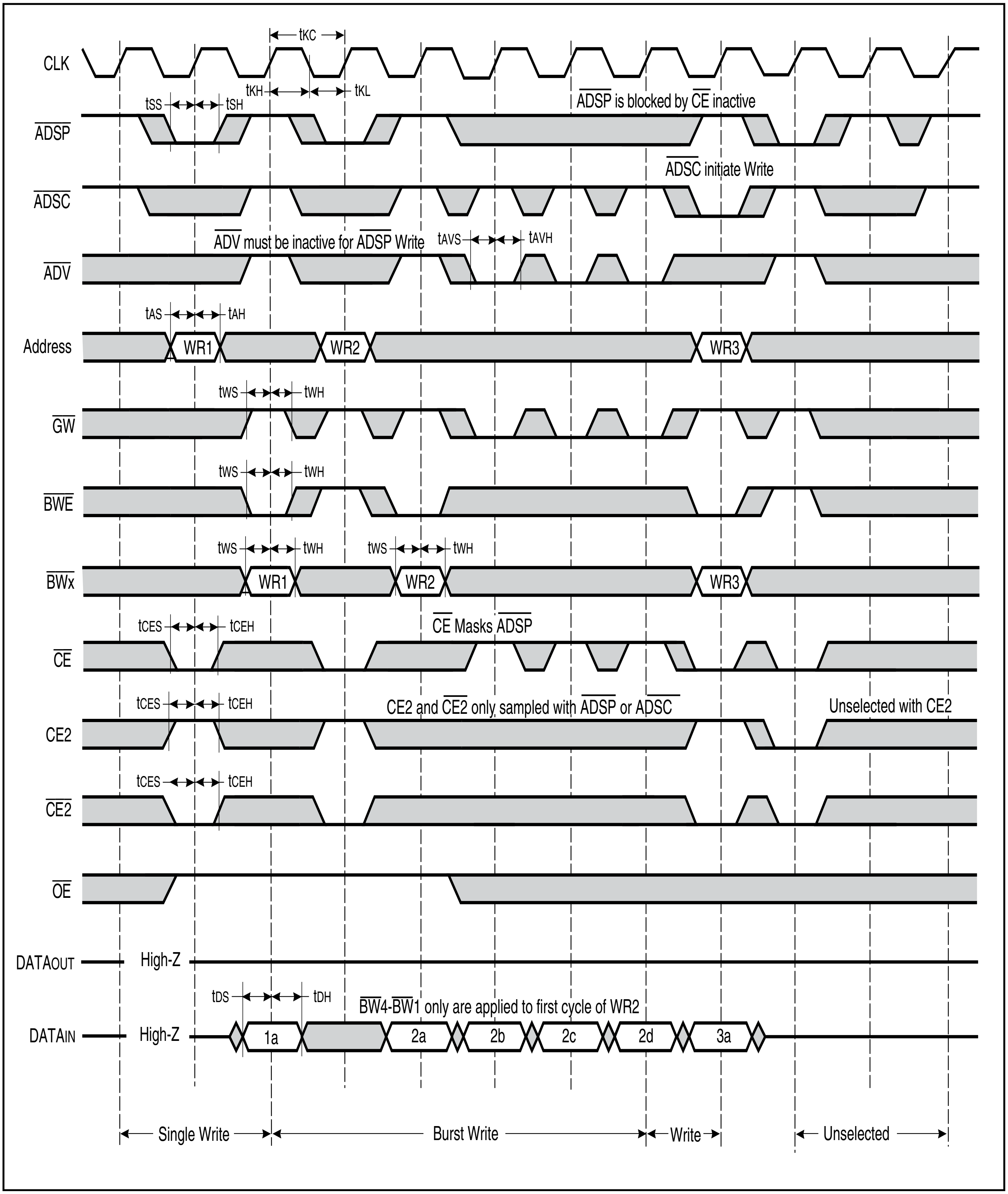
Symbol	Parameter	-250 Min.	-250 Max.	-200 Min.	-200 Max.	-166 Min.	-166 Max.	Unit
f_{MAX}	Clock Frequency	—	250	—	200	—	166	MHz
t_{KC}	Cycle Time	4.0	—	5	—	6	—	ns
t_{KH}	Clock High Time	1.7	—	2	—	2.4	—	ns
t_{KL}	Clock Low Time	1.7	—	2	—	2.3	—	ns
t_{KQ}	Clock Access Time	—	2.8	—	3.1	—	3.8	ns
t_{KQX}(2)	Clock High to Output Invalid	0.8	—	1.5	—	1.5	—	ns
t_{KQLZ}(2,3)	Clock High to Output Low-Z	0.8	—	1	—	1.5	—	ns
t_{KQHZ}(2,3)	Clock High to Output High-Z	—	2.8	—	3.1	—	3.8	ns
t_{OEQ}	Output Enable to Output Valid	—	2.8	—	3.1	—	3.8	ns
t_{OELZ}(2,3)	Output Enable to Output Low-Z	0	—	0	—	0	—	ns
t_{OEHZ}(2,3)	Output Disable to Output High-Z	—	2.8	—	3.1	—	3.8	ns
t_{AS}	Address Setup Time	1.4	—	1.4	—	1.5	—	ns
t_{SS}	Address Status Setup Time	1.4	—	1.4	—	1.5	—	ns
t_{WS}	Read/Write Setup Time	1.4	—	1.4	—	1.5	—	ns
t_{CES}	Chip Enable Setup Time	1.4	—	1.4	—	1.5	—	ns
t_{AVS}	Address Advance Setup Time	1.4	—	1.4	—	1.5	—	ns
t_{DS}	Data Setup Time	1.4	—	1.4	—	1.5	—	ns
t_{AH}	Address Hold Time	0.4	—	0.4	—	0.5	—	ns
t_{SH}	Address Status Hold Time	0.4	—	0.4	—	0.5	—	ns
t_{WH}	Write Hold Time	0.4	—	0.4	—	0.5	—	ns
t_{CEH}	Chip Enable Hold Time	0.4	—	0.4	—	0.5	—	ns
t_{AVH}	Address Advance Hold Time	0.4	—	0.4	—	0.5	—	ns
t_{DH}	Data Hold Time	0.4	—	0.4	—	0.5	—	ns
t_{POWER}(4)	V_{DD} (typical) to First Access	1	—	1	—	1	—	ms

Note:
1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.
4. t_{POWER} is the time that the power needs to be supplied above V_{DD} (min) initially before READ or WRITE operation can be initiated.

READ CYCLE TIMING



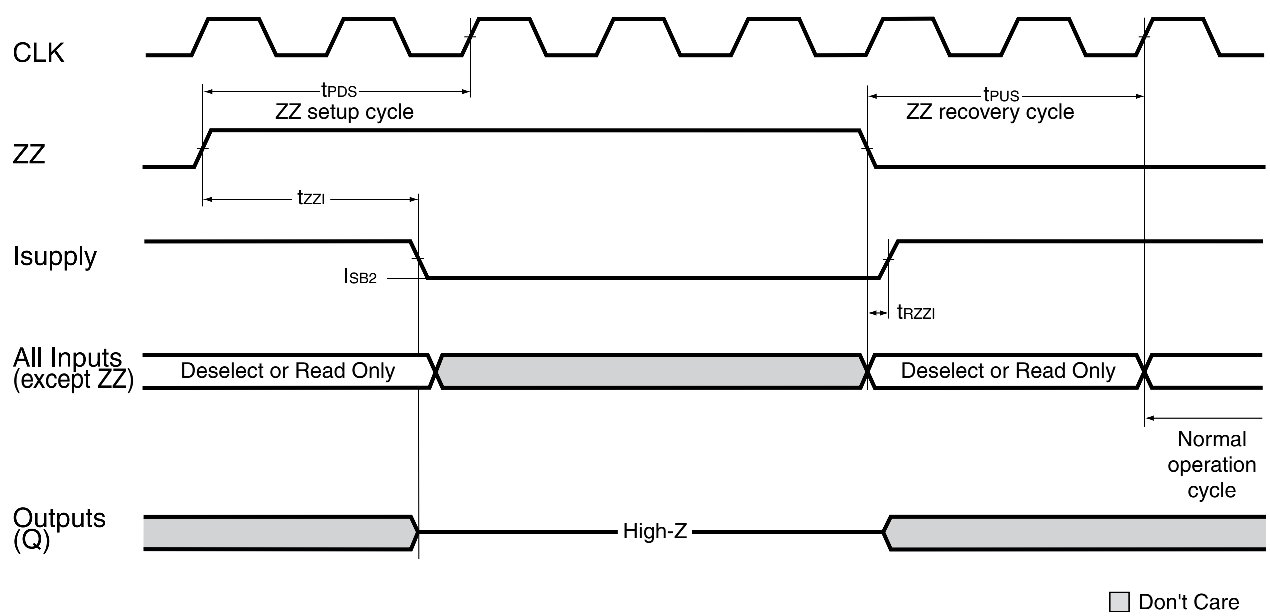
WRITE CYCLE TIMING



SNOOZE MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Temperature Range	Min.	Max.	Unit
I_{SB2}	Current during SNOOZE MODE	ZZ ≥ V_{DD} - 0.2V	Com. Ind. Auto.	— — —	120 130 250	mA
t_{PDS}	ZZ active to input ignored			—	2	cycle
t_{PUS}	ZZ inactive to input sampled			2	—	cycle
t_{ZZI}	ZZ active to SNOOZE current			—	2	cycle
t_{RZZI}	ZZ inactive to exit SNOOZE current			0	—	ns

SNOOZE MODE TIMING



IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

The serial boundary scan Test Access Port (TAP) is only available in the BGA package. (The QFP package not available.) This port operates in accordance with IEEE Standard 1149.1-1900, but does not include all functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because they place added delay in the critical speed path of the SRAM. The TAP controller operates in a manner that does not conflict with the performance of other devices using 1149.1 fully compliant TAPs.

DISABLING THE JTAG FEATURE

The SRAM can operate without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (Vss) to prevent clocking of the device. TDI and TMS are internally pulled up and may be disconnected. They may alternately be connected to VDD through a pull-up resistor. TDO should be left disconnected. On power-up, the device will start in a reset state which will not interfere with the device operation.

TEST ACCESS PORT (TAP) - TEST CLOCK

The test clock is only used with the TAP controller. All inputs are captured on the rising edge of TCK and outputs are driven from the falling edge of TCK.

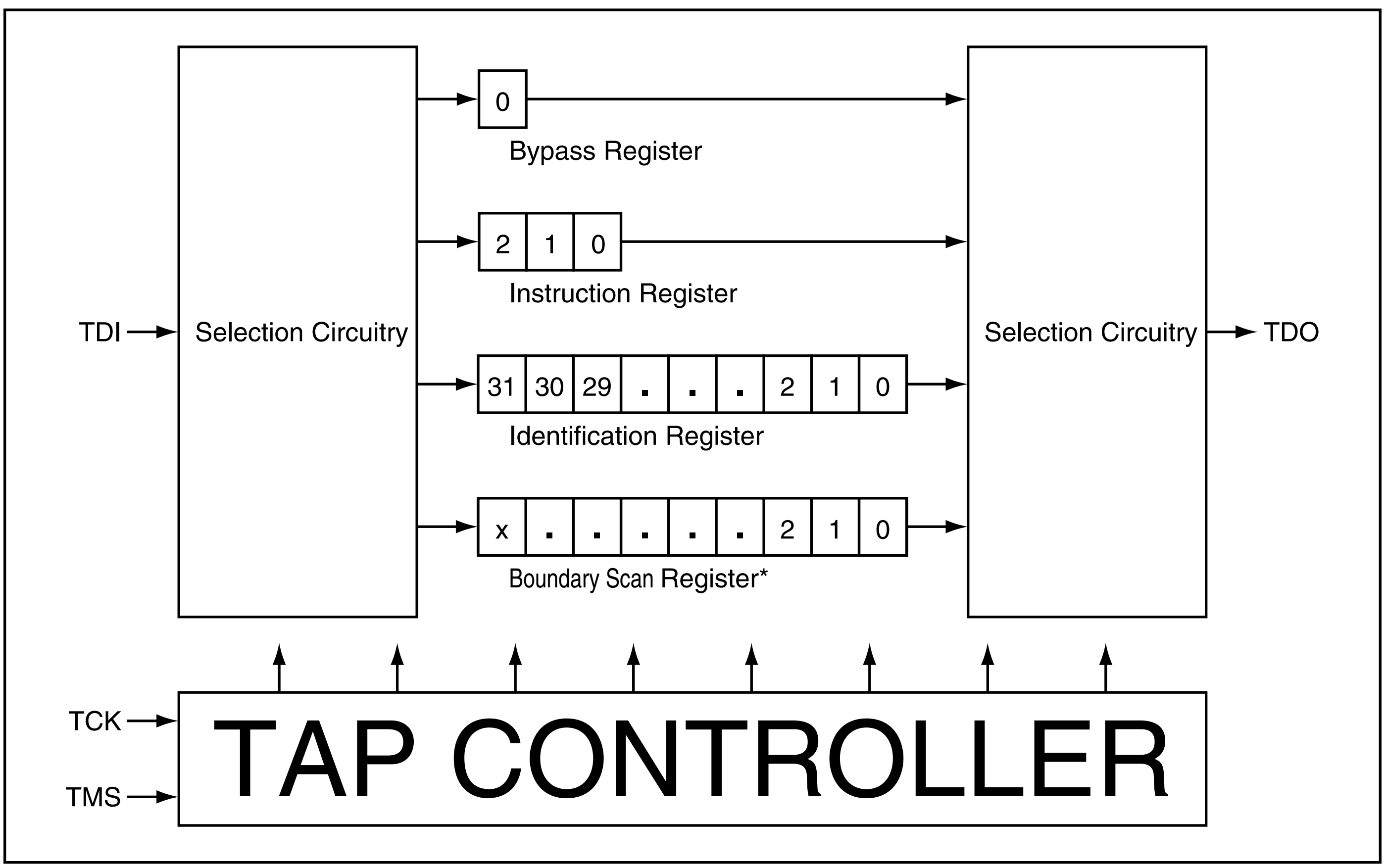
TEST MODE SELECT (TMS)

The TMS input is used to send commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left disconnected if the TAP is not used. The pin is internally pulled up, resulting in a logic HIGH level.

TEST DATA-IN (TDI)

The TDI pin is used to serially input information to the registers and can be connected to the input of any register. The register between TDI and TDO is chosen by the instruction loaded into the TAP instruction register. For information on instruction register loading, see the TAP Controller State Diagram. TDI is internally pulled up and can be disconnected if the TAP is unused in an application. TDI is connected to the Most Significant Bit (MSB) on any register.

TAP CONTROLLER BLOCK DIAGRAM



TEST DATA OUT (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending on the current state of the TAP state machine (see TAP Controller State Diagram). The output changes on the falling edge of TCK and TDO is connected to the Least Significant Bit (LSB) of any register.

PERFORMING A TAP RESET

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. RESET may be performed while the SRAM is operating and does not affect its operation. At power-up, the TAP is internally reset to ensure that TDO comes up in a high-Z state.

TAP REGISTERS

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK and output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins. (See TAP Controller Block Diagram) At power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as previously described.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The x36 configuration has a 75-bit-long register and the x18 configuration also has a 75-bit-long register. The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE-Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Scan Register Sizes

Register Name	Bit Size (x18)	Bit Size (x36)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan	75	75

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded to the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has vendor code and other information described in the Identification Register Definitions table.

IDENTIFICATION REGISTER DEFINITIONS

Instruction Field	Description	1M x 36	2M x 18
Revision Number (31:28)	Reserved for version number.	xxxx	xxxx
Device Depth (27:23)	Defines depth of SRAM. 1M or 2M	01001	01010
Device Width (22:18)	Defines width of the SRAM. x36 or x18	00100	00011
ISSI Device ID (17:12)	Reserved for future use.	xxxxx	xxxxx
ISSI JEDEC ID (11:1)	Allows unique identification of SRAM vendor.	00001010101	00001010101
ID Register Presence (0)	Indicate the presence of an ID register.	1	1

TAP INSTRUCTION SET

Eight instructions are possible with the three-bit instruction register and all combinations are listed in the Instruction Code table. Three instructions are listed as RESERVED and should not be used and the other five instructions are described below. The TAP controller used in this SRAM is not fully compliant with the 1149.1 convention because some mandatory instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals and cannot preload the Input or Output buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; instead it performs a capture of the Inputs and Output ring when these instructions are executed. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted from the instruction register through the TDI and TDO pins. To execute an instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. Because EXTEST is not implemented in the TAP controller, this device is not 1149.1 standard compliant. The TAP controller recognizes an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is a difference between the instructions, unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE-Z

The SAMPLE-Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1 compliant. When the SAMPLE/PRELOAD instruction is loaded to the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

It is important to realize that the TAP controller clock operates at a frequency up to 10 MHz, while the SRAM clock runs more than an order of magnitude faster. Because of the clock frequency differences, it is possible that during the Capture-DR state, an input or output will under-go a transition. The TAP may attempt a signal capture while in transition (metastable state). The device will not be harmed, but there is no guarantee of the value that will be captured or repeatable results.

To guarantee that the boundary scan register will capture the correct signal value, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (t_{CS} and t_{CH}). To insure that the SRAM clock input is captured correctly, designs need a way to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is not an issue, it is possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

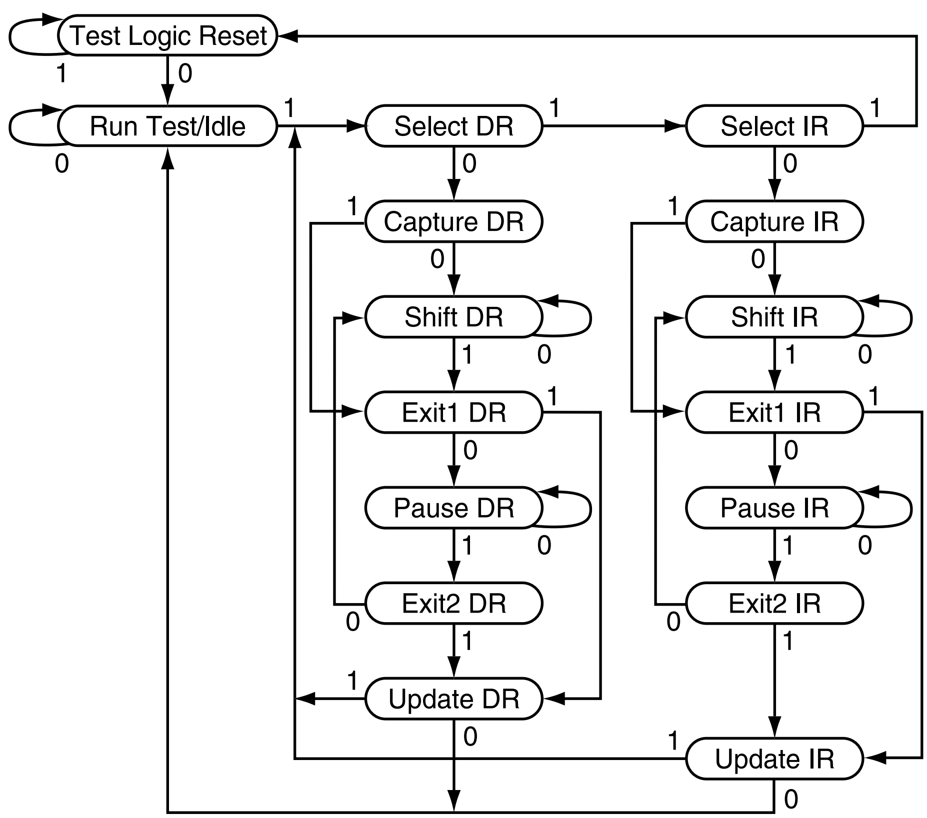
RESERVED

These instructions are not implemented but are reserved for future use. Do not use these instructions.

INSTRUCTION CODES

Code	Instruction	Description
000	EXTEST	Captures the Input/Output ring contents. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1 compliant.
001	IDCODE	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
010	SAMPLE-Z	Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
011	RESERVED	Do Not Use: This instruction is reserved for future use.
100	SAMPLE/PRELOAD	Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1 compliant.
101	RESERVED	Do Not Use: This instruction is reserved for future use.
110	RESERVED	Do Not Use: This instruction is reserved for future use.
111	BYPASS	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

TAP CONTROLLER STATE DIAGRAM



TAP Electrical Characteristics (VDDQ = 3.3V Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{OH1}	Output HIGH Voltage	I_{OH} = -4 mA	2.4	—	V
V_{OH2}	Output HIGH Voltage	I_{OH} = -100 µA	2.9	—	V
V_{OL1}	Output LOW Voltage	I_{OL} = 8 mA	—	0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA	—	0.2	V
V_{IH}	Input HIGH Voltage		2.0	V_{DD}+0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	V
I_X	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{DDQ}$	–30	30	µA

TAP Electrical Characteristics (VDDQ = 2.5V Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{OH1}	Output HIGH Voltage	I_{OH} = -1 mA	2.0	—	V
V_{OH2}	Output HIGH Voltage	I_{OH} = -100 µA	2.1	—	V
V_{OL1}	Output LOW Voltage	I_{OL} = 1 mA	—	0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA	—	0.2	V
V_{IH}	Input HIGH Voltage		1.7	V_{DD}+0.3	V
V_{IL}	Input LOW Voltage		-0.3	0.7	V
I_X	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{DDQ}$	–30	30	µA

TAP Electrical Characteristics (VDDQ = 1.8V Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{OH1}	Output HIGH Voltage	I_{OH} = -1 mA	V_{DD} -0.4	—	V
V_{OL1}	Output LOW Voltage	I_{OL} = 1 mA	—	0.5	V
V_{IH}	Input HIGH Voltage		1.3	V_{DD} +0.3	V
V_{IL}	Input LOW Voltage		-0.3	0.7	V
I_X	Input Load Current	$V_{SS} \leq V\ I \leq V_{DDQ}$	-30	30	µA