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2M x 36 and 4M x 18
72Mb, PIPELINE 'NO WAIT' STATE BUS SRAM

AUGUST 2014

FEATURES

- 100 percent bus utilization
- No wait cycles between Read and Write
- Internal self-timed write cycle
- Individual Byte Write Control
- Single R/W (Read/Write) control pin
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Power Down mode
- Common data inputs and data outputs
- $\overline{CKE}$ pin to enable clock and suspend operation
- JEDEC 100-pin TQFP, 165-ball PBGA and 119-ball PBGA packages
- Power supply:
  NLP: V_{DD} 3.3V (± 5%), V_{DDQ} 3.3V/2.5V (± 5%)
  NVP: V_{DD} 2.5V (± 5%), V_{DDQ} 2.5V (± 5%)
  NVVP: V_{DD} 1.8V (± 5%), V_{DDQ} 1.8V (± 5%)
- JTAG Boundary Scan for PBGA packages
- Industrial temperature available
- Lead-free available

DESCRIPTION

The 72 Meg product family features high-speed, low-power synchronous static RAMs designed to provide a burstable, high-performance, 'no wait' state, device for networking and communications applications. They are organized as 2,096,952 words by 36 bits and 4,193,904 words by 18 bits, fabricated with *ISSI*'s advanced CMOS technology.

Incorporating a 'no wait' state feature, wait cycles are eliminated when the bus switches from read to write, or write to read. This device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit.

All synchronous inputs pass through registers are controlled by a positive-edge-triggered single clock input. Operations may be suspended and all synchronous inputs ignored when Clock Enable, $\overline{CKE}$ is HIGH. In this state the internal device will hold their previous values.

All Read, Write and Deselect cycles are initiated by the ADV input. When the ADV is HIGH the internal burst counter is incremented. New external addresses can be loaded when ADV is LOW.

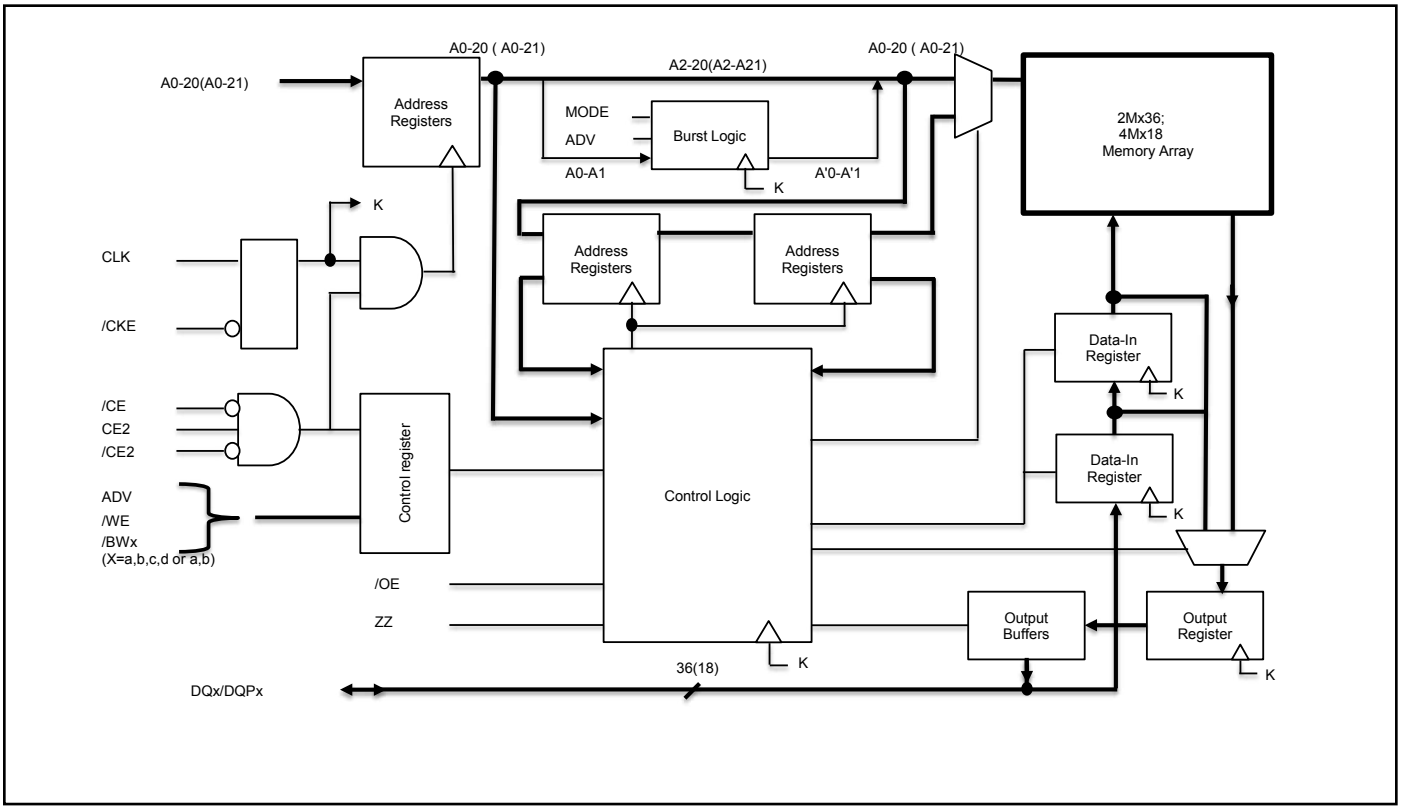
Write cycles are internally self-timed and are initiated by the rising edge of the clock inputs and when $\overline{WE}$ is LOW. Separate byte enables allow individual bytes to be written.

A burst mode pin (MODE) defines the order of the burst sequence. When tied HIGH, the interleaved burst sequence is selected. When tied LOW, the linear burst sequence is selected.

FAST ACCESS TIME

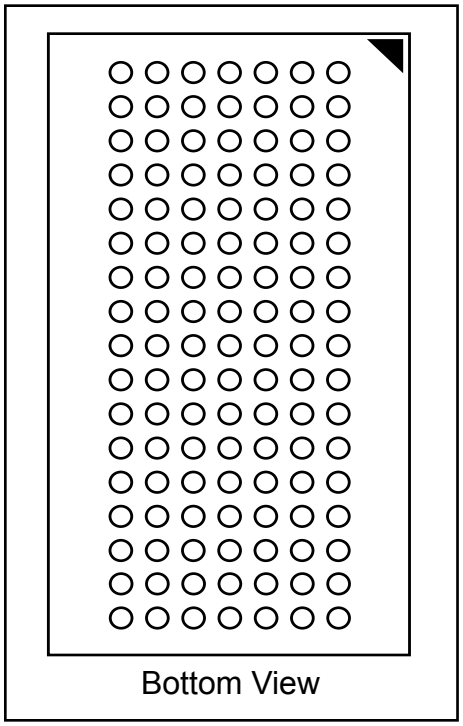
Symbol	Parameter	250	200	166	Units
t_{KQ}	Clock Access Time	2.8	3.1	3.8	ns
t_{KC}	Cycle Time	4	5	6	ns
	Frequency	250	200	166	MHz

BLOCK DIAGRAM



119-PIN BGA

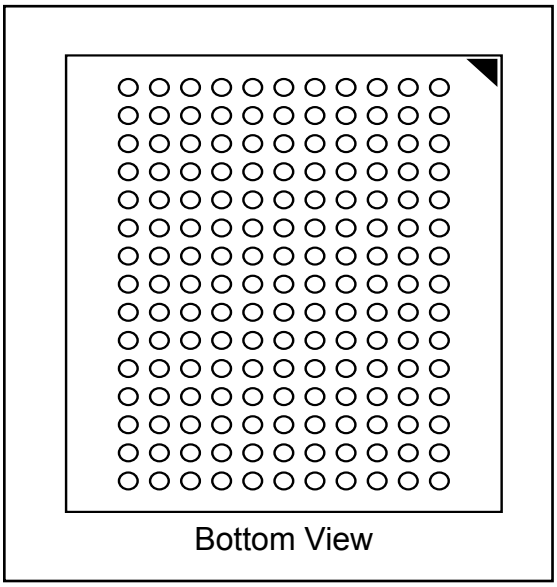
119-Ball, 14x22 mm BGA
1.27 mm Ball Pitch, 7 x 17 Ball Array



Bottom View

165-PIN BGA

165-Ball, 13x15 mm BGA
165-Ball, 15x17 mm BGA
1 mm Ball Pitch, 11 x 15 Ball Array



Bottom View

PIN CONFIGURATION — 2M x 36, 165-Ball PBGA (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}$	$\overline{BW}$c	$\overline{BW}$b	$\overline{CE}$2	$\overline{CKE}$	ADV	A	A	NC
B	NC	A	CE2	$\overline{BW}$d	$\overline{BW}$a	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC
C	DQPc	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPb
D	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
H	NC	NC	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
M	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
N	DQPd	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	DQPa
P	NC	A	A	A	TDI	A1*	TDO	A	A	A	NC
R	MODE	A	A	A	TMS	A0*	TCK	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name
A	Synchronous Address Inputs
A0, A1	Synchronous Burst Address Inputs
ADV	Synchronous Burst Address Advance/ Load
$\overline{WE}$	Synchronous Read/Write Control Input
CLK	Synchronous Clock
$\overline{CKE}$	Synchronous Clock Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
$\overline{BW}$a-$\overline{BW}$d	Synchronous Byte Write Inputs
$\overline{OE}$	Asynchronous Output Enable
ZZ	Asynchronous Power Sleep Mode
MODE	Burst Sequence Selection
TCK, TDI TDO, TMS	JTAG Pins
V_{DD}	Power Supply
NC	No Connect
DQa-DQd	Synchronous Data Inputs/Outputs
DQPa-DQPd	Synchronous Parity Data Inputs/Outputs
V_{DDQ}	I/O Power Supply
V_{SS}	Ground

119-PIN PBGA PACKAGE CONFIGURATION ——2M x 36 (TOP VIEW)

	1	2	3	4	5	6	7
A	VDDQ	A	A	A	A	A	VDDQ
B	NC	CE2	A	ADV	A	$\overline{CE}$2	NC
C	NC	A	A	VDD	A	A	NC
D	DQc	DQPc	VSS	NC	VSS	DQPb	DQb
E	DQc	DQc	VSS	$\overline{CE}$	VSS	DQb	DQb
F	VDDQ	DQc	VSS	$\overline{OE}$	VSS	DQb	VDDQ
G	DQc	DQc	$\overline{BW}$c	A	$\overline{BW}$b	DQb	DQb
H	DQc	DQc	VSS	$\overline{WE}$	VSS	DQb	DQb
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	DQd	DQd	VSS	CLK	VSS	DQa	DQa
L	DQd	DQd	$\overline{BW}$d	NC	$\overline{BW}$a	DQa	DQa
M	VDDQ	DQd	VSS	$\overline{CKE}$	VSS	DQa	VDDQ
N	DQd	DQd	VSS	A1*	VSS	DQa	DQa
P	DQd	DQPd	VSS	A0*	VSS	DQPa	DQa
R	NC	A	MODE	VDD	NC	A	NC
T	NC	A	A	A	A	A	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

Note: A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name
A	Synchronous Address Inputs
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CLK	Synchronous Clock
$\overline{CKE}$	Synchronous Clock Enable
$\overline{CE}$	Synchronous Chip Select
$\overline{CE}$2	Synchronous Chip Select
CE2	Synchronous Chip Select
$\overline{BW}$a-$\overline{BW}$d	Synchronous Byte Write Inputs
$\overline{OE}$	Asynchronous Output Enable
ZZ	Asynchronous Power Sleep Mode
MODE	Burst Sequence Selection
TCK, TDO TMS, TDI	JTAG Pins
V_{DD}	Power Supply
V_{SS}	Ground
NC	No Connect
DQa-DQd	Synchronous Data Inputs/Outputs
DQPa-DQPd	Synchronous Parity Data Inputs/Outputs
V_{DDQ}	I/O Power Supply

165-PIN PBGA PACKAGE CONFIGURATION ——4M x 18 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}$	$\overline{BW}$b	NC	$\overline{CE}$2	$\overline{CKE}$	ADV	A	A	A
B	NC	A	CE2	NC	$\overline{BW}$a	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPa
D	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
E	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
F	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
G	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
H	NC	NC	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
K	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
L	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
M	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
N	DQPb	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	NC
P	NC	A	A	A	TDI	A1*	TDO	A	A	A	NC
R	MODE	A	A	A	TMS	A0*	TCK	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name
A	Synchronous Address Inputs
A0, A1	Synchronous Burst Address Inputs
ADV	Synchronous Burst Address Advance/ Load
$\overline{WE}$	Synchronous Read/Write Control Input
CLK	Synchronous Clock
$\overline{CKE}$	Synchronous Clock Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
$\overline{BW}$a-$\overline{BW}$b	Synchronous Byte Write Inputs
$\overline{OE}$	Asynchronous Output Enable
ZZ	Asynchronous Power Sleep Mode
MODE	Burst Sequence Selection
TCK, TDI TDO, TMS	JTAG Pins
V_{DD}	Power Supply
NC	No Connect
DQa-DQb	Synchronous Data Inputs/Outputs
DQPa-DQPb	Synchronous Parity Data Inputs/Outputs
V_{DDQ}	I/O Power Supply
V_{SS}	Ground

119-PIN PBGA PACKAGE CONFIGURATION ——4M x 18 (TOP VIEW)

	1	2	3	4	5	6	7
A	VDDQ	A	A	A	A	A	VDDQ
B	NC	CE2	A	ADV	A	$\overline{CE}$2	NC
C	NC	A	A	VDD	A	A	NC
D	DQb	NC	VSS	NC	VSS	DQPa	NC
E	NC	DQb	VSS	$\overline{CE}$	VSS	NC	DQa
F	VDDQ	NC	VSS	$\overline{OE}$	VSS	DQa	VDDQ
G	NC	DQb	$\overline{BW}$b	A	NC	NC	DQa
H	DQb	NC	VSS	$\overline{WE}$	VSS	DQa	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	DQb	VSS	CLK	VSS	NC	DQa
L	DQb	NC	NC	NC	$\overline{BW}$a	DQa	NC
M	VDDQ	DQb	VSS	$\overline{CKE}$	VSS	NC	VDDQ
N	DQb	NC	VSS	A1*	VSS	DQa	NC
P	NC	DQPb	VSS	A0*	VSS	NC	DQa
R	NC	A	MODE	VDD	NC	A	NC
T	A	A	A	A	A	A	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

Note: A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

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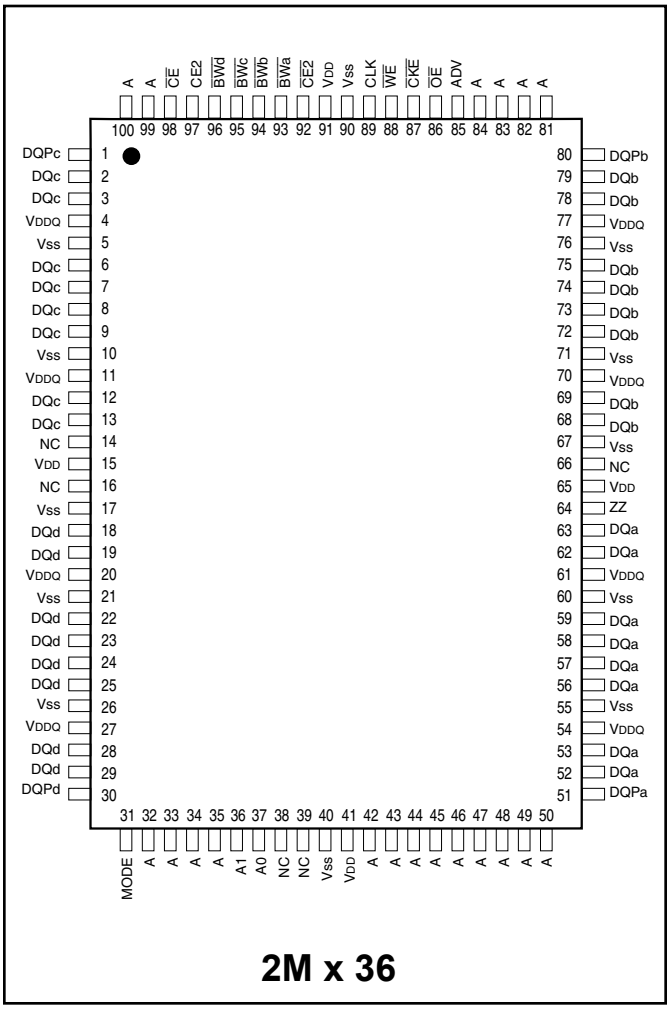
$\overline{CKE}$	Synchronous Clock Enable
$\overline{CE}$	Synchronous Chip Select
$\overline{CE}$2	Synchronous Chip Select
CE2	Synchronous Chip Select
$\overline{BWa}$-$\overline{BWb}$	Synchronous Byte Write Inputs
$\overline{OE}$	Asynchronous Output Enable
ZZ	Asynchronous Power Sleep Mode
MODE	Burst Sequence Selection
TCK, TDO TMS, TDI	JTAG Pins
V_{DD}	Power Supply
V_{SS}	Ground
NC	No Connect
DQa-DQb	Synchronous Data Inputs/Outputs
DQPa-DQPb	Synchronous Parity Data Inputs/Outputs
V_{DDQ}	I/O Power Supply

PIN CONFIGURATION
100-Pin TQFP



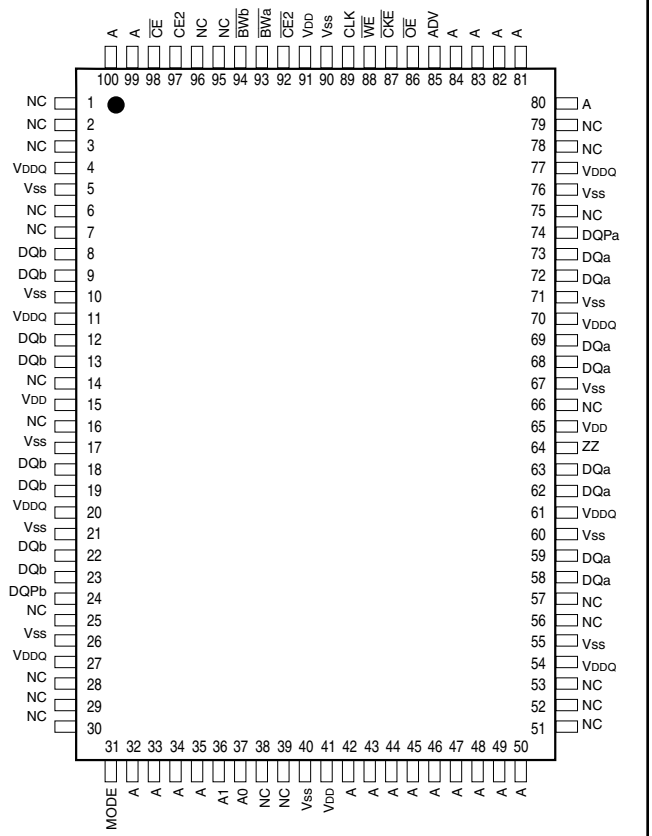
2M x 36

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
CLK	Synchronous Clock
ADV	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWd}$	Synchronous Byte Write Enable
$\overline{WE}$	Synchronous Write Enable
$\overline{CKE}$	Synchronous Clock Enable
Vss	Ground for Core
NC	Not Connected

$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Enable
$\overline{OE}$	Asynchronous Output Enable
DQa-DQd	Synchronous Data Inputs/Outputs
DQPa-DQPd	Synchronous Parity Data Inputs/Outputs
MODE	Burst Sequence Selection
V_{DD}	Power Supply
V_{SS}	Ground for output Buffer
V_{DDQ}	I/O Power Supply
ZZ	Asynchronous Snooze Enable

PIN CONFIGURATION
100-Pin TQFP



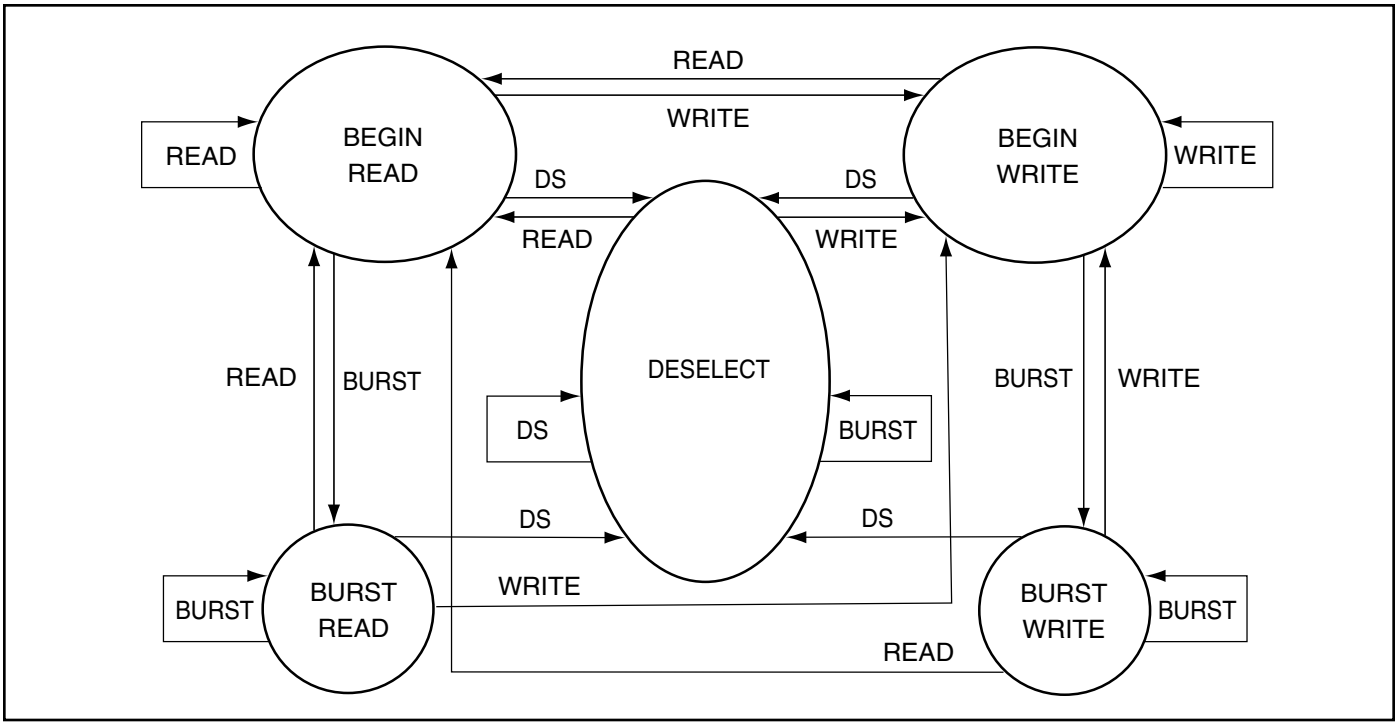
4M x 18

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
CLK	Synchronous Clock
ADV	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWb}$	Synchronous Byte Write Enable
$\overline{WE}$	Synchronous Write Enable
$\overline{CKE}$	Synchronous Clock Enable
Vss	Ground for Core
NC	Not Connected

$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Enable
$\overline{OE}$	Asynchronous Output Enable
DQa-DQb	Synchronous Data Inputs/Outputs
DQPa-DQPb	Synchronous Parity Data Inputs/Outputs
MODE	Burst Sequence Selection
V_{DD}	Power Supply
V_{SS}	Ground for output Buffer
V_{DDQ}	I/O Power Supply
ZZ	Asynchronous Snooze Enable

STATE DIAGRAM



SYNCHRONOUS TRUTH TABLE(1)

Operation	Address Used	$\overline{CE}$	CE2	$\overline{CE}$2	ADV	$\overline{WE}$	$\overline{BW}$x	$\overline{OE}$	$\overline{CKE}$	CLK
Not Selected	N/A	H	X	X	L	X	X	X	L	↑
Not Selected	N/A	X	L	X	L	X	X	X	L	↑
Not Selected	N/A	X	X	H	L	X	X	X	L	↑
Not Selected Continue	N/A	X	X	X	H	X	X	X	L	↑
Begin Burst Read	External Address	L	H	L	L	H	X	L	L	↑
Continue Burst Read	Next Address	X	X	X	H	X	X	L	L	↑
NOP/Dummy Read	External Address	L	H	L	L	H	X	H	L	↑
Dummy Read	Next Address	X	X	X	H	X	X	H	L	↑
Begin Burst Write	External Address	L	H	L	L	L	L	X	L	↑
Continue Burst Write	Next Address	X	X	X	H	X	L	X	L	↑
NOP/Write Abort	N/A	L	H	L	L	L	H	X	L	↑
Write Abort	Next Address	X	X	X	H	X	H	X	L	↑
Ignore Clock	Current Address	X	X	X	X	X	X	X	H	↑

Notes:
1. "X" means don't care.
2. The rising edge of clock is symbolized by ↑
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. $\overline{WE}$ = L means Write operation in Write Truth Table.
   $\overline{WE}$ = H means Read operation in Write Truth Table.
5. Operation finally depends on status of asynchronous pins (ZZ and $\overline{OE}$).

ASYNCHRONOUS TRUTH TABLE(1)

Operation	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes:

1. X means "Don't Care".
2. For write cycles following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
3. Sleep Mode means power Sleep Mode where stand-by current does not depend on cycle time.
4. Deselected means power Sleep Mode where stand-by current depends on cycle time.

WRITE TRUTH TABLE (x18)

Operation	$\overline{WE}$	$\overline{BW}$**a**	$\overline{BW}$**b**
READ	H	X	X
WRITE BYTE a	L	L	H
WRITE BYTE b	L	H	L
WRITE ALL BYTEs	L	L	L
WRITE ABORT/NOP	L	H	H

Notes:

1. X means "Don't Care".
2. All inputs in this table must beet setup and hold time around the rising edge of CLK.

WRITE TRUTH TABLE (x36)

Operation	$\overline{WE}$	$\overline{BW}$a	$\overline{BW}$b	$\overline{BW}$c	$\overline{BW}$d
READ	H	X	X	X	X
WRITE BYTE a	L	L	H	H	H
WRITE BYTE b	L	H	L	H	H
WRITE BYTE c	L	H	H	L	H
WRITE BYTE d	L	H	H	H	L
WRITE ALL BYTEs	L	L	L	L	L
WRITE ABORT/NOP	L	H	H	H	H

Notes:

1. X means "Don't Care".
2. All inputs in this table must beet setup and hold time around the rising edge of CLK.

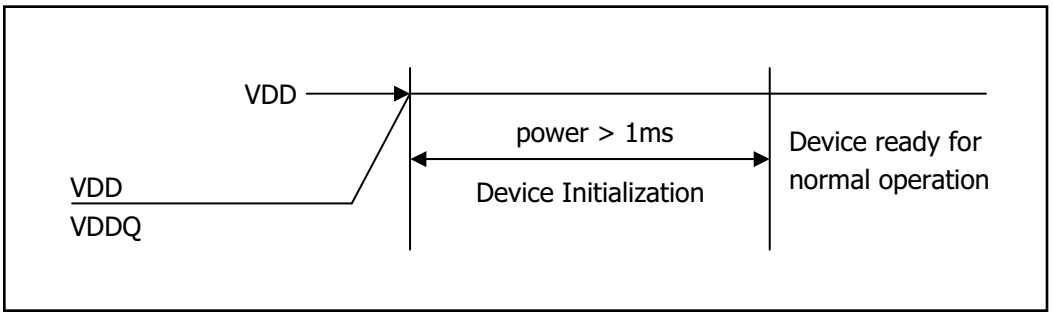
POWER UP SEQUENCE

$V_{DDQ} \rightarrow V_{DD}$[1] $\rightarrow$ I/O Pins[2]

Notes:

1. V_{DD} can be applied at the same time as V_{DDQ}
2. Applying I/O inputs is recommended after V_{DDQ} is ready. The inputs of the I/O pins can be applied at the same time as V_{DDQ} provided V_{IH} (level of I/O pins) is lower than V_{DDQ}.

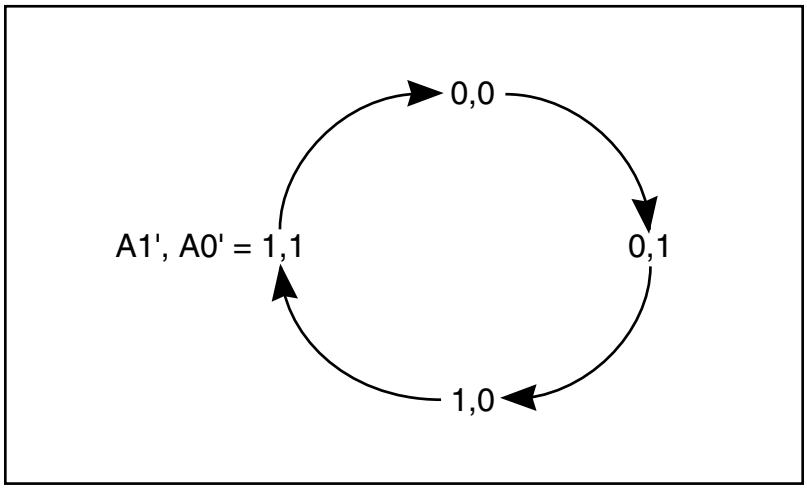
POWER-UP INITIALIZATION TIMING



INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or NC)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = V_{SS})



ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	NLP Value	NVP/NVVP Value	Unit
T_{STG}	Storage Temperature	–65 to +150	–65 to +150	°C
P_D	Power Dissipation	1.6	1.6	W
I_{OUT}	Output Current (per I/O)	100	100	mA
V_{IN}, V_{OUT}	Voltage Relative to V_{SS} for I/O Pins	–0.5 to V_{DDQ} + 0.3	–0.5 to V_{DDQ} + 0.3	V
V_{IN}	Voltage Relative to V_{SS} for for Address and Control Inputs	–0.3 to V_{DD}+0.5	–0.3 to V_{DD}+0.3	V

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE (IS61NLPx)

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V ± 5%	3.3V / 2.5V ± 5%
Industrial	-40°C to +85°C	3.3V ± 5%	3.3V / 2.5V ± 5%

OPERATING RANGE (IS61NVPx)

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	2.5V ± 5%	2.5V ± 5%
Industrial	-40°C to +85°C	2.5V ± 5%	2.5V ± 5%

OPERATING RANGE (IS61NVVPx)

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	1.8V ± 5%	1.8V ± 5%
Industrial	-40°C to +85°C	1.8V ± 5%	1.8V ± 5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range) [1, 2, 3]

Symbol	Parameter	Test Conditions	3.3V Min.	3.3V Max.	2.5V Min.	2.5V Max.	1.8V Min.	1.8V Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –4.0 mA (3.3V) I_{OH} = –1.0 mA (2.5V, 1.8V)	2.4	—	2.0	—	V_{DDQ} - 0.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA (3.3V) I_{OL} = 1.0 mA (2.5V, 1.8V)	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{DD} + 0.3	1.7	V_{DD} + 0.3	0.6V_{DD}	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	–0.3	0.7	–0.3	0.3V_{DD}	V
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{DD}$ [1,4]	–5	5	–5	5	–5	5	µA
	Input Current of MODE	$V_{SS} \le V_{IN} \le V_{DD}$ [5]	–30	5	–30	5	–30	5	
	Input Current of ZZ	$V_{SS} \le V_{IN} \le V_{DD}$ [6]	–5	30	–5	30	–5	30	
I_{LO}	Output Leakage Current	$V_{SS} \le V_{OUT} \le V_{DDQ}$, $\overline{OE}$ = V_{IH}	–5	5	–5	5	–5	5	µA

Notes:
1. All voltages referenced to ground.
2. Overshoot:
   3.3V and 2.5V: V_{IH} (AC) ≤ V_{DD} + 1.5V (Pulse width less than t_{KC} /2)
   1.8V: V_{IH} (AC) ≤ V_{DD} + 0.5V (Pulse width less than t_{KC} /2)
3. Undershoot:
   3.3V and 2.5V: V_{IL} (AC) ≥ -1.5V (Pulse width less than t_{KC} /2)
   1.8V: V_{IL} (AC) ≥ -0.5V (Pulse width less than t_{KC} /2)
4. Except MODE and ZZ
5. MODE is connected to pull-up resister internally.
6. ZZ is connected to pull-down resister internally.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions	Temp. range	-250 MAX x18	-250 MAX x36	-200 MAX x18	-200 MAX x36	-166 MAX x18	-166 MAX x36	Unit
I_{CC}	AC Operating Supply Current	Device Selected, $\overline{OE}$ = V_{IH}, ZZ ≤ V_{IL}, All Inputs ≤ 0.2V or ≥ V_{DD} – 0.2V, Cycle Time ≥ t_{KC} min.	Com.	450	450	400	400	350	350	mA
			Ind.	500	500	450	450	400	400	
I_{SB}	Standby Current TTL Input	Device Deselected, V_{DD} = Max., All Inputs ≤ V_{IL} or ≥ V_{IH}, ZZ ≤ V_{IL}, f = Max.	Com.	200	200	200	200	200	200	mA
			Ind.	220	220	220	220	220	220	
I_{SBI}	Standby Current CMOS Input	Device Deselected, V_{DD} = Max., V_{IN} ≤ V_{SS} + 0.2V or ≥V_{DD} – 0.2V f = 0	Com.	180	180	180	180	180	180	mA
			Ind.	200	200	200	200	200	200	

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

3.3V I/O OUTPUT LOAD EQUIVALENT

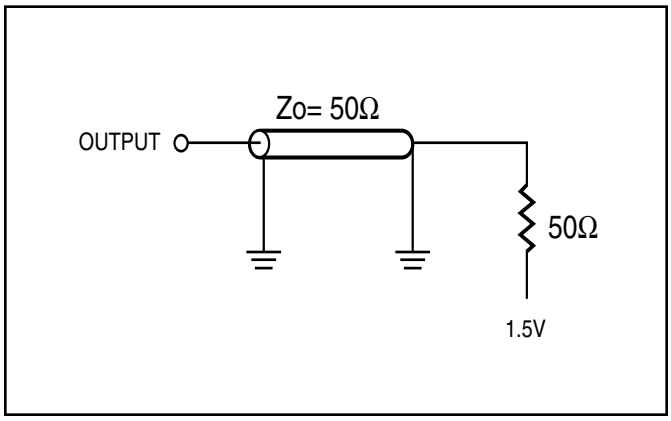


Figure 1

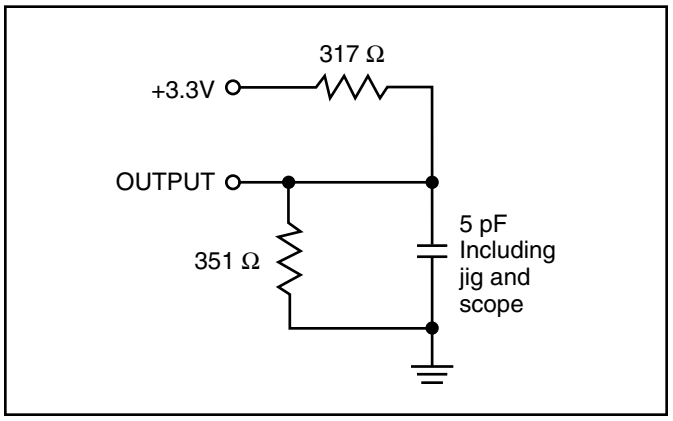


Figure 2

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.25V
Output Load	See Figures 3 and 4

2.5V I/O OUTPUT LOAD EQUIVALENT

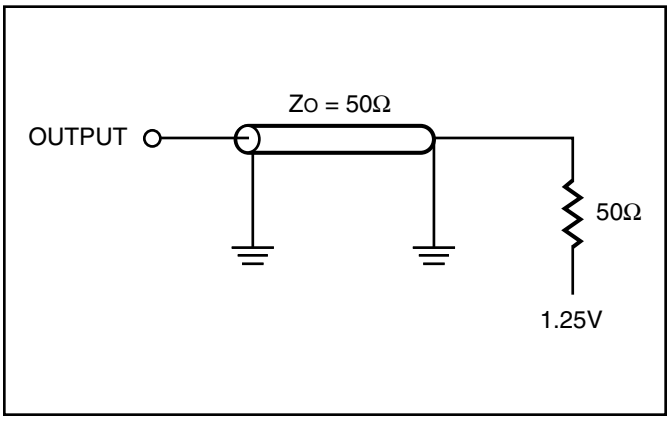


Figure 3

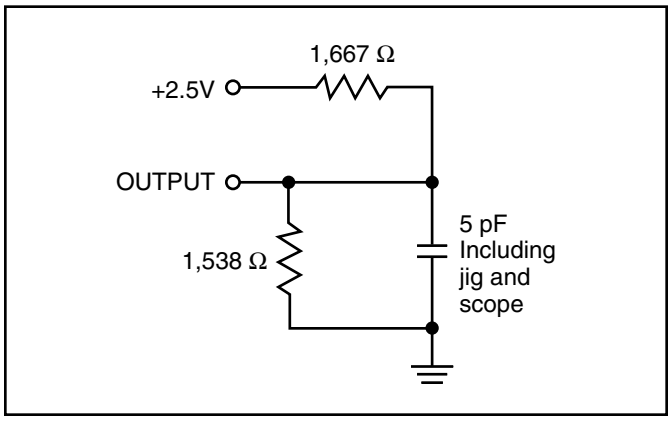


Figure 4

1.8V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 1.8V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	0.9V
Output Load	See Figures 5 and 6

1.8V I/O OUTPUT LOAD EQUIVALENT

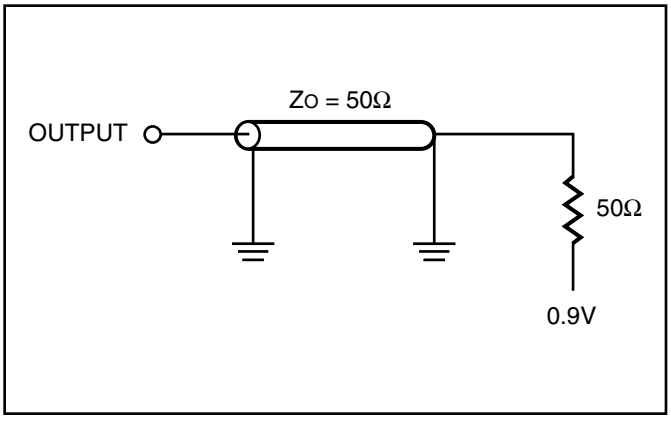


Figure 5

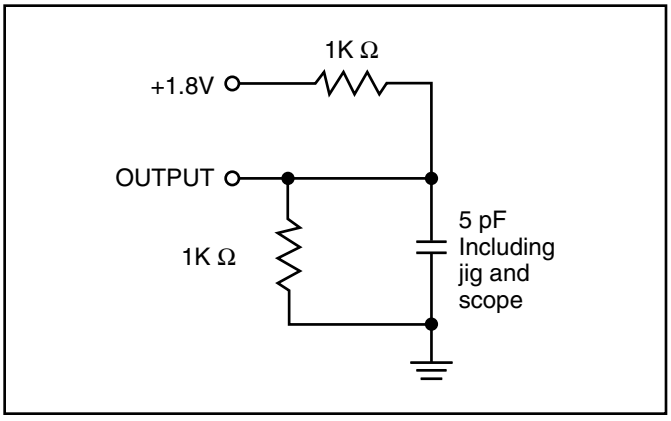


Figure 6

READ/WRITE CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

		-250		-200		-166		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
fmax	Clock Frequency	—	250	—	200	—	166	MHz
t_{KC}	Cycle Time	4.0	—	5	—	6	—	ns
t_{KH}	Clock High Time	1.7	—	2	—	2.4	—	ns
t_{KL}	Clock Low Time 1.7	1.7	—	—		2.3	—	ns
t_{KQ}	Clock Access Time	—	2.8	—	3.1	—	3.8	ns
t_{KQX}[2]	Clock High to Output Invalid	0.8	—	1.5	—	1.5	—	ns
t_{KQLZ}[2,3]	Clock High to Output Low-Z	0.8	—	1	—	1.5	—	ns
t_{KQHZ}[2,3]	Clock High to Output High-Z	—	2.8	—	3.1		3.8	ns
t_{OEQ}	Output Enable to Output Valid	—	2.8	—	3.1		3.8	ns
t_{OELZ}[2,3]	Output Enable to Output Low-Z	0	—	0	—	0	—	ns
t_{OEHZ}[2,3]	Output Disable to Output High-Z	—	2.8	—	3.1		3.8	ns
t_{AS}	Address Setup Time	1.4	—	1.4	—	1.5	—	ns
t_{WS}	Read/Write Setup Time	1.4	—	1.4	—	1.5	—	ns
t_{CES}	Chip Enable Setup Time	1.4	—	1.4	—	1.5	—	ns
t_{SE}	Clock Enable Setup Time	1.4	—	1.4	—	1.5	—	ns
t_{ADVS}	Address Advance Setup Time	1.4	—	1.4	—	1.5	—	ns
t_{DS}	Data Setup Time	1.4	—	1.4	—	1.5	—	ns
t_{AH}	Address Hold Time	0.4	—	0.4	—	0.5	—	ns
t_{HE}	Clock Enable Hold Time	0.4	—	0.4	—	0.5	—	ns
t_{WH}	Write Hold Time	0.4	—	0.4	—	0.5	—	ns
t_{CEH}	Chip Enable Hold Time	0.4	—	0.4	—	0.5	—	ns
t_{ADVH}	Address Advance Hold Time	0.4	—	0.4	—	0.5	—	ns
t_{DH}	Data Hold Time	0.4	—	0.4	—	0.5	—	ns
t_{POWER}[4]	V_{DD} (typical) to First Access	1	—	1	—	1	—	ms

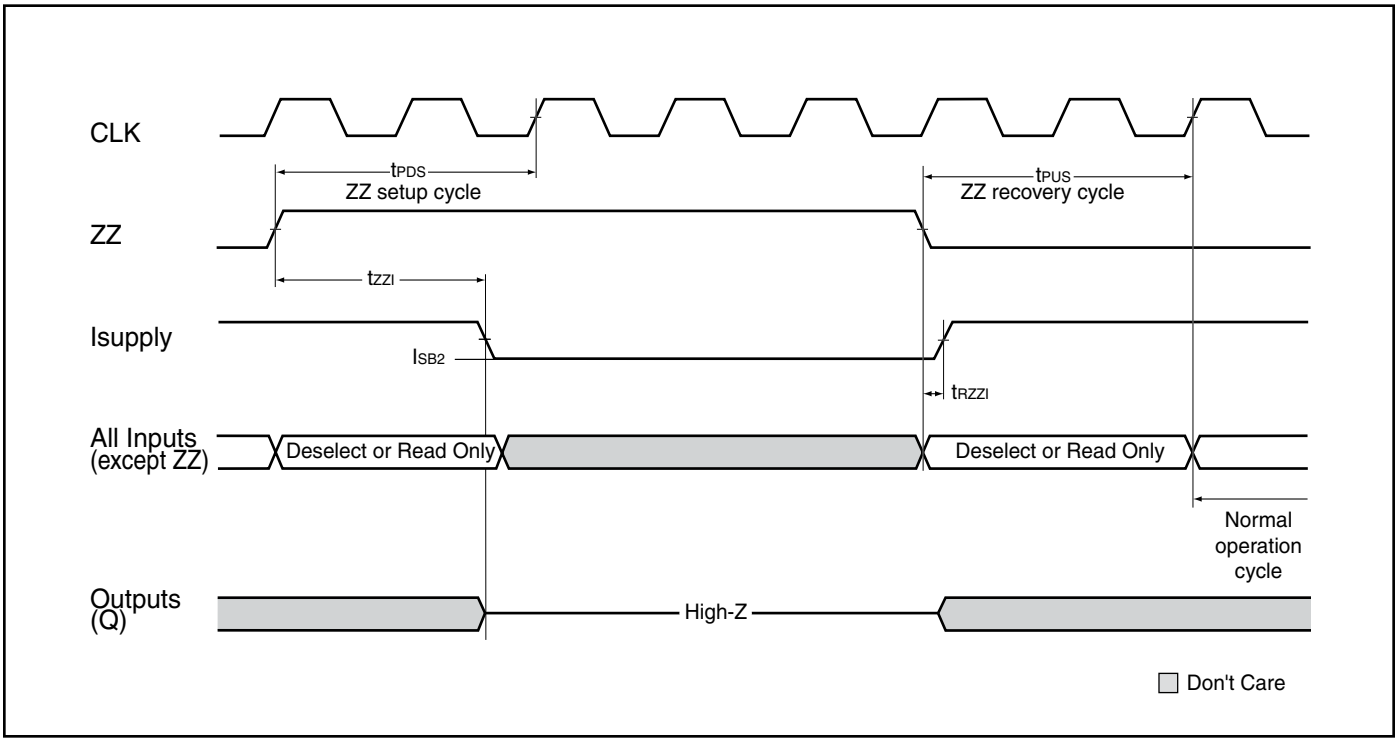
Notes:

1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.
4. t_{POWER} is the time that the power needs to be supplied above V_{DD} (min) initially before READ or WRITE operation can be initiated.

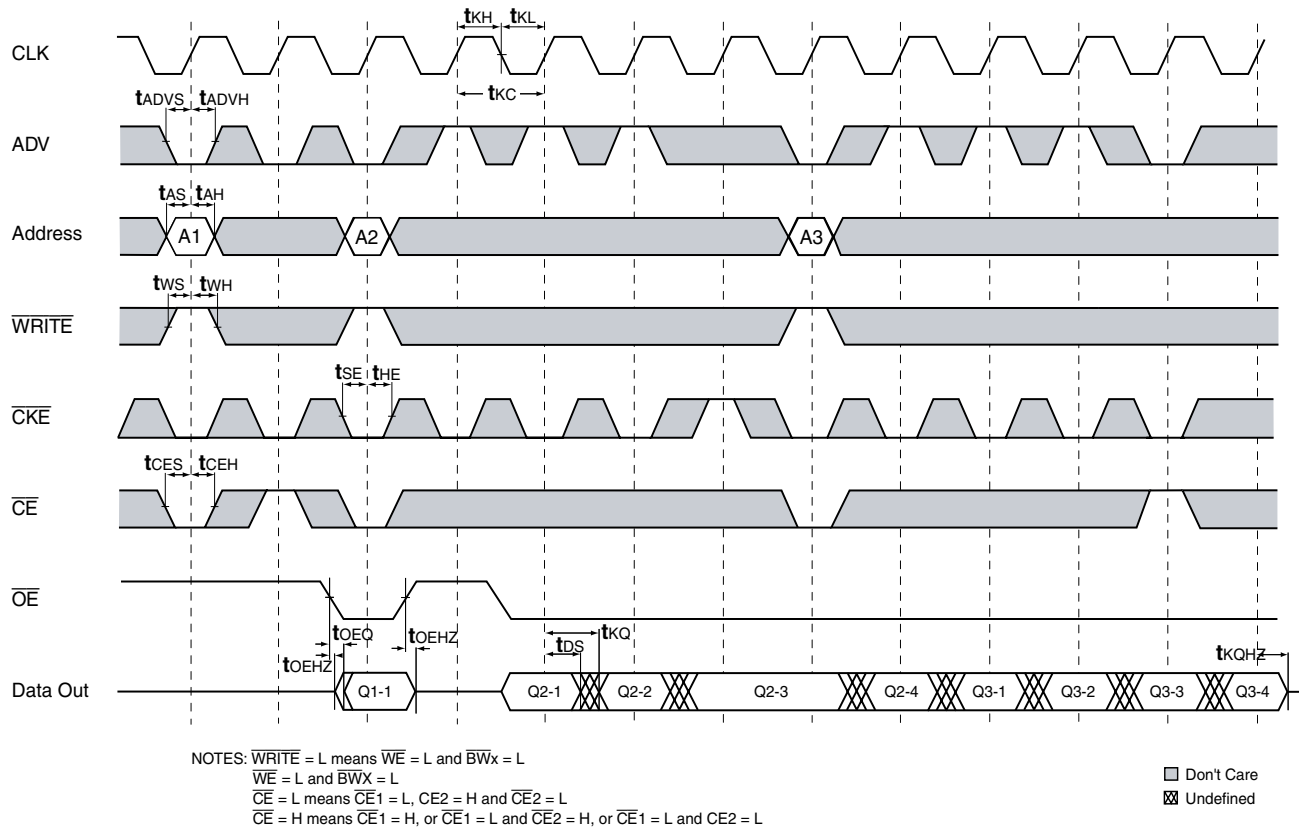
SNOOZE MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Temperature Range	Min.	Max.	Unit
I_{SB2}	Current during SNOOZE MODE	ZZ ≥ V_{DD} - 0.2V	Com.	—	80	mA
			Ind.	—	90	
			Auto.	—	100	
t_{PDS}	ZZ active to input ignored			—	2	cycle
t_{PUS}	ZZ inactive to input sampled			2	—	cycle
t_{ZZI}	ZZ active to SNOOZE current			—	2	cycle
t_{RZZI}	ZZ inactive to exit SNOOZE current			0	—	ns

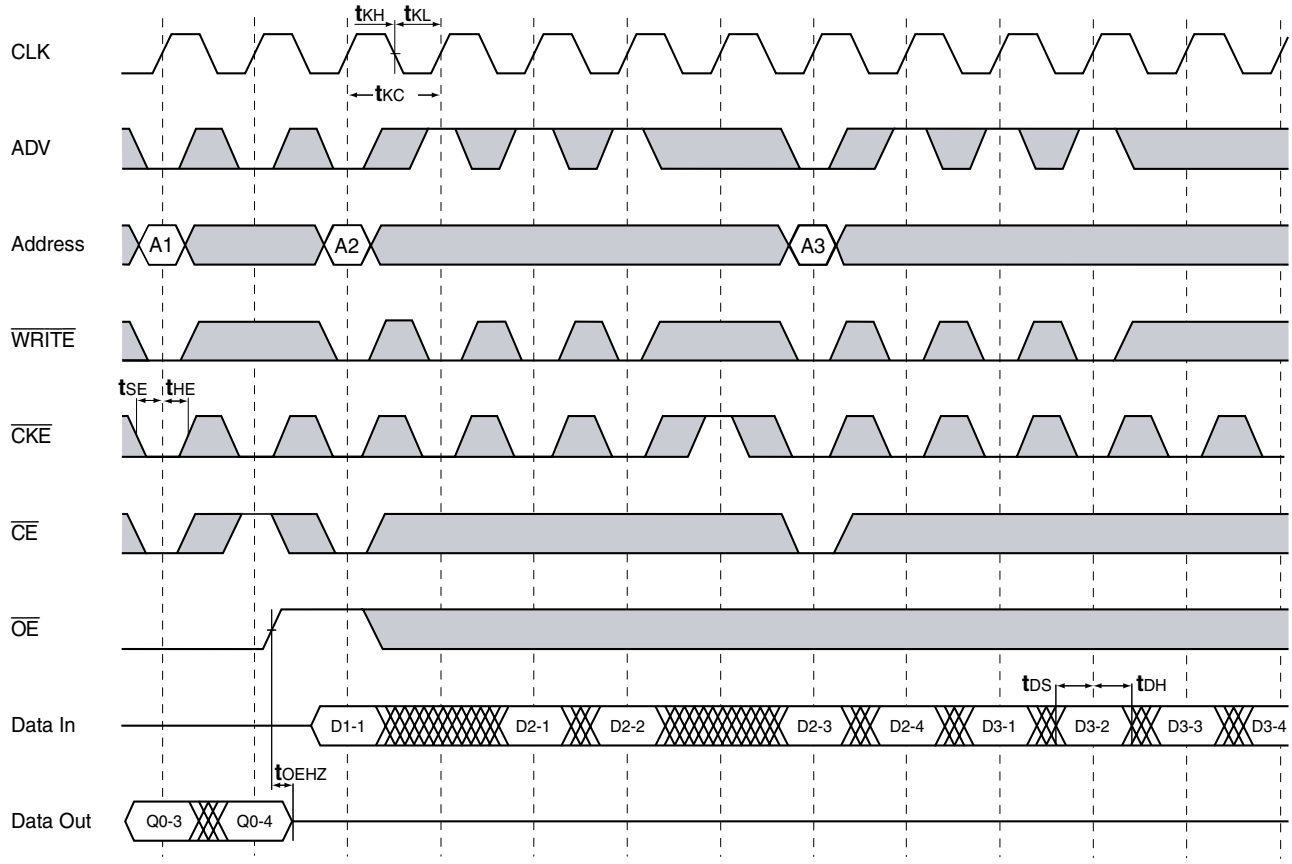
SLEEP MODE TIMING



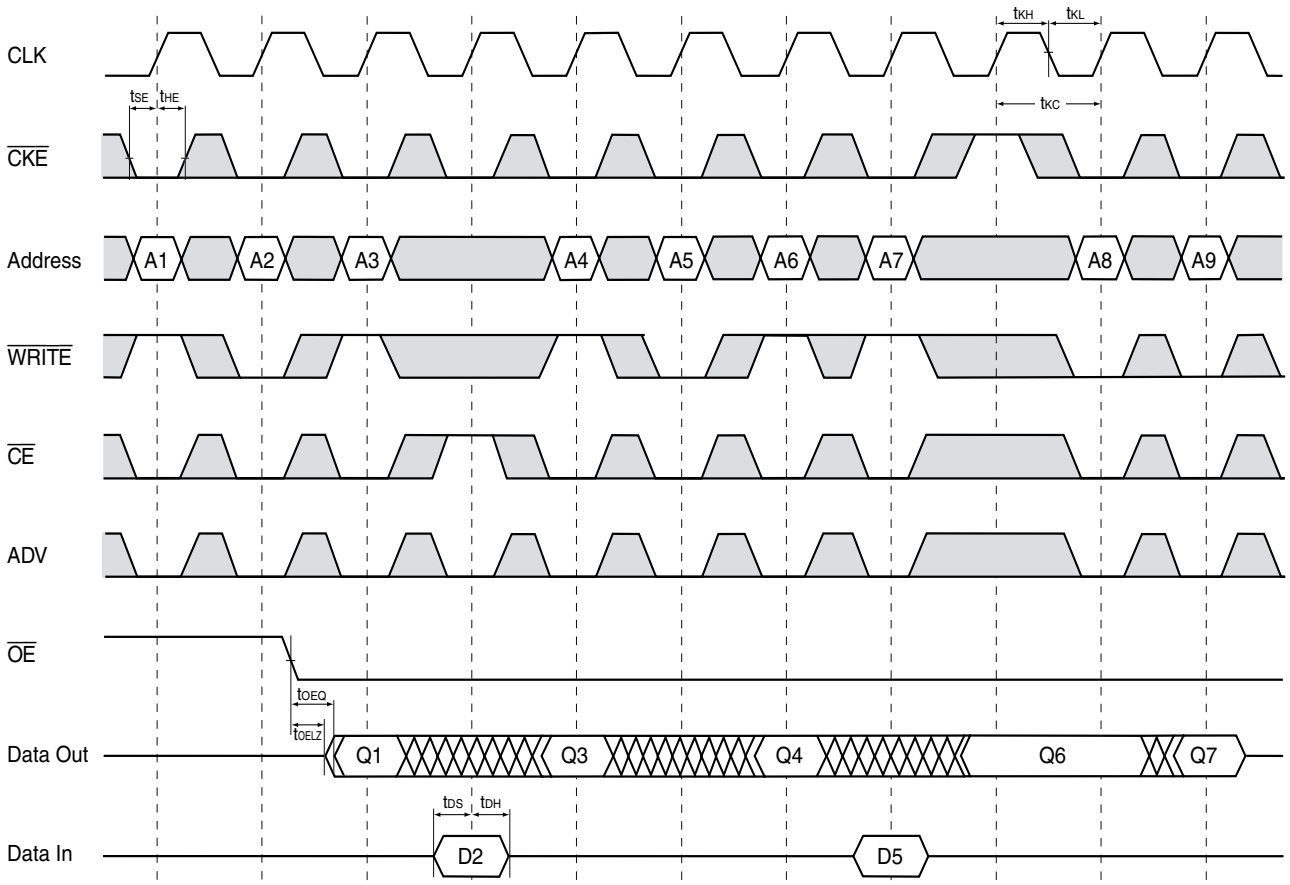
READ CYCLE TIMING



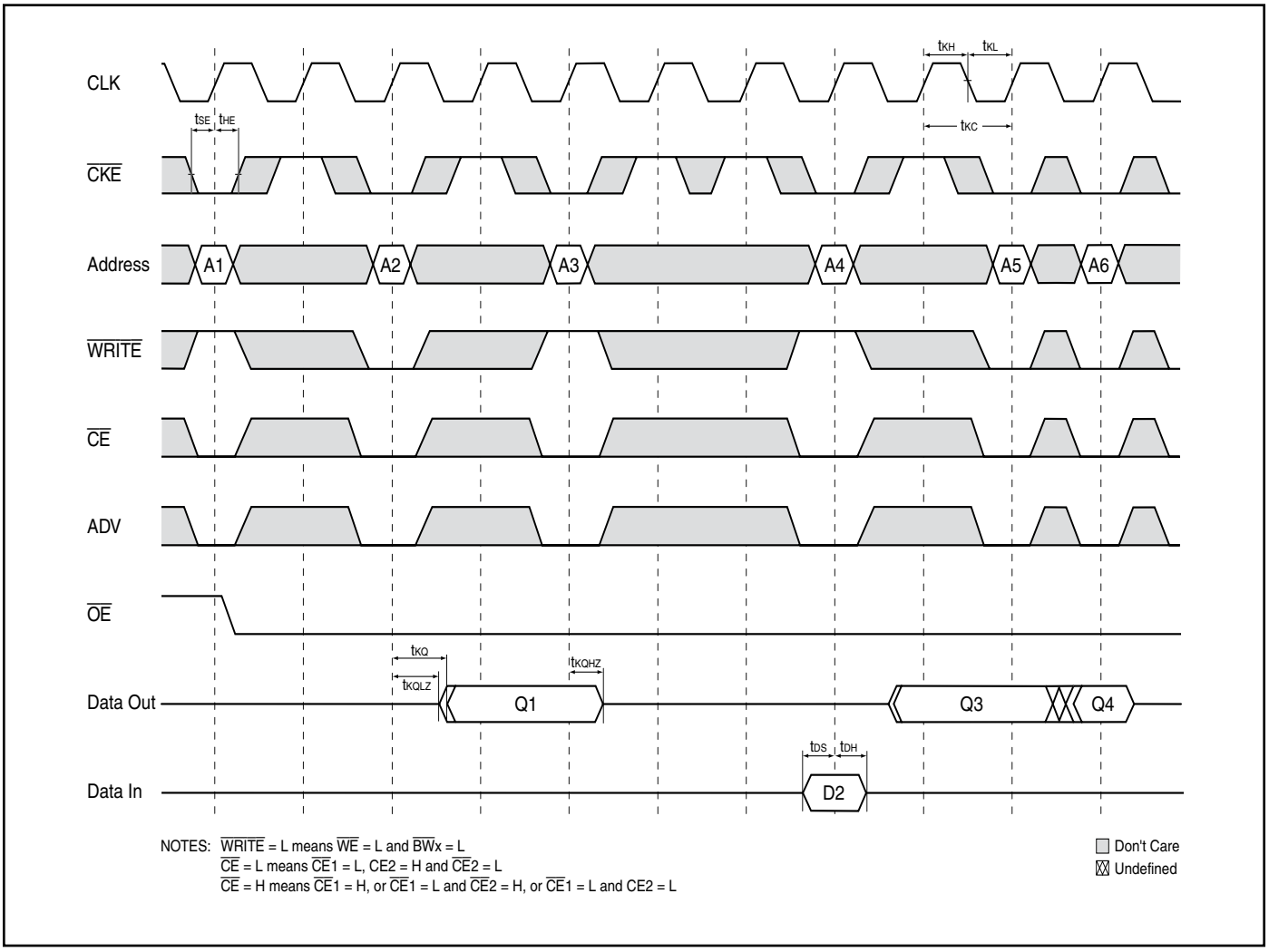
WRITE CYCLE TIMING



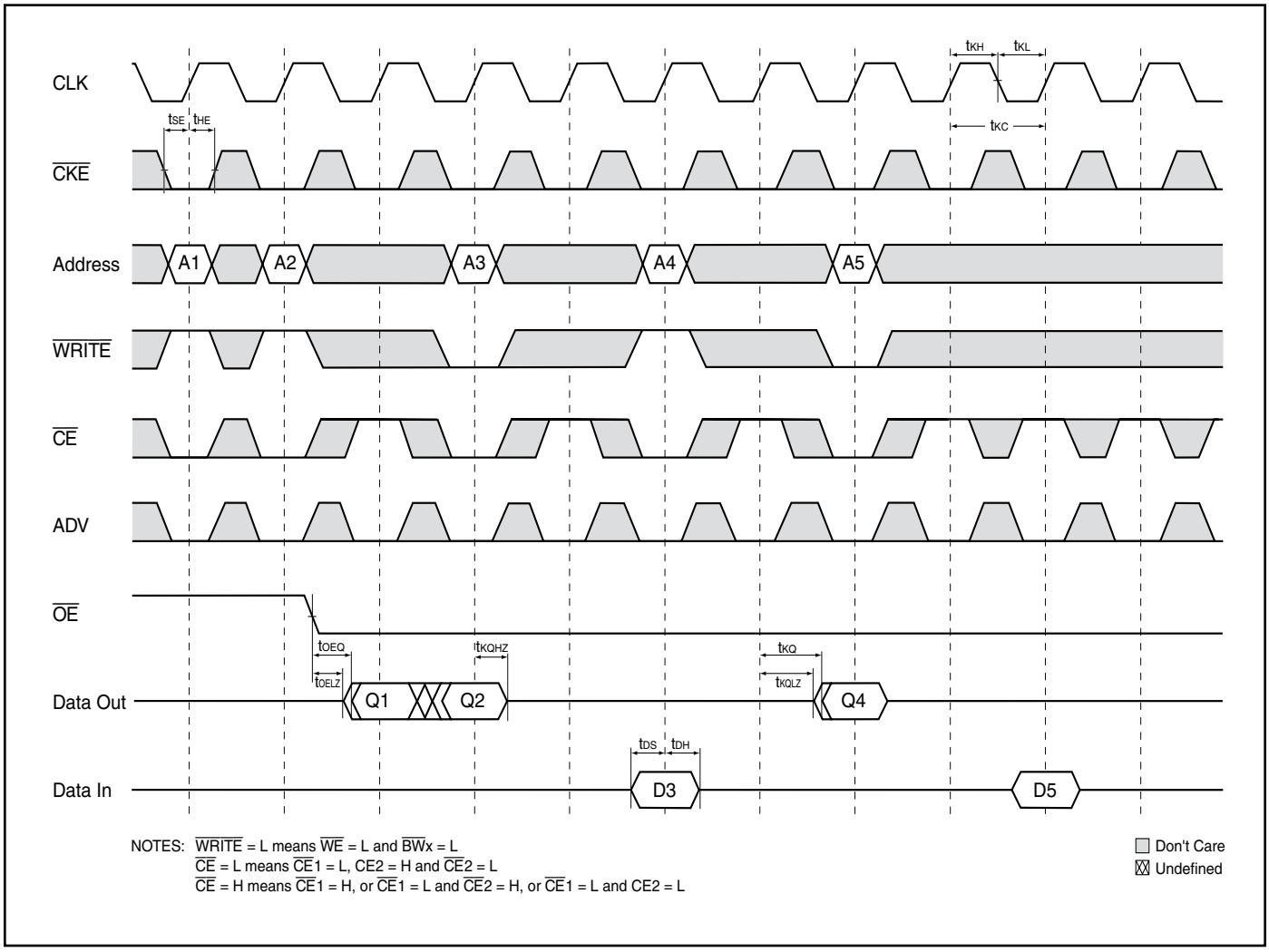
SINGLE READ/WRITE CYCLE TIMING



$\overline{\text{CKE}}$ OPERATION TIMING



$\overline{CE}$ OPERATION TIMING



IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

The serial boundary scan Test Access Port (TAP) is only available in the PBGA package. (Not available in TQFP package.) This port operates in accordance with IEEE Standard 1149.1-1900, but does not include all functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because they place added delay in the critical speed path of the SRAM. The TAP controller operates in a manner that does not conflict with the performance of other devices using 1149.1 fully compliant TAP.

DISABLING THE JTAG FEATURE

The SRAM can operate without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be disconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left disconnected. On power-up, the device will start in a reset state which will not interfere with the device operation.

TEST ACCESS PORT (TAP) - TEST CLOCK

The test clock is only used with the TAP controller. All inputs are captured on the rising edge of TCK and outputs are driven from the falling edge of TCK.

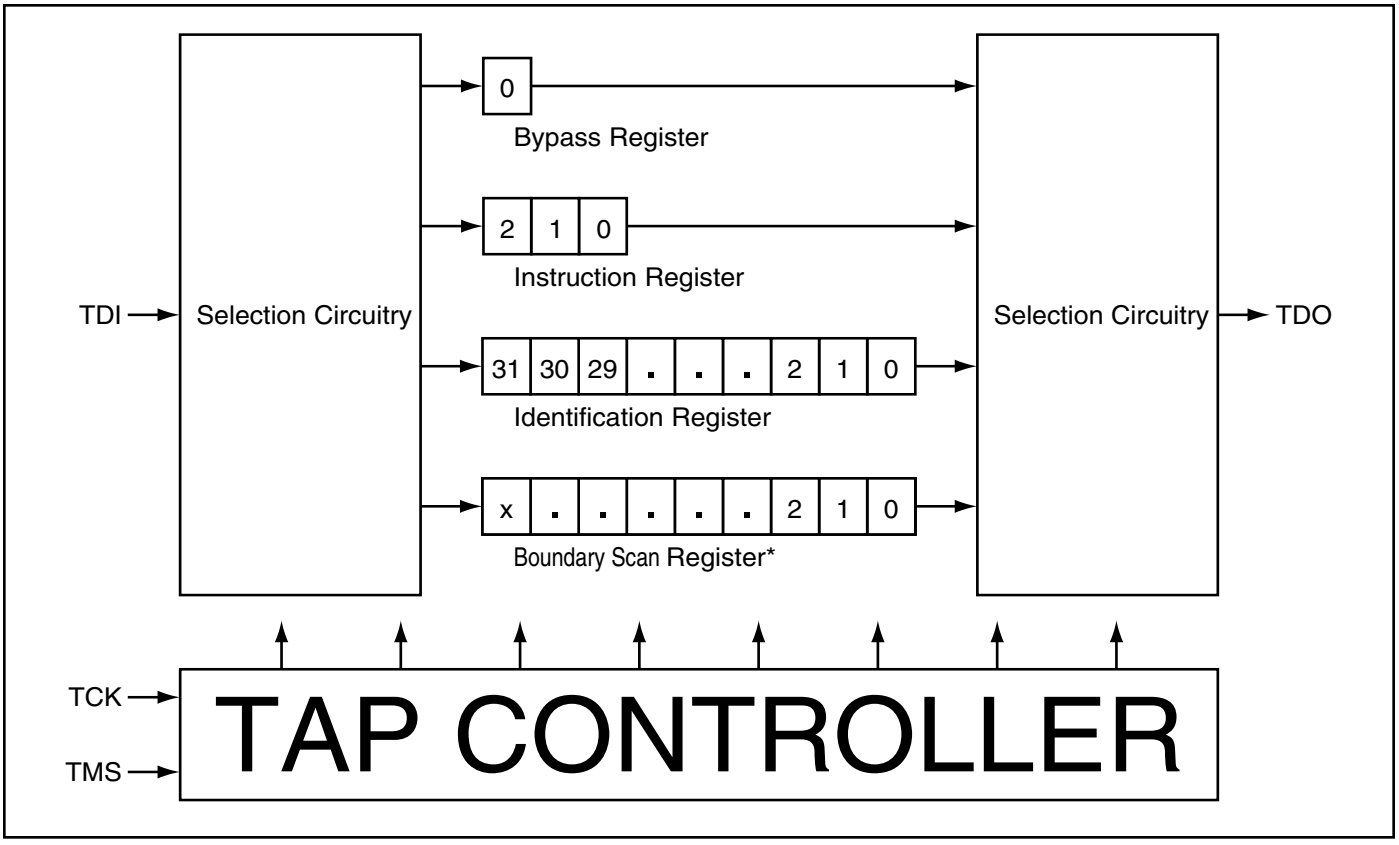
TEST MODE SELECT (TMS)

The TMS input is used to send commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left disconnected if the TAP is not used. The pin is internally pulled up, resulting in a logic HIGH level.

TEST DATA-IN (TDI)

The TDI pin is used to serially input information to the registers and can be connected to the input of any register. The register between TDI and TDO is chosen by the instruction loaded into the TAP instruction register. For information on instruction register loading, see the TAP Controller State Diagram. TDI is internally pulled up and can be disconnected if the TAP is unused in an application. TDI is connected to the Most Significant Bit (MSB) on any register.

TAP CONTROLLER BLOCK DIAGRAM



TEST DATA OUT (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending on the current state of the TAP state machine (see TAP Controller State Diagram). The output changes on the falling edge of TCK and TDO is connected to the Least Significant Bit (LSB) of any register.

PERFORMING A TAP RESET

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. RESET may be performed while the SRAM is operating and does not affect its operation. At power-up, the TAP is internally reset to ensure that TDO comes up in a high-Z state.

TAP REGISTERS

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK and output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins. (See TAP Controller Block Diagram) At power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as previously described.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The x36 configuration has a 75-bit-long register and the x18 configuration also has a 75-bit-long register. The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE-Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Scan Register Sizes

Register Name	Bit Size (x18)	Bit Size (x36)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan	75	75

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded to the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has vendor code and other information described in the Identification Register Definitions table.

IDENTIFICATION REGISTER DEFINITIONS

Instruction Field	Description	2M x 36	4M x 18
Revision Number (31:28)	Reserved for version number.	xxxx	xxxx
Device Depth (27:23)	Defines depth of SRAM. 2M or 4M	01010	01011
Device Width (22:18)	Defines width of the SRAM. x36 or x18	00100	00011
ISSI Device ID (17:12)	Reserved for future use.	xxxxx	xxxxx
ISSI JEDEC ID (11:1)	Allows unique identification of SRAM vendor.	00001010101	00001010101
ID Register Presence (0)	Indicate the presence of an ID register.	1	1