Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

512K x36 and 1024K x18 18Mb, FLOW THROUGH 'NO WAIT' STATE BUS SYNCHRONOUS SRAM

JUNE 2015

FEATURES

- 100 percent bus utilization
- No wait cycles between Read and Write
- Internal self-timed write cycle
- Individual Byte Write Control
- Single R/W (Read/Write) control pin
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Power Down mode
- Common data inputs and data outputs
- /CKE pin to enable clock and suspend operation
- JEDEC 100-pin QFP, 165-ball BGA and 119-ball BGA packages
- Power supply:
  NLF: V_{DD} 3.3V (± 5%), V_{DDQ} 3.3V/2.5V (± 5%)
  NVF: V_{DD} 2.5V (± 5%), V_{DDQ} 2.5V (± 5%)
  NVVF: V_{DD} 1.8V (± 5%), V_{DDQ} 1.8V (± 5%)
- JTAG Boundary Scan for BGA packages
- Commercial, Industrial and Automotive temperature support
- Lead-free available
- For leaded option, please contact ISSI.

FAST ACCESS TIME

Symbol	Parameter	-6.5	-7.5	Units
tKQ	Clock Access Time	6.5	7.5	ns
tKC	Cycle time	7.5	8.5	ns
	Frequency	133	117	MHz

DESCRIPTION

The 18Meg product family features high-speed, low-power synchronous static RAMs designed to provide a burstable, high-performance, 'no wait' state, device for networking and communications applications. They are organized as 512K words by 36 bits and 1024K words by 18 bits, fabricated with *ISSI*'s advanced CMOS technology.

Incorporating a 'no wait' state feature, wait cycles are eliminated when the bus switches from read to write, or write to read. This device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit.

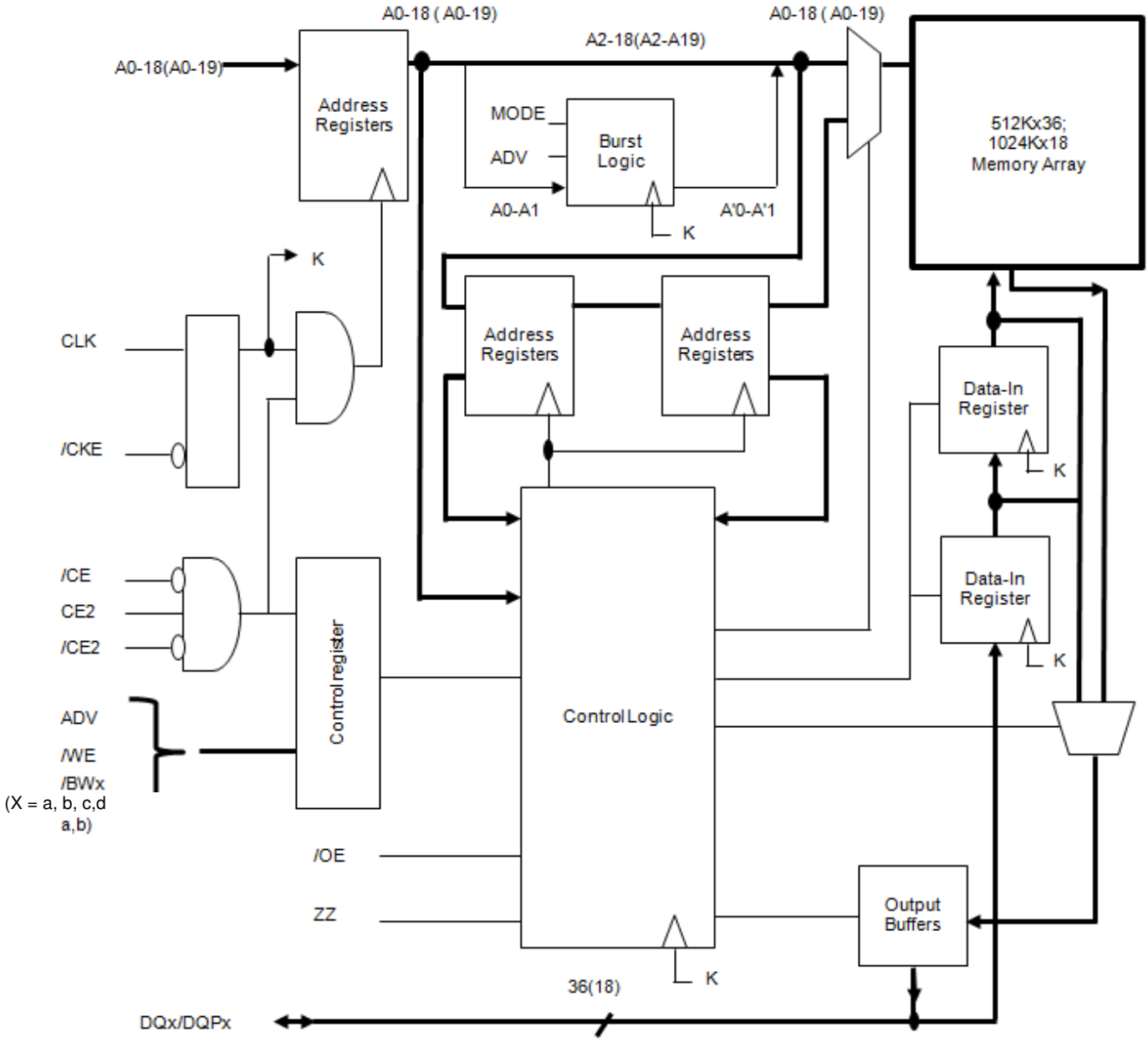
All synchronous inputs pass through registers are controlled by a positive-edge-triggered single clock input. Operations may be suspended and all synchronous inputs ignored when Clock Enable, /CKE is HIGH. In this state the internal device will hold their previous values.

All Read, Write and Deselect cycles are initiated by the ADV input. When the ADV is HIGH the internal burst counter is incremented. New external addresses can be loaded when ADV is LOW.

Write cycles are internally self-timed and are initiated by the rising edge of the clock inputs and when /WE is LOW. Separate byte enables allow individual bytes to be written.

A burst mode pin (MODE) defines the order of the burst sequence. When tied HIGH, the interleaved burst sequence is selected. When tied LOW, the linear burst sequence is selected.

BLOCK DIAGRAM

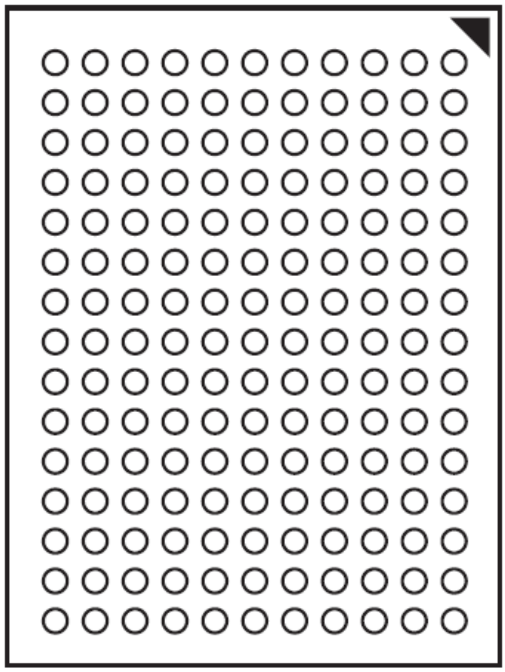


PIN CONFIGURATION

512K x 36, 165-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	/CE	/BWc	/BWb	/CE2	/CKE	ADV	A	A	NC
B	NC	A	CE2	/BWd	/BWa	CLK	/WE	/OE	A	A	NC
C	DQPc	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQPb
D	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
E	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
F	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
G	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
K	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
L	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
M	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
N	DQPd	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DQPa
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	NC
R	MODE	NC	A	A	TMS	A0*	TCK	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
165-Ball, 13 mm x 15mm BGA

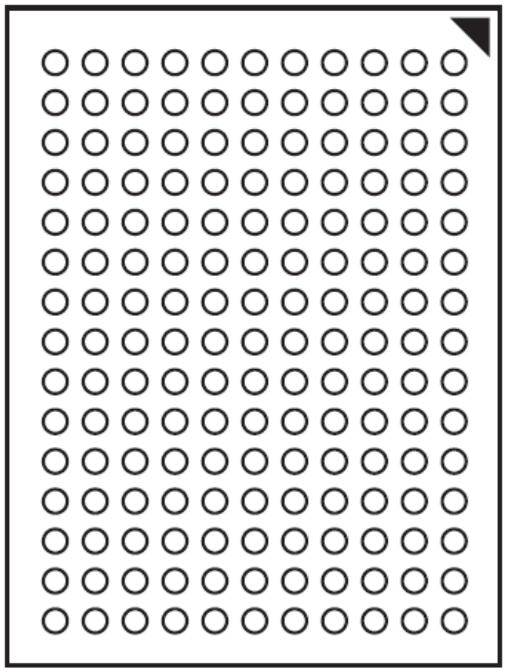
PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
/CKE	Clock Enable
A0,A1	Synchronous Burst Address Inputs
A	Address Inputs
ADV	Synchronous Burst Address Advance/Load
MODE	Burst Sequence Selection
/CE,CE2,/CE2	Synchronous Chip Enable
/WE	Synchronous Read/Write Control Input
/BWx (x=a-d)	Synchronous Byte Write Inputs
/OE	Output Enable
DQx	Data Inputs/Outputs
DQPx	Parity Data I/O
TCK,TDI, TDO,TMS	JTAG Pins
ZZ	Power Sleep Mode
NC	No Connect
V_{DD}	Power Supply
V_{DDQ}	I/O Power Supply
V_{SS}	Ground

512K x 32, 165-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	/CE	/BWc	/BWb	/CE2	/CKE	ADV	A	A	NC
B	NC	A	CE2	/BWd	/BWa	CLK	/WE	/OE	A	A	NC
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC
D	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
E	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
F	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
G	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
K	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
L	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
M	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
N	NC	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	NC
R	MODE	NC	A	A	TMS	A0*	TCK	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
165-Ball, 13 mm x 15mm BGA

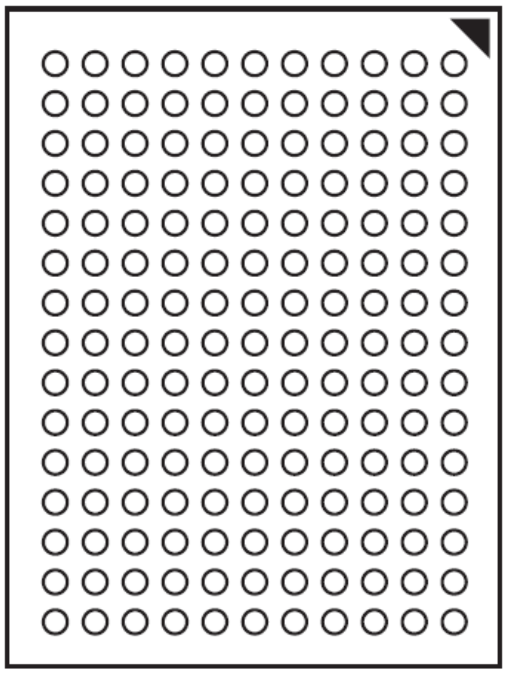
PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
/CKE	Clock Enable
A0,A1	Synchronous Burst Address Inputs
A	Address Inputs
ADV	Synchronous Burst Address Advance/Load
MODE	Burst Sequence Selection
/CE,CE2,/CE2	Synchronous Chip Enable
/WE	Synchronous Read/Write Control Input
/BWx (x=a-d)	Synchronous Byte Write Inputs
/OE	Output Enable
DQx	Data Inputs/Outputs
TCK,TDI, TDO,TMS	JTAG Pins
ZZ	Power Sleep Mode
NC	No Connect
V_{DD}	Power Supply
V_{DDQ}	I/O Power Supply
V_{SS}	Ground

1024K x 18, 165-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	/CE	/BWb	NC	/CE2	/CKE	ADV	A	A	A
B	NC	A	CE2	NC	/BWa	CLK	/WE	/OE	A	A	NC
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQPa
D	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
E	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
F	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
G	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
K	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
L	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
M	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
N	DQPb	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	NC
R	MODE	NC	A	A	TMS	A0*	TCK	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
165-Ball, 13 mm x 15mm BGA

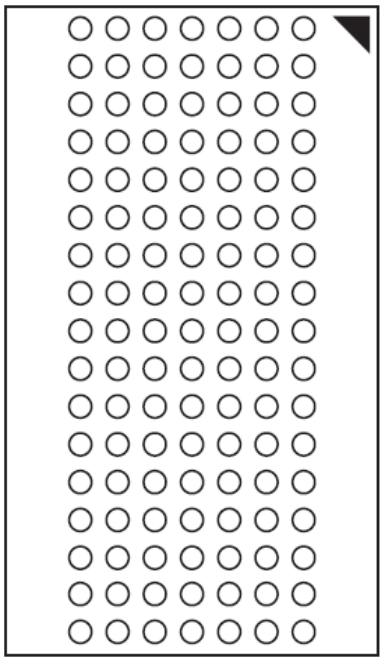
PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
/CKE	Clock Enable
A0,A1	Synchronous Burst Address Inputs
A	Address Inputs
ADV	Synchronous Burst Address Advance/Load
MODE	Burst Sequence Selection
/CE,CE2,/CE2	Synchronous Chip Enable
/WE	Synchronous Read/Write Control Input
/BWx (x=a-b)	Synchronous Byte Write Inputs
/OE	Output Enable
DQx	Data Inputs/Outputs
DQPx	Parity Data I/O
TCK,TDI, TDO,TMS	JTAG Pins
ZZ	Power Sleep Mode
NC	No Connect
V_{DD}	Power Supply
V_{DDQ}	I/O Power Supply
V_{SS}	Ground

512K x 36, 119-Ball BGA (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	A	A	A	V_{DDQ}
B	NC	CE2	A	ADV	A	/CE2	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	DQPc	V_{SS}	NC	V_{SS}	DQPb	DQb
E	DQc	DQc	V_{SS}	/CE	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	/OE	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	/BWc	A	/BWb	DQb	DQb
H	DQc	DQc	V_{SS}	/WE	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	V_{SS}	DQa	DQa
L	DQd	DQd	/BWd	NC	/BWa	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	/CKE	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A1*	V_{SS}	DQa	DQa
P	DQd	DQPd	V_{SS}	A0*	V_{SS}	DQPa	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
119-Ball, 14 mm x 22 mm BGA

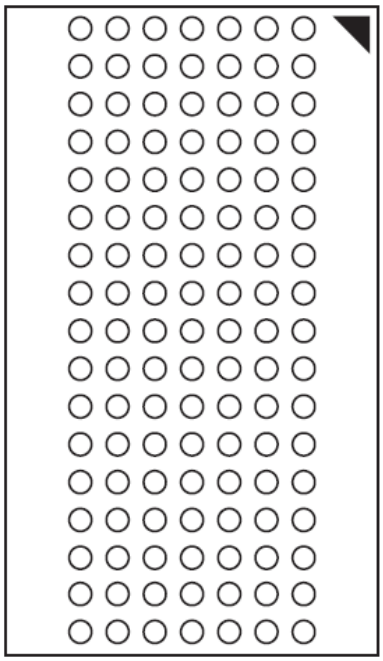
PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
/CKE	Clock Enable
A0,A1	Synchronous Burst Address Inputs
A	Address Inputs
ADV	Synchronous Burst Address Advance/Load
MODE	Burst Sequence Selection
/CE,CE2,/CE2	Synchronous Chip Enable
/WE	Synchronous Read/Write Control Input
/BWx (x=a-d)	Synchronous Byte Write Inputs
/OE	Output Enable
DQx	Data Inputs/Outputs
DQPx	Parity Data I/O
TCK,TDI, TDO,TMS	JTAG Pins
ZZ	Power Sleep Mode
NC	No Connect
V_{DD}	Power Supply
V_{DDQ}	I/O Power Supply
V_{SS}	Ground

512K x 32, 119-Ball BGA (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	A	A	A	V_{DDQ}
B	NC	CE2	A	ADV	A	/CE2	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	NC	V_{SS}	NC	V_{SS}	NC	DQb
E	DQc	DQc	V_{SS}	/CE	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	/OE	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	/BWc	A	/BWb	DQb	DQb
H	DQc	DQc	V_{SS}	/WE	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	V_{SS}	DQa	DQa
L	DQd	DQd	/BWd	NC	/BWa	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	/CKE	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A1*	V_{SS}	DQa	DQa
P	DQd	NC	V_{SS}	A0*	V_{SS}	NC	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.



Bottom View
119-Ball, 14 mm x 22 mm BGA

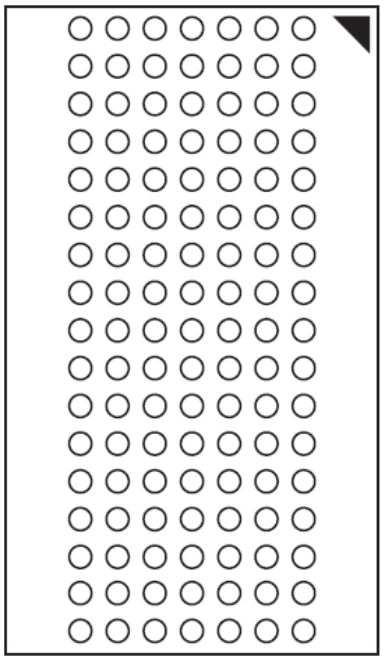
PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
/CKE	Clock Enable
A0,A1	Synchronous Burst Address Inputs
A	Address Inputs
ADV	Synchronous Burst Address Advance/Load
MODE	Burst Sequence Selection
/CE,CE2,/CE2	Synchronous Chip Enable
/WE	Synchronous Read/Write Control Input
/BWx (x=a-d)	Synchronous Byte Write Inputs
/OE	Output Enable
DQx	Data Inputs/Outputs
TCK,TDI, TDO,TMS	JTAG Pins
ZZ	Power Sleep Mode
NC	No Connect
V_{DD}	Power Supply
V_{DDQ}	I/O Power Supply
V_{SS}	Ground

1024K x 18, 119-Ball BGA (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	A	A	A	V_{DDQ}
B	NC	CE2	A	ADV	A	/CE2	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQPa	NC
E	NC	DQb	V_{SS}	/CE	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	/OE	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	/BWb	A	NC	NC	DQa
H	DQb	NC	VSS	/WE	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	VSS	CLK	V_{SS}	NC	DQa
L	DQb	NC	NC	NC	/BWa	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	/CKE	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	A1*	V_{SS}	DQa	NC
P	NC	DQPb	V_{SS}	A0*	V_{SS}	NC	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

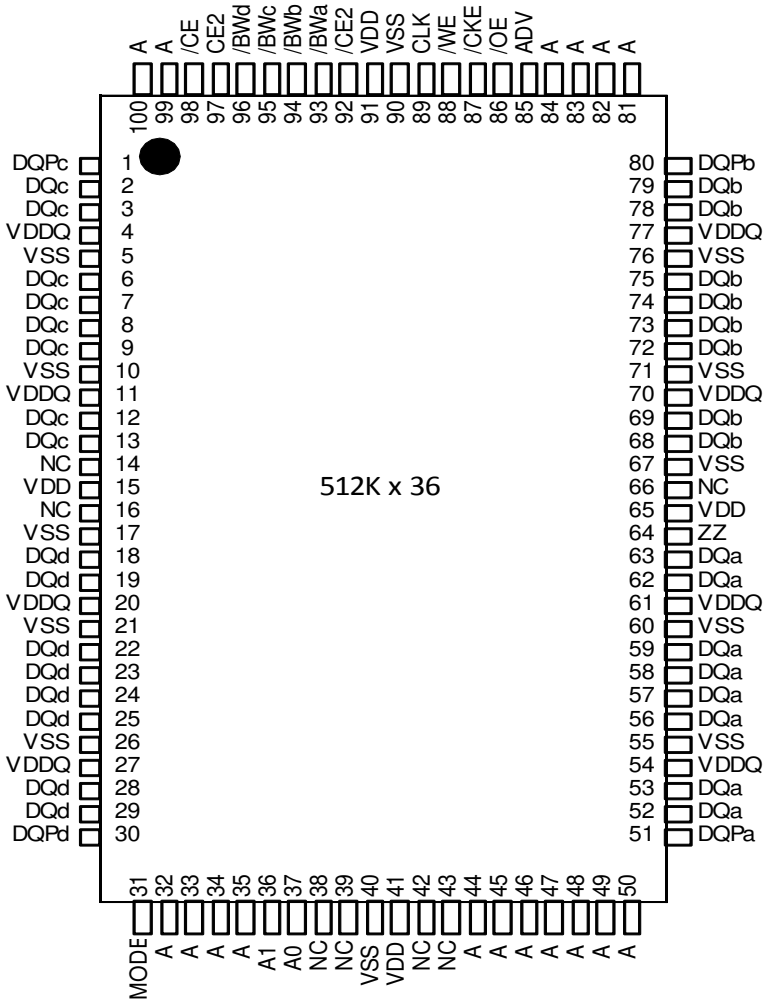


Bottom View
119-Ball, 14 mm x 22 mm BGA

PIN DESCRIPTIONS

Symbol	Pin Name
CLK	Synchronous Clock
/CKE	Clock Enable
A0,A1	Synchronous Burst Address Inputs
A	Address Inputs
ADV	Synchronous Burst Address Advance/Load
MODE	Burst Sequence Selection
/CE,CE2,/CE2	Synchronous Chip Enable
/WE	Synchronous Read/Write Control Input
/BWx (x=a-b)	Synchronous Byte Write Inputs
/OE	Output Enable
DQx	Data Inputs/Outputs
DQPx	Parity Data I/O
TCK,TDI, TDO,TMS	JTAG Pins
ZZ	Power Sleep Mode
NC	No Connect
V_{DD}	Power Supply
V_{DDQ}	I/O Power Supply
V_{SS}	Ground

512K x 36, 100PIN QFP (Top View)

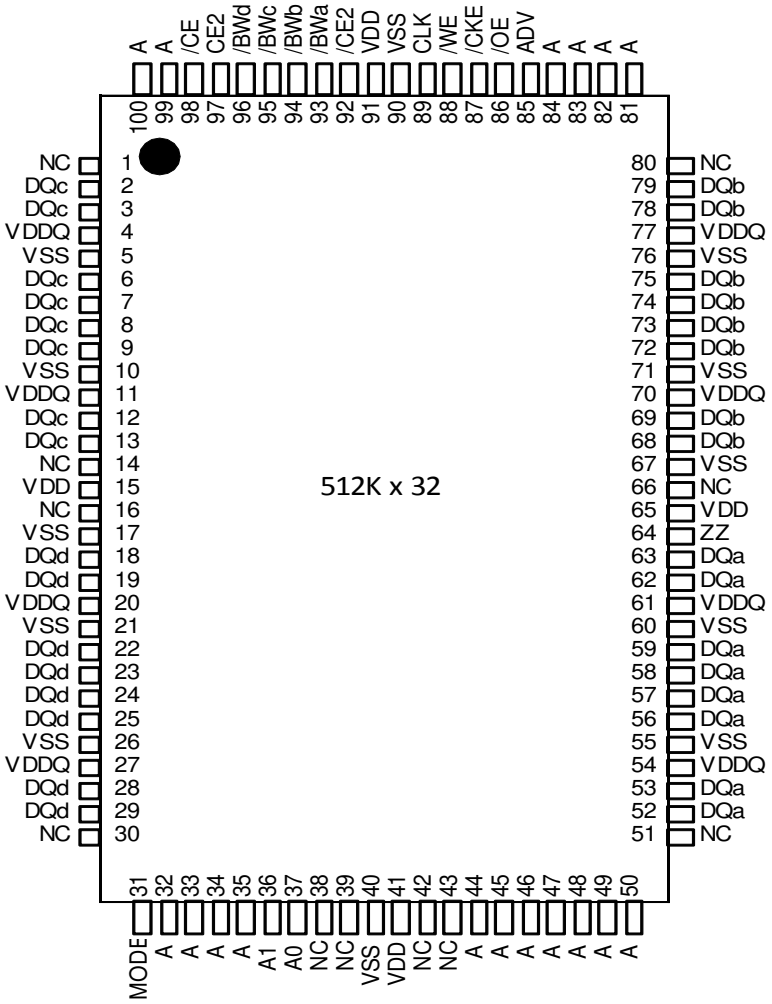


Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name	Symbol	Pin Name
A	Address Inputs	ZZ	Power Sleep Mode
A0,A1	Synchronous Burst Address Inputs	MODE	Burst Sequence Selection
ADV	Synchronous Burst Address Advance/Load	V_{DD}	Power Supply
/WE	Synchronous Read/Write Control Input	NC	No Connect
CLK	Synchronous Clock	DQx	Data Inputs/Outputs
/CKE	Clock Enable	DQPx	Parity Data I/O; NC for x32 option
/CE,CE2,/CE2	Synchronous Chip Enable	V_{DDQ}	I/O Power Supply
/BWx (x=a-d)	Synchronous Byte Write Inputs	V_{SS}	Ground
/OE	Output Enable		

512K x 32, 100PIN QFP (Top View)

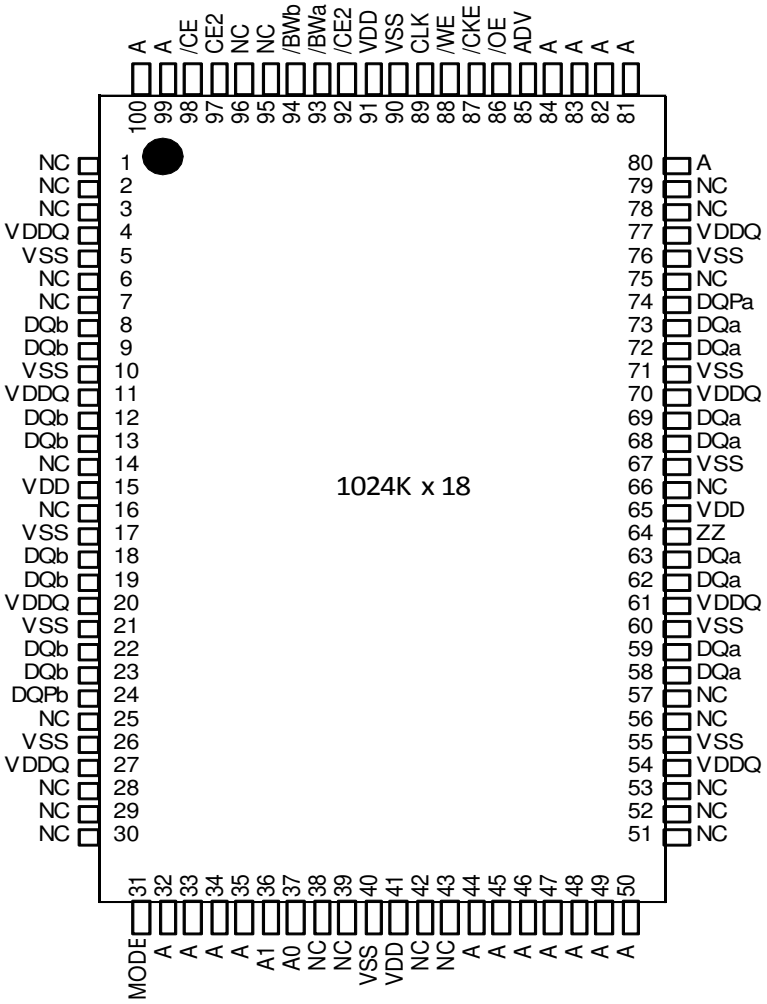


Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name	Symbol	Pin Name
A	Address Inputs	ZZ	Power Sleep Mode
A0,A1	Synchronous Burst Address Inputs	MODE	Burst Sequence Selection
ADV	Synchronous Burst Address Advance/Load	V_{DD}	Power Supply
/WE	Synchronous Read/Write Control Input	NC	No Connect
CLK	Synchronous Clock	DQx	Data Inputs/Outputs
/CKE	Clock Enable	DQPx	Parity Data I/O; NC for x32 option
/CE,CE2,/CE2	Synchronous Chip Enable	V_{DDQ}	I/O Power Supply
/BWx (x=a-d)	Synchronous Byte Write Inputs	V_{SS}	Ground
/OE	Output Enable		

1024K x 18, 100PIN QFP (Top View)

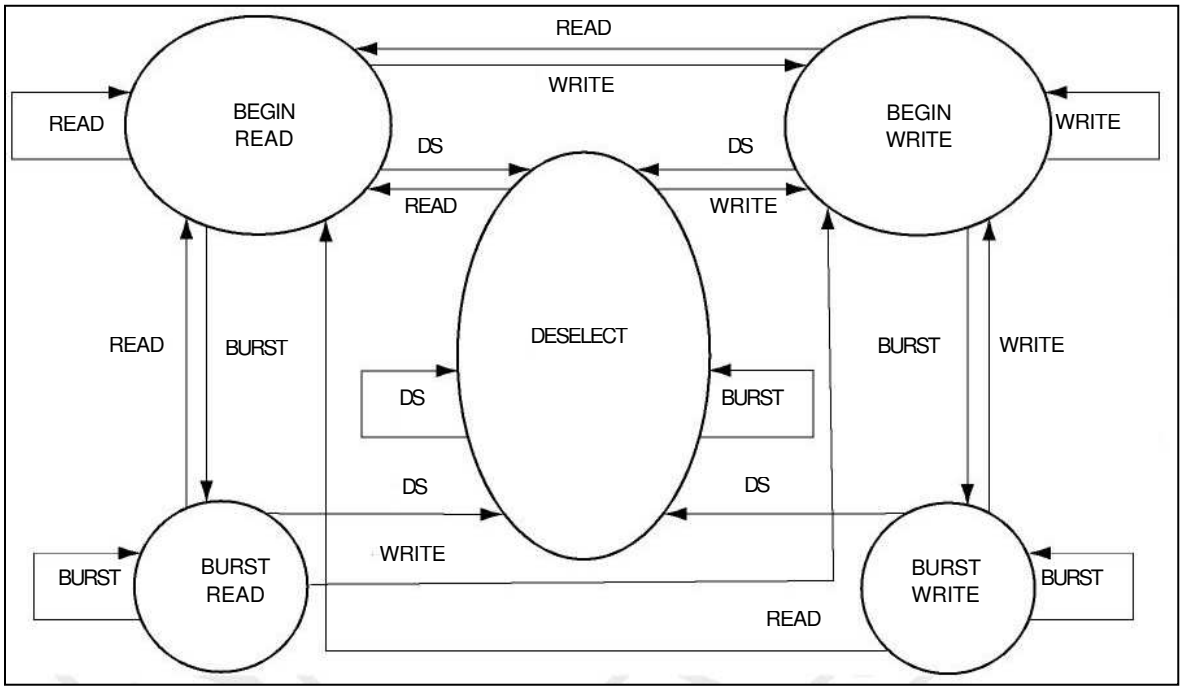


Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name	Symbol	Pin Name
A	Address Inputs	ZZ	Power Sleep Mode
A0,A1	Synchronous Burst Address Inputs	MODE	Burst Sequence Selection
ADV	Synchronous Burst Address Advance/Load	V_{DD}	Power Supply
/WE	Synchronous Read/Write Control Input	NC	No Connect
CLK	Synchronous Clock	DQx	Data Inputs/Outputs
/CKE	Clock Enable	DQPx	Parity Data I/O
/CE,CE2,/CE2	Synchronous Chip Enable	V_{DDQ}	I/O Power Supply
/BWx (x=a-b)	Synchronous Byte Write Inputs	V_{SS}	Ground
/OE	Output Enable		

STATE DIAGRAM



TRUTH TABLE

SYNCHRONOUS TRUTH TABLE

Operation	Address Used	/CE	CE2	/CE2	ADV	/WE	/BWx	/OE	/CKE	CLK
Not Selected	N/A	H	X	X	L	X	X	X	L	↑
Not Selected	N/A	X	L	X	L	X	X	X	L	↑
Not Selected	N/A	X	X	H	L	X	X	X	L	↑
Not Selected Continue	N/A	X	X	X	H	X	X	X	L	↑
Begin Burst Read	External Address	L	H	L	L	H	X	L	L	↑
Continue Burst Read	Next Address	X	X	X	H	X	X	L	L	↑
NOP/Dummy Read	External Address	L	H	L	L	H	X	H	L	↑
Dummy Read	Next Address	X	X	X	H	X	X	H	L	↑
Begin Burst Write	External Address	L	H	L	L	L	L	X	L	↑
Continue Burst Write	Next Address	X	X	X	H	X	L	X	L	↑
NOP/Write Abort	N/A	L	H	L	L	L	H	X	L	↑
Write Abort	Next Address	X	X	X	H	X	H	X	L	↑
Ignore Clock	Current Address	X	X	X	X	X	X	X	H	↑

Notes:
1. "X" means don't care.
2. The rising edge of clock is symbolized by ↑
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. /WE = L means Write operation in Write Truth Table.
5. /WE = H means Read operation in Write Truth Table.
6. Operation finally depends on status of asynchronous pins (ZZ and /OE).

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	/OE	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes:
1. X means "Don't Care".
2. For write cycles following read cycles, the output buffers must be disabled with /OE, otherwise data bus contention will occur.
3. Sleep Mode means power Sleep Mode where stand-by current does not depend on cycle time.
4. Deselected means power Sleep Mode where stand-by current depends on cycle time.

WRITE TRUTH TABLE (x18)

Operation	/WE	/BWa	/BWb
READ	H	X	X
WRITE BYTE a	L	L	H
WRITE BYTE b	L	H	L
WRITE ALL BYTEs	L	L	L
WRITE ABORT/NOP	L	H	H

Notes:
1. X means "Don't Care".
2. All inputs in this table must beet setup and hold time around the rising edge of CLK.

WRITE TRUTH TABLE (x36)

Operation	/WE	/BWa	/BWb	/BWc	/BWd
READ	H	X	X	X	X
WRITE BYTE a	L	L	H	H	H
WRITE BYTE b	L	H	L	H	H
WRITE BYTE c	L	H	H	L	H
WRITE BYTE d	L	H	H	H	L
WRITE ALL BYTEs	L	L	L	L	L
WRITE ABORT/NOP	L	H	H	H	H

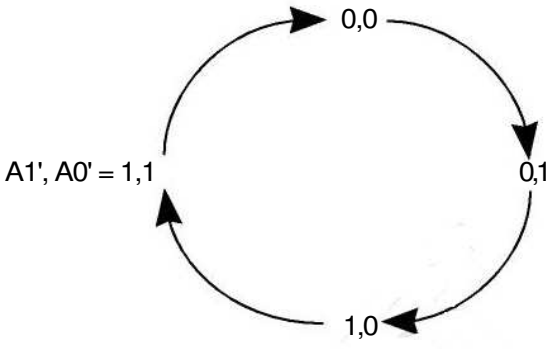
Notes:
1. X means "Don't Care".
2. All inputs in this table must beet setup and hold time around the rising edge of CLK.

ADDRESS SEQUENCE IN BURST MODE

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or NC)

External Address	1st Burst Address	2nd Burst Address	3rd Burst Address
A1 A0	A1 A0	A1 A0	A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = V_{ss})



Power Up Sequence

V_{DDQ} → V_{DD}[1] → I/O Pins[2]

Notes:
1. V_{DD} can be applied at the same time as V_{DDQ}
2. Applying I/O inputs is recommended after V_{DDQ} is stable. The inputs of the I/O pins can be applied at the same time as V_{DDQ} as long as Vih (level of I/O pins) is lower than V_{DDQ}.

ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	NLF Value	NVF/NVVF Value	Unit
Tstg	Storage Temperature	–65 to +150	–65 to +150	°C
Pd	Power Dissipation	1.6	1.6	W
Iout	Output Current (per I/O)	20	20	mA
Vin, Vout	Voltage Relative to Vss for I/O Pins	–0.5 to V_{DD}+0.3	–0.5 to V_{DDQ} + 0.3	V
Vin	Voltage Relative to Vss for Address and Control Inputs	–0.3 to V_{DD}+0.5	–0.3 to V_{DDQ} + 0.3	V

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE (IS61NLFx)

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V ± 5%	3.3V / 2.5V ± 5%
Industrial	-40°C to +85°C	3.3V ± 5%	3.3V / 2.5V ± 5%
Automotive	-40°C to +125°C	3.3V ± 5%	3.3V / 2.5V ± 5%

OPERATING RANGE (IS61NVFx)

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	2.5V ± 5%	2.5V ± 5%
Industrial	-40°C to +85°C	2.5V ± 5%	2.5V ± 5%
Automotive	*Please contact ISSI		

OPERATING RANGE (IS61NVVFx)

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	1.8V ± 5%	1.8V ± 5%
Industrial	-40°C to +85°C	1.8V ± 5%	1.8V ± 5%
Automotive	*Please contact ISSI		

CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS (Over operating temperature range)

Symbol	Parameter	Test Conditions	3.3V		2.5V		1.8V		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Voh	Output HIGH Voltage	Ioh=-4.0 mA(3.3V) Ioh=–1.0 mA(2.5V,1.8V)	2.4	—	2.0	—	V_{DDQ} -0.4	—	V
Vol	Output LOW Voltage	Iol=8.0 mA(3.3V) Iol=1.0 mA(2.5V,1.8V)	—	0.4	—	0.4	—	0.4	V
Vih	Input HIGH Voltage		2.0	V_{DD} +0.3	1.7	V_{DD} +0.3	0.7* V_{DD}	V_{DD} +0.3	V
Vil	Input LOW Voltage		–0.3	0.8	–0.3	0.7	–0.3	0.3* V_{DD}	V
Ili	Input Leakage Current	Vss≤Vin≤ V_{DD}	–1	1	–1	1	–1	1	µA
Ilo	Output Leakage Current	Vss≤Vout≤ V_{DDQ},/OE=Vih	–1	1	–1	1	–1	1	µA

Notes:
1. All voltages referenced to ground.
2. Overshoot:
   3.3V and 2.5V: Vih (AC) ≤ V_{DD} + 1.5V (Pulse width less than tkc /2)
   1.8V: Vih (AC) ≤ V_{DD} + 0.5V (Pulse width less than tkc /2)
3. Undershoot:
   3.3V and 2.5V: Vil (AC) ≥ -1.5V (Pulse width less than tkc /2)
   1.8V: Vil (AC) ≥ -0.5V (Pulse width less than tkc /2)
4. MODE pin has an internal pull-up and should be tied to V_{DD} or Vss . It exhibits ±100µA maximum leakage current when tied to ≤Vss+0.2V or ≥ V_{DD} – 0.2V.
5. ZZ pin has an internal pull-down and should be tied to V_{DD} or Vss . It exhibits ±100µA maximum leakage current when tied to ≤Vss+0.2V or ≥ V_{DD}–0.2V.

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Temp. range	-6.5		-7.5		Unit
				Max		Max		
				x18	x36	x18	x36	
Icc	AC Operating, Supply Current	Device Selected, OE = Vih, ZZ ≤ Vil,All Inputs ≤ 0.2V or ≥ V_{DD} – 0.2V,Cycle Time ≥ tkc min.	Com.	240	240	190	190	mA
			Ind.	260	260	210	210	
Isb	Standby Current TTL Input	Device Deselected, V_{DD} = Max.,All Inputs ≤ Vil or ≥ Vih,ZZ ≤ Vil, f = Max.	Com.	80	80	70	70	mA
			Ind.	90	90	80	80	
Isb1	Standby Current CMOS Input	Device Deselected, V_{DD} = Max.,Vin ≤ Vss + 0.2V or ≥ V_{DD} – 0.2V,f = 0	Com.	60	60	60	60	mA
			Ind.	70	70	70	70	

Note:
1. Power-up assumes a linear ramp from 0V to V_{DD} (min) within 200ms. During this time Vih < V_{DD} and V_{DDQ} < V_{DD}

CAPACITANCE

Symbol	Parameter	Conditions	Max.	Unit
Cin	Input Capacitance	Vin = 0V	6	pF
Cout	Input/Output Capacitance	Vout = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: Ta = 25°C, f = 1 MHz, V_{DD} = 3.3V.

READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-6.5		-7.5		Unit
		Min.	Max.	Min.	Max.	
fmax	Clock Frequency	—	133	—	117	MHz
tkc	Cycle Time	7.5	—	8.5	—	ns
tkh	Clock High Time	2.2	—	2.5	—	ns
tkl	Clock Low Time	2.2	—	2.5	—	ns
tkq	Clock Access Time	—	6.5	—	7.5	ns
tkqx(2)	Clock High to Output Invalid	2.5	—	2.5	—	ns
tkqlz(2,3)	Clock High to Output Low-Z	2.5	—	2.5	—	ns
tkqhz(2,3)	Clock High to Output High-Z	—	3.8	—	4.0	ns
toeq	Output Enable to Output Valid	—	3.2	—	3.4	ns
toelz(2,3)	Output Enable to Output Low-Z	0	—	0	—	ns
toehz(2,3)	Output Disable to Output High-Z	—	3.5	—	3.5	ns
tas	Address Setup Time	1.5	—	1.5	—	ns
tws	Read/Write Setup Time	1.5	—	1.5	—	ns
tces	Chip Enable Setup Time	1.5	—	1.5	—	ns
tse	Clock Enable Setup Time	1.5	—	1.5	—	ns
tadvs	Address Advance Setup Time	1.5	—	1.5	—	ns
tds	Data Setup Time	1.5	—	1.5	—	ns
tah	Address Hold Time	0.5	—	0.5	—	ns
the	Clock Enable Hold Time	0.5	—	0.5	—	ns
twh	Write Hold Time	0.5	—	0.5	—	ns
tceh	Chip Enable Hold Time	0.5	—	0.5	—	ns
tadvh	Address Advance Hold Time	0.5	—	0.5	—	ns
tdh	Data Hold Time	0.5	—	0.5	—	ns

Notes:
1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
V_{TT}	1.5V
V_{LOAD}	3.3V
R1, R2	317Ω, 351Ω
Output Load	See Figures 1 and 2

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.25V
V_{TT}	1.25V
V_{LOAD}	2.5V
R1, R2	1667Ω, 1538Ω
Output Load	See Figures 1 and 2

1.8V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 1.8V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	0.9V
V_{TT}	0.9V
V_{LOAD}	1.8V
R1, R2	1KΩ, 1KΩ
Output Load	See Figures 1 and 2

I/O OUTPUT LOAD EQUIVALENT

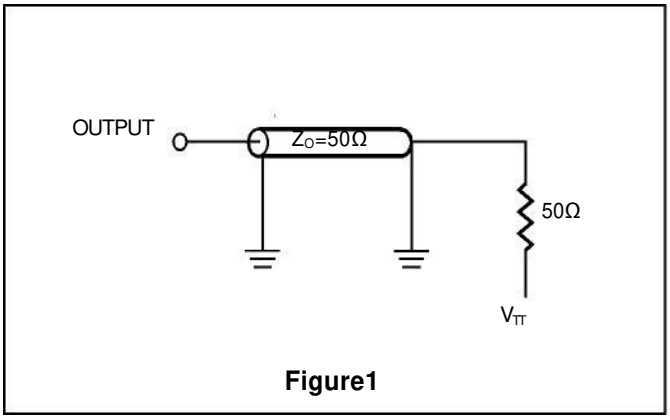


Figure1

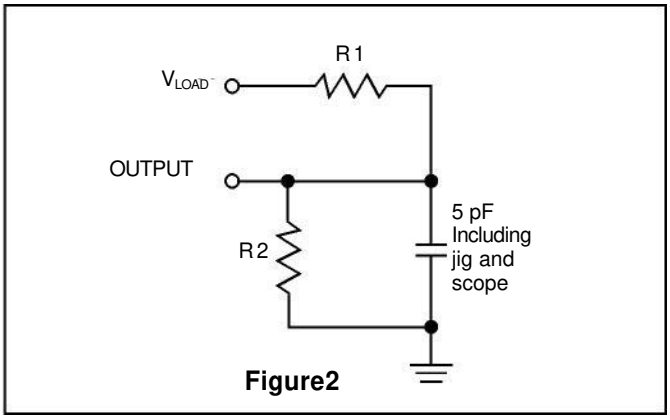
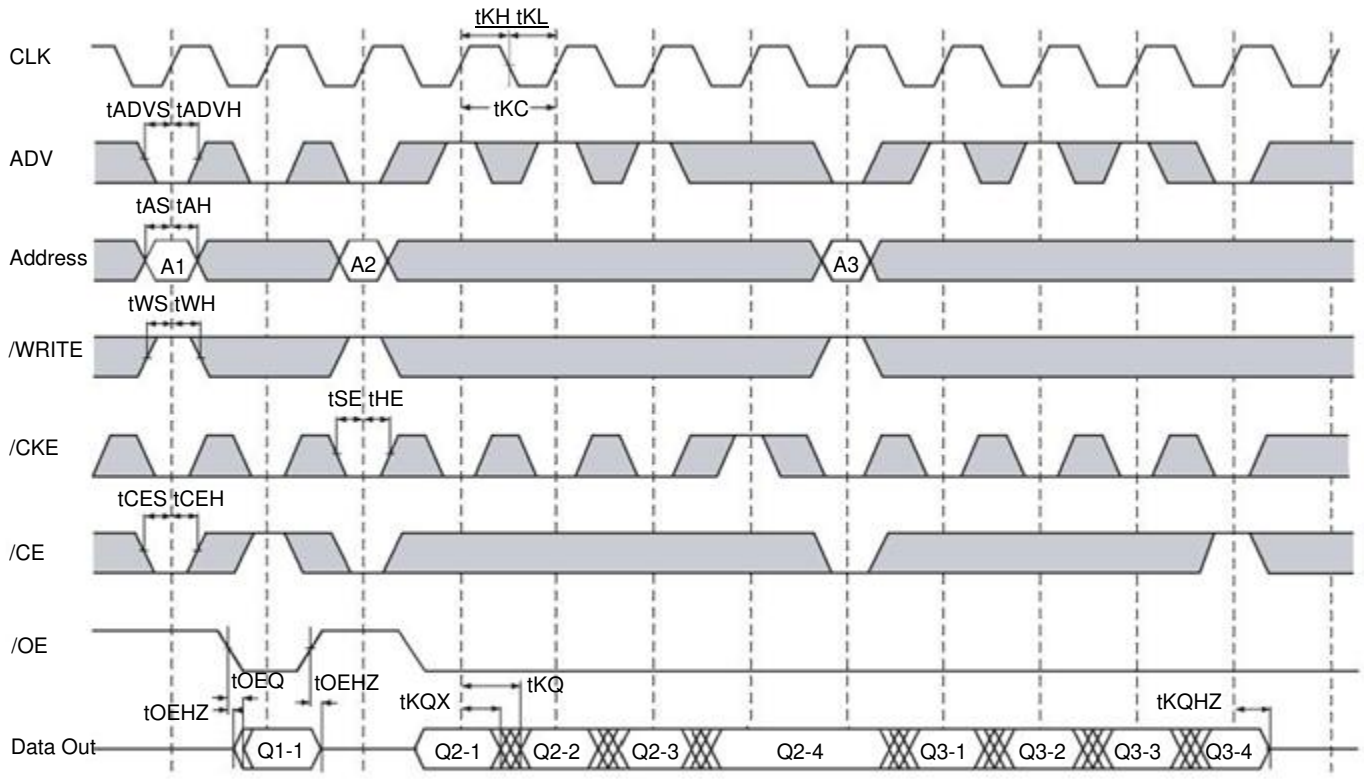
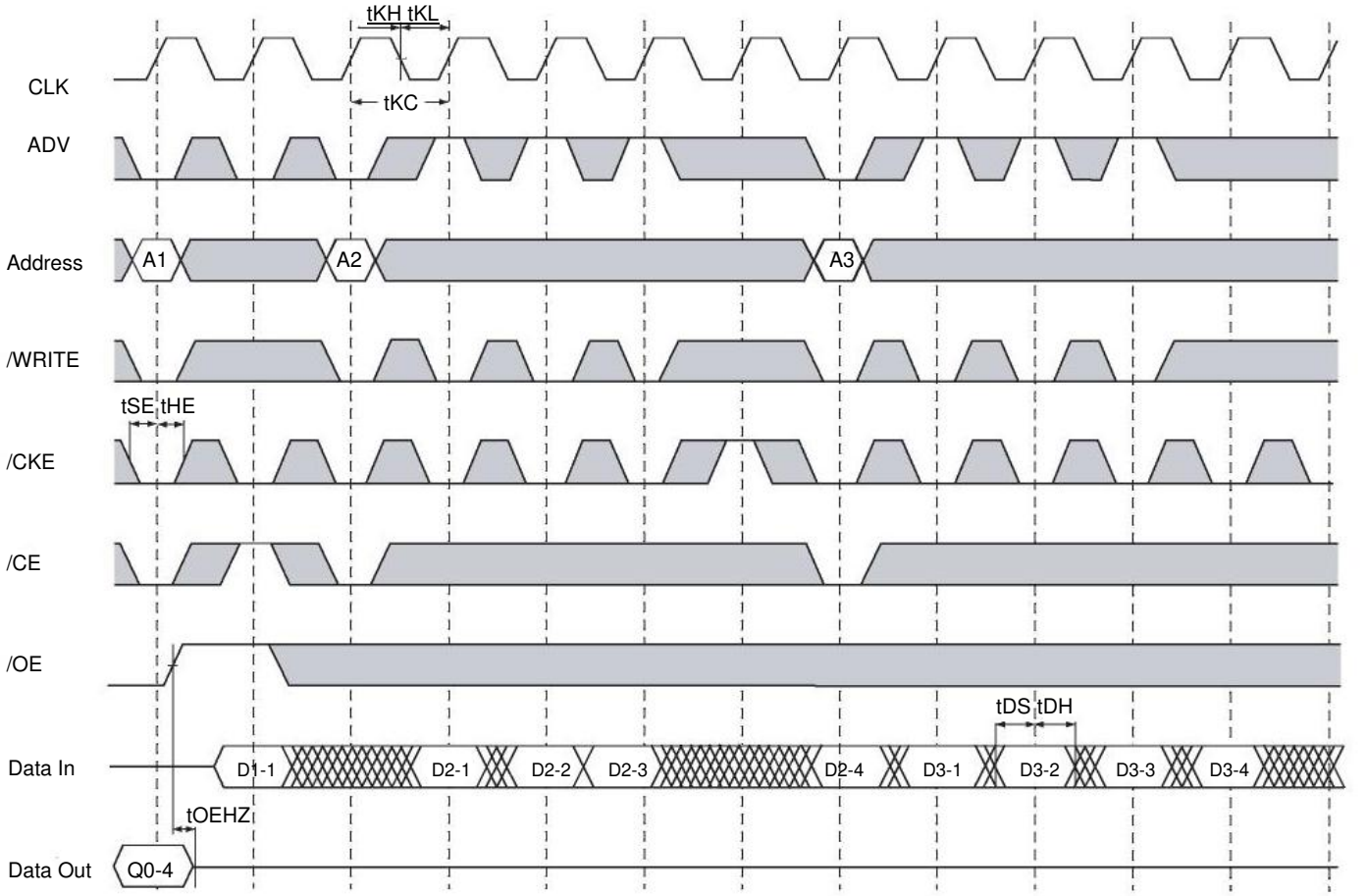


Figure2

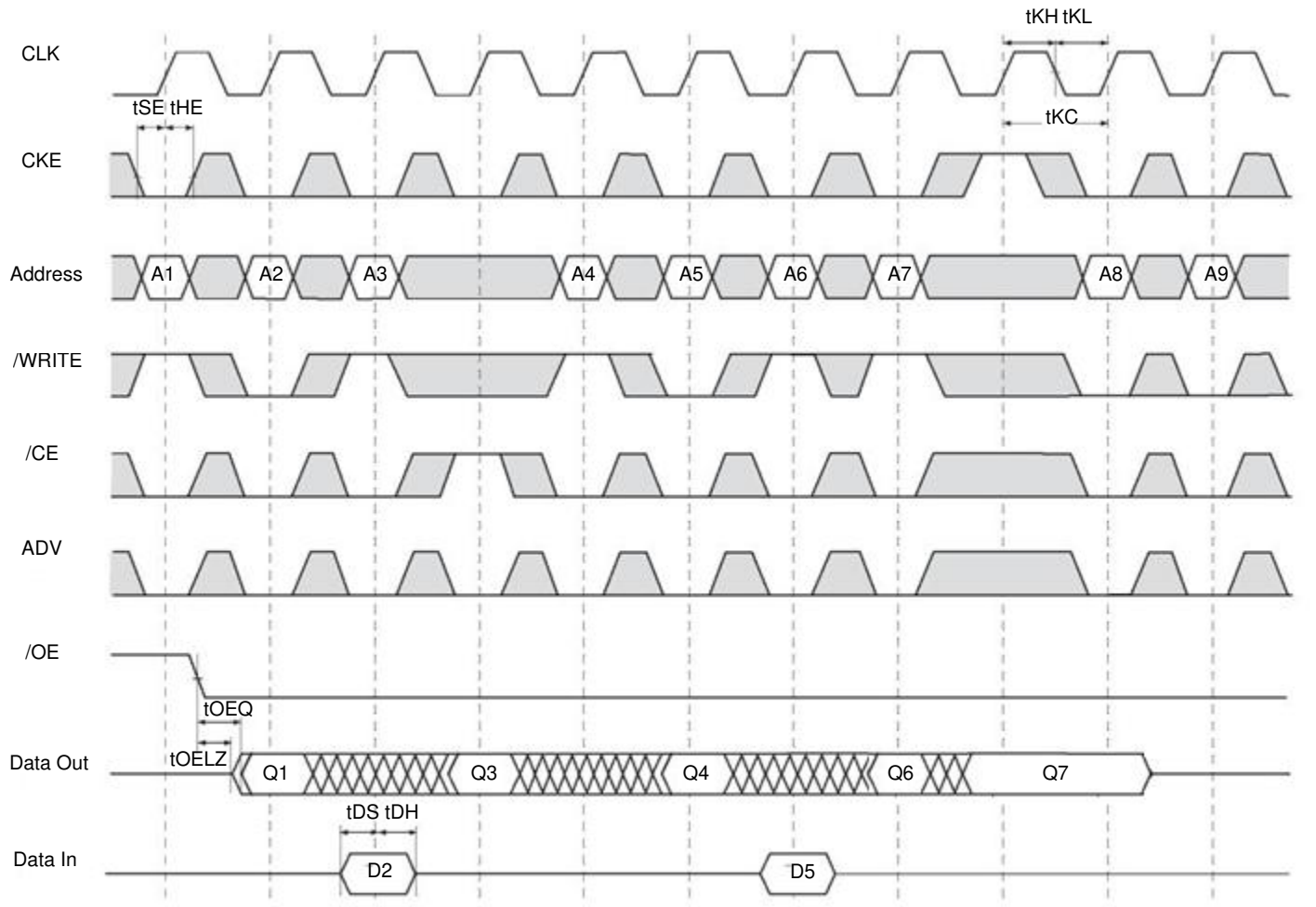
READ CYCLE TIMING



WRITE CYCLE TIMING

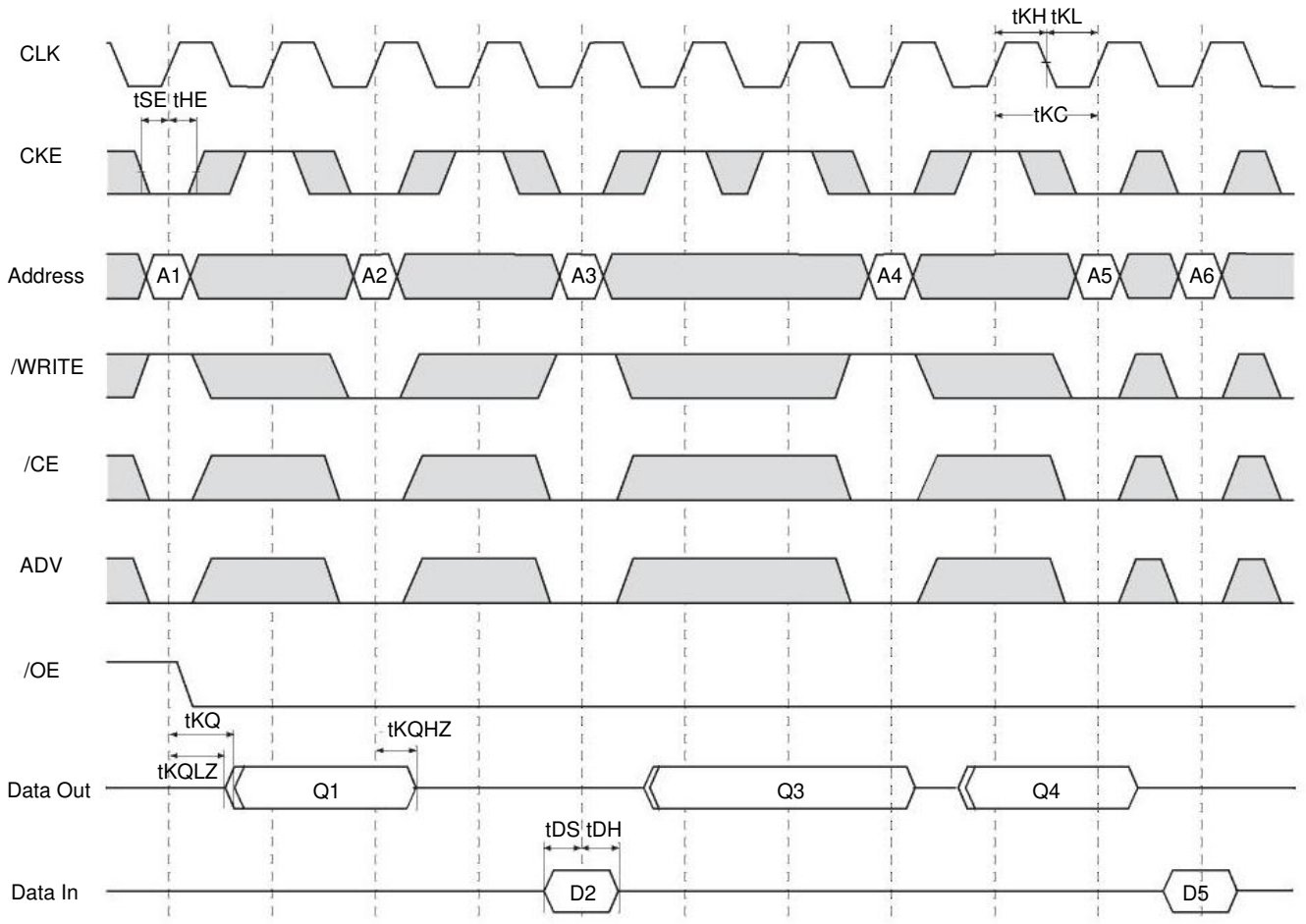


SINGLE READ/WRITE CYCLE TIMING



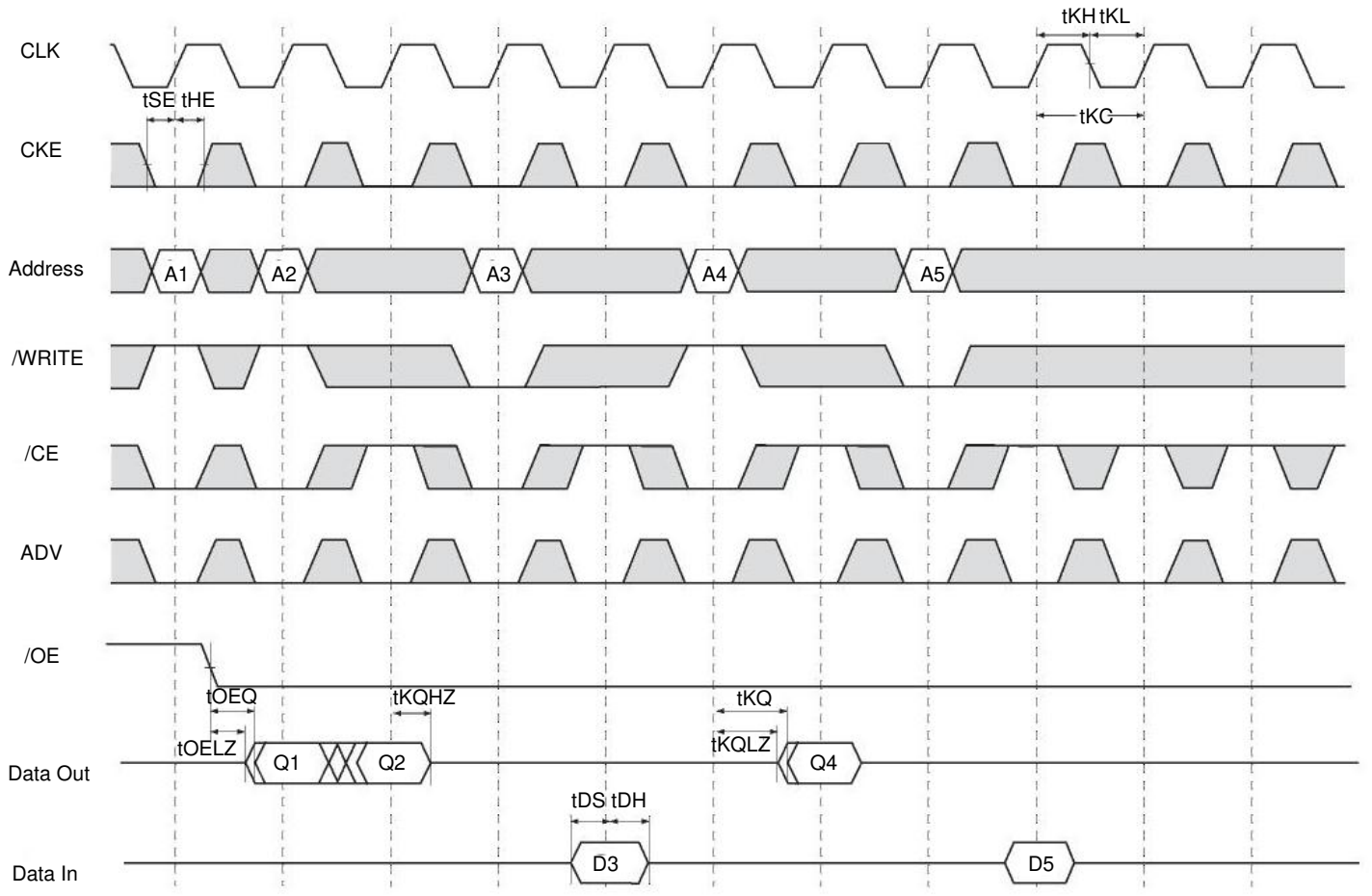
NOTES: /WRITE = L means /WE = L and /BW_X = L
/CE = L means /CE1 = L, CE2 = H and /CE2 = L
/CE = H means /CE1= H, or /CE1 = L and /CE2 = H, or /CE1 = L and CE2 = L

/CKE OPERATION TIMING



NOTES: /WRITE = L means /WE = L and /BW_X = L
/CE = L means /CE1 = L, CE2 = H and /CE2 = L
/CE = H means /CE1= H, or /CE1 = L and /CE2 = H, or /CE1 = L and CE2 = L

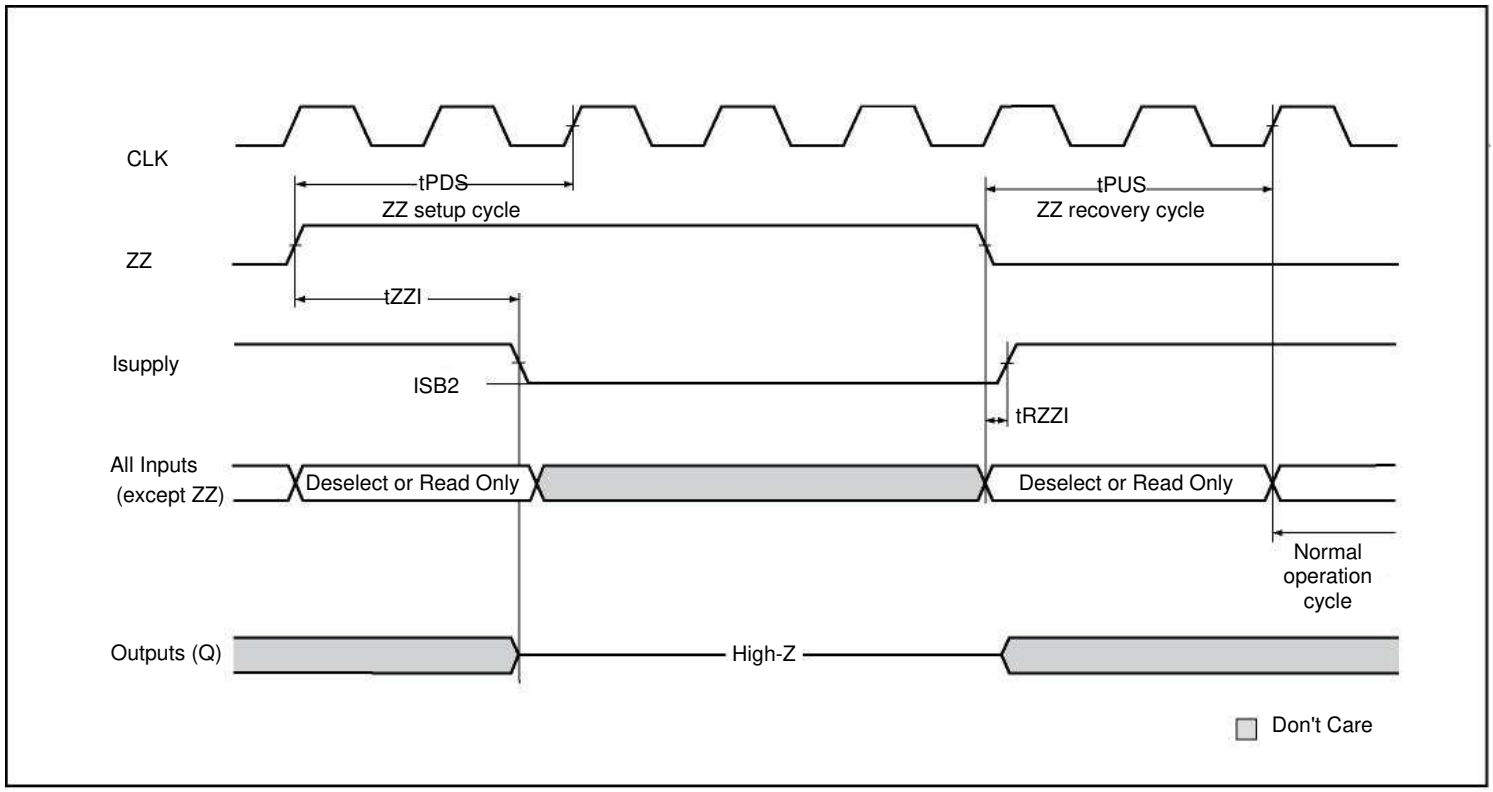
/CE OPERATION TIMING



SNOOZE MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Temperature Range	Min.	Max.	Unit
ISB2	Current during SNOOZE MODE	ZZ ≥ Vih	Com.	—	40	mA
			Ind.	—	50	
			Auto.	—	TBD	
tPDS	ZZ active to input ignored		—	—	2	cycle
tPUS	ZZ inactive to input sampled		—	2	—	cycle
tZZI	ZZ active to SNOOZE current		—	—	2	cycle
tRZZI	ZZ inactive to exit SNOOZE current		—	0	—	ns

SLEEP MODE TIMING



IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE Standard 1149.1, the SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

The TAP controller has a standard 16-state machine that resets internally on power-up. Therefore, a TRST signal is not required

Disabling the JTAG feature

The SRAM can operate without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (VSS) to prevent clocking of the device. TDI and TMS are internally pulled up and may be left disconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left disconnected. On power-up, the device will come up in a reset state, which will not interfere with device operation.

Test Access Port Signal List:

1. Test Clock (TCK)
This signal uses V_{DD} as a power supply. The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

2. Test Mode Select (TMS)
This signal uses V_{DD} as a power supply. The TMS input is used to send commands to the TAP controller and is sampled on the rising edge of TCK.

3. Test Data-In (TDI)
This signal uses V_{DD} as a power supply. The TDI input is used to serially input test instructions and information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is connected to the most significant bit (MSB) of any register. For more information regarding instruction register loading, please see the TAP Controller State Diagram.

4. Test Data-Out (TDO)
This signal uses V_{DDQ} as a power supply. The TDO output ball is used to serially clock test instructions and data out from the registers. The TDO output driver is only active during the Shift-IR and Shift-DR TAP controller states. In all other states, the TDO pin is in a High-Z state. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. For more information, please see the TAP Controller State Diagram.