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2Mx18, 1Mx36 36Mb QUADP (Burst 4) SYNCHRONOUS SRAM (2.5 Cycle Read Latency)

JANUARY 2015

FEATURES

- 1Mx36 and 2Mx18 configuration available.
 - On-chip Delay-Locked Loop (DLL) for wide data valid window.
 - Separate independent read and write ports with concurrent read and write operations.
 - Synchronous pipeline read with late write operation.
 - Double Data Rate (DDR) interface for read and write input ports.
 - 2.5 cycle read latency.
 - Fixed 4-bit burst for read and write operations.
 - Clock stop support.
 - Two input clocks (K and K#) for address and control registering at rising edges only.
 - Two echo clocks (CQ and CQ#) that are delivered simultaneously with data.
 - Data Valid Pin (QVLD).
 - +1.8V core power supply and 1.5, 1.8V VDDQ, used with 0.75, 0.9V VREF.
 - HSTL input and output levels.
 - Registered addresses, write and read controls, byte writes, data in, and data outputs.
 - Full data coherency.
 - Boundary scan using limited set of JTAG 1149.1 functions.
 - Byte write capability.
 - Fine ball grid array (FBGA) package:
 - 13mmx15mm and 15mmx17mm body size
 - 165-ball (11 x 15) array
 - Programmable impedance output drivers via 5x user-supplied precision resistor.
 - ODT (On Die Termination) feature is supported optionally on data input, K/K#, and BW,#.
 - The end of top mark (A/A1/A2) is to define options.
 - IS61QDPB41M36A : Don't care ODT function and pin connection
 - IS61QDPB41M36A1 : Option1
 - IS61QDPB41M36A2 : Option2
- Refer to more detail description at page 6 for each ODT option.

DESCRIPTION

The 36Mb IS61QDPB41M36A/A1/A2 and IS61QDPB42M18A/A1/A2 are synchronous, high-performance CMOS static random access memory (SRAM) devices. These SRAMs have separate I/Os, eliminating the need for high-speed bus turnaround. The rising edge of K clock initiates the read/write operation, and all internal operations are self-timed. Refer to the *Timing Reference Diagram for Truth Table* for a description of the basic operations of these QUADP (Burst of 4) SRAMs. Read and write addresses are registered on alternating rising edges of the K clock. Reads and writes are performed in double data rate.

The following are registered internally on the rising edge of the K clock:

- Read/write address
- Read enable
- Write enable
- Byte writes for burst addresses 1 and 3
- Data-in for burst addresses 1 and 3

The following are registered on the rising edge of the K# clock:

- Byte writes for burst addresses 2 and 4
- Data-in for burst addresses 2 and 4

Byte writes can change with the corresponding data-in to enable or disable writes on a per-byte basis. An internal write buffer enables the data-ins to be registered one cycle after the write address. The first data-in burst is clocked one cycle later than the write command signal, and the second burst is timed to the following rising edge of the K# clock. Two full clock cycles are required to complete a write operation.

During the burst read operation, the data-outs from the first and third bursts are updated from output registers of the third and fourth rising edges of the K# clock (starting 2.5 cycles later after read command). The data-outs from the second and fourth bursts are updated with the fourth and fifth rising edges of the K clock where the read command receives at the first rising edge of K. Two full clock cycles are required to complete a read operation.

The device is operated with a single +1.8V power supply and is compatible with HSTL I/O interfaces.

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- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
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Package ballout and description

x36 FBGA Ball ballout (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	NC/SA ¹	NC/SA ¹	W#	BW ₂ #	K#	BW ₁ #	R#	SA	NC/SA ¹	CQ
B	Q27	Q18	D18	SA	BW ₃ #	K	BW ₀ #	SA	D17	Q17	Q8
C	D27	Q28	D19	V _{SS}	SA	NC	SA	V _{SS}	D16	Q7	D8
D	D28	D20	Q19	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	Q16	D15	D7
E	Q29	D29	Q20	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	Q13	D13	D5
H	Doff#	V _{REF}	V _{DDQ}	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	V _{DDQ}	V _{REF}	ZQ
J	D31	Q31	D23	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	D10	Q1	D2
N	D34	D26	Q25	V _{SS}	SA	SA	SA	V _{SS}	Q10	D9	D1
P	Q35	D35	Q26	SA	SA	QVLD	SA	SA	Q9	D0	Q0
R	TDO	TCK	SA	SA	SA	ODT	SA	SA	SA	TMS	TDI

Notes:

- The following balls are reserved for higher densities: 3A for 72Mb, 10A for 144Mb, and 2A for 288Mb.

x18 FBGA Ball ballout (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	NC/SA ¹	SA	W#	BW ₁ #	K#	NC/SA ¹	R#	SA	NC/SA ¹	CQ
B	NC	Q9	D9	SA	NC	K	BW ₀ #	SA	NC	NC	Q8
C	NC	NC	D10	V _{SS}	SA	NC	SA	V _{SS}	NC	Q7	D8
D	NC	D11	Q10	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	NC	NC	D7
E	NC	NC	Q11	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	NC	D5
H	Doff#	V _{REF}	V _{DDQ}	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	V _{DDQ}	V _{REF}	ZQ
J	NC	NC	D14	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	NC	Q2
M	NC	NC	D16	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	NC	Q1	D2
N	NC	D17	Q16	V _{SS}	SA	SA	SA	V _{SS}	NC	NC	D1
P	NC	NC	Q17	SA	SA	QVLD	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	ODT	SA	SA	SA	TMS	TDI

Notes:

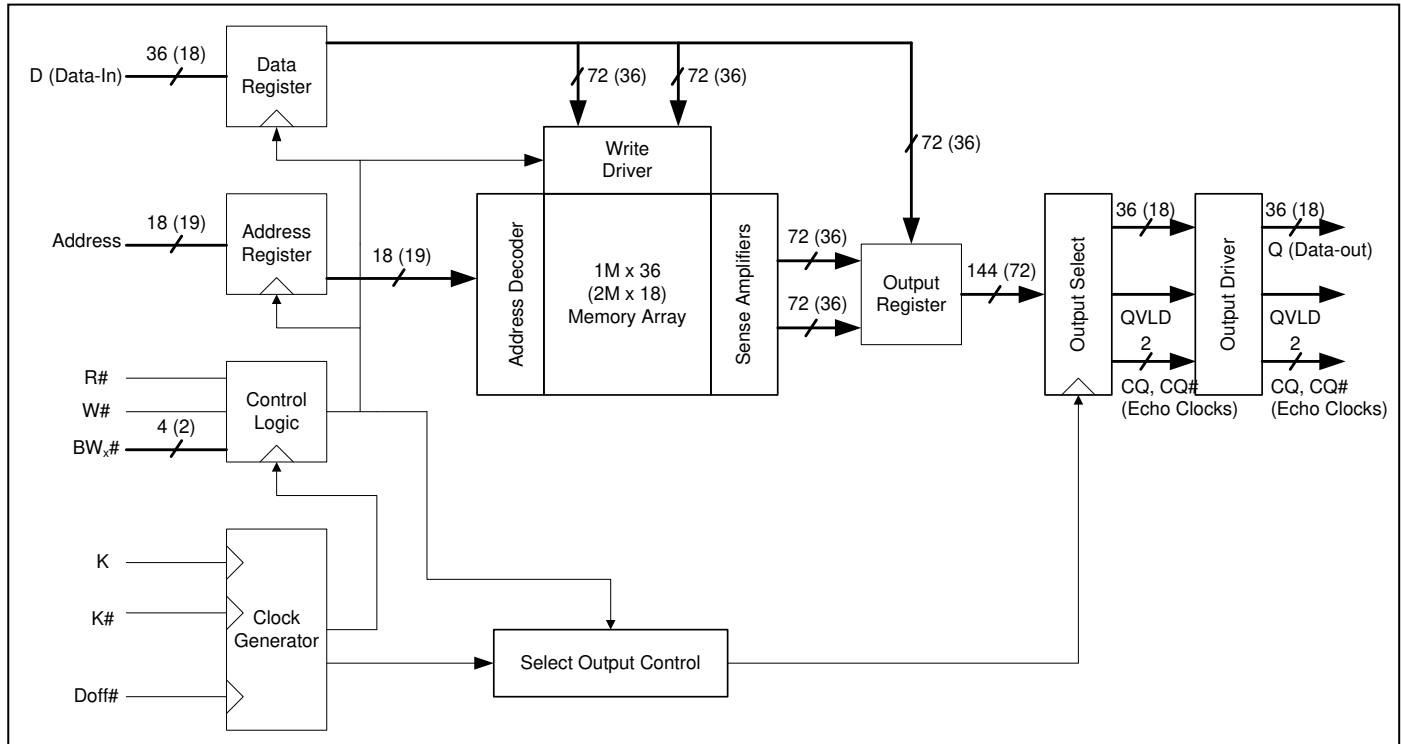
- The following balls are reserved for higher densities: 10A for 72Mb, 2A for 144Mb, and 7A for 288Mb.

Ball Description

Symbol	Type	Description
K, K#	Input	Input clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of K#. K# is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges. These balls cannot remain VREF level.
CQ, CQ#	Output	Synchronous echo clock outputs: The edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals are free running clocks and do not stop when Q tri-states.
Doff#	Input	DLL disable and reset input : when low, this input causes the DLL to be bypassed and reset the previous DLL information. When high, DLL will start operating and lock the frequency after tCK lock time. The device behaves in one read latency mode when the DLL is turned off. In this mode, the device can be operated at a frequency of up to 167 MHz.
QVLD	Output	Valid output indicator: The Q Valid indicates valid output data. QVLD is edge aligned with CQ and CQ#.
SA	Input	Synchronous address inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K. These inputs are ignored when device is deselected.
D0 - Dn	Input	Synchronous data inputs: Input data must meet setup and hold times around the rising edges of K and K# during WRITE operations. See BALL CONFIGURATION figures for ball site location of individual signals. The x18 device uses D0~D17. D18~D35 should be treated as NC pin. The x36 device uses D0~D35.
Q0 - Qn	Output	Synchronous data outputs: Output data is synchronized to the respective CQ and CQ#, or to the respective K and K# if C and /C are tied to high. This bus operates in response to R# commands. See BALL CONFIGURATION figures for ball site location of individual signals. The x18 device uses Q0~Q17. Q18~Q35 should be treated as NC pin. The x36 device uses Q0~Q35.
W#	Input	Synchronous write: When low, this input causes the address inputs to be registered and a WRITE cycle to be initiated. This input must meet setup and hold times around the rising edge of K.
R#	Input	Synchronous read: When low, this input causes the address inputs to be registered and a READ cycle to be initiated. This input must meet setup and hold times around the rising edge of K.
BW _{x#}	Input	Synchronous byte writes: When low, these inputs cause their respective byte to be registered and written during WRITE cycles. These signals are sampled on the same edge as the corresponding data and must meet setup and hold times around the rising edges of K and #K for each of the two rising edges comprising the WRITE cycle. See Write Truth Table for signal to data relationship.
V _{REF}	Input reference	HSTL input reference voltage: Nominally VDDQ/2, but may be adjusted to improve system noise margin. Provides a reference voltage for the HSTL input buffers.
V _{DD}	supply	Power supply: 1.8 V nominal. See DC Characteristics and Operating Conditions for range.
V _{DDQ}	supply	Power supply: Isolated output buffer supply. Nominally 1.5 V. See DC Characteristics and Operating Conditions for range.
V _{SS}	supply	Ground
ZQ	Input	Output impedance matching input: This input is used to tune the device outputs to the system data bus impedance. Q and CQ output impedance are set to 0.2xRQ, where RQ is a resistor from this ball to ground. This ball can be connected directly to VDDQ, which enables the minimum impedance mode. This ball cannot be connected directly to VSS or left unconnected. In ODT (On Die Termination) enable devices, the ODT termination values tracks the value of RQ. The ODT range is selected by ODT control input.
TMS, TDI, TCK	Input	IEEE1149.1 input pins for JTAG.
TDO	Output	IEEE1149.1 output pins for JTAG.
NC	N/A	No connect: These signals should be left floating or connected to ground to improve package heat dissipation.
ODT	Input	ODT control; Refer to SRAM features for the details.

SRAM Features description

Block Diagram



Note: Numerical values in parentheses refer to the x18 device configuration.

Read Operations

The SRAM operates continuously in a burst-of-four mode. Read cycles are started by registering R# in active low state at the rising edge of the K clock. R# can be activated every other cycle because two full cycles are required to complete the burst of four in DDR mode. A set of free-running echo clocks, CQ and CQ#, are produced internally with timings identical to the data-outs. The echo clocks can be used as data capture clocks by the receiver device.

The data corresponding to the first address is clocked 2.5 cycles later by the rising edge of the K# clock. The data corresponding to the second burst is clocked 3 cycles later by the following rising edge of the K clock. The third data-out is clocked by the subsequent rising edge of the K# clock, and the fourth data-out is clocked by the subsequent rising edge of the K clock.

A NOP operation (R# is high) does not terminate the previous read.

Write Operations

Write operations can also be initiated at every other rising edge of the K clock whenever W# is low. The write address is provided simultaneously. Again, the write always occurs in bursts of four.

The write data is provided in a 'late write' mode; that is, the data-in corresponding to the first address of the burst, is presented 1 cycle later or at the rising edge of the following K clock. The data-in corresponding to the second write burst address follows next, registered by the rising edge of K#. The third data-in is clocked by the subsequent rising edge of the K clock, and the fourth data-in is clocked by the subsequent rising edge of the K# clock.

The data-in provided for writing is initially kept in write buffers. The information in these buffers is written into the array on the third write cycle. A read cycle to the last two write addresses produces data from the write buffers. The SRAM maintains data coherency.

During a write, the byte writes independently control which byte of any of the four burst addresses is written (see *X18/X36 Write Truth Tables* and *Timing Reference Diagram for Truth Table*).

Whenever a write is disabled ($W\#$ is high at the rising edge of K), data is not written into the memory.

RQ Programmable Impedance

An external resistor, RQ , must be connected between the ZQ pin on the SRAM and V_{SS} to enable the SRAM to adjust its output driver impedance. The value of RQ must be $5x$ the value of the intended line impedance driven by the SRAM. For example, an RQ of 250Ω results in a driver impedance of 50Ω . The allowable range of RQ to guarantee impedance matching is between 175Ω and 350Ω at $V_{DDQ}=1.5V$. The RQ resistor should be placed less than two inches away from the ZQ ball on the SRAM module. The capacitance of the loaded ZQ trace must be less than $7.5pF$.

The ZQ pin can also be directly connected to V_{DDQ} to obtain a minimum impedance setting. ZQ should not be connected to V_{SS} .

Programmable Impedance and Power-Up Requirements

Periodic readjustment of the output driver impedance is necessary as the impedance is greatly affected by drifts in supply voltage and temperature. During power-up, the driver impedance is in the middle of allowable impedances values. The final impedance value is achieved within 1024 clock cycles.

Depth Expansion

Separate input and output ports enable easy depth expansion, as each port can be selected and deselected independently. Read and write operations can occur simultaneously without affecting each other. Also, all pending read and write transactions are always completed prior to deselecting the corresponding port.

Valid Data Indicator (QVLD)

A data valid pin (QVLD) is available to assist in high-speed data output capture. This output signal is edge-aligned with the echo clock and is asserted HIGH half a cycle before valid read data is available and asserted LOW half a cycle before the final valid read data arrives.

Delay Locked Loop (DLL)

Delay Lock Loop (DLL) is a new system to align the output data coincident with clock rising or falling edge to enhance the output valid timing characteristics. It is locked to the clock frequency and is constantly adjusted to match the clock frequency. Therefore device can have stable output over the temperature and voltage variation.

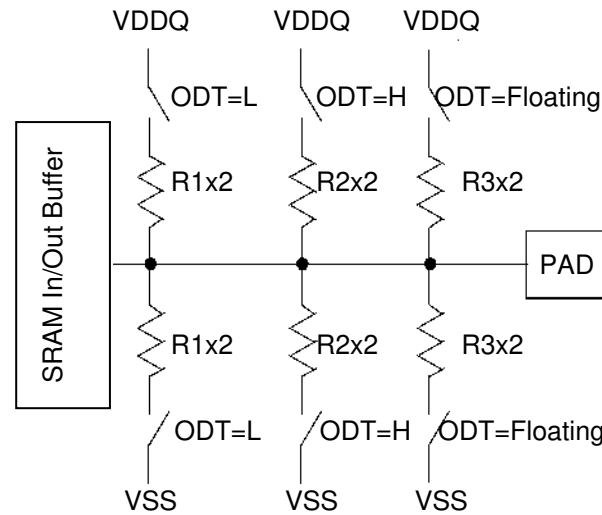
DLL has a limitation of locking range and jitter adjustment which are specified as t_{KHKH} and t_{KCvar} respectively in the AC timing characteristics. In order to turn this feature off, applying logic low to the $Doff\#$ pin will bypass this. In the DLL off mode, the device behaves with one cycle latency and a longer access time which is known in DDR-I or legacy QUAD mode.

The DLL can also be reset without power down by toggling $Doff\#$ pin low to high or stopping the input clocks K and $K\#$ for a minimum of 30ns. (K and $K\#$ must be stayed either at higher than V_{IH} or lower than V_{IL} level. Remaining V_{ref} is not permitted.) DLL reset must be issued when power up or when clock frequency changes abruptly. After DLL being reset, it gets locked after 2048 cycles of stable clock.

ODT (On Die Termination)

On Die Termination (ODT) is a feature that allows a SRAM to change input resistive termination condition by ODT pin which function can have three status, High, Low, and Floating. Each status can have different ODT termination value that tracks the value of RQ (Refer to the table of Fig1) and ODT of QUADP is always turned on during the read and write function after ODT level to connect with ODT resistor is forced.

Fig1. Functional representation of ODT



	R1	R2	R3
Option1 ³	0.3x RQ ¹	0.6x RQ ²	0.6x RQ ²
Option2 ⁴	ODT disable	0.6x RQ ²	ODT disable

Notes

1. Allowable range of RQ to guarantee impedance matching a tolerance of $\pm 20\%$ is $175\Omega < RQ < 350\Omega$.
2. Allowable range of RQ to guarantee impedance matching a tolerance of $\pm 20\%$ is $175\Omega < RQ < 250\Omega$.
3. ODT control pin is connected to VDDQ through 3.5k Ω . Therefore it is recommended to connect it to VSS through less than 100 Ω to make it low.
4. ODT control pin is connected to VSS through 3.5k Ω . Therefore it is recommended to connect it to VDDQ through less than 100 Ω to make it high.

ODT PIN

For option1 case, low input level of ODT pin can select strong (RQ¹) input termination range ($175\Omega < RQ < 350\Omega$) and high input level of ODT pin can select weak (RQ²) input termination range ($175\Omega < RQ < 250\Omega$) with K, K#, D0 to Dn, BWx# and if ODT pin is on floating condition, it set weak (RQ²) input termination range which ODT pin is connected by pull-up resistor internally. For option2 case, high input level of ODT pin can select weak (RQ²) input termination range ($175\Omega < RQ < 250\Omega$) with D0 to Dn, BWx# and low input level or floating of ODT pin can select disable of the ODT function.

Power-Up and Power-Down Sequences

The recommendation of voltage apply sequence is : $V_{DD} \rightarrow V_{DDQ} \xrightarrow{1)} \rightarrow V_{REF} \xrightarrow{2)} \rightarrow V_{IN}$

Notes:

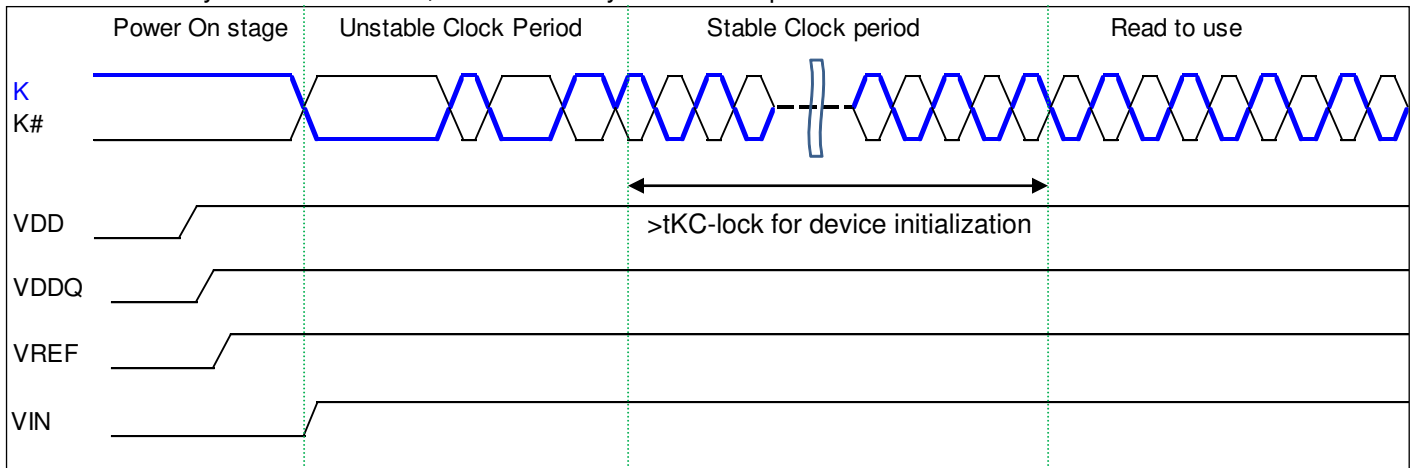
V_{DDQ} can be applied concurrently with V_{DD} .

V_{REF} can be applied concurrently with V_{DDQ} .

After power and clock signals are stabilized, device can be ready for normal operation after t_{KC-Lock} cycles. In t_{KC-Lock} cycle period, device initializes internal logics and locks DLL. Depending on /Doff status, locking DLL will be skipped. The following timing pictures are possible examples of power up sequence.

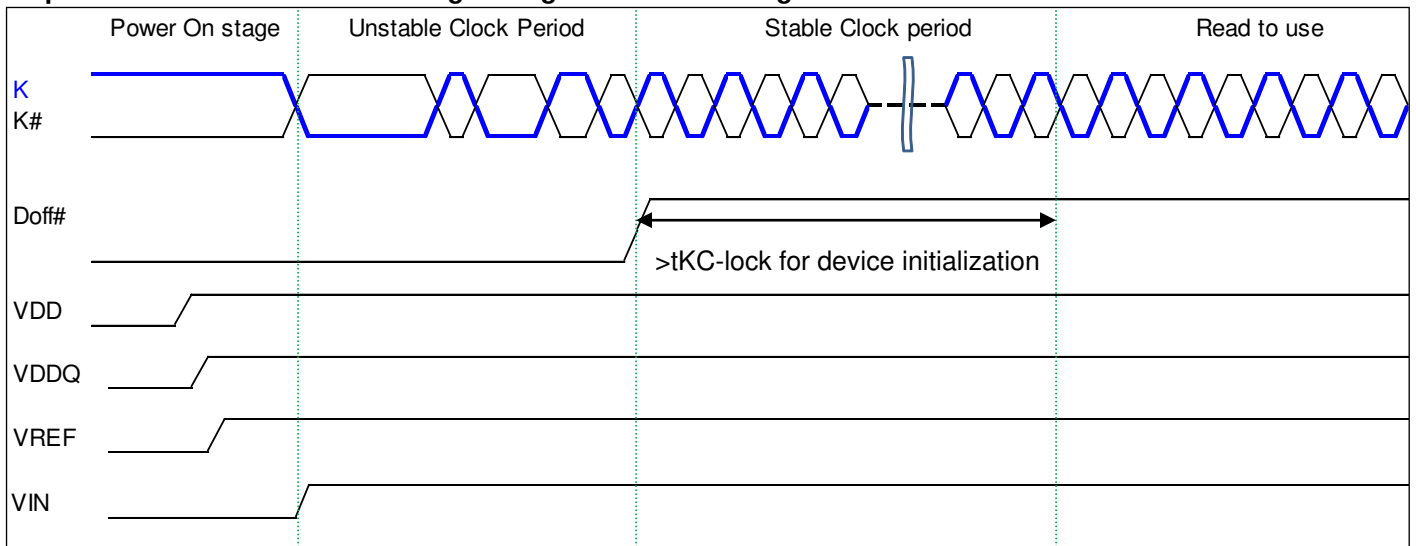
Sequence1. /Doff is fixed low

After t_{KC-Lock} cycle of stable clock, device is ready for normal operation.



Note) All inputs including clocks must be either logically High or Low during Power On stage. Timing above shows only one of cases.

Sequence2. /Doff is controlled and goes high after clock being stable.



Note) All inputs including clocks must be either logically High or Low during Power On stage. Timing above shows only one of cases.

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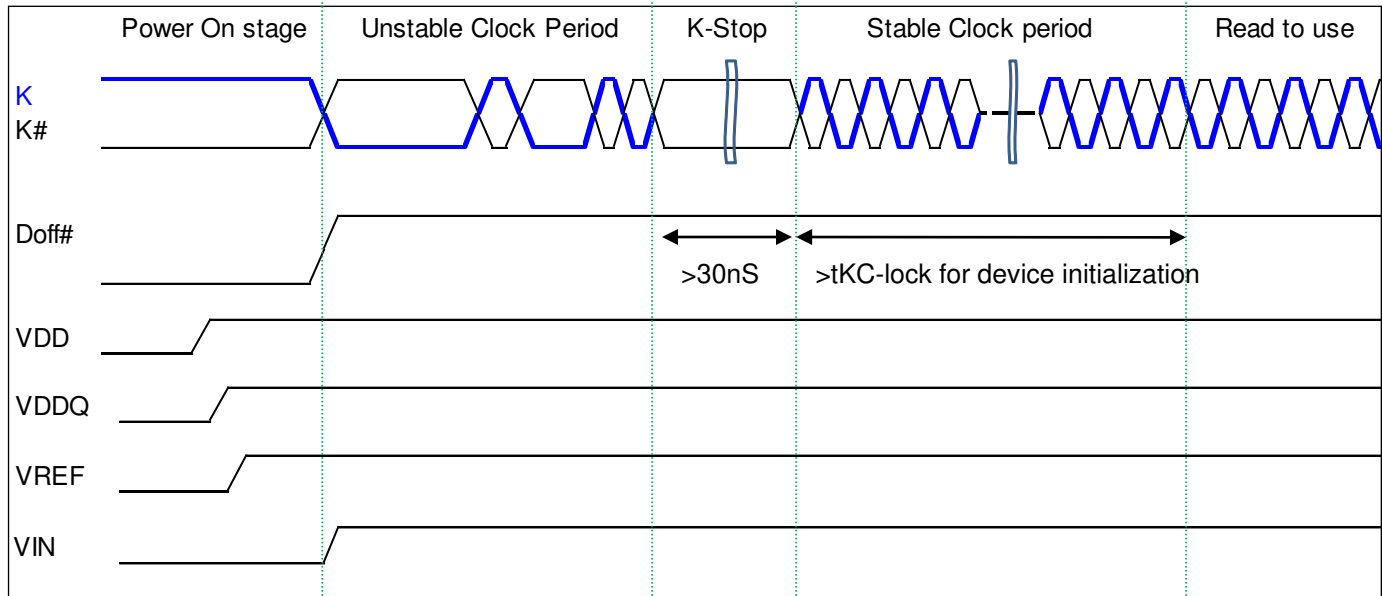
IS61QDPB41M36A/A1/A2



Sequence3. /Doff is controlled but goes high before clock being stable.

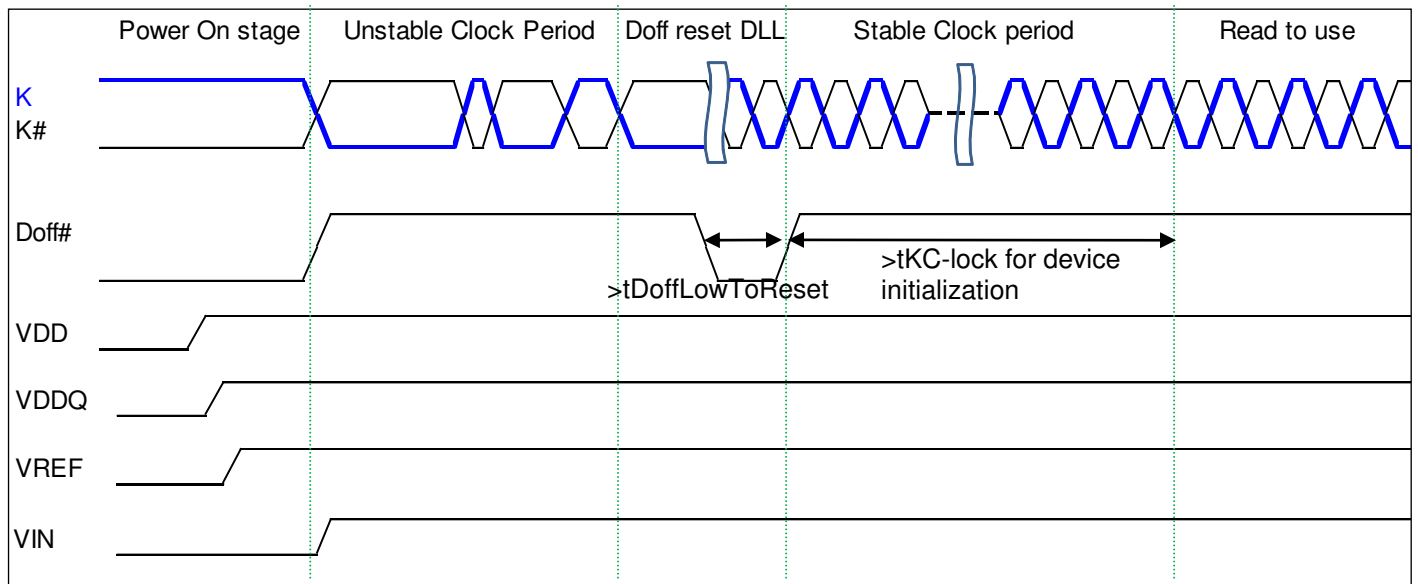
Because DLL has a risk to be locked with the unstable clock, DLL needs to be reset and locked with the stable input.

a) K-stop to reset. If K or K# stays at VIH or VIL for more than 30nS, DLL will be reset and ready to re-lock. In tKC-Lock period, DLL will be locked with a new stable value. Device can be ready for normal operation after that.



Note) All inputs including clocks must be either logically High or Low during Power On stage. Timing above shows only one of cases.

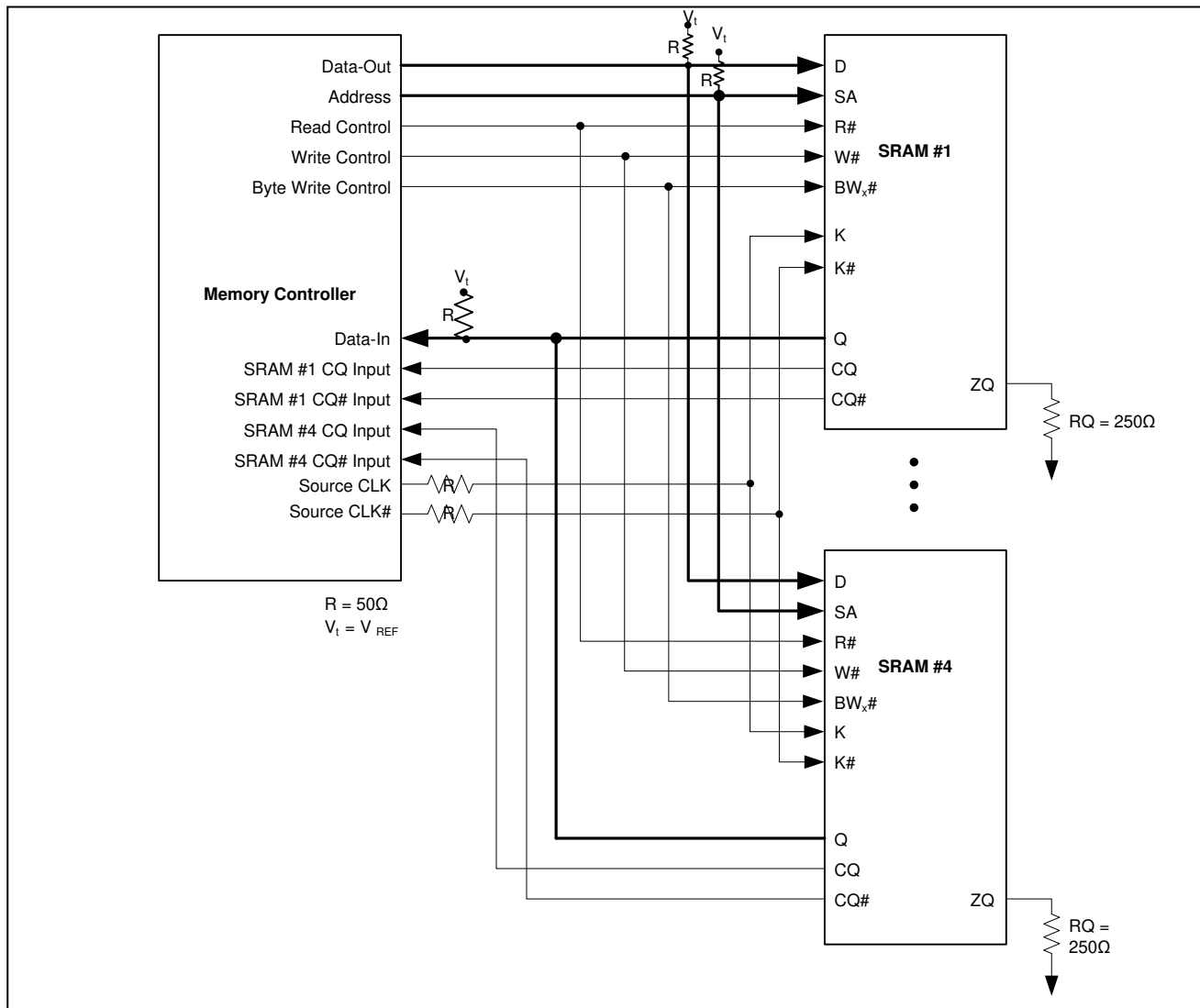
a) /Doff Low to reset. If /Doff toggled low to high, DLL will be reset and ready to re-lock. In tKC-Lock period, DLL will be locked with a new stable value. Device can be ready for normal operation after that.



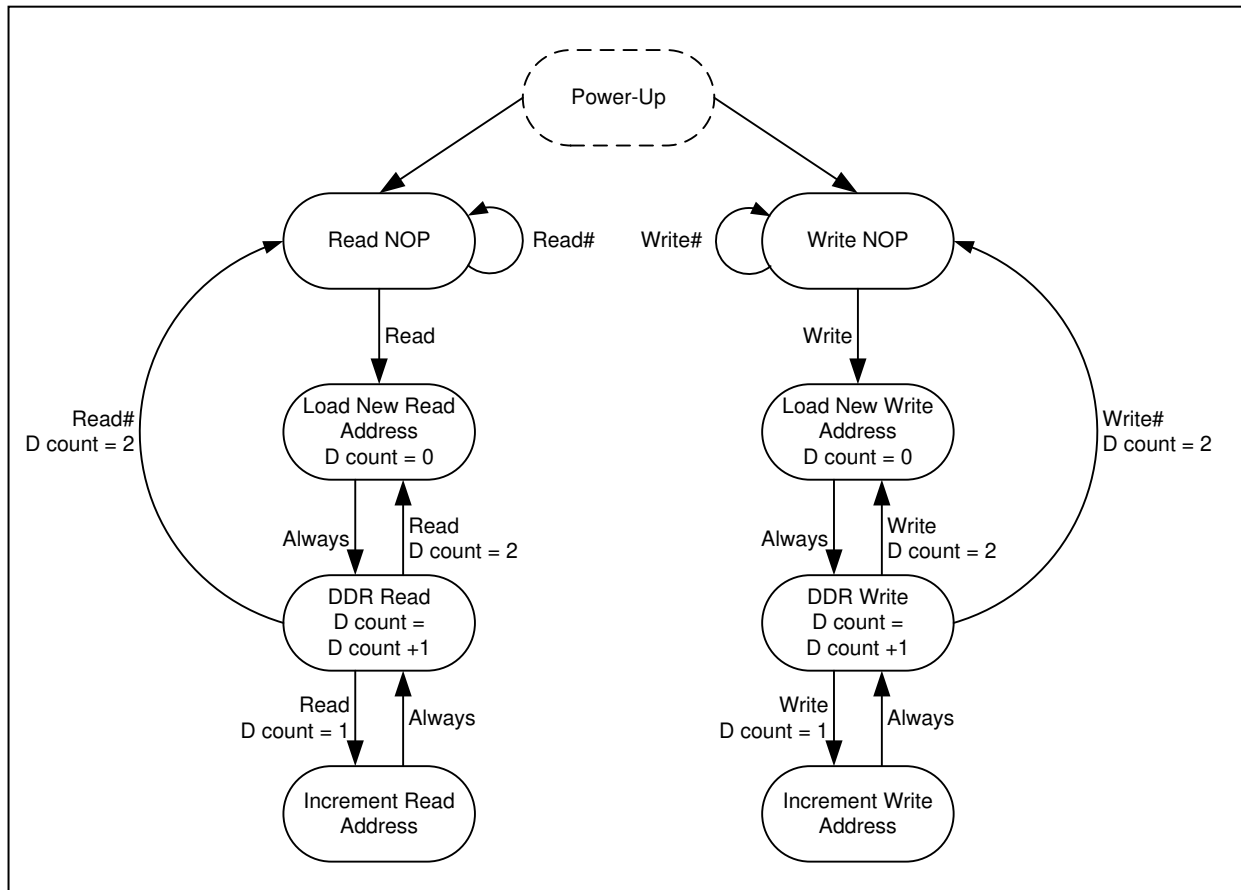
Note) Applying DLL reset sequences (sequence 3a, 3b) are also required when operating frequency is changed without power off.

Note) All inputs including clocks must be either logically High or Low during Power On stage. Timing above shows only one of cases.

Application Example



State Diagram

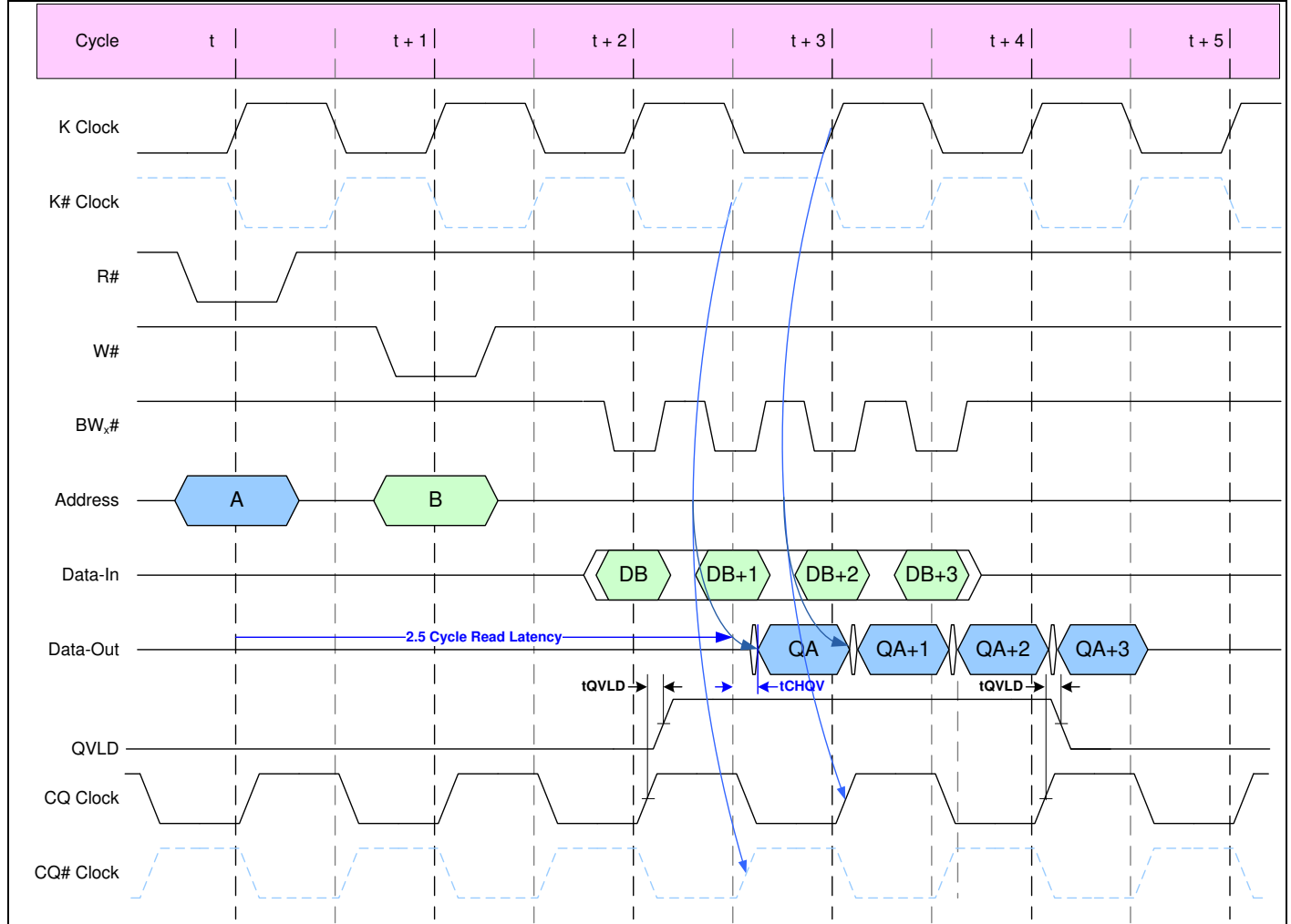


Notes:

1. Internal burst counter is fixed as four-bit linear; that is when first address is A0+0, next internal burst addresses are A0+1, A0+2, and A0+3
2. **Read** refers to read active status with R# = LOW. **Read#** refers to read inactive status with R# = HIGH.
3. **Write** refers to write active status with W# = LOW. **Write#** refers to write inactive status with W# = HIGH.
4. The read and write state machines can be active simultaneously.
5. State machine control timing sequence is controlled by K.

Timing Reference Diagram for Truth Table

The *Timing Reference Diagram for Truth Table* is helpful in understanding the *Clock and Write Truth Tables*, as it shows the cycle relationship between clocks, address, data in, data out, and control signals. Read command is issued at the beginning of cycle "t". Write command is issued at the beginning of cycle "t+1".



Clock Truth Table

(Use the following table with the *Timing Reference Diagram for Truth Table.*)

Mode	Clock	Controls		Data In				Data Out			
	K	R#	W#	D _B	D _{B+1}	D _{B+2}	D _{B+3}	Q _A	Q _{A+1}	Q _{A+2}	Q _{A+3}
Stop Clock	Stop	X	X	Previous State	Previous State	Previous State	Previous State	Previous State	Previous State	Previous State	Previous State
No Operation (NOP)	L → H	H	H	X	X	X	X	High-Z	High-Z	High-Z	High-Z
Read A	L → H	L	X	X	X	X	X	D _{OUT} at K#(t+2.5)	D _{OUT} at K (t+3.0)	D _{OUT} at K# (t+3.5)	D _{OUT} at K (t+4.0)
Write B	L → H	X	L	D _{IN} at K (t+2.0)	D _{IN} at K#(t+2.5)	D _{IN} at K (t+3.0)	D _{IN} at K# (t+3.5)	X	X	X	X

Notes:

- Internal burst counter is always fixed as four-bit.
- X = "don't care"; H = logic "1"; L = logic "0".
- A read operation is started when control signal R is active low
- A write operation is started when control signal W is active low.
- Before entering into stop clock, all pending read and write commands must be completed.
- Consecutive read or write operations can be started only at every other K clock rising edge. If two read or write operations are issued in consecutive K clock rising edges, the second one will be ignored.
- If both R# and W# are active low after a NOP operation, the write operation will be ignored.
- For timing definitions, refer to the *AC Timing Characteristics* table. Signals must meet AC specifications at timings indicated in parenthesis with respect to switching clocks K and K#.

x18 Write Truth Table

(Use the following table with the *Timing Reference Diagram for Truth Table.*)

Operation	K (t+2.0)	K# (t+2.5)	K (t+3.0)	K# (t+3.5)	BW ₀ #	BW ₁ #	D _B	D _{B+1}	D _{B+2}	D _{B+3}
Write Byte 0	L → H				L	H	D0-8 (t+2.0)			
Write Byte 1	L → H				H	L	D9-17 (t+2.0)			
Write All Bytes	L → H				L	L	D0-17 (t+2.0)			
Abort Write	L → H				H	H	Don't Care			
Write Byte 0		L → H			L	H		D0-8 (t+2.5)		
Write Byte 1		L → H			H	L		D9-17 (t+2.5)		
Write All Bytes		L → H			L	L		D0-17 (t+2.5)		
Abort Write		L → H			H	H		Don't Care		
Write Byte 0			L → H		L	H			D0-8 (t+3.0)	
Write Byte 1			L → H		H	L			D9-17 (t+3.0)	
Write All Bytes			L → H		L	L			D0-17 (t+3.0)	
Abort Write			L → H		H	H			Don't Care	
Write Byte 0				L → H	L	H				D0-8 (t+3.5)
Write Byte 1				L → H	H	L				D9-17 (t+3.5)
Write All Bytes				L → H	L	L				D0-17 (t+3.5)
Abort Write				L → H	H	H				Don't Care

Notes:

- For all cases, W# needs to be active low during the rising edge of K occurring at time t.
- For timing definitions refer to the *AC Timing Characteristics* table. Signals must meet AC specifications with respect to switching clocks K and K#.

x36 Write Truth Table

(Use the following table with the *Timing Reference Diagram for Truth Table.*)

Operation	K (t+2.0)	K# (t+2.5)	K (t+3.0)	K# (t+3.5)	BW ₀ #	BW ₁ #	BW ₂ #	BW ₃ #	D _B	D _{B+1}	D _{B+2}	D _{B+3}
Write Byte 0	L → H				L	H	H	H	D0-8 (t+2.0)			
Write Byte 1	L → H				H	L	H	H	D9-17 (t+2.0)			
Write Byte 2	L → H				H	H	L	H	D18-26 (t+2.0)			
Write Byte 3	L → H				H	H	H	L	D27-35 (t+2.0)			
Write All Bytes	L → H				L	L	L	L	D0-35 (t+2.0)			
Abort Write	L → H				H	H	H	H	Don't Care			
Write Byte 0		L → H			L	H	H	H		D0-8 (t+2.5)		
Write Byte 1		L → H			H	L	H	H		D9-17 (t+2.5)		
Write Byte 2		L → H			H	H	L	H		D18-26 (t+2.5)		
Write Byte 3		L → H			H	H	H	L		D27-35 (t+2.5)		
Write All Bytes		L → H			L	L	L	L		D0-35 (t+2.5)		
Abort Write		L → H			H	H	H	H		Don't Care		
Write Byte 0			L → H		L	H	H	H			D0-8 (t+3.0)	
Write Byte 1			L → H		H	L	H	H			D9-17 (t+3.0)	
Write Byte 2			L → H		H	H	L	H			D18-26 (t+3.0)	
Write Byte 3			L → H		H	H	H	L			D27-35 (t+3.0)	
Write All Bytes			L → H		L	L	L	L			D0-35 (t+3.0)	
Abort Write			L → H		H	H	H	H			Don't Care	
Write Byte 0				L → H	L	H	H	H				D0-8 (t+3.5)
Write Byte 1				L → H	H	L	H	H				D9-17 (t+3.5)
Write Byte 2				L → H	H	H	L	H				D18-26 (t+3.5)
Write Byte 3				L → H	H	H	H	L				D27-35 (t+3.5)
Write All Bytes				L → H	L	L	L	L				D0-35 (t+3.5)
Abort Write				L → H	H	H	H	H				Don't Care

Notes:

1. For all cases, W# needs to be active low during the rising edge of K occurring at time t.
2. For timing definitions refer to the *AC Timing Characteristics* table. Signals must meet AC specifications with respect to switching clocks K and K#.

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	V_{DD}	-0.5	2.9	V
I/O Power Supply Voltage	V_{DDQ}	-0.5	2.9	V
DC Input Voltage	V_{IN}	-0.5	$V_{DD}+0.3$	V
Data Out Voltage	V_{DOUT}	-0.5	2.6	V
Junction Temperature	T_J	-	110	°C
Storage Temperature	T_{STG}	-55	+125	°C

Note:

Stresses greater than those listed in this table can cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Temperature Range

Temperature Range	Symbol	Min	Max	Units
Commercial	T_A	0	+70	°C
Industrial	T_A	-40	+85	°C

DC Electrical Characteristics

(Over the Operating Temperature Range, $V_{DD}=1.8V\pm 5\%$)

Parameter	Symbol	Min	Max	Units	Notes
x36 Average Power Supply Operating Current ($I_{OUT}=0$, $V_{IN}=V_{IH}$ or V_{IL})	I_{DD22} I_{DD25} I_{DD30} I_{DD33}	-	620 580 560 520	mA	1,2
x18 Average Power Supply Operating Current ($I_{OUT}=0$, $V_{IN}=V_{IH}$ or V_{IL})	I_{DD22} I_{DD25} I_{DD30} I_{DD33}	-	570 530 510 470	mA	1,2
Power Supply Standby Current ($R\#=V_{IH}$, $W\#=V_{IH}$. All other inputs= V_{IH} or V_{IL} , $I_{IH}=0$)	I_{SB22} I_{SB25} I_{SB30} I_{SB33}	-	290 280 270 260	mA	1,2
Input leakage current ($0 \leq V_{IN} \leq V_{DDQ}$ for all input balls except V_{REF} , ZQ, TCK, TMS, TDI ball)	I_{LI}	-2	+2	μA	3,4
Output leakage current ($0 \leq V_{OUT} \leq V_{DDQ}$ for all output balls except TDO ball; Output must be disabled.)	I_{LO}	-2	+2	μA	
Output "high" level voltage ($I_{OH}=-100\mu A$, Nominal ZQ)	V_{OH}	$V_{DDQ}-0.2$	V_{DDQ}	V	
Output "low" level voltage ($I_{OL}=100\mu A$, Nominal ZQ)	V_{OL}	V_{SS}	$V_{SS}+0.2$	V	

Notes:

- I_{OUT} = chip output current.
- The numeric suffix indicates the part operating at speed, as indicated in *AC Timing Characteristics* table (that is, I_{DD25} indicates 2.5ns cycle time).
- ODT must be disabled.
- Balls with ODT and DOFF# do not follow this spec, $I_{LI} = \pm 100\mu A$.

Recommended DC Operating Conditions

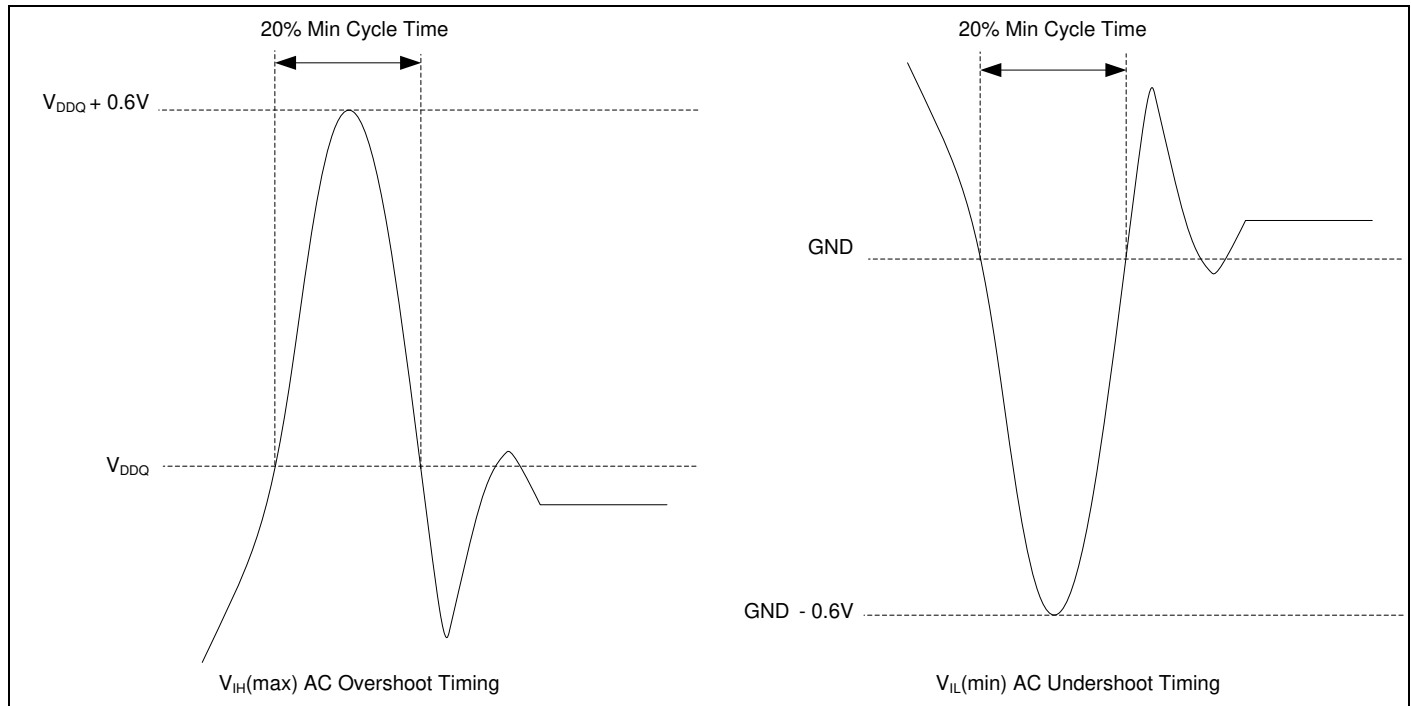
(Over the Operating Temperature Range)

Parameter	Symbol	Min	Typical	Max	Units	Notes
Supply Voltage	V_{DD}	1.8–5%	1.8	1.8+5%	V	1
Output Driver Supply Voltage	V_{DDQ}	1.4	1.5	V_{DD}	V	1
Input High Voltage	V_{IH}	$V_{REF}+0.1$	-	$V_{DDQ}+0.2$	V	1, 2
Input Low Voltage	V_{IL}	-0.2	-	$V_{REF}-0.1$	V	1, 3
Input Reference Voltage	V_{REF}	0.68	0.75	0.95	V	1, 5
Clock Signal Voltage	V_{IN-CLK}	-0.2	-	$V_{DDQ}+0.2$	V	1, 4

Notes:

1. All voltages are referenced to V_{SS} . All V_{DD} , V_{DDQ} , and V_{SS} pins must be connected.
2. $V_{IH}(\text{max})$ AC = See *Overshoot and Undershoot Timings*.
3. $V_{IL}(\text{min})$ AC = See *Overshoot and Undershoot Timings*.
4. V_{IN-CLK} specifies the maximum allowable DC excursions of each clock (K and K#).
5. Peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of V_{REF} .

Overshoot and Undershoot Timings



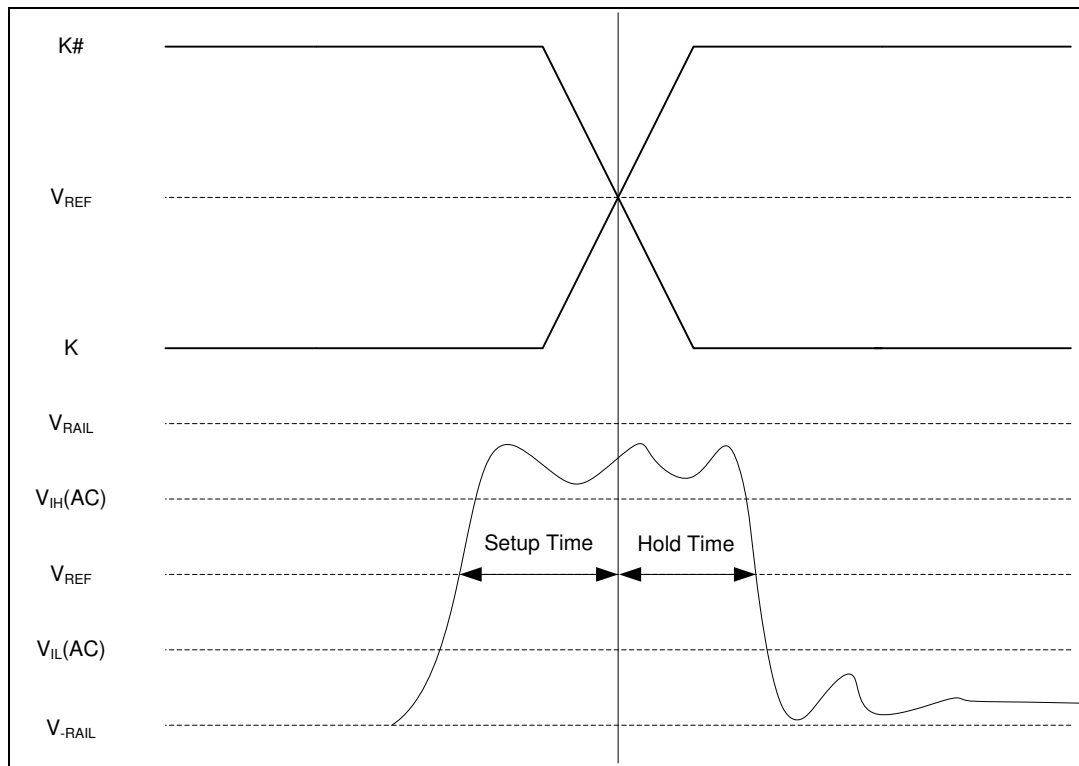
Typical AC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
AC Input Logic HIGH	$V_{IH}(AC)$	$V_{REF}+0.2$		V	1, 2, 3, 4
AC Input Logic LOW	$V_{IL}(AC)$		$V_{REF}-0.2$	V	1, 2, 3, 4
Clock Input Logic HIGH	$V_{IH-CLK}(AC)$	$V_{REF}+0.2$		V	1, 2, 3
Clock Input Logic LOW	$V_{IL-CLK}(AC)$		$V_{REF}-0.2$	V	1, 2, 3

Notes:

1. The peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF} .
2. Performance is a function of V_{IH} and V_{IL} levels to clock inputs.
3. See the *AC Input Definition* diagram.
4. See the *AC Input Definition* diagram. The signals should swing monotonically with no steps rail-to-rail with input signals never ringing back past $V_{IH}(AC)$ and $V_{IL}(AC)$ during the input setup and input hold window. $V_{IH}(AC)$ and $V_{IL}(AC)$ are used for timing purposes only.

AC Input Definition



PBGA Thermal Characteristics

Parameter	Symbol	13x15 BGA	15x17 BGA	Units
Thermal resistance (junction to ambient at airflow = 1m/s)	$R_{\theta JA}$	19.6	18.0	$^{\circ}C/W$
Thermal resistance (junction to pins)	$R_{\theta JB}$	4.02	3.30	$^{\circ}C/W$
Thermal resistance (junction to case)	$R_{\theta JC}$	4.53	4.20	$^{\circ}C/W$

Note: these parameters are guaranteed by design and tested by a sample basis only.

Pin Capacitance

Parameter	Symbol	Test Condition	Max	Units
Input or output capacitance except D and Q pins	C_{IN}, C_O	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{DD} = 1.8\text{V}, V_{DDQ} = 1.5\text{V}$	5	pF
D and Q capacitance (D0-Dx, Q0-Qx)	C_{DQ}		6	pF
Clocks Capacitance (K, K, C, C)	C_{CLK}		4	pF

Note: these parameters are guaranteed by design and tested by a sample basis only.

Programmable Impedance Output Driver DC Electrical Characteristics

(Over the Operating Temperature Range, $V_{DD}=1.8\text{V}\pm 5\%$, $V_{DDQ}=1.5\text{V}/1.8\text{V}$)

Parameter	Symbol	Min	Max	Units	Notes
Output Logic HIGH Voltage	V_{OH}	$V_{DDQ}/2 - 0.12$	$V_{DDQ}/2 + 0.12$	V	1, 3
Output Logic LOW Voltage	V_{OL}	$V_{DDQ}/2 - 0.12$	$V_{DDQ}/2 + 0.12$	V	2, 3

Notes:

1. For $175\Omega \leq R_Q \leq 350\Omega$:

$$I_{OH} = \frac{\left(\frac{V_{DDQ}}{2}\right)}{\left(\frac{R_Q}{5}\right)}$$

2. For $175\Omega \leq R_Q \leq 350\Omega$:

$$I_{OL} = \frac{\left(\frac{V_{DDQ}}{2}\right)}{\left(\frac{R_Q}{5}\right)}$$

3. Parameter Tested with $R_Q=250\Omega$ and $V_{DDQ}=1.5\text{V}$

AC Test Conditions

(Over the Operating Temperature Range, $V_{DD}=1.8\text{V}\pm 5\%$)

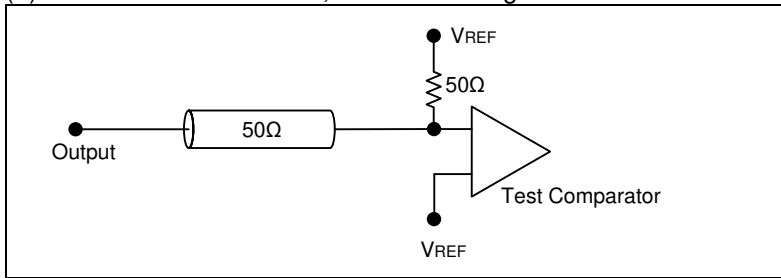
Parameter	Symbol	Conditions	Units	Notes
Output Drive Power Supply Voltage	V_{DDQ}	1.5	V	2
Input Logic HIGH Voltage	V_{IH}	1.25	V	
Input Logic LOW Voltage	V_{IL}	0.25	V	
Input Reference Voltage	V_{REF}	0.75	V	
Input Rise Time	T_R	2	V/ns	
Input Fall Time	T_F	2	V/ns	
Output Timing Reference Level		$V_{DDQ}/2$	V	
Clock Reference Level		0.75	V	
Output Load Conditions				1, 2

Notes:

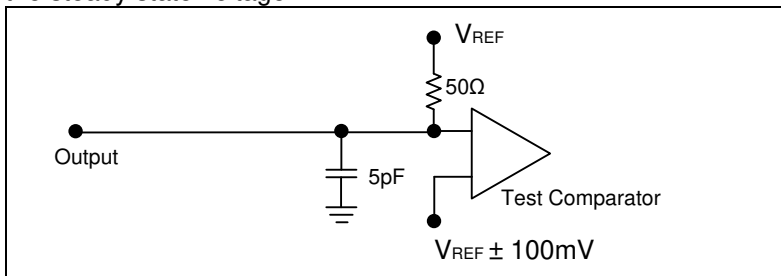
- See *AC Test Loading*.
- Parameters are tested with $R_Q=250\Omega$ and $V_{DDQ}=1.5\text{V}$, but ISSI devices are able to support $V_{DDQ}=1.4\text{V}$ to V_{DD}

AC Test Loading

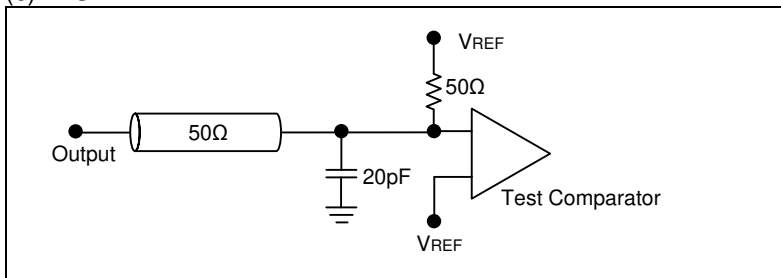
(a) Unless otherwise noted, AC test loading assume this condition.



(b) t_{CHQZ} and t_{CHQX1} are specified with 5pF load capacitance and measured when transition occurs $\pm 100\text{mV}$ from the steady state voltage.



(c) TDO



AC Timing Characteristics

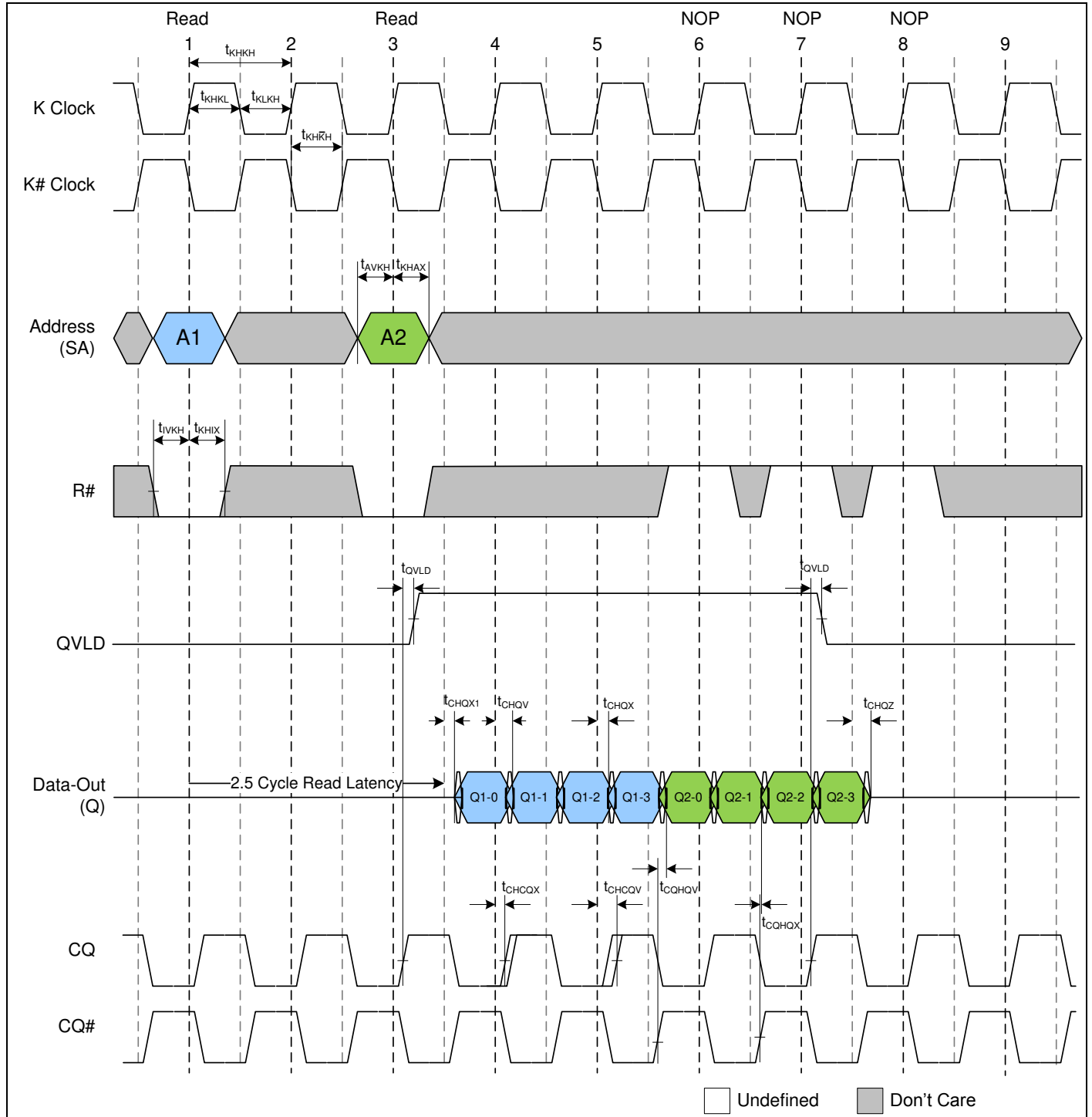
(Over the Operating Temperature Range, $V_{DD}=1.8V\pm5\%$, $V_{DDQ}=1.5V/1.8V$)

Parameter	Symbol	22 (450MHz)		25 (400MHz)		30 (333MHz)		33 (300MHz)		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock											
Clock Cycle Time (K, K#)	tKHKH	2.2	8.40	2.50	8.40	3.00	8.4	3.33	8.4	ns	
Clock Phase Jitter (K, K#)	tKC var		0.15		0.20		0.3		0.3	ns	4
Clock High Time (K, K#)	tKHKL	0.4		0.4		0.4		0.4		cycle	
Clock Low Time (K, K#)	tKLKH	0.4		0.4		0.4		0.4		cycle	
Clock to Clock# (K, K#)	tKHK#H	0.99		1.10		1.35		1.50		ns	
DLL Lock Time (K)	tKC lock	2048		2048		2048		2048		cycles	5
Doff Low period to DLL reset	tDoffLowToReset	5		5		5		5		ns	
K static to DLL reset	tKcreset	30		30		30		30		ns	
Output Times											
K, K# High to Output Valid	tCHQV		0.45		0.45		0.45		0.45	ns	
K, K# High to Output Hold	tCHQX	-0.45		-0.45		-0.45		-0.45		ns	
K, K# High to Echo Clock Valid	tCHCQV		0.45		0.45		0.45		0.45	ns	
K, K# High to Echo Clock Hold	tCHCQX	-0.45		-0.45		-0.45		-0.45		ns	
CQ, CQ# High to Output Valid	tCQHQV		0.2		0.2		0.25		0.27	ns	6
CQ, CQ# High to Output Hold	tCQHQX	-0.2		-0.2		-0.25		-0.27		ns	6
K, High to Output High-Z	tCHQZ		0.45		0.45		0.45		0.45	ns	
K, High to Output Low-Z	tCHQX1	-0.45		-0.45		-0.45		-0.45		ns	
CQ, CQ# High to QVLD Valid	tQVLD	-0.20	0.20	-0.20	0.20	-0.25	0.25	-0.27	0.27	ns	
Setup Times											
Address valid to K rising edge	tAVKH	0.30		0.40		0.40		0.40		ns	
R#,W# control inputs valid to K rising edge	tIVKH	0.30		0.40		0.40		0.40		ns	2
BW,# control inputs valid to K rising edge	tIVKH2	0.25		0.28		0.30		0.30		ns	2
Data-in valid to K, K# rising edge	tDVKH	0.25		0.28		0.30		0.30		ns	
Hold Times											
K rising edge to address hold	tKHAX	0.30		0.40		0.40		0.40		ns	2
K rising edge to R#,W# control inputs hold	tKHIX	0.30		0.40		0.40		0.40		ns	2
K rising edge to BW,# control inputs hold	tKHIX2	0.25		0.28		0.30		0.30		ns	
K, K# rising edge to data-in hold	tKHDX	0.25		0.28		0.30		0.30		ns	

Notes:

- All address inputs must meet the specified setup and hold times for all latching clock edges.
- Control signals are R#, W#, BW₀#, BW₁# and (BW₂#, BW₃# for x36)
- To avoid bus contention, at a given voltage and temperature tCHQX1 is bigger than tCHQZ. The specs as shown do not imply bus contention because tCHQX1 is a MIN parameter that is worst case at totally different test conditions (0 C, 1.9V) than tCHQZ, which is a MAX parameter (worst case at 70 C, 1.7V) It is not possible for two SRAMs on the same board to be at such different voltage and temperature.
- Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
- V_{DD} slew rate must be less than 0.1V DC per 50ns for DLL lock retention. DLL lock time begins once V_{DD} and input clock are stable.
- The data sheet parameters reflect tester guard bands and test setup variations.

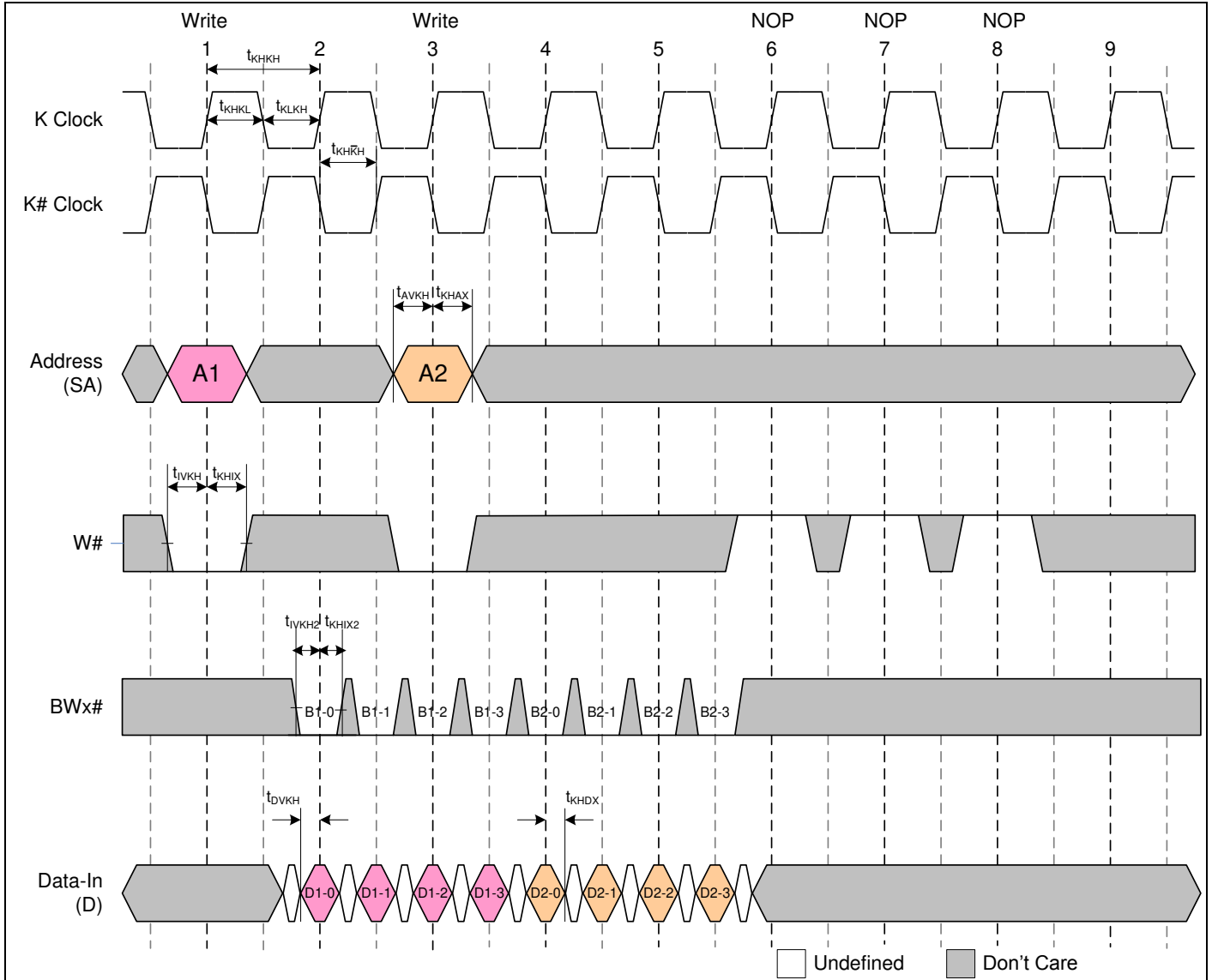
Read and Deselect Cycles Timing Diagram



Notes:

1. Q1-0, Q1-1, Q1-2, and Q1-3 refer to the output from address A1, Internal burst counter will assign them separately.
2. Outputs are disabled one cycle after NOP.

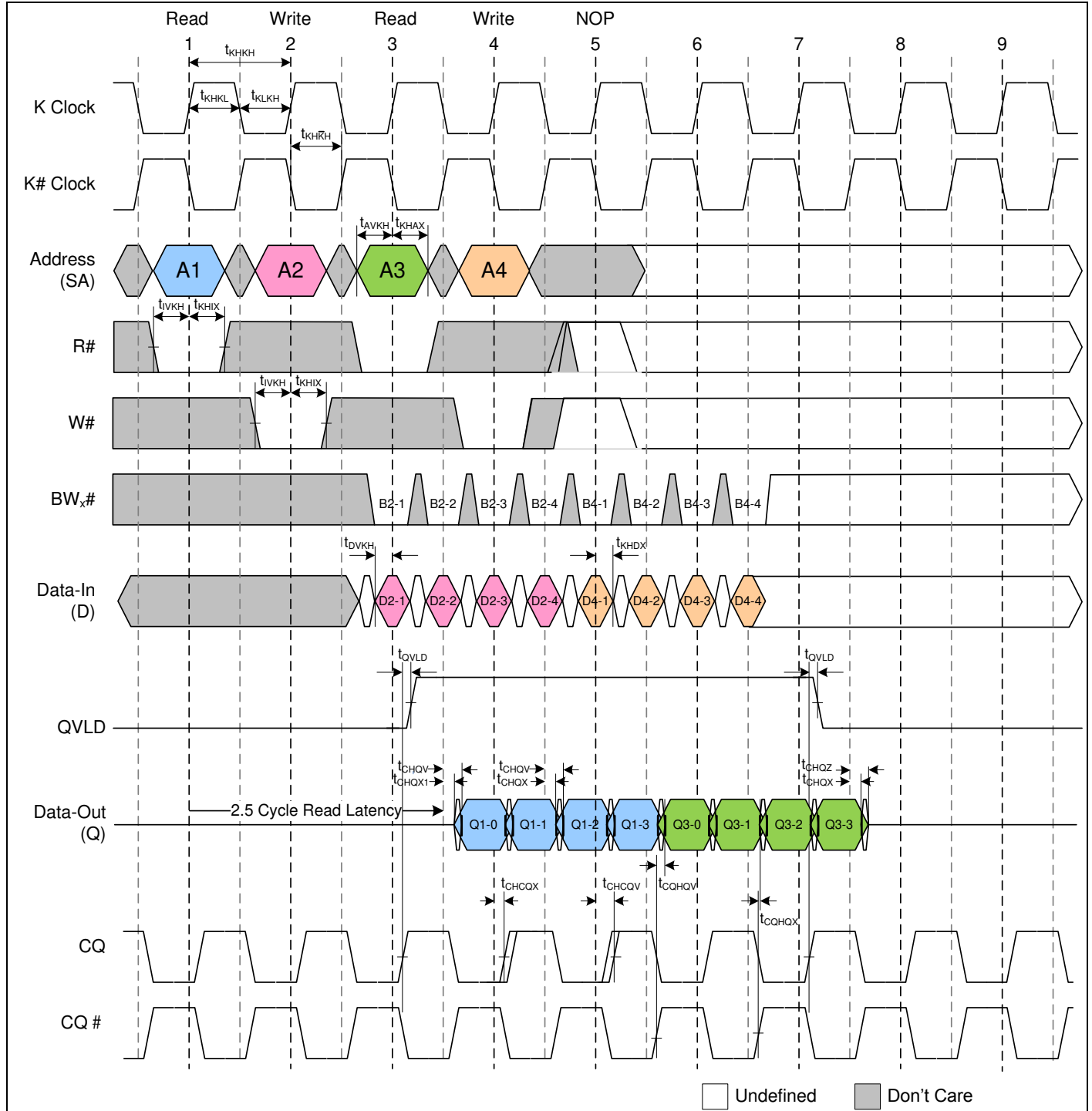
Write and NOP Timing Diagram



Notes:

1. D1-0, D1-1, D1-2, and D1-3 refer to the output from address A1, Internal burst counter will assign them separately.
2. B1-0 refers to all BWx# byte controls for D1-0. B1-1, B1-2, and B1-3 refer to all BWx# byte controls for D1-1, D1-2, and D1-3 respectively.
3. B2-0 refers to all BWx# byte controls for D2-0. B2-1, B2-2, and B2-3 refer to all BWx# byte controls for D2-1, D2-2, and D2-3 respectively.

Read, Write, and NOP Timing Diagram



Notes:

1. If address A3 = A2, data Q3-0 = D2-0, data Q3-1 = D2-1, data Q3-2 = D2-2, data Q3-3 = D2-3. Write data is forwarded immediately as read results.
2. B1-0 refers to all BWx# byte controls for D1-0. B1-1, B1-2, and B1-3 refer to all BWx# byte controls for D1-1, D1-2, and D1-3 respectively.
3. B2-0 refers to all BWx# byte controls for D2-0. B2-1, B2-2, and B2-3 refer to all BWx# byte controls for D2-1, D2-2, and D2-3 respectively.
4. Outputs are disabled one cycle after a NOP.

IEEE 1149.1 Serial Boundary Scan of JTAG

These SRAMs incorporate a serial boundary scan Test Access Port (TAP) controller in 165 FBGA package. That is fully compliant with IEEE Standard 1149.1-2001. The TAP controller operates using standard 1.8 V interface logic levels.

Disabling the JTAG feature

These SRAMs operate without using the JTAG feature. To disable the TAP controller, TCK must be tied Low (VSS) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternatively be connected to VDD through a pull up resistor. TDO must be left unconnected. Upon power up, the device comes up in a reset state, which does not interfere with the operation of the device.

Test Access Port Signal List:

Test Clock (TCK)

The test clock is to operate only TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is to set commands of the TAP controller and is sampled on the rising edge of TCK. This pin can be left unconnected at SRAM operation. The pin is pulled up internally to keep logic high level.

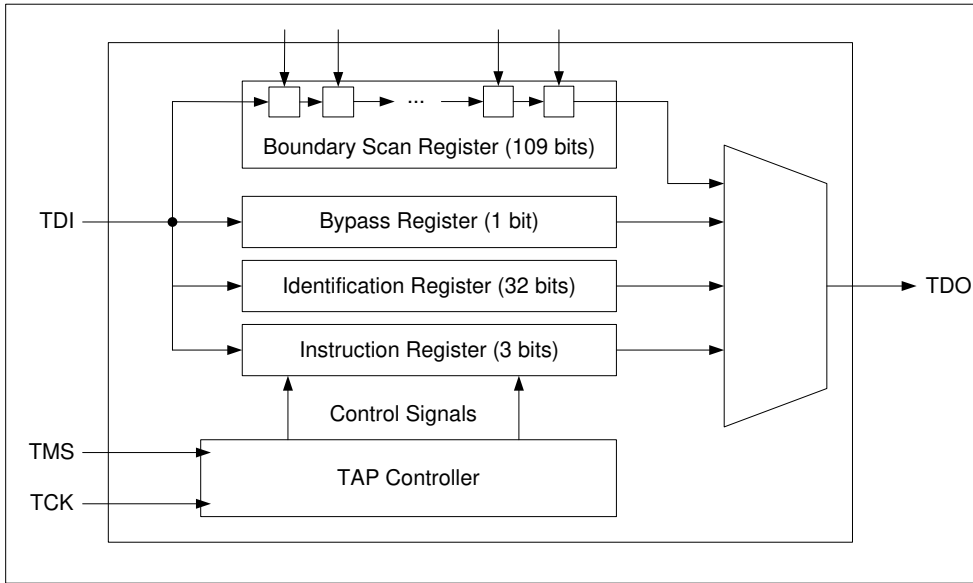
Test Data-In (TDI)

The TDI pin is to receive serially input information into the instruction and data registers. It can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register (Refer to the TAP Controller State Diagram). TDI is internally pulled up and can be unconnected at SRAM. TDI is connected to the most significant bit (MSB) on any register.

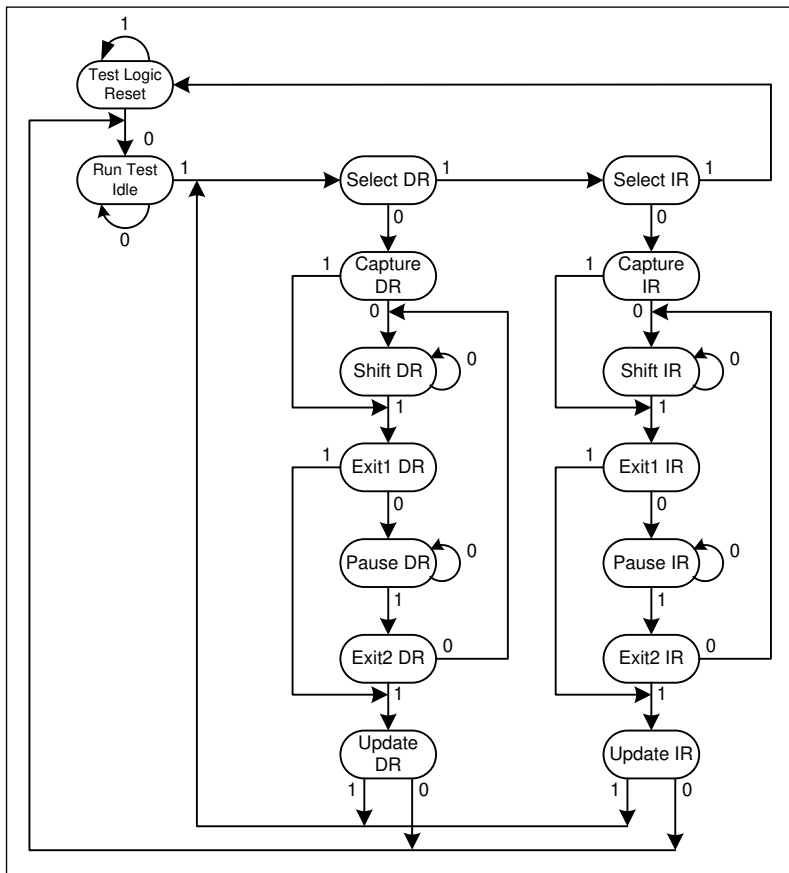
Test Data-Out (TDO)

The TDO pin is to drive serially clock data out from the JTAG registers. The output is active, depending upon the current state of the TAP state machine (Refer to instruction codes). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

TAP Controller State and Block Diagram



TAP Controller State Machine



Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. This Reset does not affect the operation of the SRAM and can be performed while the SRAM is operating. At power up, the TAP is reset internally to ensure that TDO comes up in a High Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK and output on the TDO pin on the falling edge of TCK.

Instruction Register

This register is loaded during the update-IR state of the TAP controller. Three-bit instructions can be serially loaded into the instruction register. At power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section. When the TAP controller is in the capture-IR state, the two LSBs are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

The bypass register is a single-bit register that can be placed between the TDI and TDO balls. It is to skip certain chips without serial boundary scan. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and output balls on the SRAM. Several No Connected(NC) balls are also included in the scan register to reserve other product options. The boundary scan register is loaded with the contents of the SRAM input and output ring when the TAP controller is in the capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the input and output ring. Each bit corresponds to one of the balls on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the shift-DR state. The ID register has a vendor ID code and other information

TAP Instruction Set

TAP Instruction Set is available to set eight instructions with the three bit instruction register and all combinations are listed in the TAP Instruction Code Table. Three of listed instructions on this table are reserved and must not be used. Instructions are loaded serially into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. To execute an instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction connects the boundary scan register between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High Z state until the next command is supplied during the Update IR state.