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IS62WV10248BLL

1M x 8 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

MARCH 2006

FEATURES

- High-speed access time: 55ns, 70ns
- CMOS low power operation:

  36 mW (typical) operating

  12 µW (typical) CMOS standby
- TTL compatible interface levels
- Single power supply:

  2.5V--3.6V V_{DD} (IS62WV10248BLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Industrial temperature available
- Lead-free available

DESCRIPTION

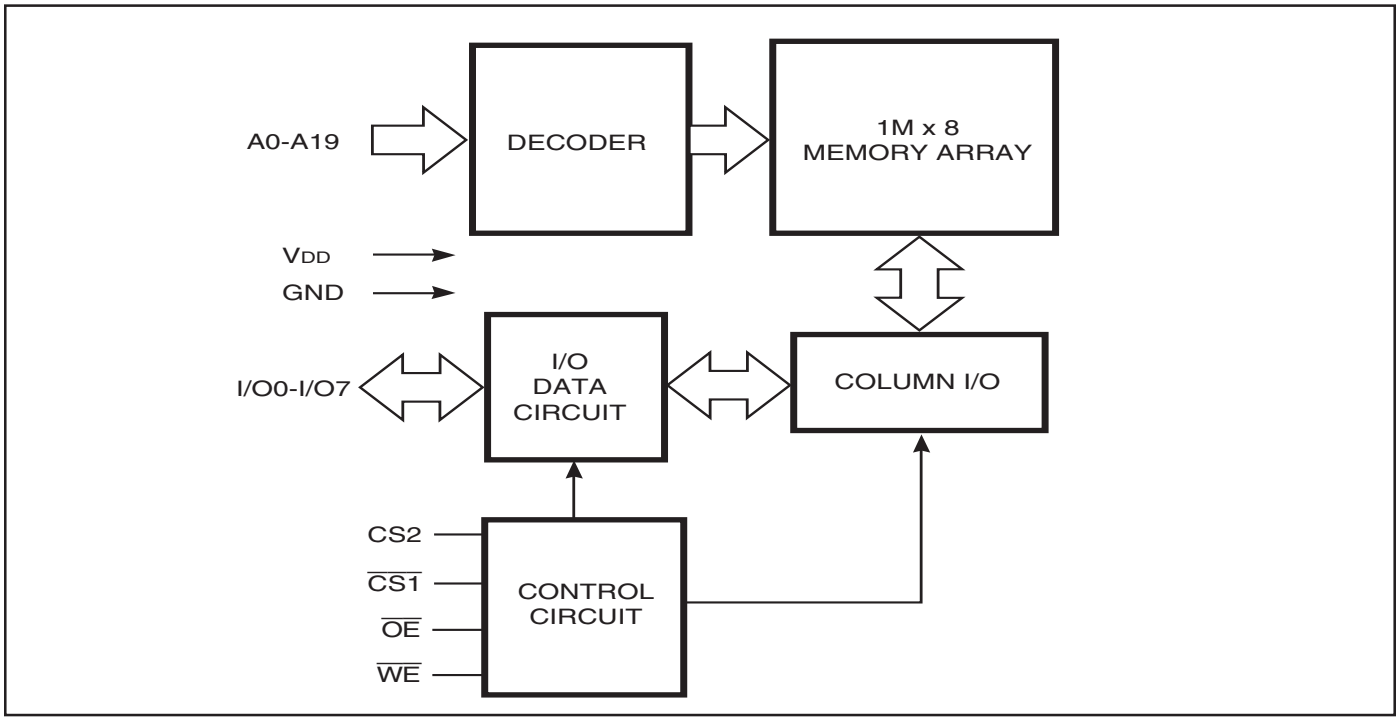
The *ISSI* IS62WV10248BLL is a high-speed, 8M bit static RAMs organized as 1M words by 8 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) or when CS2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable $\overline{(WE)}$ controls both writing and reading of the memory.

The IS62WV10248BLL is packaged in the JEDEC standard 48-pin mini BGA (7.2mm x 8.7mm).

FUNCTIONAL BLOCK DIAGRAM

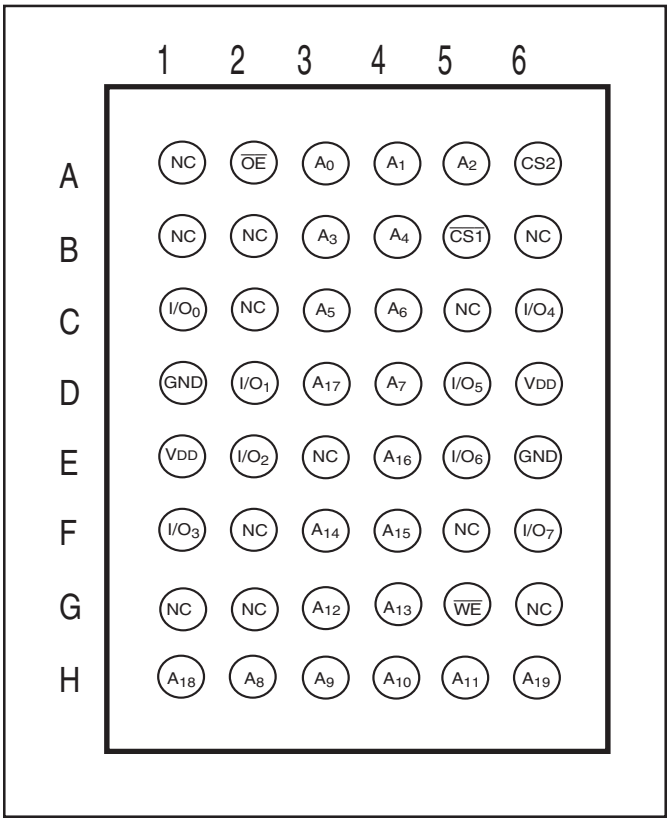


PIN DESCRIPTIONS

A0-A19	Address Inputs
$\overline{CS1}$	Chip Enable 1 Input
CS2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
NC	No Connection
V_{DD}	Power
GND	Ground

PIN CONFIGURATION

48-pin mini BGA (B) (7.2mm x 8.7mm)



TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	I/O Operation	V_{DD} Current
Not Selected	X	H	X	X	High-Z	I_{SB1}, I_{SB2}
(Power-down)	X	X	L	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	H	High-Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.2 to V_{DD}+0.3	V
V_{DD}	V_{DD} Related to GND	–0.2 to +3.8	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (V_{DD})

Range	Ambient Temperature	IS62WV10248BLL
Commercial	0°C to +70°C	2.5V - 3.6V
Industrial	–40°C to +85°C	2.5V - 3.6V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -1 mA	2.5-3.6V	2.2	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA	2.5-3.6V	—	0.4	V
V_{IH}	Input HIGH Voltage		2.5-3.6V	2.2	V_{DD} + 0.3	V
V_{IL}(1)	Input LOW Voltage		2.5-3.6V	–0.2	0.6	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled		–1	1	µA

Notes:
1. V_{IL} (min.) = –1.0V for pulse width less than 10 ns.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	10	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	IS62WV10248BLL (Unit)
Input Pulse Level	0.4 to V_{DD}-0.3V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	V_{REF}
Output Load	See Figures 1 and 2

	IS62WV10248BLL 2.5V - 3.6V
R1(Ω)	1029
R2(Ω)	1728
V_{REF}	1.5V
V_{TM}	2.8V

AC TEST LOADS

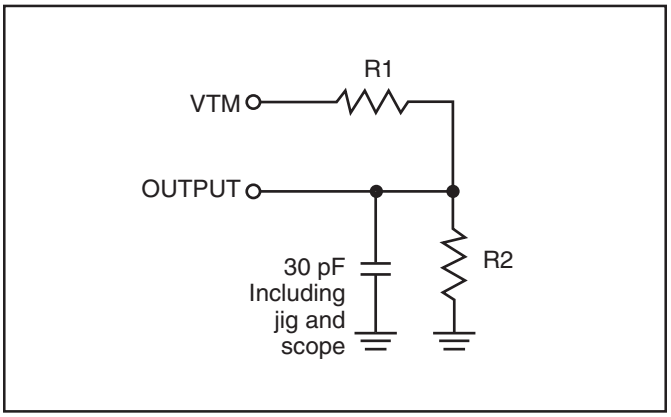


Figure 1

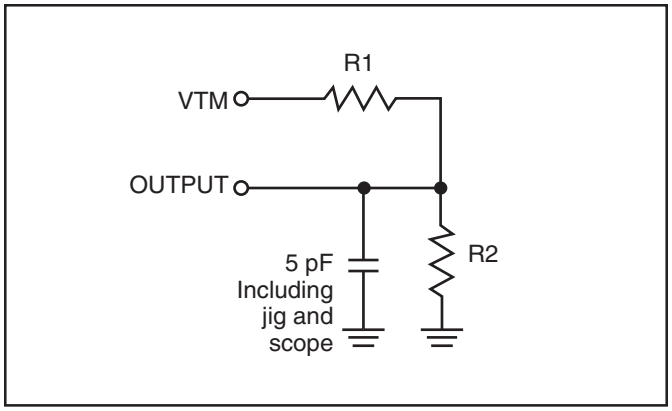


Figure 2

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

IS62WV10248BLL

Symbol	Parameter	Test Conditions		Max. 55	Max. 70	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com.	30	25	mA
			Ind.	35	30	
I_{CC1}	Operating Supply Current	V_{DD} = Max., $\overline{CS1}$ = 0.2V	Com.	5	5	mA
		$\overline{WE}$ = V_{DD} -0.2V	Ind.	5	5	
		CS2 = V_{DD} -0.2V, f = 1MHz				
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max.,	Com.	0.3	0.3	mA
		V_{IN} = V_{IH} or V_{IL}	Ind.	0.3	0.3	
		$\overline{CS1}$ = V_{IH}, CS2 = V_{IL}, f = 1 MHz				
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max.,	Com.	20	20	µA
		$\overline{CS1} \geq V_{DD} - 0.2V$,	Ind.	25	25	
		CS2 ≤ 0.2V,	typ.[1]	3	3	
		$V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq$ 0.2V, f = 0				

Note:
1. Typical Values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

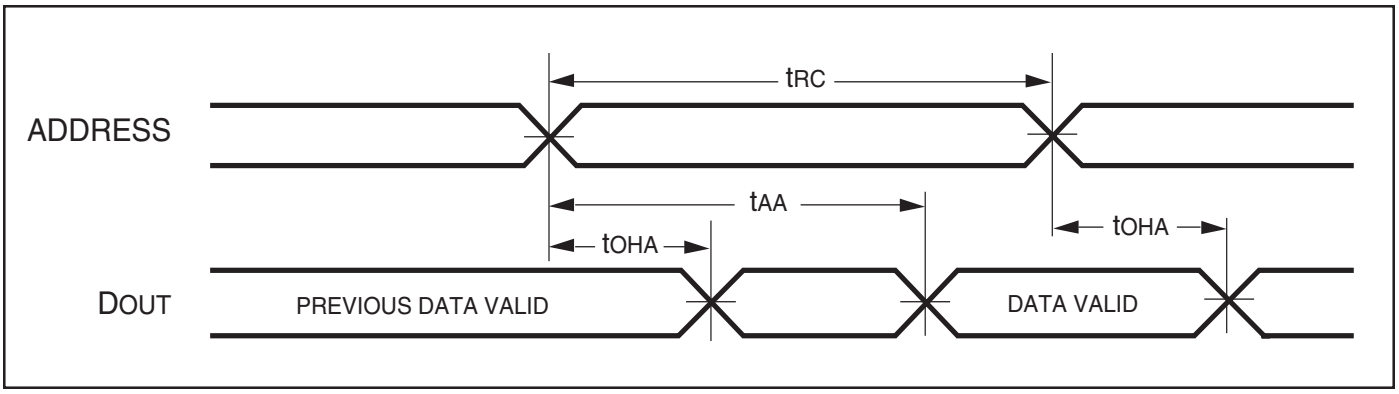
Symbol	Parameter	55 ns Min.	55 ns Max.	70 ns Min.	70 ns Max.	Unit
t_{RC}	Read Cycle Time	55	—	70	—	ns
t_{AA}	Address Access Time	—	55	—	70	ns
t_{OHA}	Output Hold Time	10	—	10	—	ns
t_{ACS1}/t_{ACS2}	$\overline{CS1}$/CS2 Access Time	—	55	—	70	ns
t_{DOE}	$\overline{OE}$ Access Time	—	25	—	35	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	20	—	25	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	ns
t_{HZCS1}/t_{HZCS2}[2]	$\overline{CS1}$/CS2 to High-Z Output	0	20	0	25	ns
t_{LZCS1}/t_{LZCS2}[2]	$\overline{CS1}$/CS2 to Low-Z Output	10	—	10	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

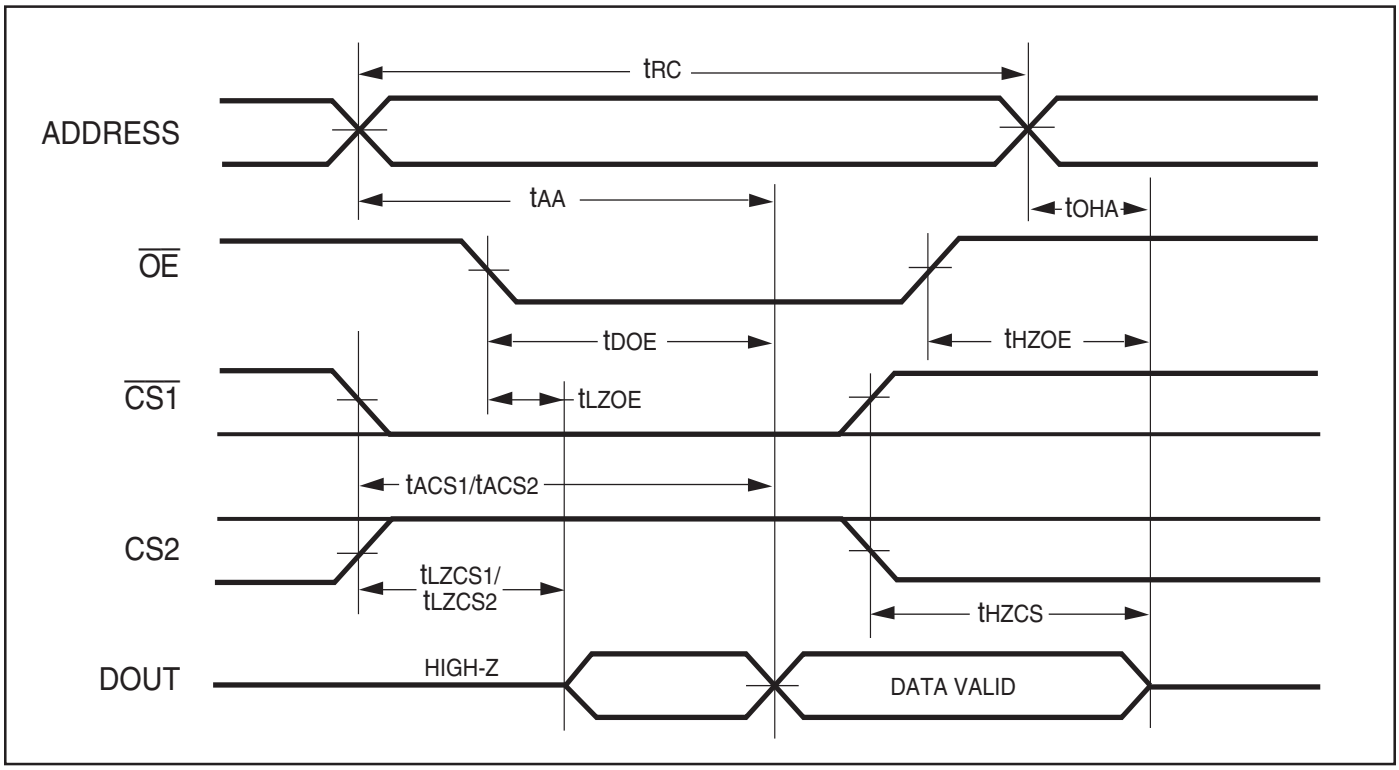
AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CS1}$ = $\overline{OE}$ = V_{IL}, CS2 = $\overline{WE}$ = V_{IH})



AC WAVEFORMS

READ CYCLE NO. 2[1,3] ($\overline{CS1}$, CS2, $\overline{OE}$ Controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS1}$= V_{IL}. CS2=$\overline{WE}$=V_{IH}.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW and CS2 HIGH transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

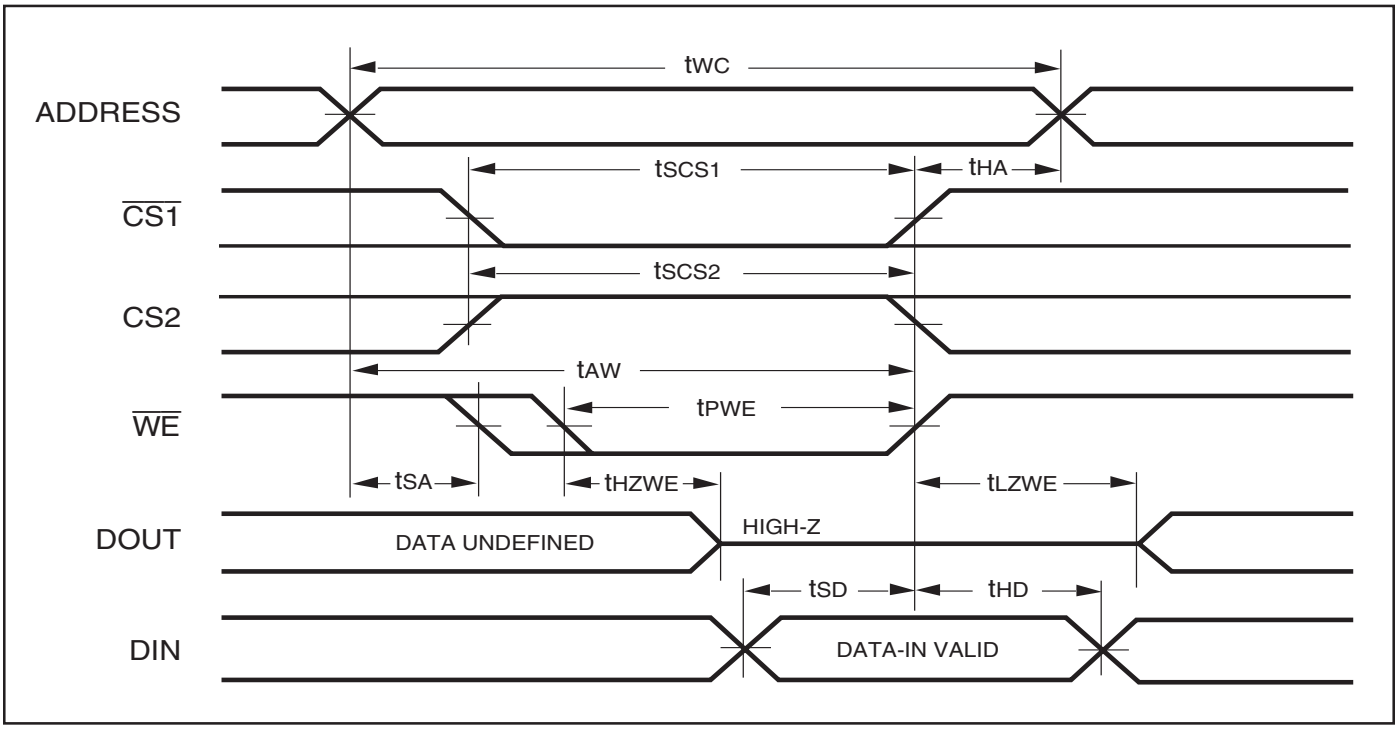
Symbol	Parameter	55 ns Min.	55 ns Max.	70 ns Min.	70 ns Max.	Unit
t_{WC}	Write Cycle Time	55	—	70	—	ns
t_{SCS1}/t_{SCS2}	$\overline{CS1}$/CS2 to Write End	45	—	60	—	ns
t_{AW}	Address Setup Time to Write End	45	—	60	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	40	—	50	—	ns
t_{SD}	Data Setup to Write End	25	—	30	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	25	—	25	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	ns

Notes:

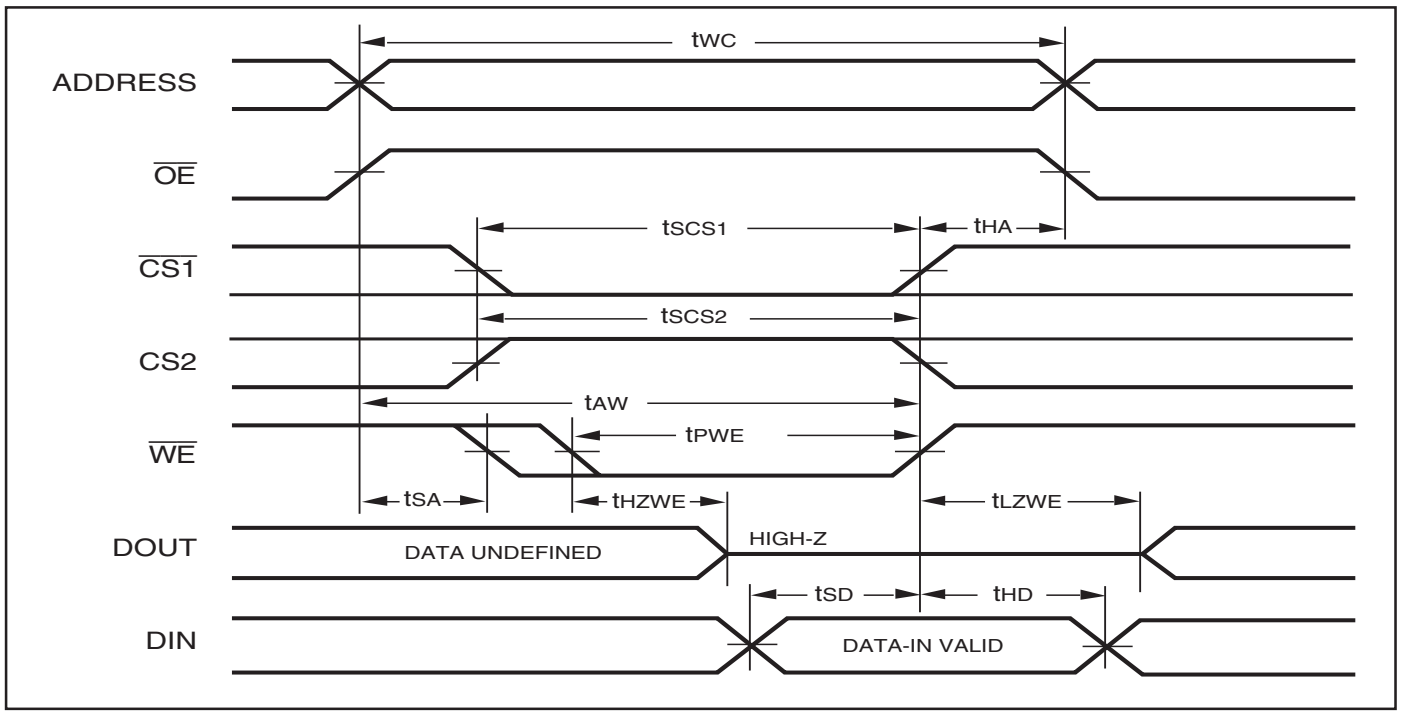
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CS1}$ LOW, CS2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
4. $t_{PWE} > t_{HZWE} + t_{SD}$ when $\overline{OE}$ is LOW.

AC WAVEFORMS

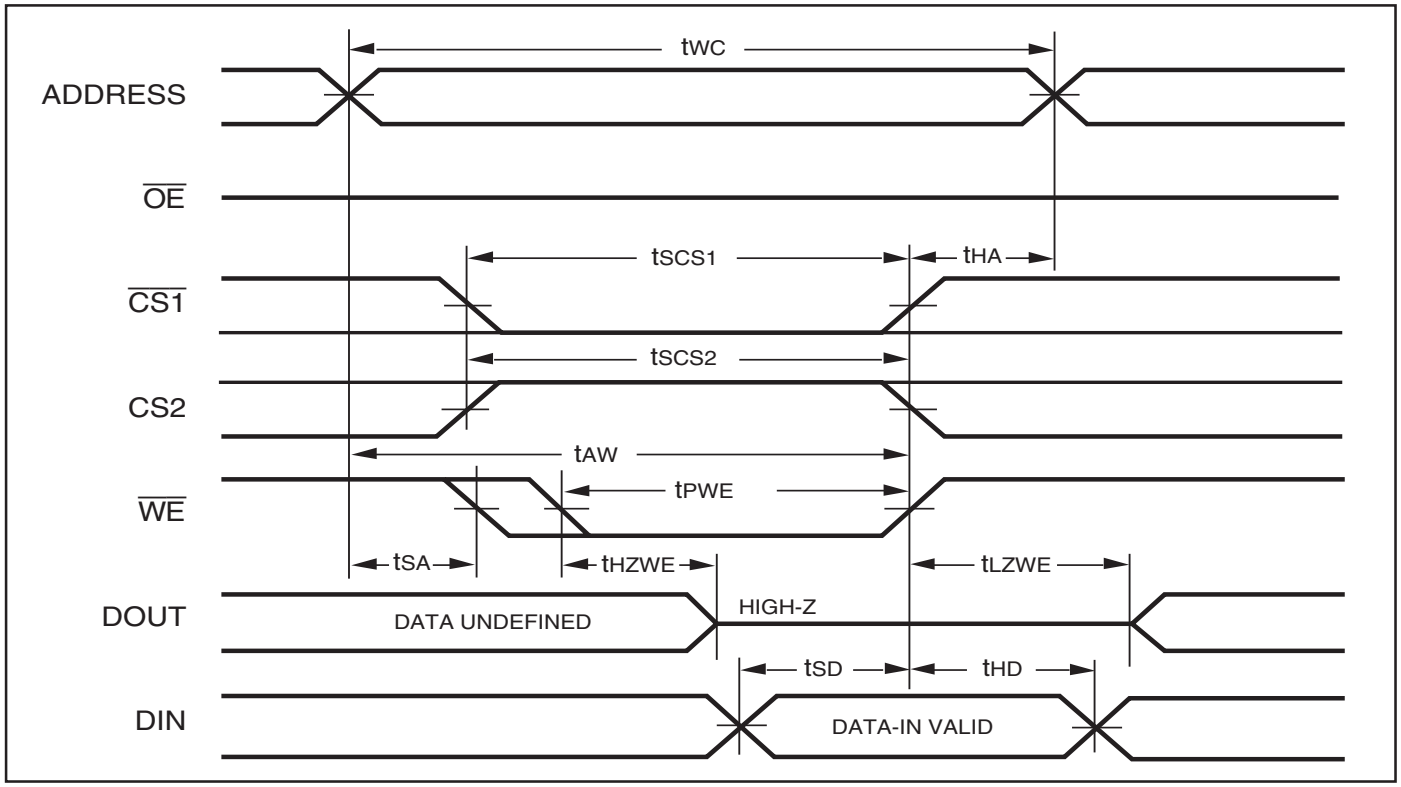
WRITE CYCLE NO. 1 ($\overline{CS1}$/CS2 Controlled, $\overline{OE}$ = HIGH or LOW)



WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)



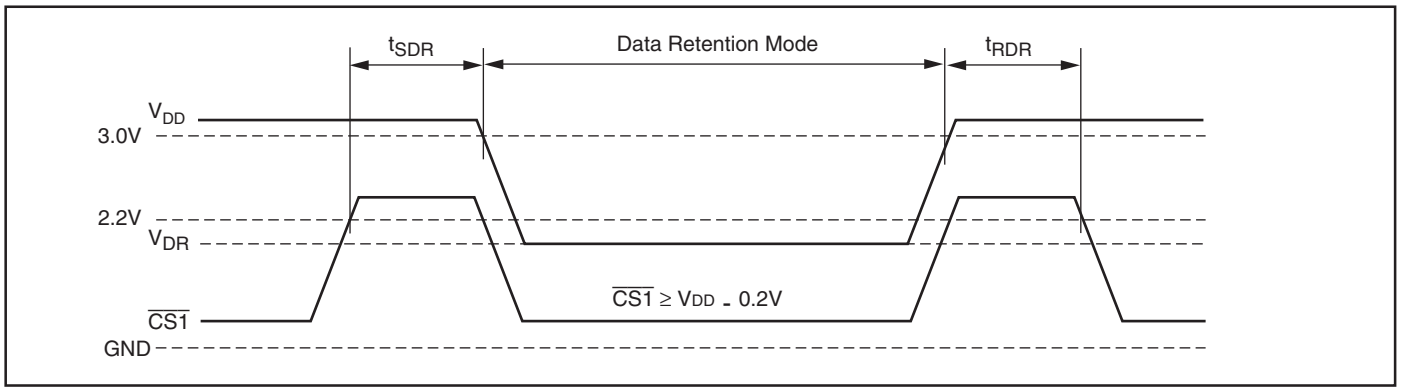
WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



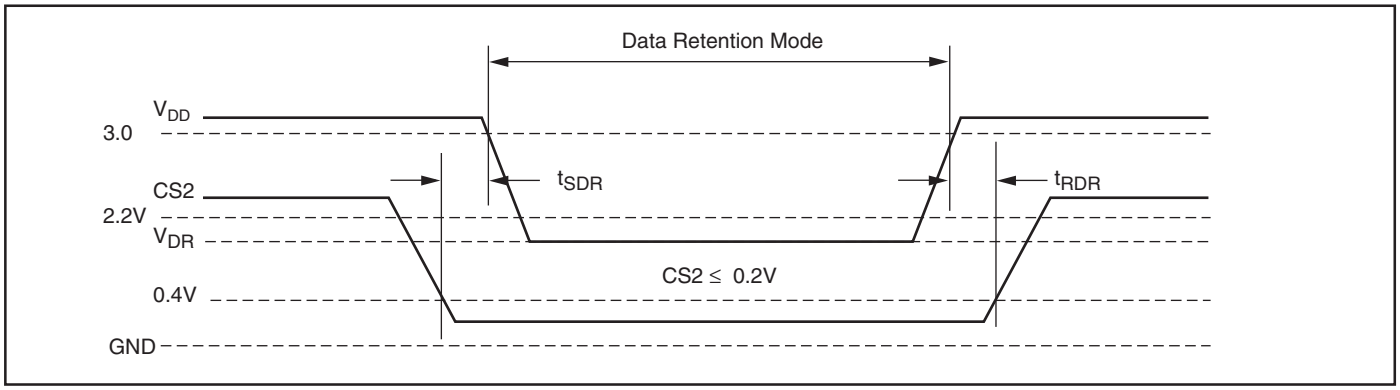
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	1.2	3.6	V
I_{DR}	Data Retention Current	V_{DD} = 1.2V, $\overline{CS1} \geq V_{DD} - 0.2V$	—	20	µA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	ns

DATA RETENTION WAVEFORM ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM (CS2 Controlled)

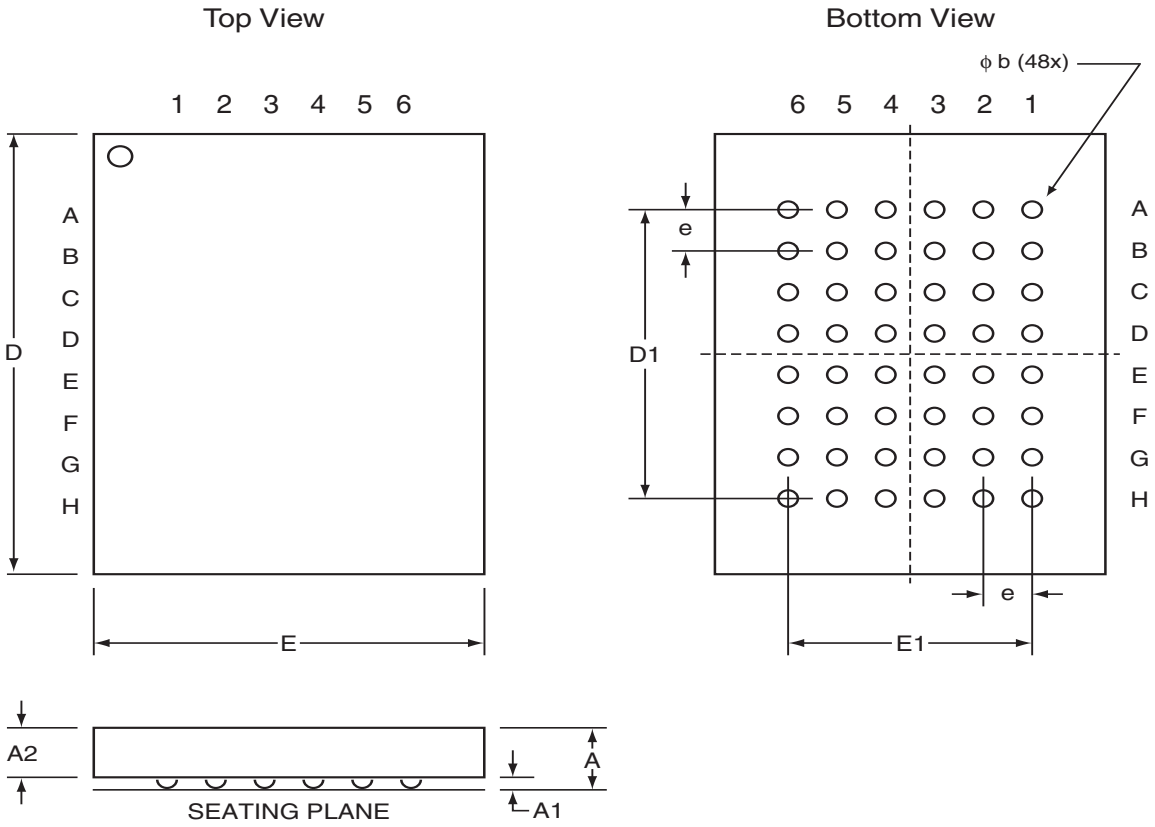


ORDERING INFORMATION: IS62WV10248BLL (2.5V - 3.6V)

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS62WV10248BLL-55BI IS62WV10248BLL-55BLI	mini BGA (7.2mm x 8.7mm) mini BGA (7.2mm x 8.7mm), Lead-free
70	IS62WV10248BLL-70BI	mini BGA (7.2mm x 8.7mm)
70	IS62WV10248BLL-70XI	DIE

Mini Ball Grid Array
Package Code: B (48-pin)



mBGA - 7.2mm x 8.7mm

	MILLIMETERS			INCHES		
Sym.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
N0. Leads		**48**				
A	—	—	1.20	—	—	0.047
A1	0 .24	—	0.30	0.009	—	0.012
A2	0.60	—	—	0.024	—	—
D	8.60	8.70	8.80	0.339	0.343	0.346
D1		5.25BSC			0.207BSC	
E	7.10	7.20	7.30	0.280	0.283	0.287
E1		3.75BSC			0.148BSC	
e		0.75BSC			0.030BSC	
b	0.30	0.35	0.40	0.012	0.014	0.016

Notes:
1. Controlling dimensions are in millimeters.