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IAR Debug probes User Guide

I-jet®, I-jet Trace, and I-scope™

for Advanced RISC Machines Ltd's ARM® Cores



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I-jet

- Introduction
- Working with I-jet
- Technical specifications

Introduction

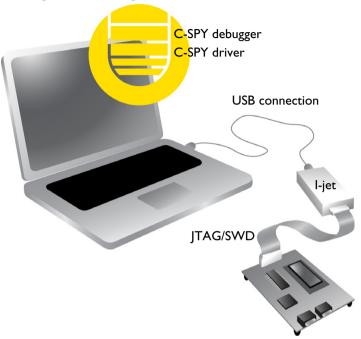
These topics are covered:

- The I-jet in-circuit debugging probe
- Requirements
- Supported ARM core families
- Target connections.

THE I-JET IN-CIRCUIT DEBUGGING PROBE

The I-jet in-circuit debugging probe has full support for on-chip trace: ETB, MTB, and TMC (Trace Memory Controller).

I-jet connects to the target board via a JTAG, SWD, or cJTAG connection, and to the host computer via the USB port.



I-jet communicates using USB 2.0. USB 1.0 is also supported but not advised. The I-jet in-circuit debugging probe is also referred to as a debug probe, debug adapter, or JTAG in-circuit emulator by different tool vendors.



I-jet streams the program counter, variables, and power measurement data to the host computer to provide a view into program execution in real time. Besides the typical JTAG debugging, I-jet is capable of providing power to the target board and measuring

it with sufficient accuracy to provide a power profile during program execution in real time. This feature is referred to as *power debugging*.

For debugging Cortex devices, I-jet also supports the SWO (Serial Wire Output) feature, which can be used for tracing the program execution and tracking variables at predefined points in your code.

The I-jet in-circuit debugging probe has full support for on-chip trace: ETB, MTB, and TMC (Trace Memory Controller).

REQUIREMENTS

I-jet needs to be controlled by the IAR C-SPY® Debugger which comes with the IAR Embedded Workbench® IDE.

SUPPORTED ARM CORE FAMILIES

These cores are currently supported:

- ARM7
- ARM9
- ARM11
- Cortex-M
- Cortex-R
- Cortex-A.

TARGET CONNECTIONS

These interfaces are supported:

- MIPI-20 (part number SHF-110-01-L-D): JTAG, cJTAG, SWD, SWO, ETM
- MIPI-10 (part number SHF-105-01-L-D): JTAG, cJTAG, SWD, SWO
- ARM-20 (part number HTST-110-01-L-DV): JTAG, cJTAG, SWD, SWO

I-jet comes with a MIPI-20 connector on the front panel and with MIPI-20 and MIPI-10 cables, as well as a legacy ARM-20 adapter.

All other available I-jet adapters are also compatible with I-jet Trace.

Working with I-jet

These tasks are covered:

- Setup and installation
- Connecting the target system.

• Updating the probe firmware

For information about debugging using I-jet, see the *C-SPY® Debugging Guide for ARM*.

SETUP AND INSTALLATION

Software

Before you can use I-jet, you need to install IAR Embedded Workbench for ARM.

Probe setup

I-jet does not require any special driver software installation. Normally, all drivers for I-jet are automatically installed as part of the installation of IAR Embedded Workbench.

If you need to install the USB driver manually, navigate to

For information about using multiple I-jet probes on the same host computer, see the *C-SPY® Debugging Guide for ARM*.

CONNECTING THE TARGET SYSTEM

Power-up your I-jet probe

- I Connect I-jet to the host computer using the USB micro cable.
- 2 Connect I-jet to the target board using the cable that matches the target board connector (MIPI-20 or MIPI-10). If a standard JTAG connector is used, you must first plug the ARM-20 to MIPI-20 adapter into the JTAG connector.

Note: No harm is done if the above order is reversed.



To prevent damage, the target GND and the USB host GND must be at the same level. When *hot-plugging*, make sure that the PC and the target board power supply are connected to the same grounded wall outlet or a common grounded desktop power strip.

Power up your evaluation board

If you have an evaluation board that is prepared for it, you can power the board via I-jet through pin 19 on the standard ARM-20 connector, or pin 11/13 on the small MIPI-20 connector. Target power of up to 420 mA can be supplied from I-jet with overload protection. Most of the IAR Systems KickStart Kits contain an evaluation board that can be powered this way. Make sure that the power jumper found on most of these boards matches your setup.

Note: The target board will get power via I-Jet once you choose the **Download and Debug** or **Debug without Downloading** command, but not before.

Note: The only way to use the power debugging feature is to power up your evaluation board via I-jet.

UPDATING THE PROBE FIRMWARE

I-jet and I-jet Trace are designed so that firmware updates are not necessary unless new features added to IAR Embedded Workbench for ARM require extra hardware support. When a new version of IAR Embedded Workbench for ARM is released and a new feature that requires new firmware is used, C-SPY displays a message in the **Debug Log** window asking you to update the firmware.

Note: Support for new MCU devices is managed totally by software updates in IAR Embedded Workbench for ARM and has nothing to do with I-jet or I-jet Trace firmware.

For more information about firmware versions, see the release notes.

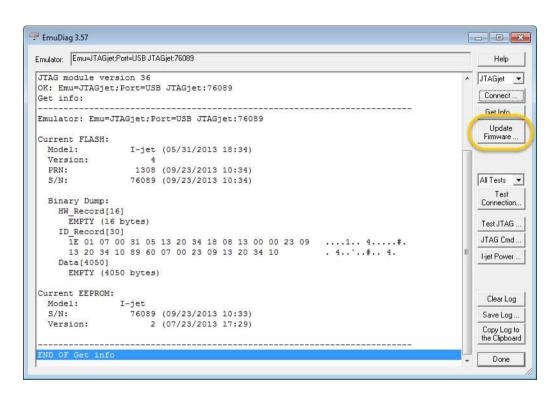
To update the probe firmware:

In IAR Embedded Workbench, choose I-jet/JTAGjet>EmuDiag to display the About to Connect to an Emulator dialog box.

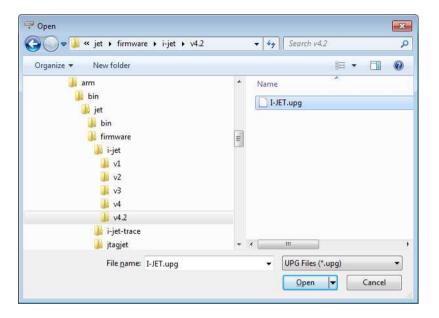


Select Connect to an Emulator Automatically and click Next.

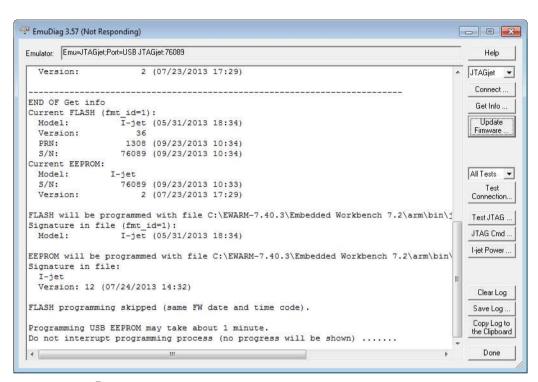
2 In the EmuDiag dialog box that is displayed, click the Update Firmware button.



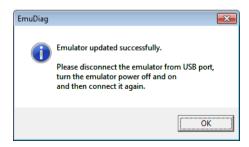
3 In the dialog box that is displayed, browse to the arm\bin\jet\firmware\i-jet folder of your IAR Embedded Workbench installation. In one of the subfolders, select the firmware file that you want to use and click **Open**.



4 The update log information is printed in the **EmuDiag** dialog box.



5 When the firmware update is complete, a message is displayed.



Technical specifications

Reference information about:

- The I-jet package, page 13
- Model specifications, page 13
- JTAG timing specification, page 15
- Hardware revision history, page 16
- Target interface, page 17
- The JTAG/SWD MIPI-20 cable, page 17
- The JTAG/SWD MIPI-10 cable, page 19
- Indicators, page 20
- Adapters, page 21.

THE I-JET PACKAGE

The I-jet package contains:

- The I-jet in-circuit debugging probe
- MIPI-20 JTAG cable
- MIPI-10 JTAG cable
- USB 2.0 Micro B cable
- MIPI-20 to ARM-20 adapter
- Welcome letter.

MODEL SPECIFICATIONS

These are the specifications of I-jet:

USB speed 480 Mbps (USB 2.0)

USB connection Micro-B

Target connection MIPI-20, MIPI-10

Adapters included MIPI-20 to ARM-20

I-jet debug interface JTAG and SWD

JTAG/SWD maximum clock 32 MHz

SWO protocols supported Manchester and UART

SWO maximum speed 60 Mbps

Power supplied to target 420 mA max at 4.4 V-5 V

Over-current protection ~520 mA

Target power measurement resolution ~160 uA

Target power measurement speed up to 200 ksps (kilo samples per second)

JTAG voltage range (auto-sensing) 1.65 V to 5.5 V

JTAG VTref measurement resolution ~2 mV

Current draw from VTref <50 uA

JTAG clock rise/fall time (TCK) <= 2 ns*

Clock fall time <= 2 ns*

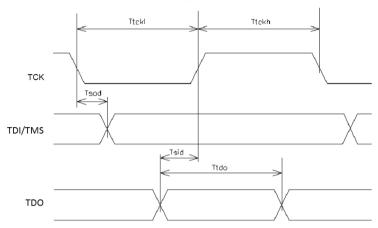
I-jet comes with a 20-pin MIPI connector (0.05 in \times 0.05 in pitch) on the front panel. It includes two cables:

- A 6-inch cable with 20-pin MIPI connectors on both ends for the Cortex-M targets with 20-pin MIPI headers. Pin 7 on each end is keyed with a white plug.
- A 6-inch cable with 20-pin MIPI connectors on one side (to connect to I-jet), and 10-pin MIPI connector on the other side for connection to Cortex-M targets with 10-pin headers. Pin 7 on each end is keyed with a white plug. A red stripe on the cable indicates pin 1 (VTref).

^{* &}lt;= 4 ns when the target board is connected

JTAG TIMING SPECIFICATION

This figure shows the JTAG timing and parameters:



In a JTAG device that fully complies to IEEE1149.1 standard, the TDI/TMS signals should be sampled on the rising edge of TCK, and TDO should be sent on the falling edge of TCK. I-jet takes advantage of these requirements and changes its TDI and TMS signals on the falling edge of TCK and samples the TDO on the rising edge of TCK. However, to accommodate target boards with long JTAG chains and fast JTAG clocks, I-jet allows TDO to be as late as 50 ns after the rising edge of TCK.

Note: In the adaptive mode of operation, I-jet samples the TDO on the rising edge of RTCK rather than TCK.

This table shows the timing specifications of the JTAG port measured at the end of its MIPI-20 cable without connection to target (VTref set to 3.3 V). The only load on the measured signals is the oscilloscope 3.9 pF probe.

Parameter	Min	Max	Description
T _{tckl}	15.6 ns	250 us	TCK LOW period
T_tckh	15.6 ns	250 us	TCK HIGH period
T _{sod} I		2.0 ns	TDI and TMS outputs valid from TCK falling
T_{sid}^2	3 ns before TCK to 50 ns after TCK		TDO setup to TCK rising
T_tdo	T_{tckl}		TDO valid length

Table 1: Timing for the I-jet JTAG port

 $1~T_{sod}$ is the maximum delay from the falling edge of TCK and a valid level on the I-jet output signals TDI and TMS. The target MCU will sample these signals on the following rising edge of TCK and so the minimum setup time for the target, relative to the rising edge of TCK, is T_{bsol} .

 $2\,T_{sid}$ is the minimum setup time for the TDO input signal, relative to the rising edge of TCK when I-jet samples this signal. Because the target MCU changes its TDO value on the previous falling edge of TCK, there might not be enough time at very-high JTAG speeds for the TDO to arrive before the positive edge of TCK. To compensate for any TDO delays, I-jet configures itself automatically to delays introduced to the TDO by the target board and will tolerate TDO delays of up to 50 ns after the positive edge of the TCK.

HARDWARE REVISION HISTORY

These are the versions of I-jet:

Version	Change specification	Date
Version A	The first version	April 2012

Table 2: I-jet versions

Version, production date, and serial number can be found on the backside of the probe.

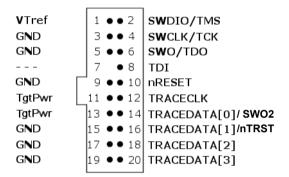
Note: In IAR Embedded Workbench, choose **I-jet/JTAGjet>EmuDiag** to open the **EmuDiag** dialog box where you can find both hardware and firmware versions of the plugged-in I-jet.

TARGET INTERFACE

This section contains descriptions of pinout, signals, and connectors.

The JTAG/SWD - MIPI-20 cable

I-jet comes with a 6-inch cable with 20-pin MIPI connectors on both ends for the Cortex-M devices with 20-pin MIPI headers. Pin 7 on each end is keyed with a white plug:



The mating connector for a target board has the part number SHF-110-01-L-D.

These are the MIPI-20 pin definitions:

Pin	Signal	Туре	Description
I	VTref	Input	The target reference voltage. Used by I-jet to check whether the target has power, to create the logic-level reference for the input comparators, and to control the output logic levels to the target. It is normally fed from JTAG I/O voltage.
2	SWDIO/TMS	I/O, output	JTAG mode set input of target CPU. This pin should be pulled up on the target. Typically connected to TMS of the target CPU.
3			This pin is a GND pin connected to GND in I-jet. It should also be connected to GND in the target system.
4	SWCLK/TCK	Output	JTAG clock signal to target CPU. It is recommended that this pin is pulled to a defined state of the target board. Typically connected to TCK of the target CPU.

Table 3: MIPI-20 pin definitions

Pin	Signal	Туре	Description
5			This pin is a GND pin connected to GND in I-jet. It should also be connected to GND in the target system.
6	SWO/TDO	Input	JTAG data output from target CPU. Typically connected to TDO of the target CPU. When using SWD, this pin is used as Serial Wire Output trace port. (Optional, but not required for SWD communication.)
			This pin (normally pin 7) does not exist.
8	TDI	Output	JTAG data input of target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TDI of the target CPU. For CPUs which do not provide TDI (SWD-only devices), this pin is not used (tri-stated).
9			This pin is a GND pin connected to GND in I-jet. It should also be connected to GND in the target system.
10	nRESET	I/O	Target CPU reset signal. Typically connected to the RESET pin of the target CPU, which is typically called nRST, nRESET, or RESET.
11	TgtPwr	Output	This pin can be used for supplying 5 V power to the target hardware from I-jet.
12 Not used	TRACECLK	Input	Input trace clock.
13	TgtPwr	Output	This pin can be used for supplying 5 V power to the target hardware from I-jet.
14 Not used	TRACEDATA[0]/ SWO2	Input	Input Trace data pin 0. This pin can be used as secondary SWO.
15			This pin is a GND pin connected to GND in I-jet. It should also be connected to GND in the target system.
16 Not used	TRACEDATA[I]/ nTRST	Input	Input Trace data pin I. This pin can be used as $nTRST$.
17			This pin is a GND pin connected to GND in I-jet. It should also be connected to GND in the target system.

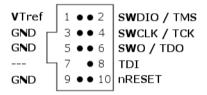
Table 3: MIPI-20 pin definitions

Pin	Signal	Туре	Description
18	TRACEDATA[2]	Input	Input Trace data pin 2.
Not used			
19			This pin is a GND pin connected to GND in I-jet. It should also be connected to GND in the target system.
20 Not used	TRACEDATA[3]	Input	Input Trace data pin 3.

Table 3: MIPI-20 pin definitions

The JTAG/SWD - MIPI-10 cable

I-jet also comes with a 6-inch cable with a 20-pin MIPI connector on one side (to connect to I-jet) and a 10-pin MIPI connector on the other side for connection to Cortex devices with 10-pin headers. Pin 7 on each end is keyed with a white plug:



The mating connector for a target board has the part number SHF-105-01-L-D.

These are the MIPI-10 pin definitions:

Pin	Signal	Туре	Description
ī	VTref	Input	The target reference voltage. Used by I-jet to check whether the target has power, to create the logic-level reference for the input comparators, and to control the output logic levels to the target. It is normally fed from JTAG I/O voltage.
2	SWDIO/TMS	I/O, output	JTAG mode set input of target CPU. This pin should be pulled up on the target. Typically connected to TMS of the target CPU. When using SWD, this pin is used as Serial Wire Output trace port. (Optional, not required for SWD communication)
3	GND	GND	Connected to logic GND on I-jet.
4	SWCLK/TCK	Output	JTAG clock signal to target CPU. It is recommended that this pin is pulled to a defined state of the target board. Typically connected to TCK of the target CPU.

Table 4: MIPI-10 pin definitions

Pin	Signal	Туре	Description
5	GND	GND	Connected to logic GND on I-jet.
6	SWO/TDO	Input	JTAG data output from target CPU. Typically connected to TDO of the target CPU.
7		KEY	KEY or GND.
8	TDI/NC	Output	JTAG data input of target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TDI of the target CPU. For CPUs that do not provide TDI (SWD-only devices), this pin is not used (tri-stated).
9	GND	GND	GND and target detect presence.
10	nRESET	Output	nRESET or TRST.

Table 4: MIPI-10 pin definitions

INDICATORS

I-jet has three LED indicators on the top, marked TPWR, DBG, and USB. This section describes the indicators and their statuses.

The TPWR indicator (Target power)

Indicator status	Description
Off	Power to target is not provided by I-jet.
Green	Power to target is provided by I-jet.
Yellow	Warning. Power to target is above 420 mA.
Red	Error. Overcurrent limit (520 mA) detected and power to target was switched off for protection.

Table 5: TPWR indicator statuses

The DBG indicator (JTAG/SWD)

Indicator status	Description
Off	vTRef on JTAG header is too low.
Green	vTRef is at or above 1.8 V.
Green blinking	Indicates JTAG/SWD communication activity.

Table 6: JTAG indicator statuses

The USB indicator

Indicator status	Description
Off	No USB power.
Green steady	Initial state or no transfer.
Green blinking	USB transfers to or from I-jet.
Red blinking	USB enumeration.
Red steady	USB did not enumerate or broken hardware.

Table 7: USB indicator statuses

ADAPTERS

There are a number of useful adapters available. All of them are automatically recognized by I-jet. The following adapters are described in detail:

- The MIPI20 isolation adapter
- The MIPI-20 to ARM-20 adapter
- The MIPI-20 to TI-14 adapter
- The MIPI-20 to cTI-20 adapter.

Adapters not included in the I-jet package can be purchased from IAR Systems.

These are the mating target headers for the adapters

TI-14	cTI-20
HTST-107-01-L-DV	TML-110-02-GD-SM-006 (shrouded)
	FTR-II0-51-S-D-06 (unshrouded)

Table 8: Mating target headers, part numbers

The ADA to MIPI20-ISO isolation adapter

The isolation adapter galvanically isolates signals between the I-jet MIPI-20 connector and the target MIPI-20 connector. You can use it to reduce the risk of damage to the I-jet debug probe associated with power ground loops, voltage spikes, electrostatic discharge (ESD), and noisy power and ground lines generated by targets which drive high-current motors and other machinery.

The adapter has two MIPI-20 headers marked **TO I-JET** and **TO TARGET**. Make sure to connect the headers correctly because switching the sides will not work and might damage the adapter. The target side of the isolation adapter can be used with any other passive I-jet adapters ID needed: ADA-MIPI20-ARM20, ADA-MIPI20-TI14, ADA-MIPI20-CTI20, and the MIPI20-MIPI10 cable.



The adapter is automatically recognized by the C-SPY, and the adapter powers up and the green RDY LED is turned on.

Specifications

• Galvanic isolation up to 3000 V peak* (< 1 sec transients. See safety note.) with continuous working voltage operation of up to 300 V.

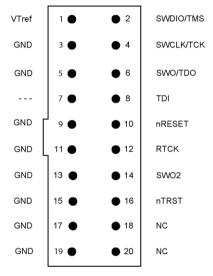
150

- Compatible with I-jet
- Supports JTAG, SWD, and SWO debug modes
- Compatible with I-jet Trace in JTAG, SWD, and SWO modes only (ETM trace is not supported)
- Powered entirely by I-jet via pins 11 and 13 on the MIPI-20 header
- The RDY LED indicates that the unit is powered and ready to use
- Supports target voltages from 2.5 to 5 V
- JTAG clock speed up to 32 MHz

Compatibility notes

- The adapter might not be automatically detected and powered by older versions of IAR Embedded Workbench for ARM. In such cases, select the Target Power option on the Project>Options>Debugger>I-jet/JTAGjet>Setup page.
- The adapter does not supply power to target and therefore does not resume the target power consumption.
- When used with the TI14 and CTI20 adapters, the EMU0 and EMU1 signals are not connected.
- Due to added JTAG signals propagation delays, some target boards might not work at the full 32 MHz JTAG clock speed, so reducing the JTAG speed in C-SPY might be needed.
- The majority of target boards have the SWO signal routed to pin 6 of the target MIPI20 debug connector. In cases when pin 14 is used for SWO, you must move the 0R shunt (marked S1) up from position 3-2 to position 2-1.
- The adapter does not support 1.8 V JTAG signals from target. The target JTAG voltage range is limited to 2.5-5 V.
- The JTAG interface on the target side automatically adapts to the voltage given on the target VTREF pin (2.5 V-5 V). Because of the isolation barrier, the I-jet side uses its own voltage, independent of the target voltage. This is for information only and has no effect on the target JTAG operation.
- ETM trace is not supported by this adapter.
- This adapter cannot be used with I-scope.

MIPI20 connector pinout on target side



For more information about the signal descriptions, see *The JTAG/SWD - MIPI-20 cable*, page 17.

Important safety and disclaimer note

The continuous normal operation voltage across the isolation barrier should not exceed $300\ V\ DC.$

The isolation voltage only represents a measure of immunity to transient voltages—the probe should never be used as an element of a safety isolation system. For use with higher continuous voltages, additional isolation/insulation systems must be used in accordance with the safety standard requirements.

Use caution and follow all safety regulations when handling equipment subjected to high voltages.

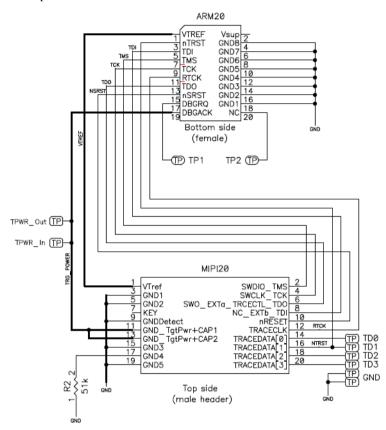


Touching any exposed circuitry on the target, the adapter, cables, or the I-jet probe can cause injuries or death.

IAR Systems or the manufacturer shall not be liable for any damages related to the use of this probe.

The MIPI-20 to ARM-20 adapter

The MIPI-20 to ARM-20 adapter is included with I-jet. It converts the MIPI-20 I-jet cable to the legacy ARM-20 (0.1 in \times 0.1 in pitch) JTAG headers. This is a diagram of the adapter:



These are the pin definitions of the ARM-20 adapter:

Pin	I-jet direction	Name	Description
nTRST	Output	Test Logic Reset	Test reset. Active LOW signal that resets the TAP controller's state machine.

Table 9: ARM-20 pin definitions