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ISD5100 SERIES

SINGLE-CHIP

1 TO 16 MINUTES DURATION

VOICE RECORD/PLAYBACK DEVICES

WITH DIGITAL STORAGE CAPABILITY

1. GENERAL DESCRIPTION

The ISD5100 ChipCorder® Series provide high quality, fully integrated, single-chip Record/Playback solutions for 1- to 16-minute messaging applications that are ideal for use in cellular phones, automotive communications, GPS/navigation systems and other portable products. The ISD5100 Series products are an enhancement of the ISD5000 architecture, providing: 1) the I^2C serial port - address, control and duration selection are accomplished through an I^2C interface to minimize pin count (ONLY two control lines required); 2) the capability of storing digital data, in addition to analog data. This feature allows customers to store phone numbers, system configuration parameters and message address locations for message management capability; 3) Various internal circuit blocks can be individually powered-up or -down for power saving.

The ISD5100 Series include:

- ISD5116 from 8 to 16 minutes
- ISD5108 from 4 to 8 minutes
- ISD5104 from 2 to 4 minutes
- ISD5102 from 1 to 2 minutes

Analog functions and audio gating have also been integrated into the ISD5100 Series products to allow easy interface with integrated digital cellular chip sets on the market. Audio paths have been designed to enable full duplex conversation record, voice memo, answering machine (including outgoing message playback) and call screening features. This product enables playback of messages while the phone is in standby, AND both simplex and duplex playback of messages while on a phone call.

Additional voice storage features for digital cellular phones include: 1) a personalized outgoing message can be sent to the person by getting caller-ID information from the host chipset, 2) a private call announce while on call can be heard from the host by giving caller-ID on call waiting information from the host chipset.

Logic Interface Options of 2.0V and 3.0V are supported by the ISD5100 Series to accommodate portable communication products (2.0- and 3.0-volt required).

Like other ChipCorder® products, the ISD5100 Series integrate the sampling clock, anti-aliasing and smoothing filters, and the multi-level storage array on a single-chip. For enhanced voice features, the ISD5100 Series eliminate external circuitry by integrating automatic gain control (AGC), a power amplifier/speaker driver, volume control, summing amplifiers, analog switches, and a car kit interface. Input level adjustable amplifiers are also included, providing a flexible interface for multiple applications.

Recordings are stored into on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through Nuvoton's patented multilevel storage technology. Voice and audio signals are stored directly into solid-state memory in their natural, uncompressed form, providing superior quality on voice and music reproduction.

2. FEATURES

Fully-Integrated Solution

- Single-chip voice record/playback solution
- Dual storage of digital and analog data
- Durations

Device	ISD5102	ISD5104	ISD5108	ISD5116
Duration	1 to 2 minutes	2 to 4 minutes	4 to 8 minutes	8 to 16 minutes

Low Power Consumption

- Supply Voltage
  - Commercial Temperature = +2.7V to +3.3V
  - Industrial Temperature = +2.7V to +3.3V (+2.7V to +3.6V for ISD5108 only)
- Supports 2.0V and 3.0V interface logic
- Operating Current:
  - $I_{CC\ Play}$ = 15 mA (typical)
  - $I_{CC\ Rec}$ = 30 mA (typical)
  - $I_{CC\ Feedthrough}$ = 12 mA (typical)
- Standby Current:
  - I_{SB} = 1μA (typical)
- Most stages can be individually powered down to minimize power consumption

Enhanced Voice Features

- One or two-way conversation record
- One or two-way message playback
- Voice memo record and playback
- Private call screening
- In-terminal answering machine
- Personalized outgoing message
- Private call announce while on call

Digital Memory Features

Device	ISD5102	ISD5104	ISD5108	ISD5116
Storage	Up to 512Kb	Up to 1 Mb	Up to 2 Mb	Up to 4 Mb

- Storage of phone numbers, system configuration parameters and message address table in some application

Easy-to-use and Control

- No compression algorithm development required
- User-controllable sampling rates
- Programmable analog interface
- Standard & Fast mode I^2C serial interface (100kHz – 400 kHz)
- Fully addressable for multiple messages

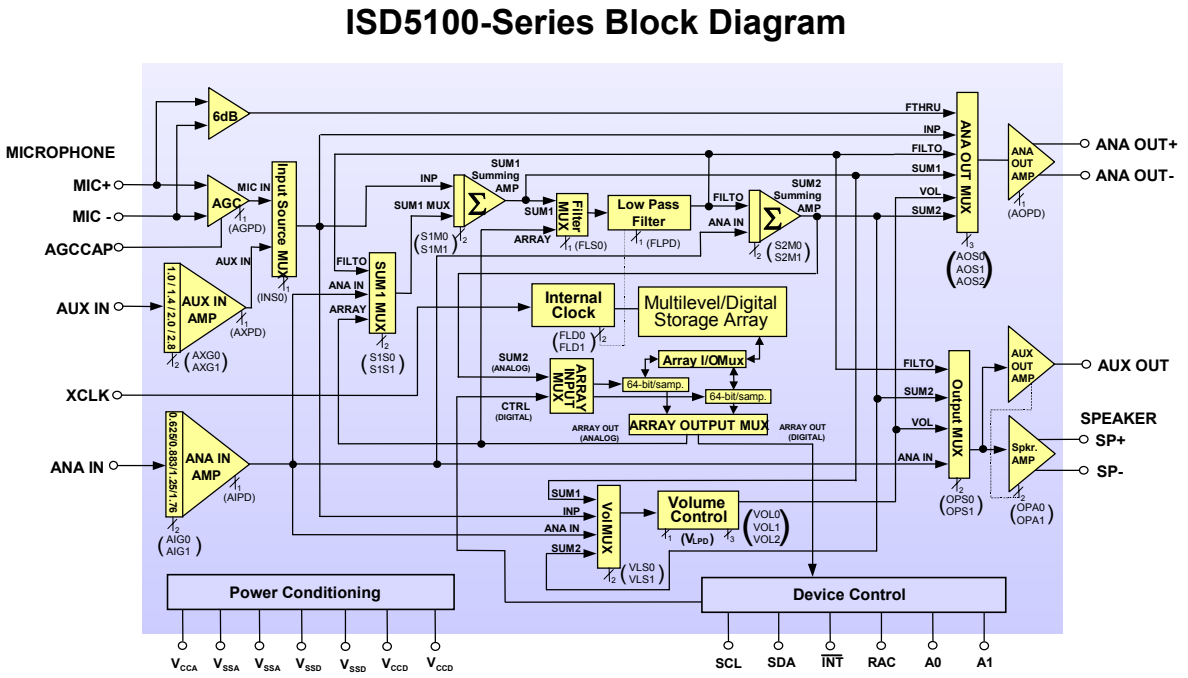
High Quality Solution

- High quality voice and music reproduction
- Nuvoton's standard 100-year message retention (typical)
- 100K record cycles (typical) for analog data
- 10K record cycles (typical) for digital data

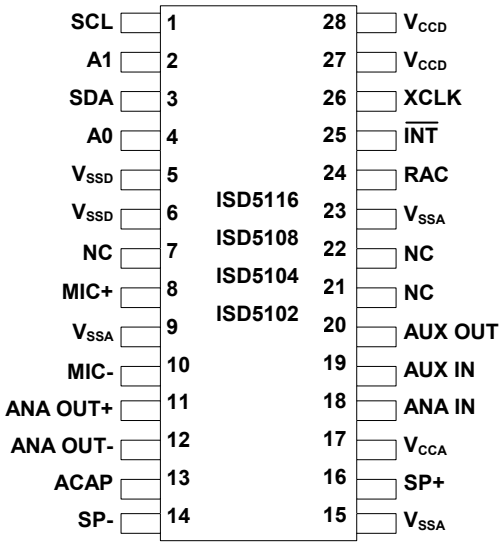
Options

- Available in die form, TSOP and SOIC and PDIP (ISD5116 Only)
- Temperature: Commercial – Packaged (0 to +70°C) & die (0 to +50°C); Industrial (-40 to +85°C)
- Pb-free package

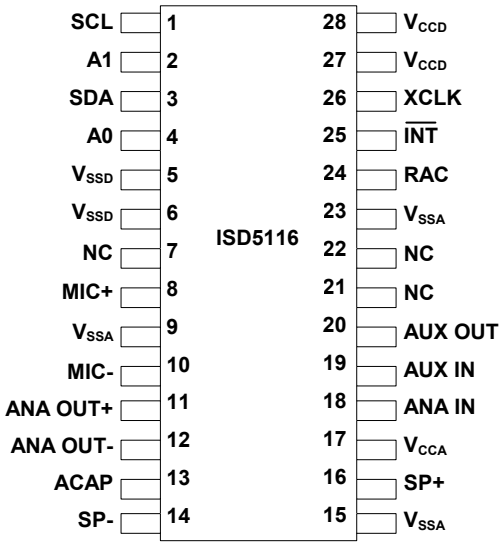
3. BLOCK DIAGRAM



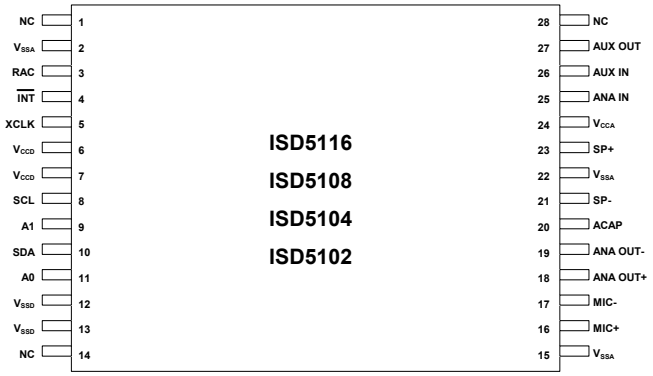
4. PIN CONFIGURATION



SOIC



PDIP



TSOP

5. PIN DESCRIPTION

Pin Name	SOIC/PDIP	TSOP	Functionality
SCL	1	8	I^2C Serial Clock Line: to clock the data into and out of the I^2C interface.
A1	2	9	Input pin that supplies the LSB +1 bit for the I^2C Slave Address.
SDA	3	10	I^2C Serial Data Line: Data is passed between devices on the bus over this line.
A0	4	11	Input pin that supplies the LSB for the I^2C Slave Address.
V_{SSD}	5,6	12,13	Digital Ground.
NC	7,21,22	1,14,28	No Connect.
MIC+	8	16	Differential Positive Input for the microphone amplifier.
V_{SSA}	9,15,23	2,15,22	Analog Ground.
MIC-	10	17	Differential Negative Input for the microphone amplifier.
ANA OUT+	11	18	Differential Positive Analog Output for ANA OUT.
ANA OUT-	12	19	Differential Negative Analog Output for ANA OUT.
ACAP	13	20	AGC/AutoMute Capacitor: Required for the on-chip AGC amplifier during record and AutoMute function during playback.
SP-	14	21	Differential Negative Speaker Output: When the speaker outputs are in use, the AUX OUT output is disabled.
SP+	16	23	Differential Positive Speaker Output.
V_{CCA}	17	24	Analog Supply Voltage: This pin supplies power to the analog sections of the device. It should be carefully bypassed to Analog Ground to insure correct device operation.
ANA IN	18	25	Analog Input: one of the analog inputs with selectable gain.
AUX IN	19	26	Auxiliary Input: one of the analog inputs with selectable gain.
AUX OUT	20	27	Auxiliary Output: one the analog outputs of the device. When this output is used, the SP+ and SP- outputs are disabled.
RAC	24	3	Row Address Clock; an open drain output. The RAC pin goes LOW T_{RACL}[1] before the end of each row of memory and returns HIGH at exactly the end of each row of memory.
$\overline{INT}$	25	4	Interrupt Output; an open drain output that indicates that a set EOM bit has been found during Playback or that the chip is in an Overflow (OVF) condition. This pin remains LOW until a Read Status command is executed.
XCLK	26	5	This pin must be grounded for utilizing internal clock. For precision timing control, external clock signal can be applied through this pin.
V_{CCD}	27,28	6,7	Digital Supply Voltage. These pins supply power to the digital sections of the device. They must be carefully bypassed to Digital Ground to insure correct device operation.

[1] See the Parameters section

6. FUNCTIONAL DESCRIPTION

6.1. OVERVIEW

6.1.1 Speech/Voice Quality

The ISD5100 ChipCorder Series can be configured via software to operate at 4.0, 5.3, 6.4 or 8.0 kHz sampling frequency to select appropriate voice quality. Increasing the duration decreases the sampling frequency and bandwidth, which affects audio quality. The table in the following section shows the relationship between sampling frequency, duration and filter pass band.

6.1.2 Duration

To meet system requirements, the ISD5100 Series are single-chip solution, which provide 1 to 16 minutes of voice record and playback, depending upon the sample rates chosen.

Sample Rate (kHz)	Duration [1]				Typical Filter Knee (kHz)
	ISD5116	ISD5108	ISD5104	ISD5102	
8.0	8 min 44 sec	4 min 22 sec	2 min 11 sec	1 min 5 sec	3.4
6.4	10 min 55 sec	5 min 27 sec	2 min 43 sec	1 min 21 sec	2.7
5.3	13 min 6 sec	6 min 33 sec	3 min 17 sec	1 min 38 sec	2.3
4.0	17 min 28 sec	8 min 44 sec	4 min 22 sec	2 min 11 sec	1.7

[1] Minus any pages selected for digital storage

6.1.3 Flash Technology

One of the benefits of Nuvoton's ChipCorder technology is the use of on-chip Flash memory, which provides zero-power message storage. The message is retained for up to 100 years (typically) without power. In addition, the device can be re-recorded over 10,000 times (typically) for the digital data and over 100,000 times (typically) for the analog messages.

A new feature has been added that allows memory space in the ISD5100 Series to be allocated to either digital or analog storage when recorded. The fact that a section has been assigned digital or analog data is stored in the Message Address Table by the system microcontroller when the recording is made.

6.1.4 Microcontroller Interface

The ISD5100 Series are controlled through an I^2C 2-wire interface. This synchronous serial port allows commands, configurations, address data, and digital data to be loaded into the device, while allowing status, digital data and current address information to be read back from the device. In addition to the serial interface, two other status pins can feedback to the microcontroller for enhanced

interface. These are the $\overline{RAC}$ timing pin and the $\overline{INT}$ pin for interrupts to the controller. Communications with all the internal registers of any operations are through the serial bus, as well as digital memory Read and Write operations.

6.1.5 Programming

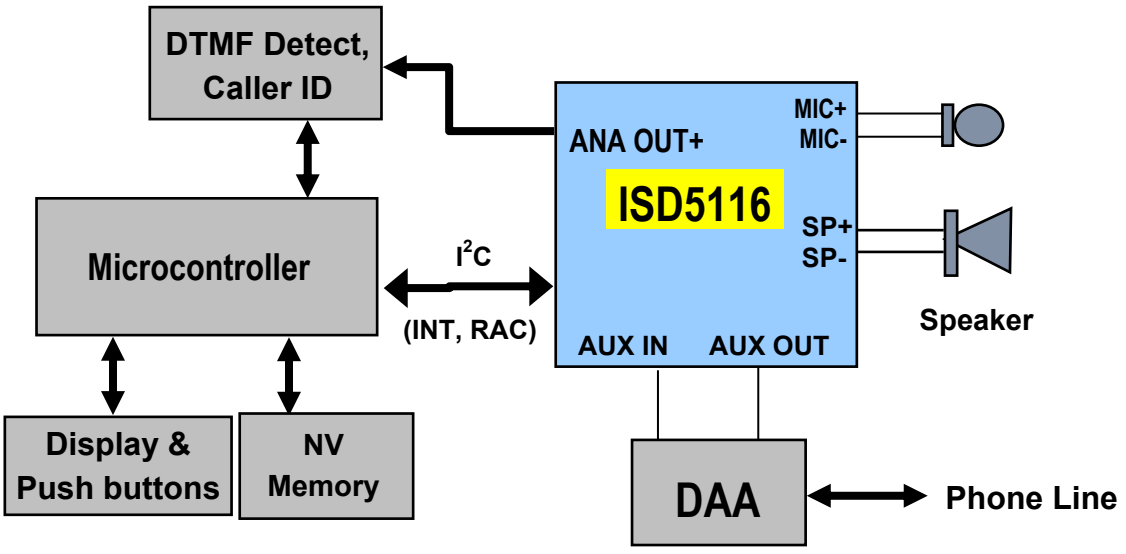
The ISD5100 Series are also ideal for playback-only applications, where single or multiple messages may be played back when desired. Playback is controlled through the I^2C interface. Once the desired message configuration is created, duplicates can easily be generated via a third-party programmer. For more information on available application tools and programmers, please see the Nuvoton web site at www.Nuvoton-usa.com

6.2. FUNCTIONAL DETAILS

The ISD5100 Series are single chip solutions for analog and digital data storage. The array can be divided between analog and digital storage according to user's choice, when the device is configured.

The below block diagram shows that the ISD5116 device can be easily designed into a telephone answering machine (TAD). Both Mic inputs transmit the voice input signal from the microphone to perform OGM recording, as well as to record the speech during phone conversation (simplex).

When the TAD is activated, the voice of the other party from the phone line feeds into the AUX IN, and is recorded into the ISD5116 device. Then the new messge is usually indicated with blinking new message LED. Hence, during playback, the recorded message is sent out to speaker with volume control. Two I^2C pins are used for all communications between the ChipCorder and the microcontroller for analog and/or digital storage, and the two outputs, INT and RAC are feedback to microcontroller for message management.



For duplex recording, speech from Mic inputs and message from received path can be directly recorded into the array simultaneously, then playback afterwards. In addition, for speaker phone

operation, voice from Mic inputs are fed to AUX OUT and transmitted to the phone line, while message from other party is input from the AUX IN, then fed through to the speaker for listening.

The ISD5100 device has the flexibility for other applications, because the audio paths can be configured differently, with each circuit block being powered-up or –down individually, according to the applications requirement.

6.2.1 Internal Registers

The ISD5100 Series have multiple internal registers that are used to store the address information and the configuration or set-up of the device. The two 16-bit configuration registers control the audio paths through the device, the sample frequency, the various gains and attenuations, power up and down of different sections, and the volume settings. These registers are discussed in detail in section 7.3.5.

6.2.2 Memory Architecture

The ISD5100 Series memory array are arranged in various pages (or rows) of each 2048 bits as follows. The primary addressing for the pages are handled by 11 bits of address input in the analog mode.

A memory page is 2048 bits organized as thirty-two 64-bit "blocks" when used for digital storage. The contents of a page are either analog or digital. This is determined by instruction (opcode) at the time the data is written. A record of where is analog and where is digital, is stored in a message address table (MAT) by the system microcontroller. The MAT is a table kept in the microcontroller memory that defines the status of each message “page”. It can be stored back into the ISD5100 Series if the power fails or the system is turned off. Using this table allows efficient message management. Segments of messages can be stored wherever there is available space in the memory array. [This is explained in detail for the ISD5008 in Applications Note #9 and will be similarly described in a later Note for the ISD5100-Series.]

Products	Pages (Rows)	Bits/Page	Memory Size
ISD5116	2048	2048	4,194,304 bits
ISD5108	1024	2048	2,097,152 bits
ISD5104	512	2048	1,048,576 bits
ISD5102	256	2048	524,288 bits

When a page is used for analog storage, the same 32 blocks are present but there are 8 EOM (End-of-Message) markers. This means that for each 4 blocks there is an EOM marker at the end. Thus, when recording, the analog recording will stop at any one of eight positions. At 8 kHz sampling frequency, this results in a resolution of 32 msec when ENDING an analog recording. Beginning an analog recording is limited to the 256 msec resolution provided by the 11-bit address. A recording does not immediately stop when the Stop command is given, but continues until the 32 millisecond block is filled. Then a bit is placed in the EOM memory to develop the interrupt that signals a message is finished playing in the Playback mode.

Digital data is sent and received serially over the I²C interface. The data is serial-to-parallel converted and stored in one of two alternating (commutating) 64-bit shift registers. When an input register is full, it becomes the register that is parallel written into the array. The prior write register becomes the new serial input register. A mechanism is built-in to ensure there is always a register available for storing new data.

Storing data in the memory is accomplished by accepting data one byte at a time and issuing an acknowledge. If data is coming in faster than it can be written, the chip issues an acknowledge to the host microcontroller, but holds SCL LOW until it is ready to accept more data. (See section 7.5.2 for details).

The read mode is the opposite of the write mode. Data is read into one of two 64-bit registers from the array and serially sent to the I²C interface. (See section 7.5.3 for details).

6.3. OPERATIONAL MODES DESCRIPTION

6.3.1 I²C Interface

To use more than four ISD5100 Series devices in an application requires some external switching of the I²C interface.

I²C interface

Important note: *The rest of this data sheet will assume that the reader is familiar with the I²C serial interface. Additional information on I²C may be found in section 10 on page 72 of this document. If you are not familiar with this serial protocol, please read this section to familiarize yourself with it. A large amount of additional information on I²C can also be found on the Philips web page at* http://www.philips.com/.

I²C Slave Address

The ISD5100 Series have 7-bit slave address of <100 00xy> where x and y are equal to the state, respectively, of the external address pins A1 and A0. Because all data bytes are required to be 8 bits, the LSB of the address byte is the Read/Write selection bit that tells the slave whether to transmit or receive data. Therefore, there are 8 possible slave addresses for the ISD5100-Series. These are:

Pinout Table

A1	A0	Slave Address	$\overline{R/W}$ Bit	HEX Value
0	0	<100 0000>	0	80
0	1	<100 0001>	0	82
1	0	<100 0010>	0	84
1	1	<100 0011>	0	86
0	0	<100 0000>	1	81
0	1	<100 0001>	1	83
1	0	<100 0010>	1	85
1	1	<100 0011>	1	87

ISD5100 Series I²C Operation Definitions

There are many control functions used to operate the ISD5100-Series. Among them are:

6.3.1.1. Read Status Command:

The Read Status command is a read request from the Host processor to the ISD5100 Series without delivering a Command Byte. The Host supplies all the clocks (SCL). In each case, the entity sending the data drives the data line (SDA). The Read Status Command is executed by the following I²C sequence.

1. Host executes I²C START
2. Send Slave Address with R/W bit = “1” (Read) 81h
3. Slave (ISD5100-Series) responds back to Host an Acknowledge (ACK) followed by 8-bit Status word
4. Host sends an Acknowledge (ACK) to Slave
5. Wait for SCL to go HIGH
6. Slave responds with Upper Address byte of internal address register
7. Host sends an ACK to Slave
8. Wait for SCL to go HIGH
9. Slave responds with Lower Address byte of internal address register (A[4:0] will always return set to 0.)
10. Host sends a NO ACK to Slave, then executes I²C STOP

Note that the processor could have sent an I²C STOP after the Status Word data transfer and aborted the transfer of the Address bytes.

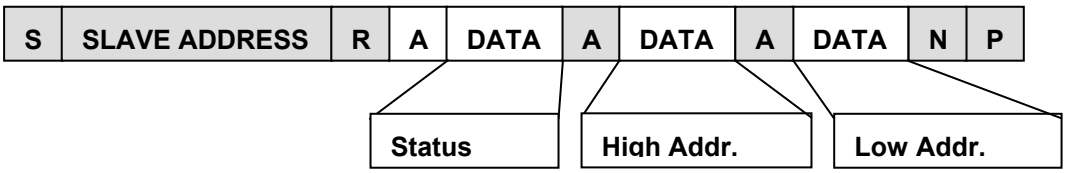
A graphical representation of this operation is found below. See the caption box above for more explanation.

Conventions used in I²C Data Transfer Diagrams

- **S** = START Condition
- **P** = STOP Condition
- **DATA** = 8-bit data transfer
- **R** = "1" in the R/W bit
- **W** = "0" in the R/W bit
- **A** = ACK (Acknowledge)
- **N** = No ACK
- **SLAVE ADDRESS** = 7-bit Slave Address

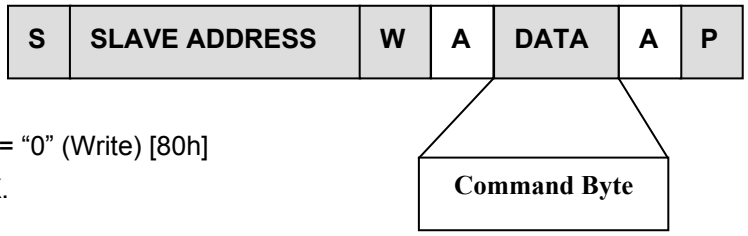
The Box color indicates the direction of data flow

- = Host to Slave (Gray)
- = Slave to Host (White)



6.3.1.2. Load Command Byte Register (Single Byte Load):

A single byte may be written to the Command Byte Register in order to power up the device, start or stop Analog Record (if no address information is needed), or do a Message Cueing function. The Command Byte Register is loaded as follows:

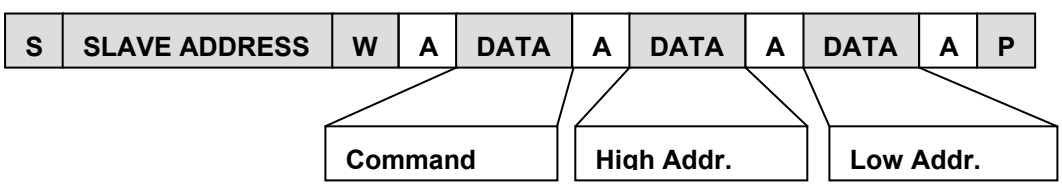


1. Host executes I²C START
2. Send Slave Address with R/W bit = "0" (Write) [80h]
3. Slave responds back with an ACK.
4. Wait for SCL to go HIGH
5. Host sends a command byte to Slave
6. Slave responds with an ACK
7. Wait for SCL to go HIGH
8. Host executes I²C STOP

6.3.1.3. Load Command Byte Register (Address Load)

For the normal addressed mode the Registers are loaded as follows:

1. Host executes I²C START
2. Send Slave Address with R/W bit = "0" (Write)
3. Slave responds back with an ACK.
4. Wait for SCL to go HIGH
5. Host sends a byte to Slave - (Command Byte)
6. Slave responds with an ACK
7. Wait for SCL to go HIGH
8. Host sends a byte to Slave - (High Address Byte)
9. Slave responds with an ACK
10. Wait for SCL to go HIGH
11. Host sends a byte to Slave - (Low Address Byte)
12. Slave responds with an ACK
13. Wait for SCL to go HIGH
14. Host executes I²C STOP



6.3.2 I²C Control Registers

The ISD5100 Series are controlled by loading commands to, or, reading from, the internal command, configuration and address registers. The Command byte sent is used to start and stop recording, write or read digital data and perform other functions necessary for the operation of the device.

Command Byte

Control of the ISD5100 Series are implemented through an 8-bit command byte, sent after the 7-bit device address and the 1-bit Read/Write selection bit. The 8 bits are:

- Global power up bit
- DAB bit: determines whether device is performing an analog or digital function
- 3 function bits: these determine which function the device is to perform in conjunction with the DAB bit.
- 3 register address bits: these determine if and when data is to be loaded to a register

Power Up Bit

C7	C6	C5	C4	C3	C2	C1	C0
PU	DAB	FN2	FN1	FN0	RG2	RG1	RG0
	Function Bits				Register Bits		

Function Bits

The command byte function bits are detailed in the table to the right. C6, the DAB bit, determines whether the device is performing an analog or digital function. The other bits are decoded to produce the individual commands. Not all decode combinations are currently used, and are reserved for future use. Out of 16 possible codes, the ISD5100 Series uses 7 for normal operation. The other 9 are undefined

Function Bits				Function
C6	C5	C4	C3	
DAB	FN2	FN1	FN0	
0	0	0	0	STOP (or do nothing)
0	1	0	1	Analog Play
0	0	1	0	Analog Record
0	1	1	1	Analog MC
1	1	0	0	Digital Read
1	0	0	1	Digital Write
1	0	1	0	Erase (row)

Register Bits

The register load may be used to modify a command sequence (such as load an address) or used with the null command sequence to load a configuration or test register. Not all registers are accessible to the user. [RG2 is always 0 as the four additional combinations are undefined.]

RG2	RG1	RG0	Function
C2	C1	C0	
0	0	0	No action
0	0	1	Reserved
0	1	0	Load CFG0
0	1	1	Load CFG1

6.3.3 Opcode Summary

OpCode Command Description

The following commands are used to access the chip through the I^2C interface.

- Play: analog play command
- Record: analog record command
- Message Cue: analog message cue command
- Read: digital read command
- Write: digital write command
- Erase: digital page and block erase command
- Power up: global power up/down bit. (C7)
- Load CFG0: load configuration register 0
- Load CFG1: load configuration register 1
- Read STATUS: Read the interrupt status and address register, including a hardwired device ID

OPCODE COMMAND BYTE TABLE

		Pwr	Function Bits				Register Bits		
OPCODE	**HEX**	**PU**	**DAB**	**FN2**	**FN1**	**FN0**	**RG2**	**RG1**	**RG0**
COMMAND BIT NUMBER	**CMD**	**C7**	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**
POWER UP	80	1	0	0	0	0	0	0	0
POWER DOWN	00	0	0	0	0	0	0	0	0
STOP (DO NOTHING) STAY ON	80	1	0	0	0	0	0	0	0
STOP (DO NOTHING) STAY OFF	00	0	0	0	0	0	0	0	0
LOAD CFG0	82	1	0	0	0	0	0	1	0
LOAD CFG1	83	1	0	0	0	0	0	1	1
RECORD ANALOG	90	1	0	0	1	0	0	0	0
RECORD ANALOG @ ADDR	91	1	0	0	1	0	0	0	1
PLAY ANALOG	A8	1	0	1	0	1	0	0	0
PLAY ANALOG @ ADDR	A9	1	0	1	0	1	0	0	1
MSG CUE ANALOG	B8	1	0	1	1	1	0	0	0
MSG CUE ANALOG @ ADDR	B9	1	0	1	1	1	0	0	1
ENTER DIGITAL MODE	C0	1	1	0	0	0	0	0	0
EXIT DIGITAL MODE	40	0	1	0	0	0	0	0	0
DIGITAL ERASE PAGE	D0	1	1	0	1	0	0	0	0
DIGITAL ERASE PAGE @ ADDR	D1	1	1	0	1	0	0	0	1
DIGITAL WRITE	C8	1	1	0	0	1	0	0	0
DIGITAL WRITE @ ADDR	C9	1	1	0	0	1	0	0	1
DIGITAL READ	E0	1	1	1	0	0	0	0	0
DIGITAL READ @ ADDR	E1	1	1	1	0	0	0	0	1
READ STATUS[1]	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

1. See section 7.2 on page 12 for details.

6.3.4 Data Bytes

In the I^2C write mode, the device can accept data sent after the command byte. If a register load option is selected, the next two bytes are loaded into the selected register. The format of the data is MSB first, the I^2C standard. Thus to load DATA<15:0> into the device, DATA<15:8> is sent first, the byte is acknowledged, and DATA<7:0> is sent next. The address register consists of two bytes. The format of the address is as follows:

ADDRESS<15:0> = PAGE_ADDRESS<10:0>, BLOCK_ADDRESS<4:0>

Note: if an analog function is selected, the block address bits must be set to 00000. Digital Read and Write are block addressable.

When the device is polled with the Read Status command, it will return three bytes of data. The first byte is the status byte, the next the upper address byte and the last the lower address byte. The status register is one byte long and its bit function is:

STATUS<7:0> = EOM, OVF, READY, PD, PRB, DEVICE_ID<2:0>

Lower address byte will always return the block address bits as zero, either in digital or analog mode.

The functions of the bits are:

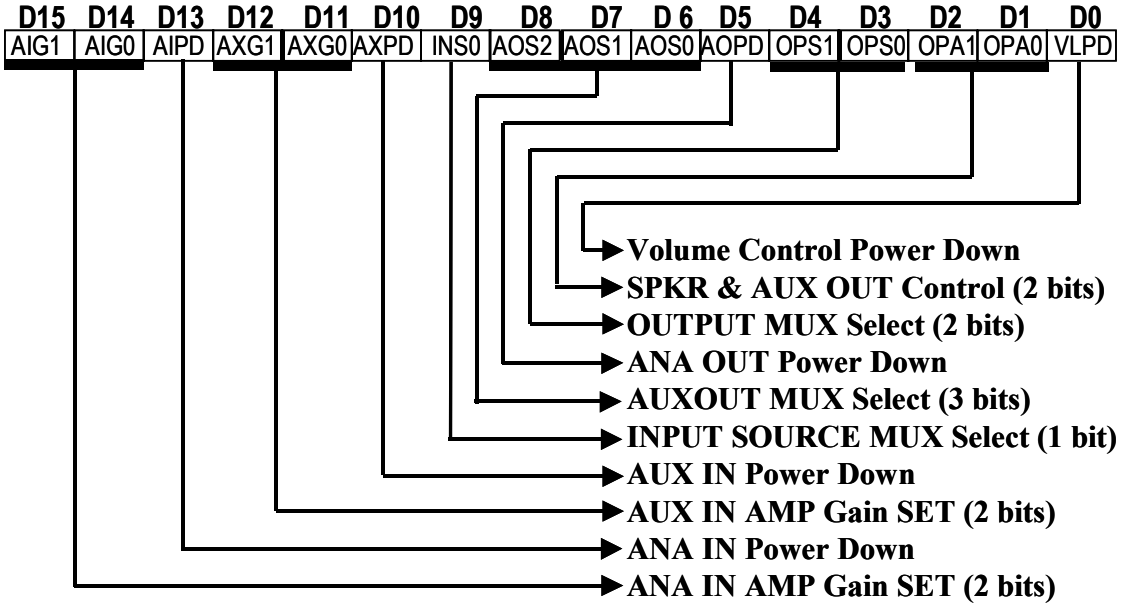
EOM	BIT 7	Indicates whether an EOM interrupt has occurred.
OVF	BIT 6	Indicates whether an overflow interrupt has occurred.
READY	BIT 5	Indicates the internal status of the device – if READY is LOW no new commands should be sent to device, i.e. Not Ready.
PD	BIT 4	Device is powered down if PD is HIGH.
PRB	BIT 3	Play/Record mode indicator. HIGH=Play/LOW=Record.
DEVICE_ID	BIT 0, 1, 2	An internal device ID. ISD5116 = 001; ISD5108 = 010; ISD5104 = 100 and ISD5102 = 101.

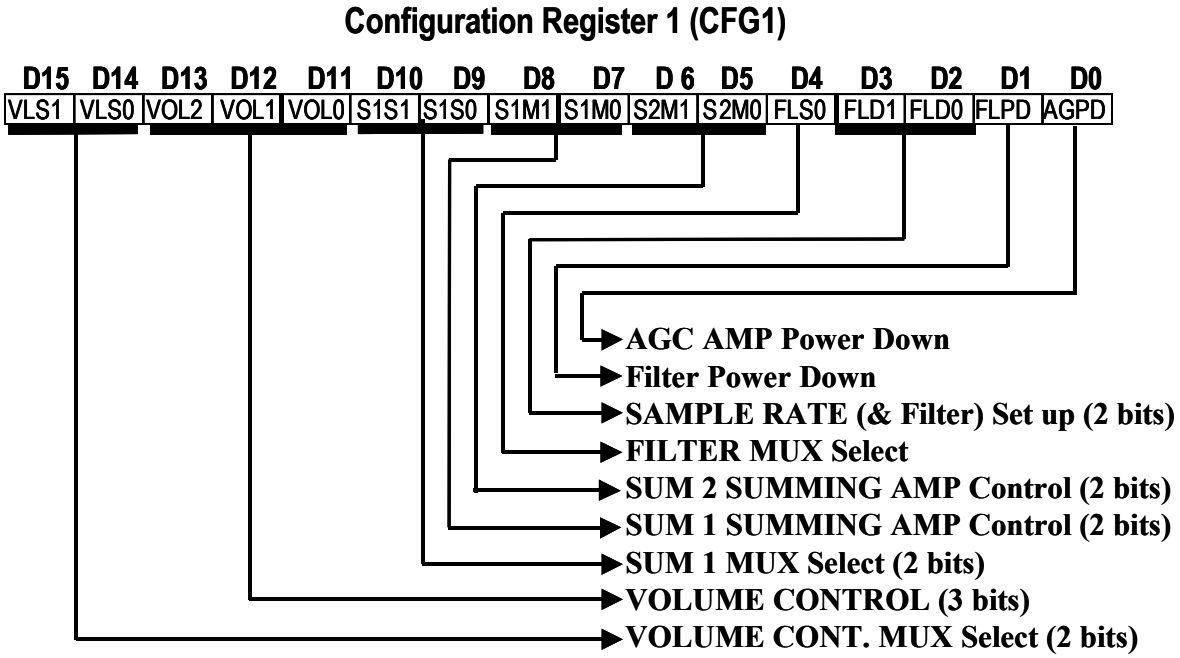
It is recommended that you read the status register after a Write or Record operation to ensure that the device is ready to accept new commands. Depending upon the design and the number of pins available on the controller, the polling overhead can be reduced. If $\overline{INT}$ and $\overline{RAC}$ are tied to the microcontroller, it does not have to poll as frequently to determine the status of the ISD5100-SERIES.

6.3.5 Configuration Register Bytes

The configuration register bytes are defined, in detail, in the drawings of section 7.4 on page 29. The drawings display how each bit enables or disables a function of the audio paths in the ISD5100-Series. The tables below give a general illustration of the bits. There are two configuration registers, CFG0 and CFG1, so there are four 8-bit bytes to be loaded during the set-up of the device.

Configuration Register 0 (CFG0)





6.3.6 Power-up Sequence

This sequence prepares the ISD5100 Series for an operation to follow, waiting the Tpud time before sending the next command sequence.

1. Send I^2C POWER UP
2. Send one byte 10000000 {Slave Address, R/W = 0} 80h
3. Slave ACK
4. Wait for SCL High
5. Send one byte 10000000 {Command Byte = Power Up} 80h
6. Slave ACK
7. Wait for SCL High
8. Send I^2C STOP

Playback Mode

The command sequence for an analog Playback operation can be handled several ways. The most straightforward approach would be to incorporate a single four byte exchange, which consists of the Slave Address (80h), the Command Byte (A9h) for Play Analog @ Address, and the two address bytes.

Record Mode

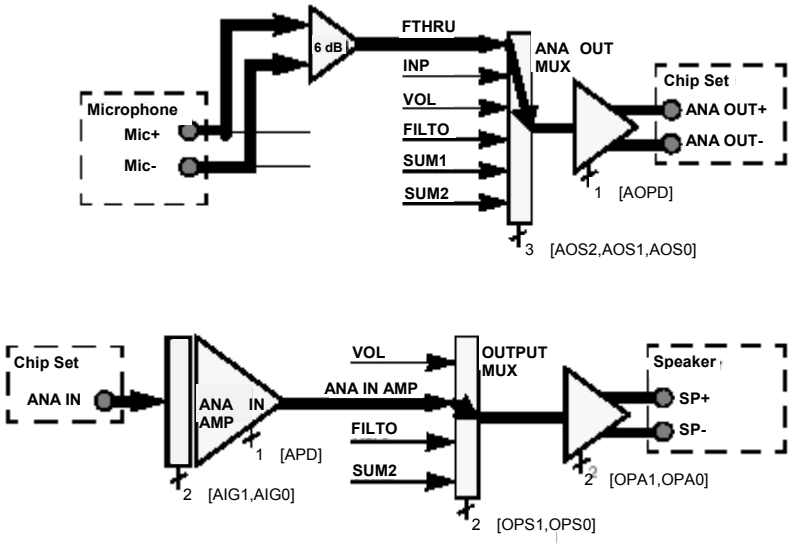
The command sequence for an Analog Record would be a four byte sequence consisting of the Slave Address (80h), the Command Byte (91h) for Record Analog @ Address, and the two address bytes. See "Load Command Byte Register (Address Load)" in section 7.3.2 on page 17.

6.3.7 Feed Through Mode

The previous examples were dependent upon the device already being powered up and the various paths being set through the device for the desired operation. To set up the device for the various paths requires loading the two 16-bit Configuration Registers with the correct data. For example, in the Feed Through Mode the device only needs to be powered up and a few paths selected.

This mode enables the ISD5100 Series to connect to a cellular or cordless base band phone chip set without affecting the audio source or destination. There are two paths involved, the transmit path and the receive path. The transmit path connects the Nuvoton chip's microphone source through to the microphone input on the base band chip set. The receive path connects the base band chip set's speaker output through to the speaker driver on the Nuvoton chip. This allows the Nuvoton chip to substitute for those functions and incidentally gain access to the audio to and from the base band chip set.

To set up the environment described above, a series of commands need to be sent to the ISD5100-Series. First, the chip needs to be powered up as described in this section. Then the Configuration Registers must be filled with the specific data to connect the paths desired. In the case of the Feed Through Mode, most of the chip can remain powered down. The following figure illustrates the affected paths.



The figure above shows the part of the ISD5100 Series block diagram that is used in Feed Through Mode. The rest of the chip will be powered down to conserve power. The bold lines highlight the audio paths. Note that the Microphone to ANA OUT +/– path is differential.

To select this mode, the following control bits must be configured in the ISD5100 Series configuration registers. To set up the transmit path:

1. Select the FTHRU path through the ANA OUT MUX—Bits AOS0, AOS1 and AOS2 control the state of the ANA OUT MUX. These are the D6, D7 and D8 bits respectively of Configuration Register 0 (CFG0) and they should all be ZERO to select the FTHRU path.

2. Power up the ANA OUT amplifier—Bit AOPD controls the power up state of ANA OUT. This is bit D5 of CFG0 and it should be a ZERO to power up the amplifier.

To set up the receive path:

1. Set up the ANA IN amplifier for the correct gain—Bits AIG0 and AIG1 control the gain settings of this amplifier. These are bits D14 and D15 respectively of CFG0. The input level at this pin determines the setting of this gain stage. The **ANA IN Amplifier Gain Settings table** on page 36 will help determine this setting. In this example, we will assume that the peak signal never goes above 1 volt p-p single ended. That would enable us to use the 9 dB attenuation setting, or where D14 is ONE and D15 is ZERO.

2. Power up the ANA IN amplifier—Bit AIPD controls the power up state of ANA IN. This is bit D13 of CFG0 and should be a ZERO to power up the amplifier.

3. Select the ANA IN path through the OUTPUT MUX—Bits OPS0 and OPS1 control the state of the OUTPUT MUX. These are bits D3 and D4 respectively of CFG0 and they should be set to the state where D3 is ONE and D4 is ZERO to select the ANA IN path.

4. Power up the Speaker Amplifier—Bits OPA0 and OPA1 control the state of the Speaker and AUX amplifiers. These are bits D1 and D2 respectively of CFG0. They should be set to the state where D1 is ONE and D2 is ZERO. This powers up the Speaker Amplifier and configures it for its higher gain setting for use with a piezo speaker element and also powers down the AUX output stage.

The status of the rest of the functions in the ISD5100 Series chip must be defined before the configuration registers settings are updated:

1. Power down the Volume Control Element—Bit VLPD controls the power up state of the Volume Control. This is bit D0 of CFG0 and it should be set to a ONE to power down this stage.

2. Power down the AUX IN amplifier—Bit AXPD controls the power up state of the AUX IN input amplifier. This is bit D10 of CFG0 and it should be set to a ONE to power down this stage.

3. Power down the SUM1 and SUM2 Mixer amplifiers—Bits S1M0 and S1M1 control the SUM1 mixer and bits S2M0 and S2M1 control the SUM2 mixer. These are bits D7 and D8 in CFG1 and bits D5 and D6 in CFG1 respectively. All 4 bits should be set to a ONE to power down these two amplifiers.

4. Power down the FILTER stage—Bit FLPD controls the power up state of the FILTER stage in the device. This is bit D1 in CFG1 and should be set to a ONE to power down the stage.

5. Power down the AGC amplifier—Bit AGPD controls the power up state of the AGC amplifier. This is bit D0 in CFG1 and should be set to a ONE to power down this stage.

6. Don't Care bits—The following stages are not used in Feed Through Mode. Their bits may be set to either level. In this example, we will set all the following bits to a ZERO. (a). Bit INS0, bit D9 of CFG0 controls the Input Source Mux. (b). Bits AXG0 and AXG1 are bits D11 and D12 respectively in CFG0. They control the AUX IN amplifier gain setting. (c). Bits FLD0 and FLD1 are bits D2 and D3 respectively in CFG1. They control the sample rate and filter band pass setting. (d). Bit FLS0 is bit D4 in CFG1. It controls the FILTER MUX. (e). Bits S1S0 and S1S1 are bits D9 and D10 of CFG1. They control the SUM1 MUX. (f). Bits VOL0, VOL1 and VOL2 are bits D11, D12 and D13 of CFG1. They control the setting of the Volume Control. (g). Bits VLS0 and VLS1 are bits D14 and D15 of CFG1. They control the Volume Control MUX.

The end result of the above set up is

CFG0=0100 0100 0000 1011 (hex 440B)

and

CFG1=0000 0001 1110 0011 (hex 01E3).

Since both registers are being loaded, CFG0 is loaded, followed by the loading of CFG1. These two registers must be loaded in this order. The internal set up for both registers will take effect synchronously with the rising edge of SCL.

6.3.8 Call Record

The call record mode adds the ability to record an incoming phone call. In most applications, the ISD5100 Series would first be set up for Feed Through Mode as described above. When the user wishes to record the incoming call, the setup of the chip is modified to add that ability. For the purpose of this explanation, we will use the 6.4 kHz sample rate during recording.

The block diagram of the ISD5100 Series shows that the Multilevel Storage array is always driven from the SUM2 SUMMING amplifier. The path traces back from there through the LOW PASS Filter, THE FILTER MUX, THE SUM1 SUMMING amplifier, the SUM1 MUX, then from the ANA in amplifier. Feed Through Mode has already powered up the ANA IN amp so we only need to power up and enable the path to the Multilevel Storage array from that point:

1. Select the ANA IN path through the SUM1 MUX—Bits S1S0 and S1S1 control the state of the SUM1 MUX. These are bits D9 and D10 respectively of CFG1 and they should be set to the state where both D9 and D10 are ZERO to select the ANA IN path.
2. Select the SUM1 MUX input (only) to the S1 SUMMING amplifier—Bits S1M0 and S1M1 control the state of the SUM1 SUMMING amplifier. These are bits D7 and D8 respectively of CFG1 and they should be set to the state where D7 is ONE and D8 is ZERO to select the SUM1 MUX (only) path.

3. Select the SUM1 SUMMING amplifier path through the FILTER MUX—Bit FLS0 controls the state of the FILTER MUX. This is bit D4 of CFG1 and it must be set to ZERO to select the SUM1 SUMMING amplifier path.

4. Power up the LOW PASS FILTER—Bit FLPD controls the power up state of the LOW PASS FILTER stage. This is bit D1 of CFG1 and it must be set to ZERO to power up the LOW PASS FILTER STAGE.

5. Select the 6.4 kHz sample rate—Bits FLD0 and FLD1 select the Low Pass filter setting and sample rate to be used during record and playback. These are bits D2 and D3 of CFG1. To enable the 6.4 kHz sample rate, D2 must be set to ONE and D3 set to ZERO.

6. Select the LOW PASS FILTER input (only) to the S2 SUMMING amplifier—Bits S2M0 and S2M1 control the state of the SUM2 SUMMING amplifier. These are bits D5 and D6 respectively of CFG1 and they should be set to the state where D5 is ZERO and D6 is ONE to select the LOW PASS FILTER (only) path.

In this mode, the elements of the original PASS THROUGH mode do not change. The sections of the chip not required to add the record path remain powered down. In fact, CFG0 does not change and remains

CFG0=0100 0100 0000 1011 (hex 440B).

CFG1 changes to

CFG1=0000 0000 1100 0101 (hex 00C5).

Since CFG0 is not changed, it is only necessary to load CFG1. Note that if only CFG0 was changed, it would be necessary to load both registers.

6.3.9 Memo Record

The Memo Record mode sets the chip up to record from the local microphone into the chip's Multilevel Storage Array. A connected cellular telephone or cordless phone chip set may remain powered down and is not active in this mode. The path to be used is microphone input to AGC amplifier, then through the INPUT SOURCE MUX to the SUM1 SUMMING amplifier. From there the path goes through the FILTER MUX, the LOW PASS FILTER, the SUM2 SUMMING amplifier, then to the MULTILEVEL STORAGE ARRAY. In this instance, we will select the 5.3 kHz sample rate. The rest of the chip may be powered down.

1. Power up the AGC amplifier—Bit AGPD controls the power up state of the AGC amplifier. This is bit D0 of CFG1 and must be set to ZERO to power up this stage.

2. Select the AGC amplifier through the INPUT SOURCE MUX—Bit INS0 controls the state of the INPUT SOURCE MUX. This is bit D9 of CFG0 and must be set to a ZERO to select the AGC amplifier.

3. Select the INPUT SOURCE MUX (only) to the S1 SUMMING amplifier—Bits S1M0 and S1M1 control the state of the SUM1 SUMMING amplifier. These are bits D7 and D8 respectively of CFG1 and they should be set to the state where D7 is ZERO and D8 is ONE to select the INPUT SOURCE MUX (only) path.