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ISD4003 SERIES

SINGLE-CHIP, MULTIPLE-MESSAGES

VOICE RECORD/PLAYBACK DEVICES

4-, 5-, 6-, AND 8-MINUTE DURATION

1. GENERAL DESCRIPTION

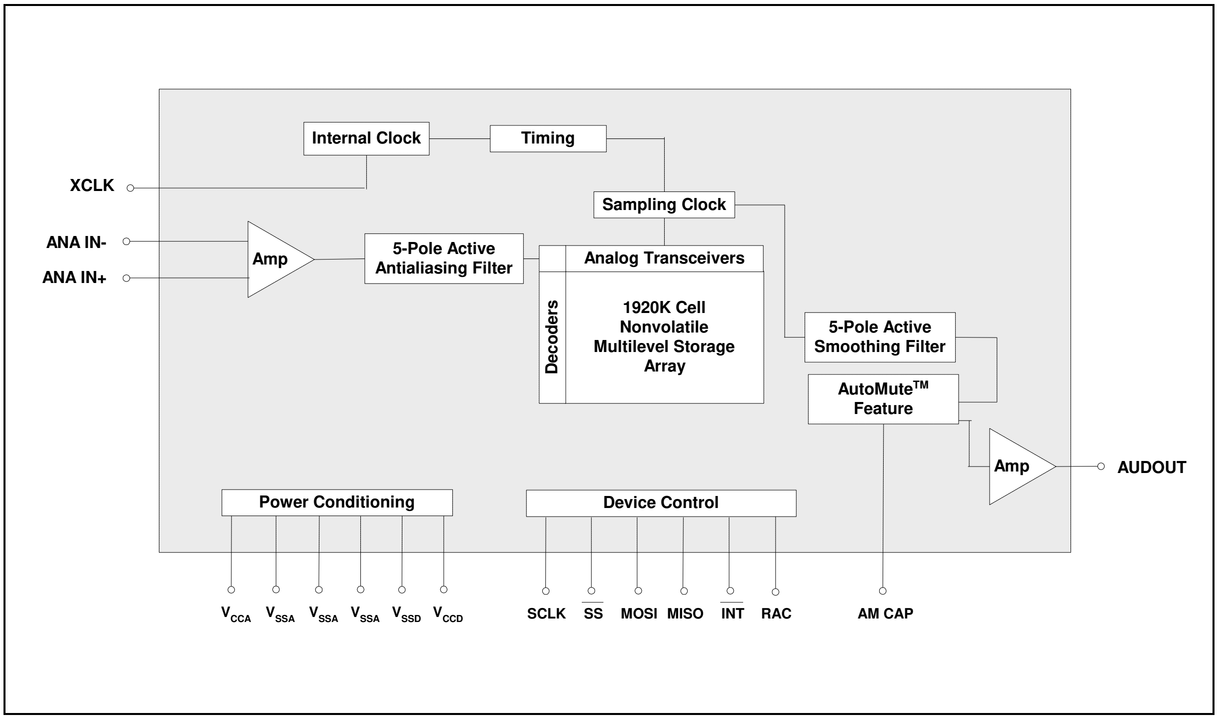
The ISD4003 ChipCorder® series provides high-quality, 3-volt, single-chip record/playback solutions for 4- to 8-minute messaging applications ideally for cellular phones and other portable products. The CMOS-based devices include an on-chip oscillator, anti-aliasing filter, smoothing filter, AutoMute® feature, audio amplifier, and high density multilevel Flash memory array. The ISD4003 series is designed to be used in a microprocessor- or microcontroller-based system. Address and control are accomplished through a Serial Peripheral Interface (SPI) or Microwire Serial Interface to minimize pin count.

Recordings are stored into the on-chip Flash memory cells, providing zero-power message storage. This unique single-chip solution utilizes Nuvoton's patented multilevel storage technology. Voice and audio signals are directly stored onto memory array in their natural form, providing high-quality voice reproduction.

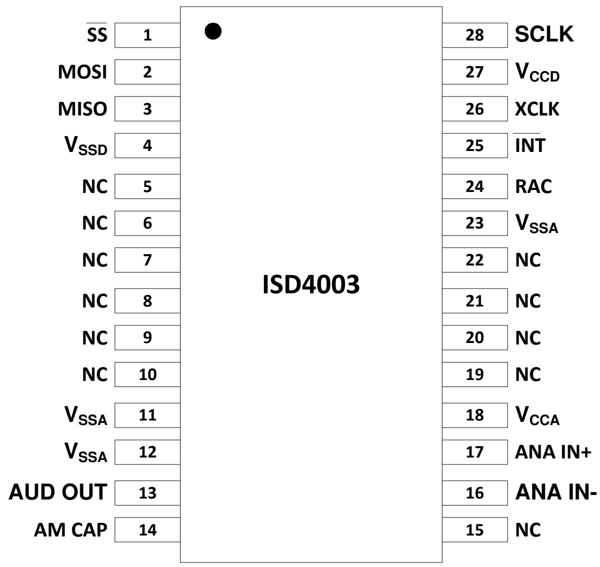
2. FEATURES

- Single-chip voice record/playback solution
- Single 3 volt supply
- Low-power consumption
  - Operating current:
    - I_{CC_Play} = 15 mA (typical)
    - I_{CC_Rec} = 25 mA (typical)
  - Standby current:
    - $I_{CC\_Standby}$ = 1 µA (typical)
- Duration: 4, 5, 6, and 8 minutes
- High-quality, natural voice/audio reproduction
- AutoMute feature provides background noise attenuation
- No algorithm development required
- Microcontroller SPI or Microwire™ Serial Interface
- Fully addressable to handle multiple messages
- Non-volatile message storage
- 100K record cycles (typical)
- 100-year message retention (typical)
- On-chip oscillator
- Power-down feature to reduce power consumption
- Available in die form, PDIP, and SOIC
- Packaged type: Lead-Free
- Temperature:
  - Commercial (die): 0°C to +50°C
  - Commercial (packaged units): 0°C to +70°C
  - Industrial (packaged units): -40°C to +85°C

3. BLOCK DIAGRAM



4. PIN CONFIGURATION



SOIC / PDIP

5. PIN DESCRIPTION

PIN NAME	SOIC / PDIP	FUNCTION
$\overline{SS}$	1	**Slave Select**: This input, when LOW, will select the ISD4003 device.
MOSI	2	**Master Out Slave IN**: This is the serial input to the ISD4003 device when it is configured as slave. The master microcontroller places data on the MOSI line one half-cycle before the rising edge of SCLK for clocking into the device.
MISO	3	**Master In Slave Out**: This is the serial output of the ISD4003 device. This output goes into a high-impedance state if the device is not selected.
V_{SSA} / V_{SSD}	11, 12, 23 / 4	**Ground**: The ISD4003 series utilizes separate analog and digital ground busses. The analog ground (V_{SSA}) pins should be tied together as close as possible and connected through a low-impedance path to power supply ground. The digital ground (V_{SSD}) pin should be connected through a separate low-impedance path to power supply ground. These ground paths should be large enough to ensure that the impedance between the V_{SSA} pins and the V_{SSD} pin is less than 3 Ω. The backside of the die is connected to V_{SS} through the substrate. For chip-on-board design, the die attach area must be connected to V_{SS} or left floating.
NC	5-10, 15, 19-22	Not connected
AUD OUT [1]	13	**Audio Output**: This pin provides an audio output of the stored data and is recommended be AC coupled. It is capable of driving a 5 KΩ impedance R_{EXT}.

[1] The AUD OUT pin is always at 1.2 volts when the device is powered up. When in playback, the output buffer connected to this pin can drive a load as small as 5 KΩ. When in record, a built-in resistor connects AUD OUT to the internal 1.2-volt analog ground supply. This resistor is approximately 850 KΩ, but will vary somewhat according to the sample rate of the device. This relatively high impedance allows this pin to be connected to an audio bus without loading it down.

PIN NAME	FUNCTION	
	SOIC / PDIP	
AM CAP	14	**AutoMute™ Feature**: The AutoMute feature only applies for playback operation and helps to minimize noise (with 6 dB of attenuation) when there is no signal (i.e. during periods of silence). A 1 µF capacitor to ground is recommended to connect to the AM CAP pin. This capacitor becomes a part of an internal peak detector which senses the signal amplitude. This peak level is compared to an internally set threshold to determine the AutoMute trip point. For large signals, the AutoMute attenuation is set to 0 dB automatically but 6 dB of attenuation occurs for silence. The 1 µF capacitor also affects the rate at which the AutoMute feature changes with the signal amplitude (or the attack time). The AutoMute feature can be disabled by connecting the AM CAP pin directly to V_{CCA}..
ANA IN-	16	**Inverting Analog Input**: This pin transfers the signal into the device during recording via differential-input mode. In this differential-input mode, a 16 mVp-p maximum input signal should be capacitively coupled to ANA IN- for optimal signal quality, as shown in Figure 1: ANA IN Modes. This capacitor value should be equal to that used on ANA IN+ pin. The input impedance at ANA IN- is normally 56 KΩ. In the single-ended mode, ANA IN- should be capacitively coupled to V_{SSA} through a capacitor equal to that used on the ANA IN+ pin.
ANA IN+	17	**Non-Inverting Analog Input**: This pin is the non-inverting analog input that transfers the signal to the device for recording. The analog input amplifier can be driven single ended or differentially. In the single-ended input mode, a 32 mVp-p (peak-to-peak) maximum signal should be capacitively connected to this pin for optimal signal quality. The external capacitor associated with ANA IN+ together with the 3 KΩ input impedance are selected to give cutoff at the low frequency end of the voice passband. In the differential-input mode, the maximum input signal at ANA IN+ should be 16 mVp-p capacitively coupled for optimal signal quality. The circuit connections for the two modes are shown in Figure 1.

PIN NAME	SOIC / PDIP	FUNCTION
V_{CCA} / V_{CCD}	18 / 27	**Supply Voltage**: To minimize noises, the analog and digital circuits in the ISD4003 devices use separate power busses. These +3V busses are brought out to separate pins and should be tied together as close to the supply as possible. In addition, these supplies should be decoupled as close to the package as possible.
RAC	24	**Row Address Clock**: This is an open drain output that provides the signal of a ROW with a 200 ms period for 8 KHz sampling frequency. (This represents a single row of memory.) This signal stays HIGH for 175 ms and stays LOW for 25 ms when it reaches the end of a row. The RAC pin stays HIGH for 109.37 µsec and stays LOW for 15.63 µsec in Message Cueing mode (see Message Cueing section for detailed description). Refer to the AC Parameters table for RAC timing information at other sample rates. When a record command is first initiated, the RAC pin remains HIGH for an extra T_{RACL} period. This is due to the need of loading the internal sample and hold circuits in the device. This pin can be used for message management techniques. A pull-up resistor is required to connect this pin to other device.
$\overline{INT}$	25	**Interrupt**: This is an open drain output pin. This pin goes LOW and stays LOW when an Overflow (OVF) or End of Message (EOM) marker is detected. Each operation that ends with an EOM or OVF will generate an interrupt. The interrupt will be cleared the next time an SPI cycle is initiated. The interrupt status can also be read by an R_{INT} instruction. A pull-up resistor is required to connect this pin to other device. *Overflow Flag (OVF)* – The Overflow flag indicates that the end of memory has been reached during a record or playback operation. *End of Message (EOM)* – The End of Message flag is set only during playback operation when an EOM is found. There are eight EOM flag position options per row.

<table>
<tr><th rowspan="2">PIN NAME</th><th colspan="2">FUNCTION</th></tr>
<tr><th>SOIC / PDIP</th><th></th></tr>
<tr><td>XCLK</td><td>26</td><td>External Clock Input: The ISD4003 series is configured at the factory with an internal sampling clock frequency centered to ±1 percent of specification. The frequency is then maintained to a variation of ±2.25 percent over the entire commercial temperature and operating voltage ranges. The internal clock has a –6/+4 percent tolerance over the industrial temperature and voltage ranges. A regulated power supply is recommended for industrial temperature range parts. If greater precision is required, the device can be clocked through the XCLK pin as follows:
<table>
<tr><th>Part Number</th><th>Sample Rate</th><th>Required Clock</th></tr>
<tr><td>ISD4003-04M</td><td>8.0 kHz</td><td>1024 kHz</td></tr>
<tr><td>ISD4003-05M</td><td>6.4 kHz</td><td>819.2 kHz</td></tr>
<tr><td>ISD4003-06M</td><td>5.3 kHz</td><td>682.7 kHz</td></tr>
<tr><td>ISD4003-08M</td><td>4.0 kHz</td><td>512 kHz</td></tr>
</table>
These recommended clock rates should not be varied because the anti-aliasing and smoothing filters are fixed. Otherwise, aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two. If the XCLK is not used, this input must be connected to ground.</td></tr>
<tr><td>SCLK</td><td>28</td><td>Serial Clock: This is the input clock to the ISD4003 device. It is generated by the master device (typically microcontoller) and is used to synchronize the data transfer in and out of the device through the MOSI and MISO lines, respectively. Data is latched into the ISD4003 on the rising edge of SCLK and shifted out of the device on the falling edge of SCLK.</td></tr>
</table>

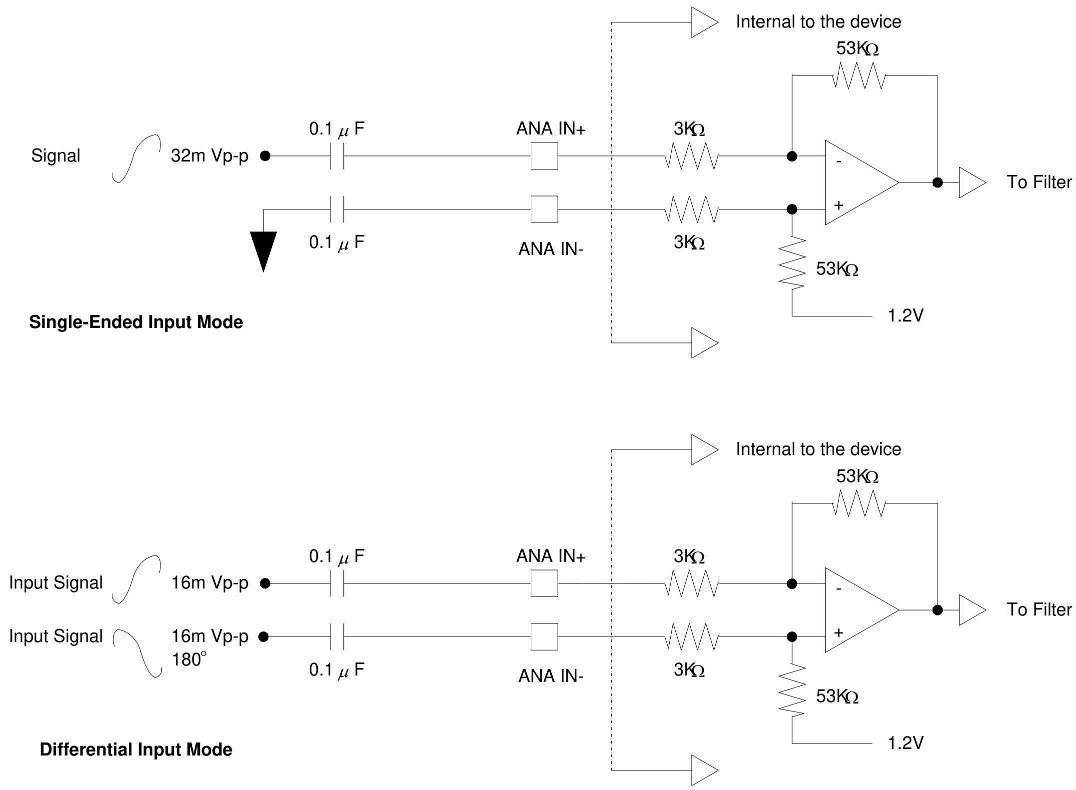


FIGURE 1: ISD4003 SERIES ANA IN MODES

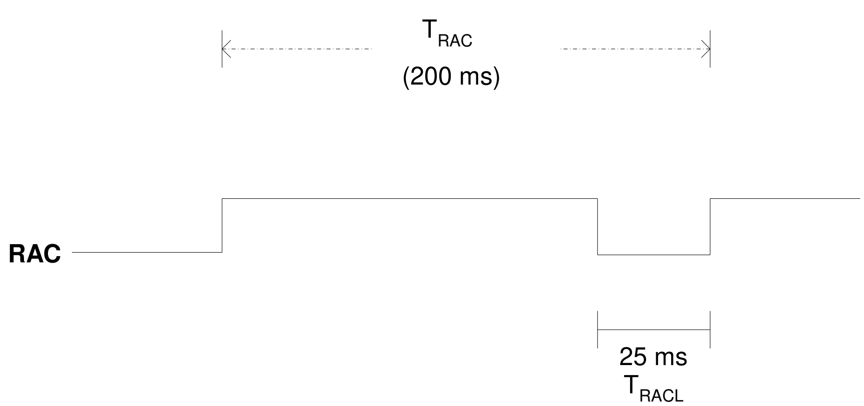


FIGURE 2: RAC TIMING WAVEFORM DURING NORMAL OPERATION

(example of 8KHz sampling rate)

6. FUNCTIONAL DESCRIPTION

6.1. DETAILED DESCRIPTION

Audio Quality

The Nuvoton's ISD4003 ChipCorder® series is offered at 8.0, 6.4, 5.3 and 4.0 kHz sampling frequencies, allowing the user a choice of speech quality options. Increasing the sampling frequency will produce better sound quality, but affects duration. Please refer to Table 1: Product Summary for details.

Analog speech samples are stored directly into on-chip non-volatile memory without the digitization and compression associated with other solutions. Direct analog storage provides higher quality reproduction of voice, music, tones, and sound effects than other solid-state solutions.

Duration

The ISD4003 Series is a single-chip solution with 4-, 5-, 6-, and 8-minute duration.

TABLE 1: PRODUCT SUMMARY OF ISD4003 SERIES

Part Number	Duration (Minutes)	Sample Rate (kHz)	Typical Filter Pass Band (kHz) *
ISD4003-04M	4	8.0	3.4
ISD4003-05M	5	6.4	2.7
ISD4003-06M	6	5.3	2.3
ISD4003-08M	8	4.0	1.7

* This is the –3dB point. This parameter is not checked during production testing and may vary due to process variations and other factors. Therefore, the customer should not rely upon this value for testing purposes.

Flash Storage

The ISD4003 series utilizes on-chip Flash memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

Memory Architecture

The ISD4003 series contains a total of 1,920K Flash memory cells, which is organized as 1,200 rows of 1,600 cells each.

Microcontroller Interface

A four-wire (SCLK, MOSI, MISO & $\overline{SS}$) SPI interface is provided for controlling and addressing functions. The ISD4003 is configured to operate as a peripheral slave device, with a microcontroller-based SPI bus interface. Read and write operations are controlled through this SPI interface. An interrupt signal ($\overline{INT}$) and internal read only Status Register are provided for handshake purposes.

Programming

The ISD4003 series is also ideal for playback-only applications, where single- or multiple-messages playback is controlled through the SPI port. Once the desired message configuration is created, duplicates can easily be generated via a programmer.

6.2. Serial Peripheral Interface (SPI) Description

The ISD4003 series operates via SPI serial interface with the following protocol.

First, the data transfer protocol assumes that the microcontroller's SPI shift registers are clocked on the falling edge of the SCLK. However, for the ISD4003, the protocols are as follows:

1. All serial data transfers begin with the falling edge of $\overline{SS}$ pin.
2. $\overline{SS}$ is held LOW during all serial communications and held HIGH between instructions.
3. Data is clocked in on the rising edge of the SCLK signal and clocked out on the falling edge of the SCLK signal, with LSB first.
4. Playback and record operations are initiated when the device is enabled by asserting the $\overline{SS}$ pin LOW, shifting in an opcode and an address data to the ISD4003 device (refer to the Opcode Summary in the following page).
5. The opcodes contain <11 address bits> and <5 control bits>.
6. Each operation that ends with an EOM or Overflow will generate an interrupt. The Interrupt will be cleared the next time a SPI cycle is initiated.
7. As Interrupt data is shifted out of the MISO pin, control and address data are simultaneously shifted into the MOSI pin. Care should be taken such that the data shifted in is compatible with current system operation. Because it is possible to read an interrupt data and start a new operation within the same SPI cycle.
8. An operation begins with the RUN bit set and ends with the RUN bit reset.
9. All operations begin after the rising edge of $\overline{SS}$.

6.2.1 OPCODES

The available Opcodes are summarized as follows:

TABLE 2: OPCODE SUMMARY

Instructions	OpCodes		Descriptions
	Address (11 bits) <A0 – A10>	Control bits (5 bits) C0 C1 C2 C3 C4	
POWERUP	<XXXXXXXXXXX>	0 0 1 0 0	Power-Up: Device will be ready for an operation after T_{PUD}.
SETPLAY	<A0 – A10>	0 0 1 1 1	Initiates playback from address <A0-A10>.
PLAY	<XXXXXXXXXXX>	0 1 1 1 1	Playback from the current address (until EOM or OVF).
SETREC	<A0 – A10>	0 0 1 0 1	Initiates a record operation from address <A0-A10>.
REC	<XXXXXXXXXXX>	0 1 1 0 1	Records from current address until OVF is reached or Stop command is sent.
SETMC	<A0 – A10>	1 0 1 1 1	Initiates Message Cueing (MC) from address <A0-A10>.
MC [1]	<XXXXXXXXXXX>	1 1 1 1 1	Performs a Message Cueing from current location. Proceeds to the end of message (EOM) or enters OVF condition if no more messages are present.
STOP	<XXXXXXXXXXX>	0 1 1 X 0	Stops the current operation.
STOPPWRDN	<XXXXXXXXXXX>	X 1 0 X 0	Stops the current operation and enters into standby (power-down) mode.
RINT [2]	<XXXXXXXXXXX>	0 1 1 X 0	Read Interrupt status bits: Overflow and EOM.

Notes:

C0 = Message cueing

C1 = Ignore address bit

C2 = Master power control

C3 = Record or playback operation

C4 = Enable or disable an operation

[1] Message Cueing can be selected only at the beginning of a playback operation.

[2] As the Interrupt data is shifted out of the ISD4003, control and address data are being shifted in. Care should be taken such that the data shifted in is compatible with current system operation. It is possible to read interrupt data and start a new operation at the same time. See Figures 5 - 8 for references.

6.2.2 SPI Diagrams

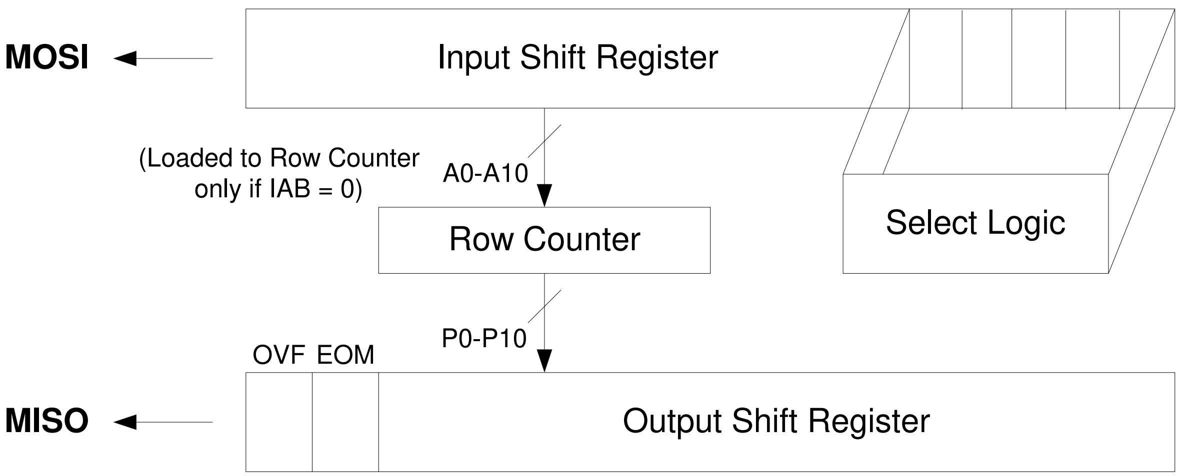


FIGURE 3: SPI INTERFACE SIMPLIFIED BLOCK DIAGRAM

The following diagram describes the SPI port and the control bits associated with it.

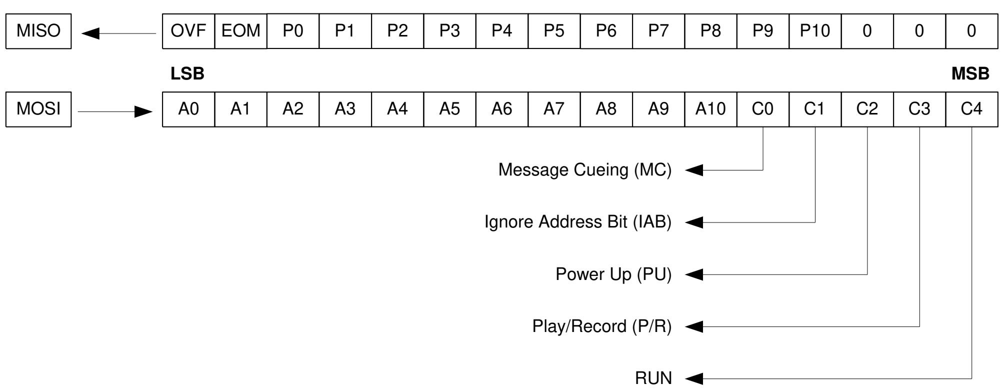


FIGURE 4: SPI PORT

6.2.3 SPI Control and Output Registers

The SPI control register provides control of individual function such as play, record, message cueing, power-up, power-down, start, stop and ignore address pointer operations.

TABLE 3: SPI CONTROL REGISTERS

Control Bit	Control Register	Bit	Device Function
C0	MC		Message Cueing function
	=	1	Enable Message Cueing
	=	0	Disable Message Cueing
C1	IAB [1]		Ignore Address bit
	=	1	Ignore input address register (A0-A10)
	=	0	Use the input address register (A0-A10)
C2	PU		Power Up
	=	1	Power-Up
	=	0	Power-Down
C3	$P/\overline{R}$		Playback or Record
	=	1	Play
	=	0	Record
C4	RUN		Enable or Disable an operation
	=	1	Start
	=	0	Stop
Address Bits	A0-A10		Input address register

TABLE 4: SPI OUTPUT REGISTERS

Output Bits	Description
OVF	Overflow
EOM	End-of-Message
P0-P10	Output of the row pointer register

[1] When IAB (Ignore Address Bit) is set to 0, a playback or record operation starts from address (A0-A10). For consecutive playback or record, IAB should be changed to a 1 before the end of that row (see RAC timing). Otherwise the ISD4003 will repeat the operation from the same row address. For memory management, the Row Address Clock (RAC) signal and IAB can be used to move around the memory segments.

Message Cueing

Message cueing (MC) allows the user to skip through messages, without knowing the actual physical location of the messages. It will stop when an EOM marker is reached. Then, the internal address counter will point to the next message. Also, it will enter into OVF condition when it reaches the end of memory. In this mode, the messages are skipped 1,600 times faster than the normal playback mode.

Power-Up Sequence

The ISD4003 will be ready for an operation after power-up command is sent and followed by the T_{PUD} timing (25 ms for 8 KHz sampling rate). Refer to the AC timing table for other T_{PUD} values with respect to different sampling rates.

The following sequences are recommended for optimized Record and Playback operations.

Record Mode

1. Send POWERUP command.
2. Wait T_{PUD} (power-up delay).
3. Send POWERUP command.
4. Wait 2 x T_{PUD} (power-up delay).
5. a). Send SETREC command with address xx, or

   b). Send REC command (recording from current location).
6. Send STOP command to stop recording.
7. Wait $T_{STOP/PAUSE.}$

For 3 & 4), please refer to Apps Brief 39A: recorded pop elimination in the ISD4000 series.

For 5.a), the device will start recording at address xx and will generate an interrupt when an overflow (end of memory array) is reached, if no STOP command is sent before that. Then, it will automatic stop recording operation.

Playback Mode

1. Send POWERUP command
2. Wait T_{PUD} (power-up delay)
3. a). Send SETPLAY command with address xx, or

   b). Send PLAY command (playback from current location).
4. a). Send STOP command to halt the playback operation, or

   b). Wait for playback operation to stop automatically, when an EOM or OVF is reached.
5. Wait $T_{STOP/PAUSE.}$

For 3.a), the device will start playback at address xx and it will generate an interrupt when an EOM or OVF is reached. It will then stop playback operation.

7. TIMING DIAGRAMS

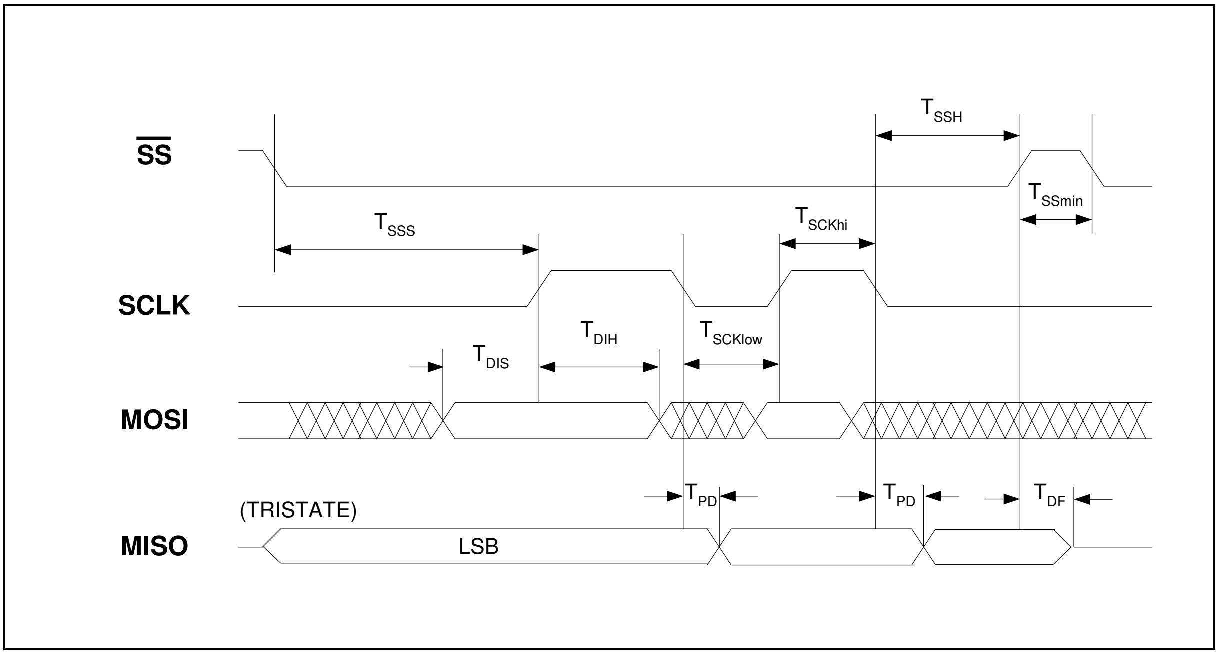


FIGURE 5: TIMING DIAGRAM

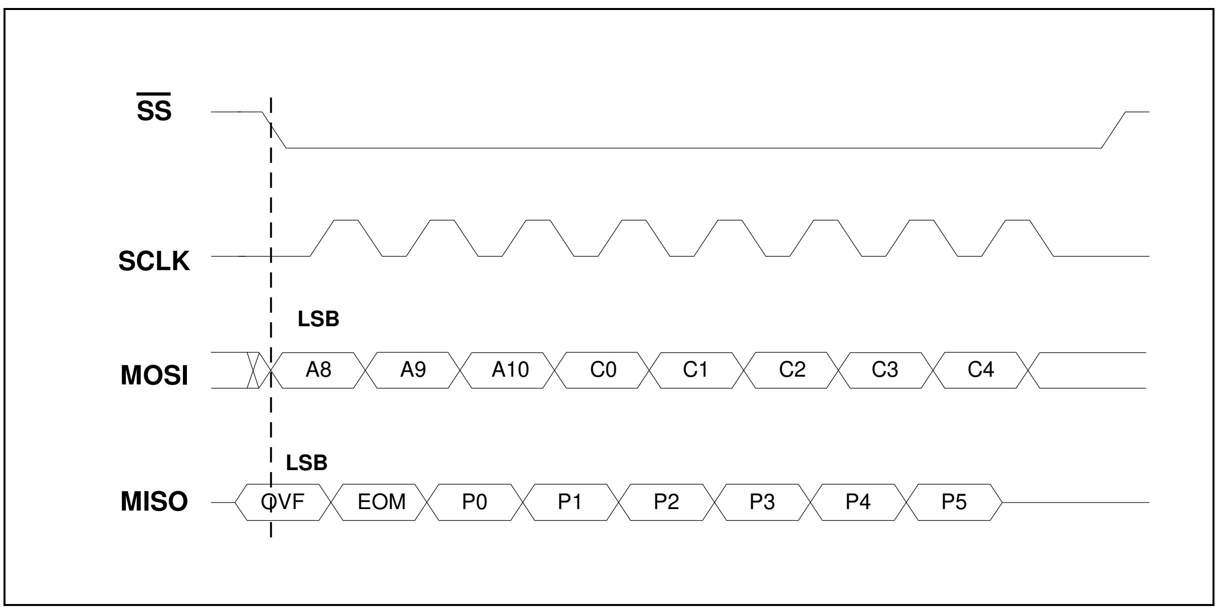


FIGURE 6: 8-BIT COMMAND FORMAT

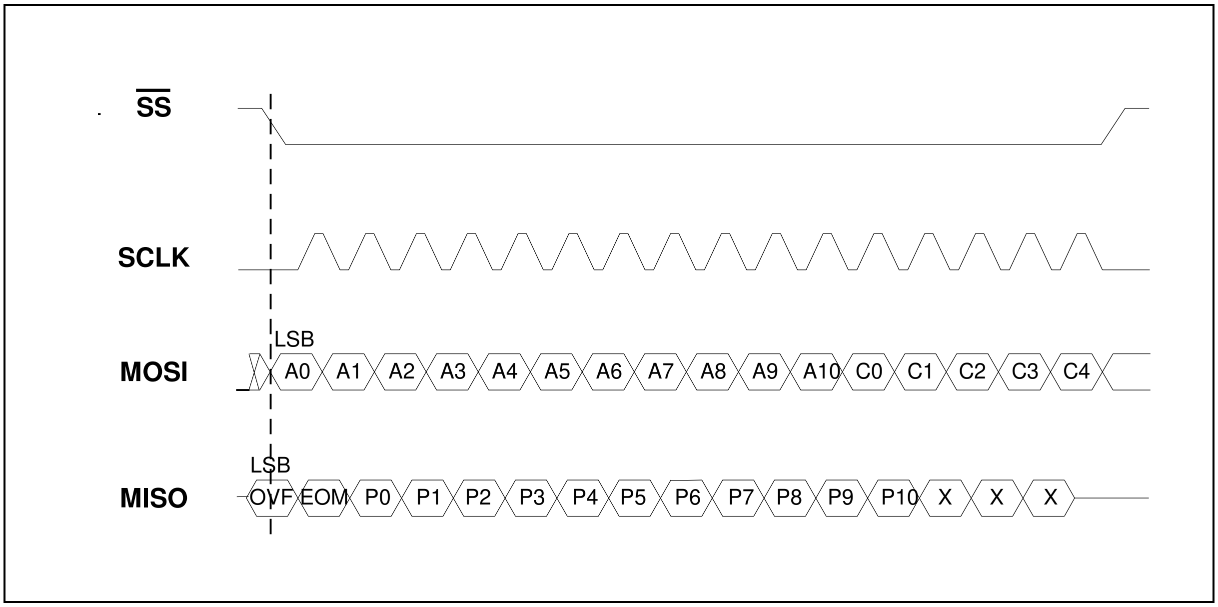


FIGURE 7: 16-BIT COMMAND FORMAT

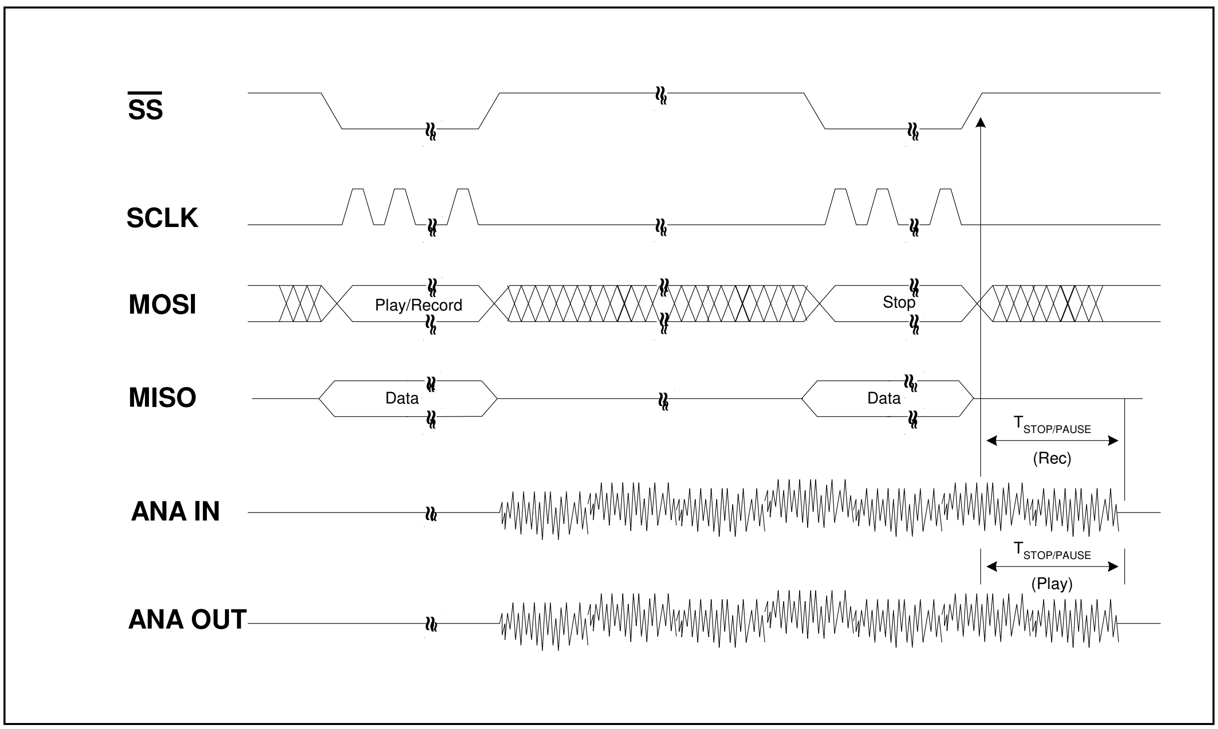


FIGURE 8: PLAYBACK/RECORD AND STOP CYCLE

8. ABSOLUTE MAXIMUM RATINGS

TABLE 5: ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS)

CONDITIONS	VALUES
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pin	(V_{SS} –0.3V) to (V_{CC} +0.3V)
Voltage applied to any pin (Input current limited to ±20mA)	(V_{SS} –1.0V) to (V_{CC} +1.0V)
Voltage applied to MOSI, SCLK, and $\overline{SS}$ pins (Input current limited to ±20mA)	(V_{SS} –1.0V) to 5.5V
Lead temperature (soldering – 10 seconds)	300°C
V_{CC} – V_{SS}	-0.3V to +7.0V

TABLE 6: ABSOLUTE MAXIMUM RATINGS (DIE)

CONDITIONS	VALUES
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pad	(V_{SS} –0.3V) to (V_{CC} +0.3V)
Voltage applied to any pad (Input current limited to ±20 mA)	(V_{SS} –1.0V) to (V_{CC} +1.0V)
Voltage applied to MOSI, SCLK, and $\overline{SS}$ pins (Input current limited to ±20mA)	(V_{SS} –1.0V) to 5.5V
V_{CC} – V_{SS}	-0.3V to +7.0V

Note: Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability and performance. Functional operation is not implied at these conditions.

8.1. Operating Conditions

TABLE 7: OPERATING CONDITIONS (PACKAGED PARTS)

CONDITIONS	VALUES
Commercial operating temperature range (Case temperature)	0°C to +70°C
Industrial operating temperature (Case temperature)	-40°C to +85°C
Supply voltage (V_{CC}) [1]	+2.7V to +3.3V
Ground voltage (V_{SS}) [2]	0V

TABLE 8: OPERATING CONDITIONS (DIE)

CONDITIONS	VALUES
Commercial operating temperature range	0°C to +50°C
Supply voltage (V_{CC}) [1]	+2.7V to +3.3V
Ground voltage (V_{SS}) [2]	0V

[1] $V_{CC} = V_{CCA} = V_{CCD}$

[2] $V_{SS} = V_{SSA} = V_{SSD}$

9. ELECTRICAL CHARACTERISTICS

9.1. PARAMETERS FOR PACKAGED PARTS

TABLE 9: DC PARAMETERS

PARAMETERS	SYMBOLS	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Input Low Voltage	V_{IL}			V_{CC} x 0.2	V	
Input High Voltage	V_{IH}	V_{CC} x 0.8			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 10 µA
RAC, $\overline{INT}$ Output Low Voltage	V_{OL1}			0.4	V	I_{OL} = 1 mA
Output High Voltage	V_{OH}	V_{CC} - 0.4			V	I_{OH} = -10 µA
V_{CC} Current (Operating) - Playback - Record	I_{CC}		 15 25	 30 40	 mA mA	 $R_{EXT} = \infty$ [3] $R_{EXT} = \infty$ [3]
V_{CC} Current (Standby)	I_{SB}		1	10	µA	[3] [4]
Input Leakage Current	I_{IL}			±1	µA	
MISO Tristate Current	I_{HZ}		1	10	µA	
Output Load Impedance	R_{EXT}	5			KΩ	
ANA IN+ Input Resistance	$R_{ANA\ IN+}$	2.2	3.0	3.8	KΩ	
ANA IN- Input Resistance	$R_{ANA\ IN-}$	40	56	71	KΩ	
ANA IN+ or ANA IN- to AUD OUT Gain	A_{ARP}		23		dB	32 mVpp 1 KHz sinewave input [5]

Notes:

[1] Typical values @ T_A = 25°C and V_{CC} = 3.0V.

[2] All Min/Max limits are guaranteed by Nuvoton via electronical testing or characterization. Not all specifications are 100 percent tested.

[3] V_{CCA} and V_{CCD} connected together.

[4] $\overline{SS}$ = V_{CCA} = V_{CCD}, XCLK = MOSI = V_{SSA} = V_{SSA} and all other pins floating.

[5] Measured with AutoMute feature disabled.

TABLE 10: AC PARAMETERS (Packaged Parts)

CHARACTERISTIC	SYMBOLS	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Sampling Frequency	F_S					
ISD4003-04M			8.0		KHz	[5]
ISD4003-05M			6.4		KHz	[5]
ISD4003-06M			5.3		KHz	[5]
ISD4003-08M			4.0		KHz	[5]
Filter Pass Band	F_{CF}					
ISD4003-04M			3.4		KHz	3 dB Roll-Off Point[3][7]
ISD4003-05M			2.7		KHz	3 dB Roll-Off Point[3][7]
ISD4003-06M			2.3		KHz	3 dB Roll-Off Point[3][7]
ISD4003-08M			1.7		KHz	3 dB Roll-Off Point[3][7]
Record Duration	T_{REC}					
ISD4003-04M			4		min	[6]
ISD4003-05M			5		min	[6]
ISD4003-06M			6		min	[6]
ISD4003-08M			8		min	[6]
Playback Duration	T_{PLAY}					
ISD4003-04M			4		min	[6]
ISD4003-05M			5		min	[6]
ISD4003-06M			6		min	[6]
ISD4003-08M			8		min	[6]
Power-Up Delay	T_{PUD}					
ISD4003-04M			25		msec	
ISD4003-05M			31.25		msec	
ISD4003-06M			37.5		msec	
ISD4003-08M			50		msec	
Stop or Pause in Record or Play	T_{STOP} or T_{PAUSE}					
ISD4003-04M			50		msec	
ISD4003-05M			62.5		msec	
ISD4003-06M			75		msec	
ISD4003-08M			100		msec	
RAC Clock Period	T_{RAC}					
ISD4003-04M			200		msec	[10]
ISD4003-05M			250		msec	[10]
ISD4003-06M			300		msec	[10]
ISD4003-08M			400		msec	[10]
RAC Clock Low Time	T_{RACL}					
ISD4003-04M			25		msec	
ISD4003-05M			31.25		msec	
ISD4003-06M			37.5		msec	
ISD4003-08M			50		msec	
RAC Clock Period in Message Cueing Mode	T_{RACM}					
ISD4003-04M			125		µsec	
ISD4003-05M			156.3		µsec	
ISD4003-06M			187.5		µsec	
ISD4003-08M			250		µsec	
RAC Clock Low Time in Message Cueing Mode	T_{RACML}					
ISD4003-04M			15.63		µsec	
ISD4003-05M			19.53		µsec	
ISD4003-06M			23.44		µsec	
ISD4003-08M			31.25		µsec	
Total Harmonic Distortion	THD		1	2	%	32 mVpp 1 KHz sinewave input [11]
ANA IN Input Voltage	V_{IN}			32	mV	Peak-to-Peak [4] [8] [9]

Notes:

[1] Typical values @ T_A = 25°C, V_{CC} = 3.0V and timing measurement at 50%.

[2] All Min/Max limits are guaranteed by Nuvoton via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions)

[4] Single-ended input mode. In the differential input mode, V_{IN} maximum for ANA IN+ and ANA IN- is 16 mVp-p.

[5] Sampling Frequency can vary as much as ±2.25 percent over the commercial temperature and voltage ranges, and –6/+4 percent over the industrial temperature and voltage ranges. For greater stability, an external clock can be utilized (see Pin Descriptions)

[6] Playback and Record Duration can vary as much as ±2.25 percent over the commercial temperature and voltage ranges, and –6/+4 percent over the industrial temperature and voltage ranges. For greater stability, an external clock can be utilized (see Pin Descriptions)

[7] Filter specification applies to the antialiasing filter and the smoothing filter. Therefore, from input to output, expect a 6 dB drop by nature of passing through both filters.

[8] The typical output voltage will be approximately 450 mVp-p with V_{IN} at 32 mVp-p.

[9] For optimal signal quality, this maximum limit is recommended.

[10] When a record command is sent, $T_{RAC} = T_{RAC} + T_{RACL}$ on the first row address.

[11] Measured with AutoMute feature disabled.

9.2. PARAMETERS FOR DIE

TABLE 11: DC PARAMETERS

PARAMETERS [6]	SYMBOLS	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Input Low Voltage	V_{IL}			V_{CC} x 0.2	V	
Input High Voltage	V_{IH}	V_{CC} x 0.8			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 10 µA
RAC, $\overline{\text{INT}}$ Output Low Voltage	V_{OL1}			0.4	V	I_{OL} = 1 mA
Output High Voltage	V_{OH}	V_{CC} - 0.4			V	I_{OH} = -10 µA
Operating Current -Playback -Record	I_{CC}		 15 25	 30 40	 mA mA	 $R_{EXT} = \infty$ [3] $R_{EXT} = \infty$ [3]
Standby Current	I_{SB}		1	10	µA	[3] [4]
Total Harmonic Distortion	THD		1	2	%	32 mVpp 1 KHz sinewave input [5]
ANA IN+ or ANA IN- to AUD OUT Gain	A_{ARP}		23		dB	32 mVpp 1 KHz sinewave input [5]

Notes:

[1] Typical values @ T_A = 25°C and V_{CC} = 3.0V. Sampling Frequency can vary as much as ±2.25 percent over the commercial temperature and voltage ranges

[2] All Min/Max limits are guaranteed by Nuvoton via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] V_{CCA} and V_{CCD} connected together.

[4] $\overline{\text{SS}}$ = V_{CCA} = V_{CCD}, XCLK = MOSI = V_{SSA} = V_{SSA} and all other pins floating.

[5] Measured with AutoMute feature disabled.

[6] The test coverage for die is limited to room temperature testing. The test conditions may differ from that of packaged parts.