Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

ISD5008

SINGLE-CHIP,

VOICE RECORD / PLAYBACK DEVICE

4-, 5-, 6- AND 8-SECOND DURATION

Publication Release Date: May, 2005
Revision 0.1

ISD5008

Single-Chip Voice Record/Playback Device
4-, 5-, 6-, and 8-Minute Durations

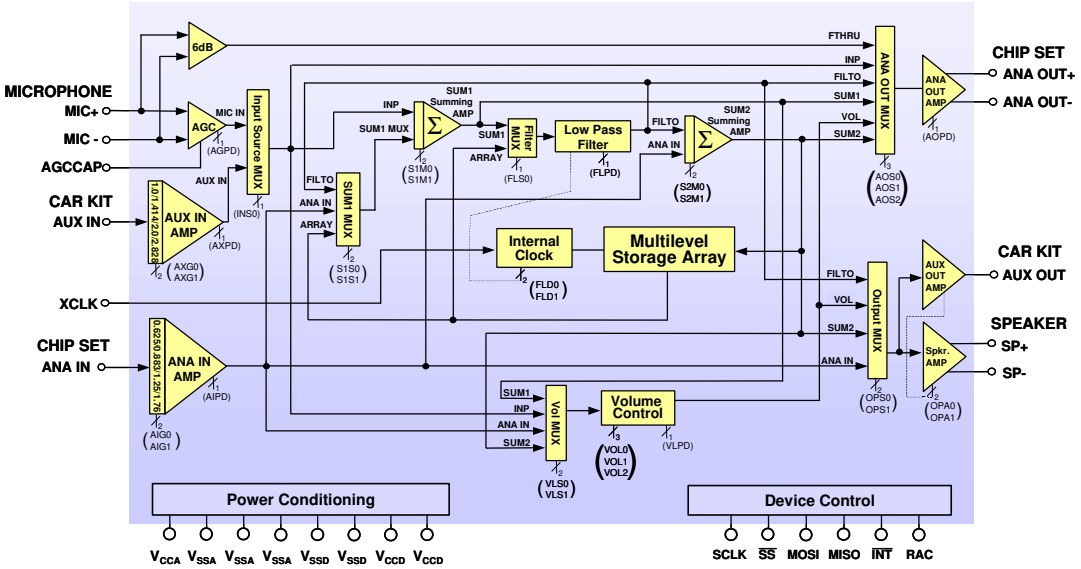
Preliminary Datasheet

ISD5008 PRODUCT SUMMARY

The ISD5008 ChipCorder product is a fully-integrated, single-chip solution which provides seamless integration of enhanced voice record and playback features for digital cellular phones (GSM, CDMA, TDMA, PDC, and PHS), automotive communications, GPS/navigation systems, and portable communication products. This low-power, 3-volt product enables customers to quickly and easily integrate 4 to 8 minutes of voice storage features such as one-way and two-way (full duplex) call record, voice memo record, and call screening/answering machine functionality.

Like other ChipCorder products, the ISD5008 integrates the sampling clock, anti-aliasing and smoothing filters, and the multi-level storage array on a single-chip. For enhanced voice features, the ISD5008 eliminates external circuitry by also integrating automatic gain control (AGC), a power amplifier/speaker driver, volume control, summing amplifiers, analog switches, and a car kit interface. Input level adjustable amplifiers are also included, providing a flexible interface for multiple applications.

Figure: ISD5008 Block Diagram



ISD · 2727 North First Street, San Jose, CA 95134 · TEL: 408/943-6666 · FAX: 408/544-1787 · http://www.isd.com

Duration/sample rate selection is accomplished via software, allowing customers to optimize quality and duration for various features within the same end product.

The ISD5008 device is designed for use in a microprocessor- or microcontroller-based system. Address, control, and duration selection are accomplished through a Serial Peripheral Interface (SPI) or Microwire Serial Interface to minimize pin count.

Recordings are stored in on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through ISD's patented multilevel storage technology. Voice and audio signals are stored directly into solid-state memory in their natural, uncompressed form, providing superior quality voice and music reproduction.

ISD5008 FEATURES

FULLY-INTEGRATED SOLUTION

- Single-chip voice record/playback solution
- Integrated sampling clock, anti-aliasing and smoothing filters, and multi-level storage array
- Integrated analog features such as automatic gain control (AGC), audio gating switches, speaker driver (23mW with 8 ohm load), summing amplifiers, volume control, and an AUX IN/AUX OUT interface (e.g., for car kits).

LOW-POWER CONSUMPTION

- Single + 3 volt supply
- Operating current:
  $I_{CC\ Play}$ = 15 mA (typical)
  $I_{CC\ Rec}$ = 25 mA (typical)
  $I_{CC\ Feedthru}$ = 12 mA (typical)
- Standby current:
  I_{SB} = 1 µA
- Power consumption controlled by SPI or Microwire control register
- Most stages can be individually powered down for minimum power consumption

ENHANCED VOICE FEATURES

- One or two-way (full duplex) conversation record (record signal summation)
- One- or two-way (full duplex) message playback (while on a call)
- Voice memo record and playback
- Private call screening
- In-terminal answering machine
- Personalized outgoing message (given caller ID information from host chip set)
- Private call announce while on call (given CIDCW information from host chip set)

EASY-TO-USE AND CONTROL

- No compression algorithm development required
- User-controllable sample rates of 8.0 kHz, 6.4 kHz, 5.3 kHz, or 4.0 kHz providing up to 8 minutes of voice storage.
- Microcontroller SPI or Microwire™ Serial Interface
- Fully addressable to handle multiple messages in 1200 rows

HIGH QUALITY SOLUTION

- High quality voice and music reproduction
- ISD's standard 100-year message retention (typical)
- 100,000 record cycles (typical)

OPTIONS

- Available in die form, PDIP, SOIC, TSOP, and chip scale packaging (CSP)
- Compact µBGA chip scale package available for portable applications
- Extended temperature (-20 to + 70°C) and industrial temperature (-40 to + 85°C) versions available

Table of Contents

1 DETAILED DESCRIPTION 1
- 1.1 Speech/Sound Quality 1
- 1.2 Duration 1
- 1.3 Flash Storage 1
- 1.4 Microcontroller Interface 1
- 1.5 Programming 1

2 PIN DESCRIPTIONS 2
- 2.1 Digital I/O Pins 2
- 2.2 Analog I/O Pins 3
- 2.3 Power and Ground Pins 6

3 INTERNAL FUNCTIONAL BLOCKS 7

4 SERIAL PERIPHERAL INTERFACE (SPI) DESCRIPTION 13
- 4.1 Message Cueing 13
- 4.2 Power-Up Sequence 14
- 4.3 SPI Port 15
- 4.4 SPI Control Register 15

5 OPERATIONAL MODES DESCRIPTION 21
- 5.1 Feed Through Mode 21
- 5.2 Call Record 23
- 5.3 Memo Record 24
- 5.4 Memo and Call Record Playback 24

6 TIMING DIAGRAMS 34

7 DEVICE PHYSICAL DIMENSIONS 36

8 ORDERING INFORMATION 42

1 DETAILED DESCRIPTION

1.1 SPEECH/SOUND QUALITY

The ISD5008 ChipCorder product can be configured via software to operate at 4.0, 5.3, 6.4, and 8.0 kHz sampling frequencies, allowing the user a choice of speech quality options. Increasing the duration decreases the sampling frequency and bandwidth, which affects sound quality. Table 1 compares filter pass band and product durations.

The speech samples are stored directly into on-chip nonvolatile memory without the digitization and compression associated with other solutions. Direct analog storage provides a natural sounding reproduction of voice, music, tones, and sound effects not available with most solid-state solutions.

1.2 DURATION

To meet end system requirements, the ISD5008 device is a single-chip solution which provides from 4 to 8 minutes of voice record and playback, depending on the sample rates defined by customer software.

Table 1: Input Sample Rate to Duration

Input Sample Rate (kHz)	Duration (Minutes)	Typical Filter Pass Band (kHz)
8.0	4.0	3.4
6.4	5.0	2.7
5.3	6.0	2.3
4.0	8.0	1.7

1.3 FLASH STORAGE

One of the benefits of ISD's ChipCorder technology is the use of on-chip nonvolatile memory, which provides zero-power message storage. The message is retained for up to 100 years (typically) without power. In addition, the device can be re-recorded over 100,000 times (typically).

1.4 MICROCONTROLLER INTERFACE

A four-wire (SCLK, MOSI, MISO, $\overline{SS}$) SPI interface is provided for ISD5008 control, addressing functions, and sample rate selection. The ISD5008 is configured to operate as a peripheral slave device with a microcontroller-based SPI bus interface. Read/Write access to all the internal registers occurs through this SPI interface. An interrupt signal ($\overline{INT}$) and internal read-only Status Register are provided for handshake purposes.

1.5 PROGRAMMING

The ISD5008 series is also ideal for playback-only applications, where single or multiple message Playback is controlled through the SPI port. Once the desired message configuration is created, duplicates can easily be generated via an ISD or third-party programmers. For more information on available application tools and programmers please see the ISD web site at www.isd.com.

2 PIN DESCRIPTIONS

2.1 DIGITAL I/O PINS

SCLK (Serial Clock)

The SCLK is the clock input to the ISD5008. Generated by the master microcontroller, the SCLK synchronizes data transfers in and out of the device through the MISO and MOSI lines. Data is latched into the ISD5008 on the rising edge of SCLK and shifted out on the falling edge.

$\overline{SS}$ (Slave Select)

This input, when LOW, will select the ISD5008 device.

MOSI (Master Out Slave In)

MOSI is the serial data input to the ISD5008 device. The master microcontroller places data to be clocked into the ISD5008 device on the MOSI line one-half cycle before the rising edge of SCLK. Data is clocked into the device LSB (Least Significant Bit) first.

MISO (Master In Slave Out)

MISO is the serial data output of the ISD5008 device. Data is clocked out on the falling edge of SCLK. This output goes into a high-impedance state when the device is not selected. Data is clocked out of the device LSB first.

$\overline{INT}$ (Interrupt)

$\overline{INT}$ is an open drain output pin. The ISD5008 interrupt pin goes LOW and stays LOW when an Overflow (OVF) or End of Message (EOM) marker is detected. Each operation that ends in an EOM or OVF generates an interrupt, including the message cueing cycles. The interrupt is cleared the next time an SPI cycle is completed. The interrupt status can be read by a RINT instruction that will give one of the two flags out the MISO line.

OVF Flag. The overflow flag indicates that the end of the ISD5008's analog memory has been reached during a record or playback operation.

EOM Flag. The end of message flag is set only during playback, when an EOM is found. There are eight possible EOM markers per row.

RAC (Row Address Clock)

RAC is an open drain output pin that marks the end of a row. At the 8 kHz sample frequency, the duration of this period is 200 ms. There are 1,200 rows of memory in the ISD5008 devices. RAC stays HIGH for 175 ms and stays LOW for the remaining 25 ms before it reaches the end of the row.

The RAC pin remains HIGH for 109.38 µsec and stays LOW for 15.63 µsec under the Message Cueing mode. See Table 15 Timing Parameters for RAC timing information at other sample rates. When a record command is first initiated, the RAC pin remains HIGH for an extra T_{RACLO} period, to load sample and hold circuits internal to the device. The RAC pin can be used for message management techniques.

XCLK (External Clock Input)

The external clock input for the ISD5008 product has an internal pull-down device. Normally, the ISD5008 is operated at one of four internal rates selected for its internal oscillator by the Sample Rate Select bits. If greater precision is required, the device can be clocked through the XCLK pin as described in Table 2.

Because the antialiasing and smoothing filters track the Sample Rate Select bits, one must, for optimum performance, change the external clock *AND* the Sample Rate Configuration bits to one of the four values to properly set the filters to the correct cutoff frequency as described in Table 3. The duty cycle on the input clock is not critical, as the clock is immediately divided by two internally. If the XCLK is not used, this input should be connected to V_{SSD}.

Table 2: External Clock Input Table

Duration (Minutes)	Sample Rate (kHz)	Required Clock (kHz)
4	8.0	1024
5	6.4	819.2
6	5.3	682.7
8	4.0	512

Table 3: Internal Clock Rate/Filter Edge

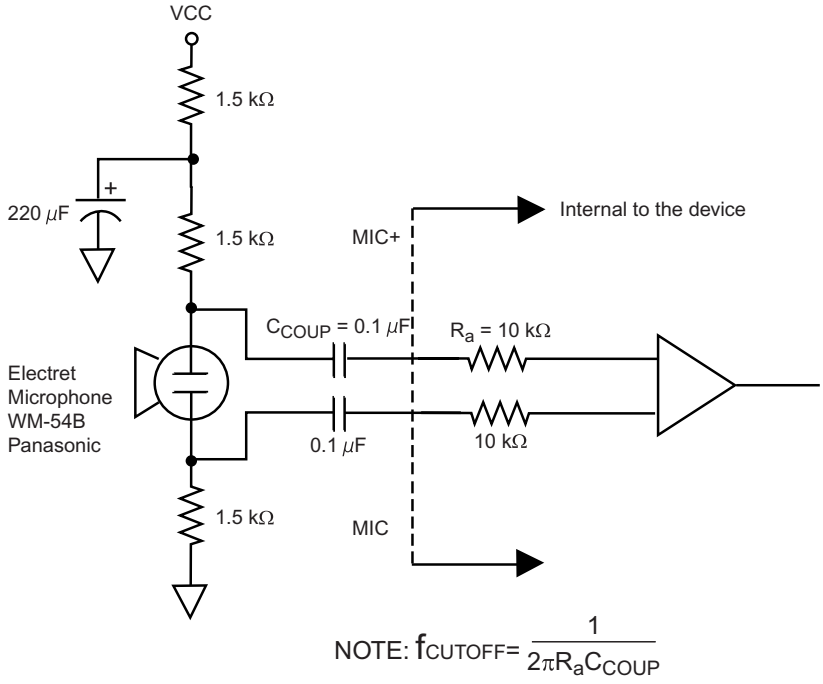
FLD1	FLD0	Sample Rate (kHz)	Filter Pass Band (kHz)
0	0	8	3.4
0	1	6.4	2.7
1	0	5.3	2.3
1	1	4	1.7

2.2 ANALOG I/O PINS

MIC+ , MIC – (Microphone Input+ /–)

The microphone input transfers the voice signal to the on-chip AGC preamplifier or directly to the ANA OUT MUX, depending on the selected path. The direct path to the ANA OUT MUX has a gain of 6 dB so a 208 mVp-p signal across the differential microphone inputs would give 416 mVp-p across the ANA OUT pins. The AGC circuit has a range of 45 dB in order to deliver a nominal 694 mVp-p into the storage array from a typical electret microphone output of 2 to 20 mVp-p. The input impedance is typically 10 kΩ

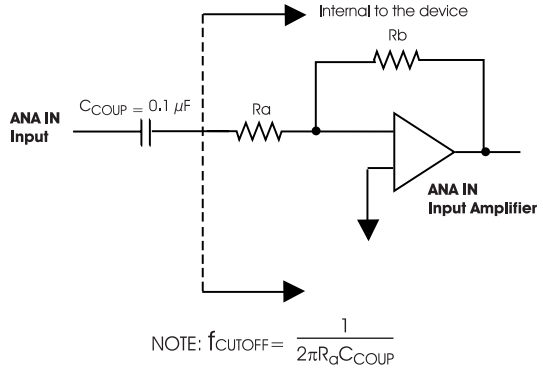
Figure 1: Microphone Input



ANA IN (Analog Input)

The ANA IN pin is the analog input from the telephone chip set. It can be switched (by the SPI bus) to the speaker output, the array input or to various other paths. This pin is designed to accept a nominal 1.11 Vp-p when at its minimum gain (6 dB) setting. There is additional gain available in 3 dB steps controlled from the SPI bus, if required, up to 15 dB.

Figure 2: ANA IN Input Modes



Gain Setting	Resistor Ratio (Rb/Ra)	Gain	Gain[2] (dB)
00	63.9/102	0.625	–4.1
01	77.9/88.1	0.88	–1.1
10	92.3/73.8	1.25	1.9
11	106/60	1.77	4.9

Table 4: ANA IN Amplifier Gain Settings

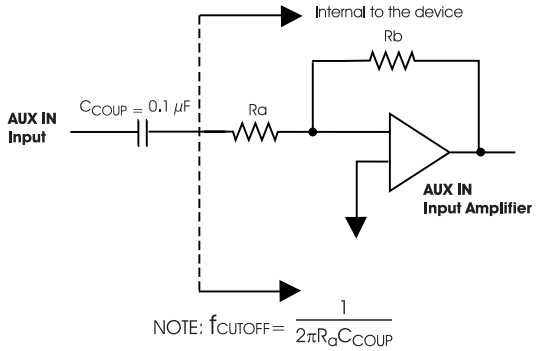
Setting[1]	0TLP Input V_{PP}[3]	CFG0		Gain[2]	Array In/Out V_{PP}	Speaker Out V_{PP}[4]
		AIG1	AIG0			
6 dB	1.11	0	0	.625	.694	2.22
9 dB	.785	0	1	.883	.694	2.22
12 dB	.555	1	0	1.250	.694	2.22
15 dB	.393	1	1	1.767	.694	2.22

1. *Gain from ANA IN to SP+ /–*
2. *Gain from ANA IN to ARRAY IN*
3. *0TLP Input is the reference Transmission Level Point that is used for testing. This level is typically 3 dB below clipping.*
4. *Speaker Out gain set to 1.6 (High). (Differential)*

AUX IN (Auxiliary Input)

The AUX IN is an additional audio input to the ISD5008, such as from the microphone circuit in a mobile phone "car kit." This input has a nominal 700 mVp-p level at its minimum gain setting (0 dB). See Table 5. Additional gain is available in 3 dB steps (controlled by the SPI bus) up to 9 dB.

Figure 3: AUX IN Input Modes



Gain Setting	Resistor Ratio (Rb/Ra)	Gain	Gain (dB)
00	40.1/40.1	1.0	0
01	47.0/33.2	1.414	3
10	53.5/26.7	2.0	6
11	59.2/21	2.82	9

Table 5: AUXIN Amplifier Gain Settings

Setting(1)	0TLP Input V_{PP}(3)	CFG0		Gain(2)	Array In/Out V_{PP}	Ana Out V_{PP}(4)
		AXG1	AXG0			
0 dB	.694	0	0	1.00	.694	.694
3 dB	.491	0	1	1.41	.694	.694
6 dB	.347	1	0	2.00	.694	.694
9 dB	.245	1	1	2.82	.694	.694

1. *Gain from AUX IN to ANA OUT*
2. *Gain from AUX IN to ARRAY IN*
3. *0TLP Input is the reference Transmission Level Point that is used for testing. This level is typically 3 dB below clipping.*
4. *Differential*

ANAOUT+ /– (Analog Outputs)

This differential output is designed to go to the microphone input of the telephone chip set. It is designed to drive a minimum of 5 kΩ between the "+ " and "–" pins to a nominal voltage level of 700 mVp-p. Both pins have DC bias of approximately 1.2 VDC. The AC signal is superimposed upon this analog ground voltage. These pins can be used single-ended, getting only half the voltage. Do **NOT** ground the unused pin.

AUX OUT (Auxiliary Output)

The AUXOUT is an additional audio output pin, to be used, for example, to drive the speaker circuit in a "car kit." It drives a minimum load of 5 kΩ and up to a maximum of 1 Vp-p. The AC signal is superimposed on approximately 1.2 VDC bias and must be capacitively coupled to the load.

SP+ , SP– (Speaker+ /–)

This is the speaker differential output circuit. It is designed to drive an 8 Ω speaker connected across the speaker pins up to a maximum of 23.5 mW power. This stage has two selectable gains, 1.32 and 1.6, which can be chosen through the configuration registers. These pins are biased to approximately 1.2 VDC and, if used single-ended, must be capacitively coupled to their load. Do **NOT** ground the unused pin.

ACAP (AGC Capacitor)

This pin provides the capacitor connection for setting the parameters of the microphone AGC circuit. It should have a 4.7 µF capacitor connected to ground. It cannot be left floating. This is because the capacitor is also used in the playback mode for the AutoMute circuit. This circuit reduces the amount of noise present in the output during quiet pauses. Tying this pin to ground gives maximum gain; to V_{CCA} gives minimum gain for the AGC amplifier but will cancel the AutoMute function.

2.3 POWER AND GROUND PINS

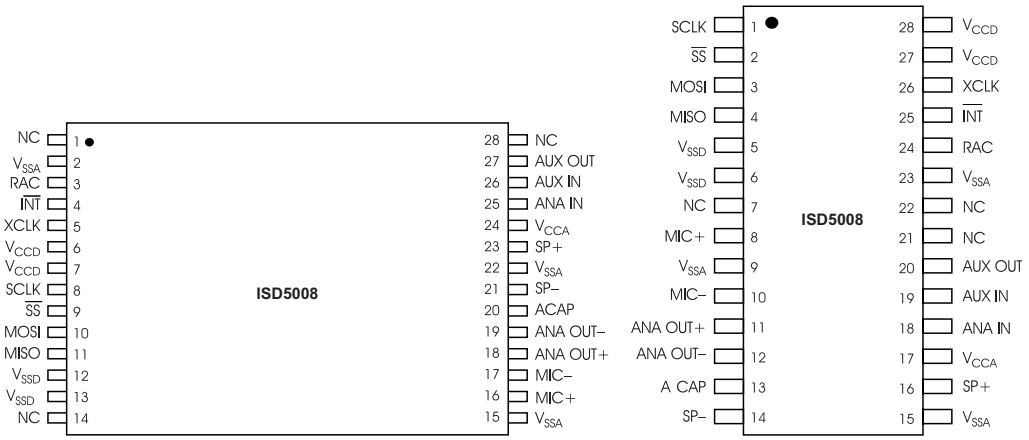
V_{CCA}, V_{CCD} (Voltage Inputs)

To minimize noise, the analog and digital circuits in the ISD5008 device uses separate power busses. These + 3 V busses lead to separate pins. Tie the V_{CCD} pins together as close as possible and decouple both supplies as near to the package as possible.

V_{SSA}, V_{SSD} (Ground Inputs)

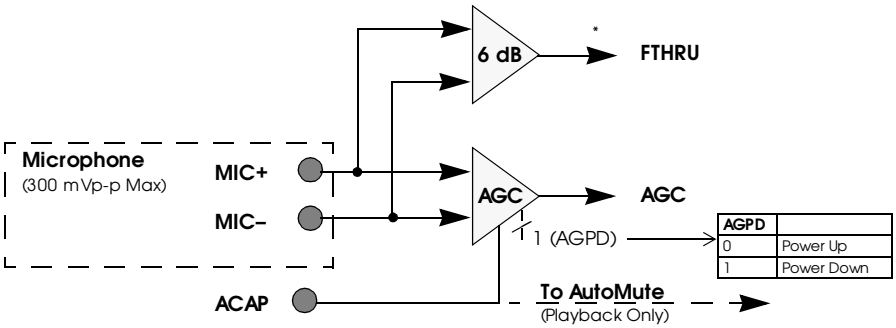
The ISD5008 series utilizes separate analog and digital ground busses. The analog ground (V_{SSA}) pins should be tied together as close to the package as possible and connected through a low-impedance path to power supply ground. The digital ground (V_{SSD}) pin should be connected through a separate low-impedance path to power supply ground. These ground paths should be large enough to ensure that the impedance between the V_{SSA} pins and the V_{SSD} pin is less than 3 Ω The backside of the die is connected to V_{SSD} through the substrate resistance. In a chip-on-board design, the die attach area must be connected to V_{SSD}.

Figure 4: ISD5008 Series TSOP and PDIP/SOIC Pinouts



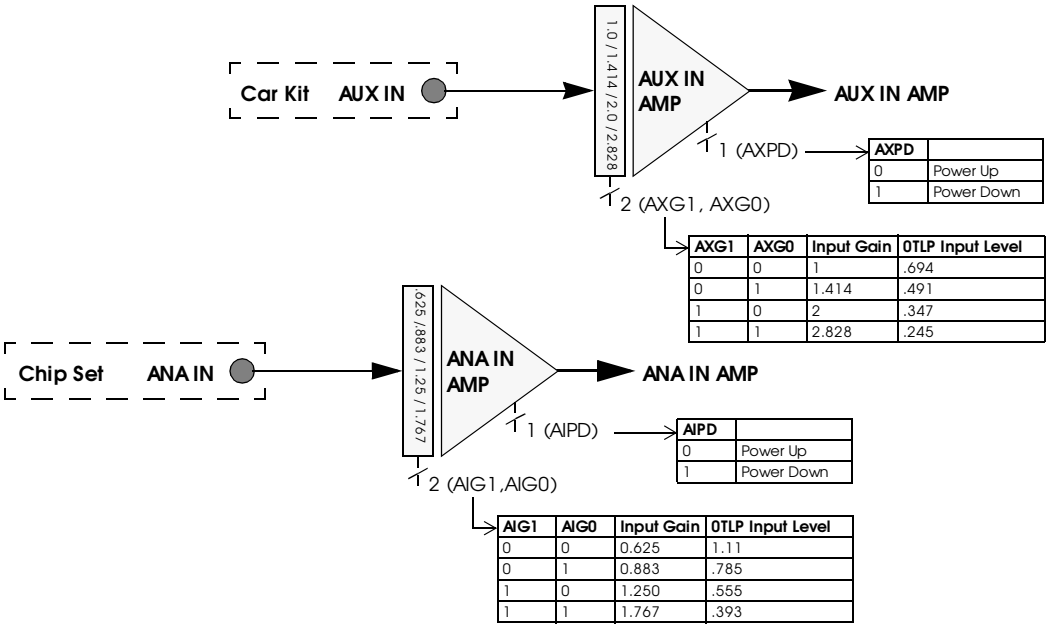
3 INTERNAL FUNCTIONAL BLOCKS

Figure 5: Microphone Amplifier



15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
VLS1	VLS0	VOL2	VOL1	VOL0	S1S1	S1S0	S1M1	S1M0	S2M1	S2M0	FLS0	FLD1	FLD0	FLPD	AGPD	CFG1

Figure 6: AUX IN and ANA IN



AXPD	
0	Power Up
1	Power Down

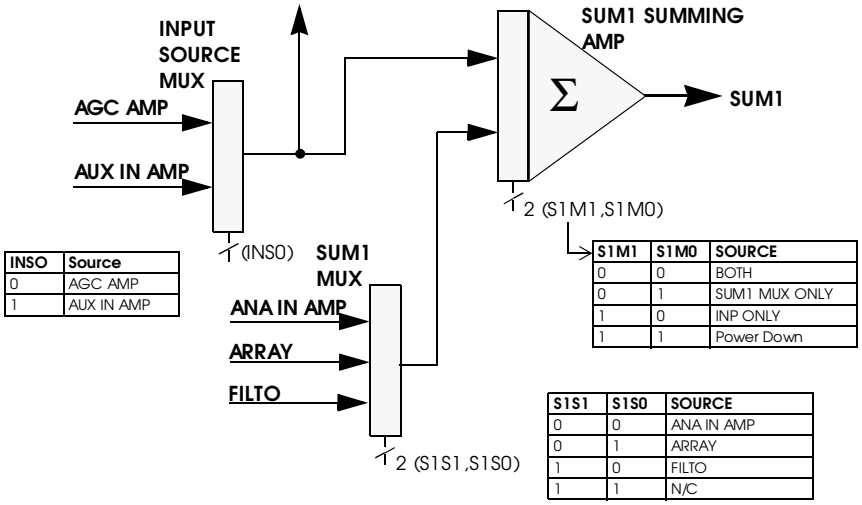
AXG1	AXG0	Input Gain	0TLP Input Level
0	0	1	.694
0	1	1.414	.491
1	0	2	.347
1	1	2.828	.245

AIPD	
0	Power Up
1	Power Down

AIG1	AIG0	Input Gain	0TLP Input Level
0	0	0.625	1.11
0	1	0.883	.785
1	0	1.250	.555
1	1	1.767	.393

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
AIG1	AIG0	AIPD	AXG1	AXG0	AXPD	INS0	AOS2	AOS1	AOS0	AOPD	OPS1	OPS0	OPA1	OPA0	VLPD	CFG0

Figure 7: ISD5008 Core (Left Half)



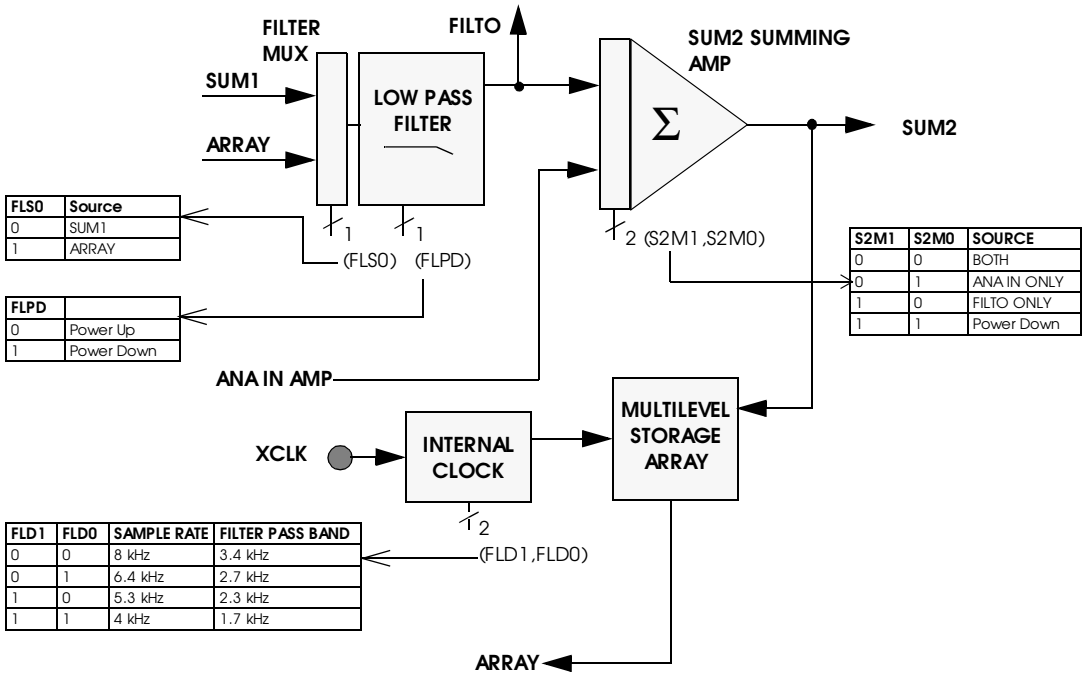
INSO	Source
0	AGC AMP
1	AUX IN AMP

S1M1	S1M0	SOURCE
0	0	BOTH
0	1	SUM1 MUX ONLY
1	0	INP ONLY
1	1	Power Down

S1S1	S1S0	SOURCE
0	0	ANA IN AMP
0	1	ARRAY
1	0	FILTO
1	1	N/C

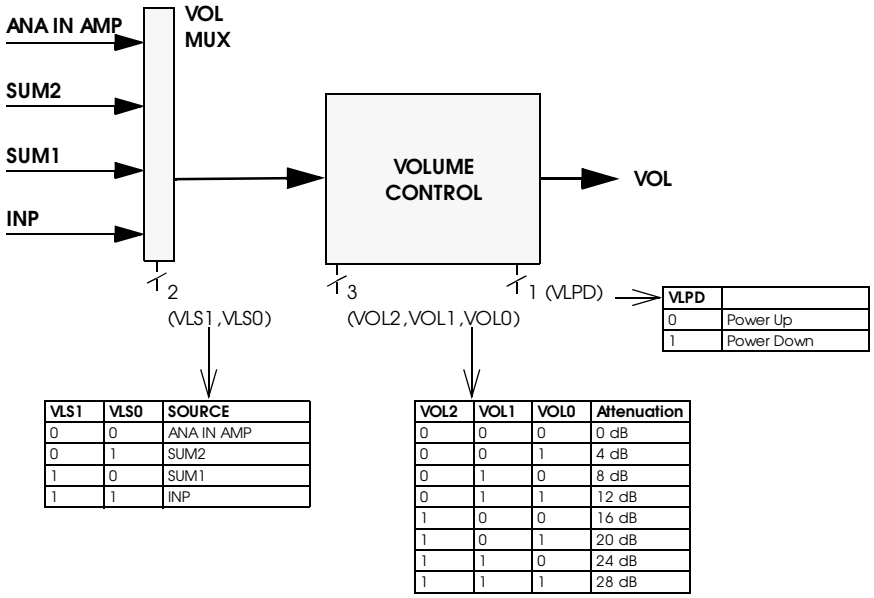
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
AIG1	AIG0	AIPD	AXG1	AXG0	AXPD	**INS0**	AOS2	AOS1	AOS0	AOPD	OPS1	OPS0	OPA1	OPA0	VLPD	**CFG0**
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
VLS1	VLS0	VOL2	VOL1	VOL0	**S1S1**	**S1S0**	**S1M1**	**S1M0**	S2M1	S2M0	FLS0	FLD1	FLD0	FLPD	AGPD	**CFG1**

Figure 8: ISD5008 Core (Right Half)



15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
VLS1	VLS0	VOL2	VOL1	VOL0	S1S1	S1S0	S1M1	S1M0	**S2M1**	**S2M0**	**FLS0**	**FLD1**	**FLD0**	**FLPD**	AGPD	**CFG1**

Figure 9: Volume Control



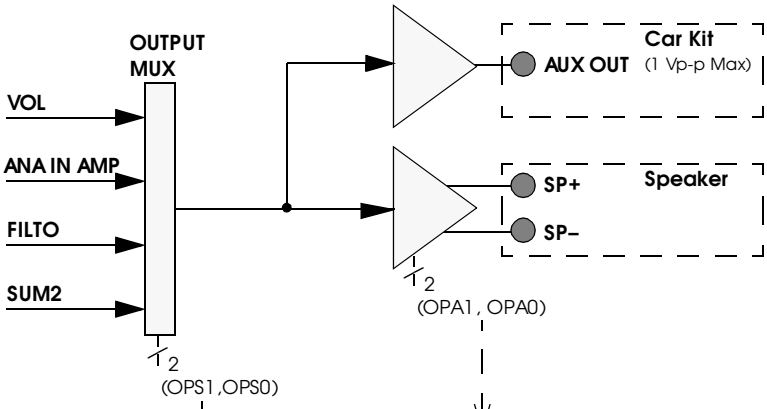
VLPD	
0	Power Up
1	Power Down

VLS1	VLS0	SOURCE
0	0	ANA IN AMP
0	1	SUM2
1	0	SUM1
1	1	INP

VOL2	VOL1	VOL0	Attenuation
0	0	0	0 dB
0	0	1	4 dB
0	1	0	8 dB
0	1	1	12 dB
1	0	0	16 dB
1	0	1	20 dB
1	1	0	24 dB
1	1	1	28 dB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
AIG1	AIG0	AIPD	AXG1	AXG0	AXPD	INS0	AOS2	AOS1	AOS0	AOPD	OPS1	OPS0	OPA1	OPA0	**VLPD**	**CFG0**
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
VLS1	**VLS0**	**VOL2**	**VOL1**	**VOL0**	S1S1	S1S0	S1M1	S1M0	S2M1	S2M0	FLS0	FLD1	FLD0	FLPD	AGPD	**CFG1**

Figure 10: Speaker and AUX OUT

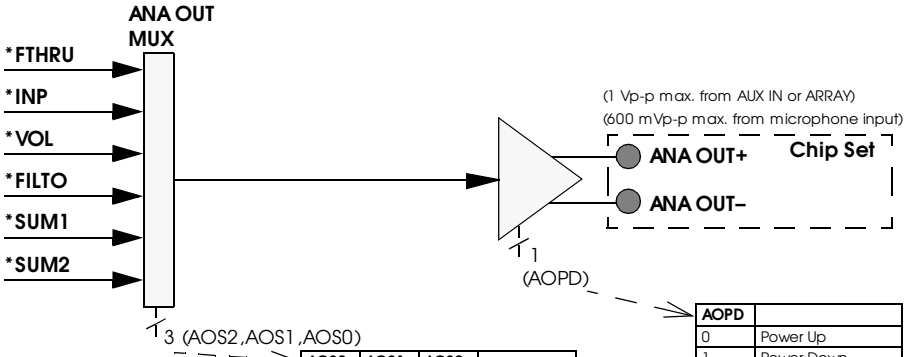


OPS1	OPS0	SOURCE
0	0	VOL
0	1	ANA IN
1	0	FILTO
1	1	SUM2

OPA1	OPA0	SPKR Drive	AUX OP
0	0	Power Down	Power Down
0	1	3.6 Vp-p @ 150 Ω	Power Down
1	0	23 mWatt @ 8 Ω	Power Down
1	1	Power Down	1 Vp-p Max @ 5kΩ

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
AIG1	AIG0	AIPD	AXG1	AXG0	AXPD	INS0	AOS2	AOS1	AOS0	AOPD	**OPS1**	**OPS0**	**OPA1**	**OPA0**	VLPD	**CFG0**

Figure 11: ANA OUT Output



AOS2	AOS1	AOS0	
0	0	0	FTHRU
0	0	1	INP
0	1	0	VOL
0	1	1	FILTO
1	0	0	SUM1
1	0	1	SUM2
1	1	0	N/C
1	1	1	N/C

AOPD	
0	Power Up
1	Power Down

*DIFFERENTIAL PATH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
AIG1	AIG0	AIPD	AXG1	AXG0	AXPD	INS0	**AOS2**	**AOS1**	**AOS0**	**AOPD**	OPS1	OPS0	OPA1	OPA0	VLPD	**CFG0**

4 SERIAL PERIPHERAL INTERFACE (SPI) DESCRIPTION

The ISD5008 product operates from an SPI serial interface. The SPI interface operates with the following protocol.

The data transfer protocol assumes that the microcontroller's SPI shift registers are clocked on the falling edge of the SCLK. With the ISD5008, data is clocked in on the MOSI pin on the rising clock edge. Data is clocked out on the MISO pin on the falling clock edge.

1. All serial data transfers begin with the falling edge of $\overline{SS}$ pin.
2. $\overline{SS}$ is held LOW during all serial communications and held HIGH between instructions.
3. Data is clocked in on the rising clock edge and data is clocked out on the falling clock edge.
4. Play and Record operations are initiated by enabling the device by asserting the $\overline{SS}$ pin LOW, shifting in an opcode and an address field to the ISD5008 device (refer to the Opcode Summary on the page 14).
5. The opcodes and address fields are as follows: < 8 control bits> and < 16 address bits> .
6. Each operation that ends in an EOM or Overflow will generate an interrupt, including the Message Cueing cycles. The Interrupt will be cleared the next time an SPI cycle is completed.
7. As Interrupt data is shifted out of the ISD5008 MISO pin, control and address data is simultaneously being shifted into the MOSI pin. Care should be taken such that the data shifted in is compatible with current system operation. It is possible to read interrupt data and start a new operation within the same SPI cycle.
8. A record or playback operation begins with the RUN bit set and the operation ends with the RUN bit reset.
9. All operations begin with the rising edge of $\overline{SS}$.

4.1 MESSAGE CUEING

Message cueing allows the user to skip through messages, without knowing the actual physical location of the message. This operation is used during playback. In this mode, the messages are skipped 1600 times faster than in normal playback mode. It will stop when an EOM marker is reached. Then, the internal address counter will point to the next message.

Table 6: Opcode Summary

Instruction	Opcode <8 bits>[1] Address <16 bits>	Operational Summary
POWERUP	0110 0000	Power-Up: See "Power-Up Sequence"
LOADCFG0[2]	01X0 0010 < D15–D0>	Loads a 16-bit value into Configuration Register 0
LOADCFG1	01X0 0100 < D15–D0>	Loads a 16-bit value into Configuration Register 1
SETPLAY	1110 0000 < A15–A0>	Initiates Playback from address < A15–A0>
PLAY	1111 0000	Playback from current address (until EOM or OVF)
SETREC	1010 0000 < A15–A0>	Initiates Record at address < A15–A0>
REC	1011 0000	Records from current address until OVF is reached
MC	1111 1000	Performs a Message Cue. Proceeds to the end of the current message (EOM) or enters OVF condition if it reaches the end of the array.
STOP	0111 0000	Stops current operation
STOPWRDN	0101 0000	Stops current operation and enters stand-by (power-down) mode.
RINT	0111 0000	Read interrupt status bits: OVF and EOM.

1. *X = Don't Care.*
2. *Changes in CFG0 are not recognized until CFG1 is loaded. The changes will occur at the rising edge of $\overline{SS}$ during the cycle that CFG1 is loaded.*

4.2 POWER-UP SEQUENCE

The ISD5008 will be ready for an operation after T_{PUD} (25 ms approximately for 8 kHz sample rate). The user needs to wait T_{PUD} before issuing an operational command. For example, to play from address 00 the following programing cycle should be used.

Playback Mode

1. Send POWERUP command.
2. Wait T_{PUD} (power-up delay).
3. Load CFG0 and CFG1 for desired operation.
4. Send SETPLAY command with address 00.

The device will start playback at address 00 and it will generate an interrupt when an EOM is reached. It will then stop playback.

Record Mode

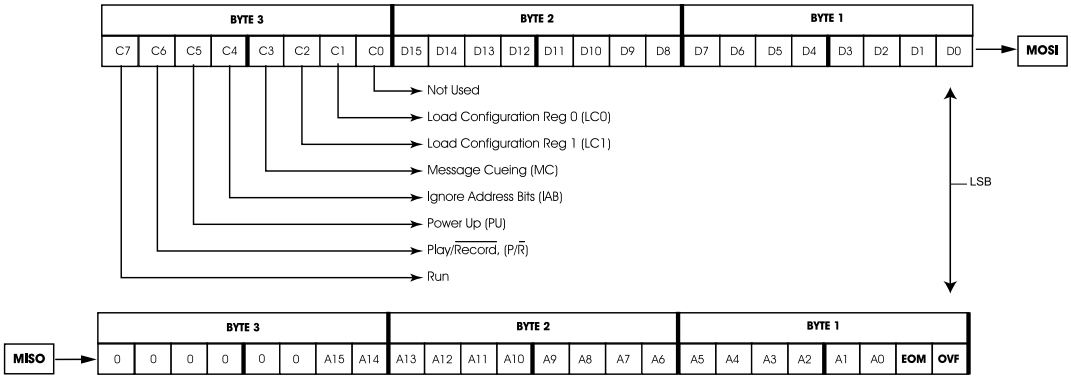
1. Send POWERUP command.
2. Wait T_{PUD} (power-up delay).
3. Load CFG0 and CFG1 for desired operation.
4. Send SETREC command with address 00.

The device will start recording at address 00 and it will generate an interrupt when an overflow is reached (end of memory array) or when it has received a STOP command. It will then stop recording.

4.3 SPI PORT

The following diagram describes the SPI port and the control bits associated with it.

Figure 12: SPI Port



NOTE: *Bytes 1 and 2 of the MOSI input may be address bits or configuration bits, depending on the selected mode in byte 3.*

4.4 SPI CONTROL REGISTER

The SPI control register provides control of individual device functions such as Play, Record, Message Cueing, Power-Up and Power-Down, Start and Stop operations, Ignore Address Pointers and Load Configuration Registers.

Table 7: SPI Control Register

Control Register	Bit	Device Function	Control Register	Bit	Device Function
RUN		Enable or Disable an operation	PU		Master power control
=	1	Start	=	1	Power-Up
=	0	Stop	=	0	Power-Down
P/$\overline{R}$		Selects Play or Record operation	IAB		Ignore address control bit
=	1	Play	=	1	Ignore input address register (A15–A0)
=	0	Record	=	0	Use the input address register contents for an operation (A15–A0)
MC		Enable or Disable Message Cueing	A15–A0		Output of the row pointer register
=	1	Enable Message Cueing	D15–D0		Input control and address register
=	0	Disable Message Cueing			
LC0			LC1		
=	1	Load Configuration Reg 0	=	1	Load Configuration Reg 1
=	0	No Load	=	0	No Load

Table 8: Configuration Register 0

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	CFG0
AIG1	AIG0	AIPD	AXG1	AXG0	AXPD	INS0	AOS2	AOS1	AOS0	AOPD	OPS1	OPS0	OPA1	OPA0	VLPD	
ANA IN AMP Gain SET (2 bits)		ANA IN Power Down	AUX IN AMP Gain SET (2 bits)		AUX IN Power Down	INPUT SOURCE MUX Select (1 bit)	ANA OUT MUX Select (3 bits)			ANA OUT Power Down	OUPUT MUX Select (2 bits)		SPKR & AUX OUT Control (2 bits)		Volume Control Power Down	

NOTE: *See details on following pages.*

Table 9: Configuration Register 1

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	CFG1
VLS1	VLS0	VOL2	VOL1	VOL0	S1S1	S1S0	S1M1	S1M0	S2M1	S2M0	FLSO	FLD1	FLD0	FLPD	AGPD	
VOLUME CONT. MUX Select (2 bits)		VOLUME CONTROL (3 bits)			SUM 1 MUX Select (2 bits)		SUM 1 SUMMING AMP Control (2 bits)			SUM2 SUMMING AMP Control (2 bits)	FILTER MUX Select		SAMPLE RATE (& Filter) Set Up (2 bits)		Filter Power Down	AGC AMP Power Down

NOTE: *See details on following pages.*

Detail of Configuration Register 0		
Volume Control Power Bit	Bit 0 (VLPD)	0 = Power ON 1 = Power OFF
SPEAKER and AUX OUT Control Bits	Bits 2,1 (OPA1, OPA0)	00 = Power down SPKR and AUX 01 = SPKR ON, HIGH GAIN, AUX Power down 10 = SPKR ON, LOW GAIN, AUX Power down 11 = SPKR Powered down, AUX ON
OUTPUT MUX Control Bits	Bits 4,3 (OPS1, OPS0)	00 = Source is VOL CONTROL (VOL) 01 = Source is ANA IN Input (ANA IN AMP) 10 = Source is LOW PASS FILTER (FILT0) 11 = Source is SUM2 SUMMING AMP (SUM2)
ANA OUT Power Bit	Bit 5 (AOPD)	0 = Power ON 1 = Power OFF
ANA OUT MUX Control Bits	Bits 8,7,6 (AOS2, AOS1, AOS0)	000 = Source is MICROPHONE AMP (FTHRU) 001 = Source is INPUT MUX (INP) 010 = Source is VOLUME CONTROL (VOL) 011 = Source is LOW PASS FILTER (FILT0) 100 = Source is SUM1 SUMMING AMP (SUM1) 101 = Source is SUM2 SUMMING AMP (SUM2) 110 = Unused 111 = Unused
INPUT SOURCE MUX Control Bit	Bit 9 (INS0)	0 = Source is Microphone AGC AMP (AGC) 1 = Source is AUX IN Input (AUX IN AMP)
AUX IN AMP Power Bit	Bit 10 (AXPD)	0 = Power ON 1 = Power OFF
AUX IN AMP Control Bits	Bits 12,11 (AXG1, AXG0)	00 = Input Gain = 1, O_{TLP} input Level = 0.694 01 = Input Gain = 1.414, O_{TLP} input Level = 0.491 10 = Input Gain = 2, O_{TLP} input Level = 0.347 11 = Input Gain = 2.828, O_{TLP} input Level = 0.245
ANA IN AMP Power Bit	Bit 13 (AIPD)	0 = Power ON 1 = Power OFF
ANA IN AMP Control Bits	Bits 15,14 (AIG1, AIG0)	00 = Input Gain = 0.625, O_{TLP} input Level = 1.11 01 = Input Gain = 0.883, O_{TLP} input Level = 0.7l85 10 = Input Gain = 1.250, O_{TLP} input Level = 0.555 11 = Input Gain = 1.767, O_{TLP} input Level = 0.393

Detail of Configuration Register 1		
AGC Power Control Bit	Bit 0 (AGPD)	0 = Power ON 1 = Power OFF
LOW PASS FILTER Power Control Bit	Bit 1 (FLPD)	0 = Power ON 1 = Power OFF
SAMPLE RATE and LOW PASS FILTER Control Bits	Bits 3,2 (FLD1, FLD0)	00 = Sample Rate = 8 KHz, FPB = 3.4 KHz 01 = Sample Rate = 6.4 KHz, FPB = 2.7 KHz 10 = Sample Rate = 5.3 KHz, FPB = 2.3 KHz 11 = Sample Rate = 4 KHz, FPB = 1.7 KHz
FILTER MUX Control bits	Bit 4 (FLS0)	0 = Source is SUM1 SUMMING AMP (SUM1) 1 = Source is Analog Memory Array (ARRAY)
SUM 2 SUMMING AMP Control Bits	Bits 6,5 (S2M1, S2M0)	00 = Source is both ANA IN AMP and FILT0 01 = Source is ANA IN Input (ANA IN AMP) ONLY 10 = Source is LOW PASS FILTER (FILT0) ONLY 11 = Power Down SUM2 SUMMING AMP
SUM1 SUMMING AMP Control Bits	Bit 8,7 (S1M1, S1M0)	00 = Source is both SUM1 and INP 01 = Source is SUM1 SUMMING AMP (SUM1) ONLY 10 = Source is INPUT MUX (INP) ONLY 11 = Power Down SUM1 SUMMING AMP
SUM1MUX Control Bits	Bit 10,9 (S1S1, S1S0)	00 = Source is ANA IN Input (ANA IN AMP) 01 = Source is Analog Memory Array (ARRAY) 10 = Source is LOW PASS FILTER (FILT0) 11 = UNUSED
VOLUME CONTROL Control Bits	Bits 13,12,11 (VOL2, VOL1, VOL0)	000 = Attenuation = 0 dB 001 = Attenuation = 4 dB 010 = Attenuation = 8 dB 011 = Attenuation = 12 dB 100 = Attenuation = 16 dB 101 = Attenuation = 20 dB 110 = Attenuation = 24 dB 111 = Attenuation = 28 dB
VOL MUX Control Bits	Bit 15,14 (VLS1, VLS0)	00 = Source is ANA IN Input (ANA IN AMP) 01 = Source is SUM2 SUMMING AMP (SUM2) 10 = Source is SUM1 SUMMING AMP (SUM1) 11 = Source is INPUT MUX (INP)

Configuration Register Notes

1. ***Important:*** All changes to the internal settings of the ISD5008 are synchronized with the load of Configuration Register 1. A command to load Configuration Register 1 immediately transfers the input data to the internal settings of the device and the changes take place immediately at the end of the command when SS\ goes HIGH. A load to Configuration Register 0 sends the new data to a temporary register in the ISD5008 and does not affect the internal settings of the device. The next time Configuration Register 1 is loaded, data will also transfer from the temporary register to the Configuration 0 Register and effect the desired changes. See Figure Table 13.
2. Configuration Registers may be loaded with data at any time, including when the chip is powered down using the PU bit in the SPI Control Register. The PU bit in the SPI Control Word will have to be set to a "1" before the changes in configuration will be seen.

Figure 13: Configuration Register Programming Sequence

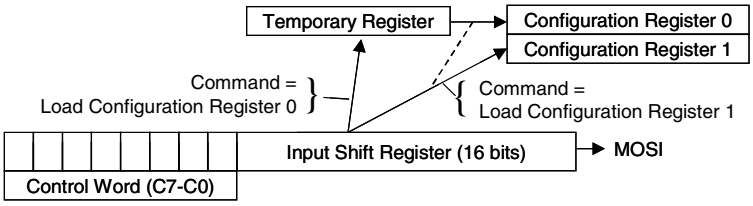
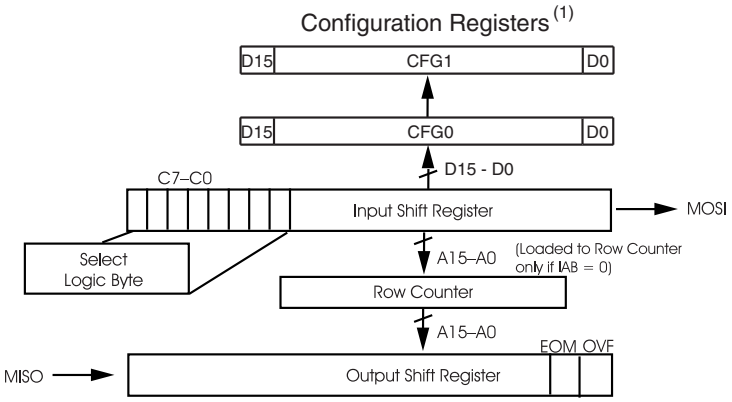
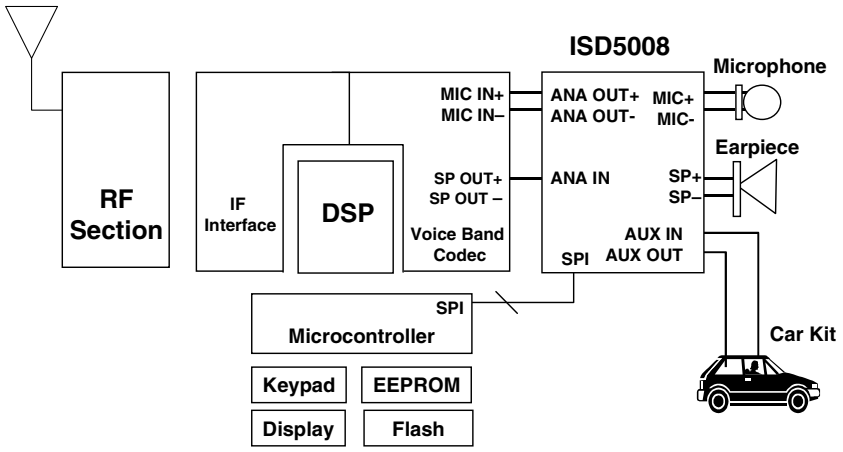


Figure 14: SPI Interface Simplified Block Diagram



1. See Table 8 for bit details.

Figure 15: Typical Digital Cellular Phone Integration



5 OPERATIONAL MODES DESCRIPTION

The ISD5008 can operate in many different modes. It's flexibility allows the user to configure the chip such that almost any input can mixed with any other input and then be directed to any output. The variable settings for the ANA and AUX input amplifiers plus the microphone AGC and speaker volume controls make it possible to use the device with most existing cell phone or cordless phone chip sets with no external level adjustment. Several modes will be found in most applications, however. Please refer to the ISD5008 block diagram to better understand the following modes. In all cases, we are assuming that the chip has been powered up with the PU bit in the SPI control register and that a time period of T_{PUD} has elapsed after that bit was set:

5.1 FEED THROUGH MODE

This mode enables the ISD5008 to connect to a base band cell phone or cordless phone chip set without affecting the audio source or destination. There are two paths involved, the transmit path and the receive path. The transmit path connects the ISD chip's microphone source through to the microphone input on the base band chip set. The receive path connects the base band chip set's speaker output through to the speaker driver on the ISD chip. This allows the ISD chip to substitute for those functions and incidentally gain access to the audio to and from the base band chip set. Figure 15 shows one possible connection to such a chip set.

Figure 16 shows the part of the ISD5008 block diagram that is used in Feed Through Mode. The rest of the chip will be powered down to conserve power. The bold lines highlight the audio paths. Note that the Microphone to ANA OUT + /– path is differential.

Figure 16: Basic Feed-Thru Mode