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ISD5008

3V, SINGLE-CHIP

VOICE RECORD/PLAYBACK DEVICE

4- TO 8-MINUTES DURATION

Table of Contents

1 GENERAL DESCRIPTION

The ISD5008 ChipCorder product is a 3V fully-integrated, single-chip solution which provides seamless integration of enhanced voice record and playback features for digital cellular phones (GSM, CDMA, TDMA, PDC, and PHS), automotive communications, GPS/navigation systems, and portable communication products. This low-power, 3-volt device enables customers to quickly and easily integrate 4 to 8 minutes of voice storage features such as one-way or two-way (full duplex) call record, voice memo record, and call screening/answering machine functionality.

Like other ChipCorder products, the ISD5008 integrates the sampling clock, anti-aliasing and smoothing filters, and the Multi-Level Storage (MLS) array into a single chip. For enhanced voice features, the ISD5008 eliminates external circuitry mostly by also integrating automatic gain control (AGC), a power amplifier/speaker driver, volume control, summing amplifiers, analog switches, and a car kit interface. Input level adjustable amplifiers are also implemented, providing a flexible interface for multiple applications.

Duration/sample rate selection is accomplished via software, allowing customers to optimize quality and duration for various features within the same end product.

The ISD5008 device is designed for use in a microprocessor- or microcontroller-based system. Address, control, and duration selection are accomplished through a Serial Peripheral Interface (SPI) or Microwire Serial Interface to minimize pin count.

Recordings are stored into on-chip non-volatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through Nuvoton's patented MLS technology. Voice and audio signals are stored directly into solid-state memory in their natural, uncompressed form, providing superior quality voice and music reproduction.

2 FEATURES

Fully-Integrated Solution

- Single-chip voice record/playback solution
- Integrated sampling clock, anti-aliasing and smoothing filters, and MLS array
- Integrated analog features such as automatic gain control (AGC), audio gating switches, speaker driver, summing amplifiers, volume control, and AUX IN/AUX OUT interface (e.g., for car kits)

Low-Power Consumption

- Single +3 volt supply
- Operating current:
  - I_{CC_Play} = 15 mA (typical)
  - I_{CC_Rec} = 25 mA (typical)
  - $I_{CC\_Feedthru}$ = 12 mA (typical)
- Standby current:
  - I_{SB} = 1 µA (typical)
- Power consumption controlled by SPI or Microwire control register
- Most stages can be individually powered down for minimum power consumption

Enhanced Voice Features

- One or two-way (full duplex) conversation record (record signal summation)
- One- or two-way (full duplex) message playback (while on a call)
- Voice memo record and playback
- Private call screening
- Answering machine
- Personalized outgoing message (given caller ID information from host chip set)
- Private call announce while on call (given CIDCW information from host chip set)

Easy-to-Use and Control

- No compression algorithm development required
- User-selectable sampling rates of 8.0 kHz, 6.4 kHz, 5.3 kHz, or 4.0 kHz
- Microcontroller SPI or Microwire™ Serial Interface
- Fully addressable to handle multiple messages

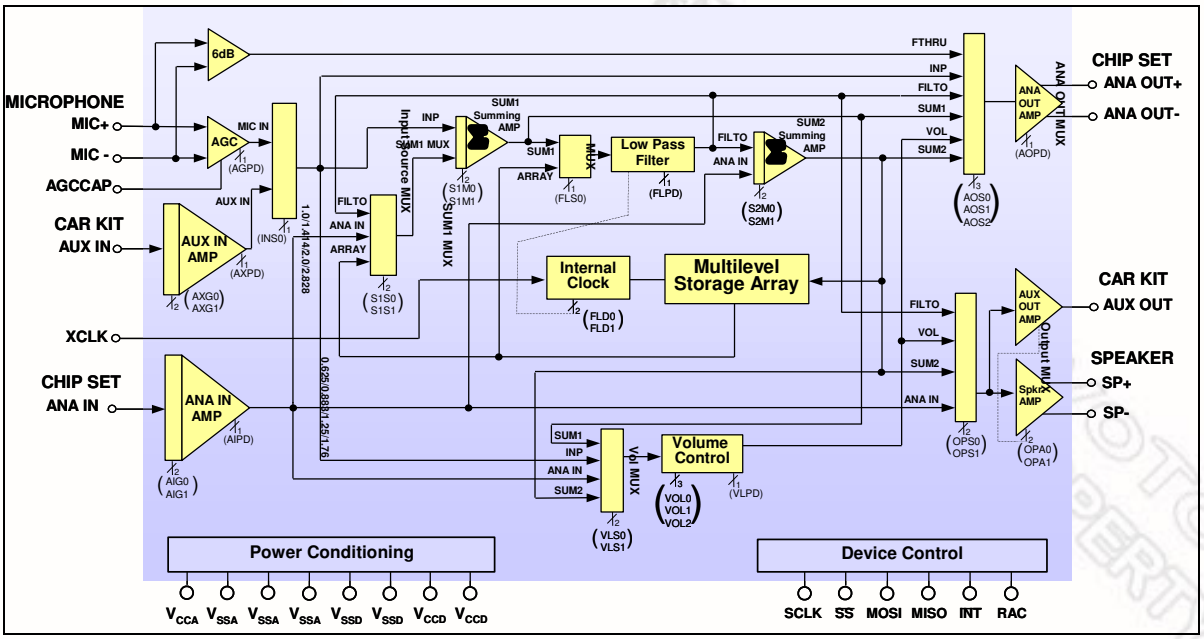
High Quality Solution

- High quality voice and music reproduction
- Standard 100-year message retention (typical)
- 100,000 record cycles (typical)

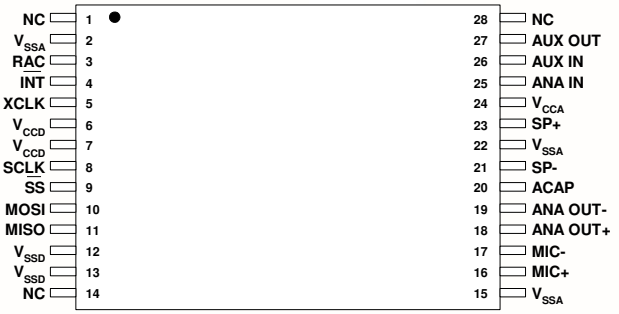
Options

- Available in die, PDIP, SOIC, TSOP, and chip scale packaging (CSP)
- Compact µBGA chip scale package available for portable applications
- Temperature : Commercial, Extended and Industrial

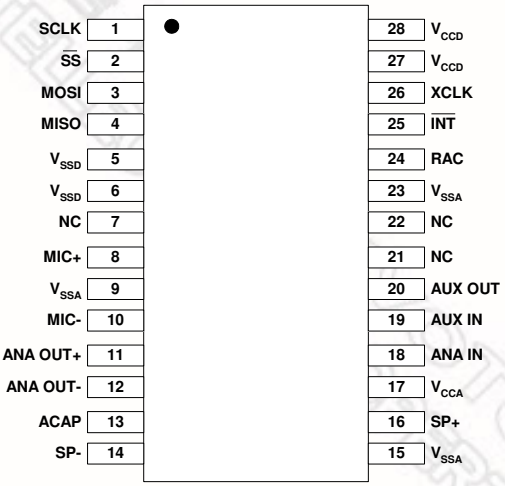
3 BLOCK DIAGRAM



4 PIN CONFIGURATION



TSOP



PDIP/SOIC

5 PIN DESCRIPTION

PIN NAME	PDIP/SOIC	TSOP	FUNCTION
SCLK	1	8	**Serial Clock**: The SCLK is the clock input to the ISD5008. Generated by the master microcontroller, the SCLK synchronizes data transfers in and out of the device through the MISO and MOSI lines.
$\overline{SS}$	2	9	**Slave Select**: This input, when LOW, selects the device.
MOSI	3	10	**Master Out Slave In**: MOSI is the serial data input to the ISD5008 device. The master microcontroller places data to be clocked into the ISD5008 device on the MOSI line one-half cycle before the rising edge of SCLK. Data is clocked into the device with LSB (Least Significant Bit) first.
MISO	4	11	**Master In Slave Out**: MISO is the serial data output of the ISD5008. Data is clocked out on the falling edge of SCLK. This output goes into a high-impedance state when the device is not selected. Data is clocked out of the device with LSB first.
V_{SSD} / V_{SSA}	5, 6 / 9, 15, 23	12, 13 / 2, 15, 22	**Ground**: The ISD5008 utilizes separate analog and digital ground busses. The analog ground (V_{SSA}) pins should be tied together as close to the package as possible and connected through a low-impedance path to power supply ground. The digital ground (V_{SSD}) pin should be connected through a separate low-impedance path to power supply ground. These ground paths should be large enough to ensure that the impedance between the V_{SSA} pins and the V_{SSD} pins is less than 3 Ω. The backside of the die is connected to V_{SSD} through the substrate resistance. In a chip-on-board design, the die attach area must be connected to V_{SSD}.
MIC+ / MIC-	8 / 10	16 / 17	**Microphone +/–**: The microphone inputs transfer the voice signal to the on-chip AGC preamplifier or directly to the ANA OUT MUX, depending on the selected path. The AGC circuit has a range of 45dB in order to deliver a nominal 694 mVp-p into the storage array from a typical electret microphone output of 2 to 20 mVp-p. The direct path to the ANA OUT MUX has a gain of 6dB so a 208 mVp-p signal across the differential microphone inputs would give 416 mVp-p across the ANA OUT pins. The input impedance is typically 10 kΩ.
ANAOUT+ / ANAOUT-	11 / 12	18 / 19	**Analog Outputs**: These differential outputs are designed to match to the microphone input of the telephone chip set. It is designed to drive a minimum of 5 kΩ between the "+" and "–" pins to a nominal voltage level of 700 mVp-p. Both pins have DC bias of approximately 1.2 VDC. The AC signal is superimposed upon this analog ground voltage. These pins can be used single-ended, getting only half the voltage. Do **NOT** ground the unused pin.

PIN NAME	PDIP/SOIC	TSOP	FUNCTION
ACAP	13	20	**AGC Capacitor**: This pin provides the capacitor connection for setting the parameters of the microphone AGC circuit. It should have a 4.7 µF capacitor connected to ground. **It cannot be floating.** This is because the capacitor is also used in the playback mode for the AutoMute circuit. This circuit reduces the amount of noise present in the output during quiet pauses. Tying this pin to ground gives maximum gain, or to V_{CCA} gives minimum gain for the AGC amplifier but will cancel the AutoMute function.
SP- / SP+	14 / 16	21 / 23	**Speaker Outputs**: This differential speaker output is designed to drive an 8Ω speaker up to a maximum power of 23.5 mW. This stage has two selectable gains, 1.32 and 1.6, which can be chosen through the configuration registers. These pins are biased to approximately 1.2 VDC and, if used single-ended, must be capacitively coupled to their load. Do **NOT** ground the unused pin.
V_{CCA} / V_{CCD}	17 / 27, 28	24 / 6, 7	**Power Supplies**: To minimize noise, the analog and digital circuits in the ISD5008 device uses separate power busses. These +3V busses lead to separate pins. Tie the V_{CCD} pins together as close as possible and decouple both supplies as near to the package as possible
ANA IN	18	25	**Analog Input**: The ANA IN pin is the analog input from the telephone chip set. It can be switched (by the SPI bus) to the speaker output, the array input or to various paths. This pin is designed to accept a nominal 1.11 Vp-p when at its minimum gain (6dB) setting. See Table 4. There is additional gain available in 3dB steps controlled from the SPI bus, if required, up to 15dB.
AUX IN	19	26	**Auxiliary Input**: The AUX IN is an additional audio input to the ISD5008, such as from the microphone circuit in a mobile phone “car kit.” This input has a nominal 700 mVp-p level at its minimum gain setting (0dB). See Table 5. Additional gain is available in 3 dB steps (controlled by the SPI bus) up to 9dB.
AUX OUT	20	27	**Auxiliary Output**: The AUXOUT is an additional audio output pin, to be used, for example, to drive the speaker circuit in a “car kit.” It drives a minimum load of 5 kΩ and up to a maximum of 1 Vp-p. The AC signal is superimposed on approximately 1.2 VDC bias and must be capacitively coupled to the load.

PIN NAME	PDIP/SOIC	TSOP	FUNCTION
RAC	24	3	**Row Address Clock**: RAC is an open drain output pin that marks the end of a row. At the 8 kHz sampling frequency, the duration of this period is 200 ms. There are 1,200 rows of memory in the ISD5008 devices. RAC stays HIGH for 175 ms and stays LOW for the remaining 25 ms before it reaches the end of the row. At the 8 kHz sampling frequency, the RAC pin remains HIGH for 109.38 µsec and stays LOW for 15.63 µsec under the Message Cueing mode. See Table 15 Timing Parameters for RAC timing information at other sample rates. When a record command is first initiated, the RAC pin remains HIGH for an extra T_{RACLO} period, to load sample and hold circuits internal to the device. The RAC pin can be used for message management techniques. A pull-up resistor is required to connect this pin to other device.
$\overline{INT}$	25	4	**Interrupt**: $\overline{INT}$ is an open drain output pin. The ISD5008 interrupt pin goes LOW and stays LOW when an Overflow (OVF), or End of Message (EOM) marker or Message Cueing is detected. The interrupt is cleared the next time an SPI cycle is completed. The interrupt status can be read by a RINT instruction that will give one of the two flags out the MISO line. A pull-up resistor is required to connect this pin to other device. ***OVF Flag***. The overflow flag indicates that the end of the ISD5008's analog memory has been reached during a record or playback operation. ***EOM Flag.*** The end of message flag is set only during playback, when an EOM is found. There are eight possible EOM markers per row.
XCLK	26	5	**External Clock**: The external clock input has an internal pull-down device. Normally, the ISD5008 is operated at one of four internal rates selected for its internal oscillator by the Sample Rate Select bits. If greater precision is required, the device can be clocked through the XCLK pin as described in Table 2. Because the anti-alising and smoothing filters track the Sample Rate Select bits, one must, for optimum performance, change the external clock AND the Sample Rate Configuration bits to one of the four values properly to set the filters to the correct cutoff frequency as described in Table 1. The duty cycle on the input clock is not critical, as the clock is immediately divided by two internally. If the XCLK is not used, this input should be connected to V_{SSD}.

6 FUNCTIONAL DESCRIPTION

6.1 DETAILED DESCRIPTION

6.1.1 Speech/Sound Quality

The ISD5008 ChipCorder product can be configured via software to operate at 4.0, 5.3, 6.4, or 8.0 kHz sampling frequency, allowing the user a choice of speech quality options. Increasing the duration decreases the sampling frequency and bandwidth, which affects sound quality. Table 1 shows the relationship between sampling frequency, duration and filter pass band.

The speech samples are stored directly into on-chip non-volatile memory without the digitization and compression associated with other solutions. Direct analog storage provides a natural sounding reproduction of voice, music, tones, and sound effects not available with most solid-state solutions.

6.1.2 Duration

To meet end system requirements, the ISD5008 device is a single-chip solution which provides from 4 to 8 minutes of voice record and playback, depending on the sample rates defined by customer software.

TABLE 1: SAMPLING RATE / DURATION / FILTER EDGE

Sample Rate (kHz)	Duration (Minutes)	Filter Pass Band* (kHz)
8	4.0	3.4
6.4	5.0	2.7
5.3	6.0	2.3
4	8.0	1.7

* -3dB point

6.1.3 Flash Storage

One of the benefits of Nuvoton's ChipCorder technology is the use of on-chip nonvolatile memory, which provides zero- power message storage. The message is retained for up to 100 years (typically) without power. In addition, the device can be re-recorded over 100,000 times (typically).

6.1.4 Microcontroller Interface

A four-wire (SCLK, MOSI, MISO, SS) SPI interface is provided for ISD5008 control, addressing functions, and sample rate selection. The ISD5008 is configured to operate as a peripheral slave device with a microcontroller-based SPI bus interface. Read/Write access to all the internal registers occurs through this SPI interface. An interrupt signal (INT) and internal read-only Status Register are provided for handshake purposes.

6.1.5 Memory Architecture

The ISD5008 device contains a total of 1,920K Flash memory cells, which is organized as 1,200 rows of 1,600 cells each. The duration is counted according to the number of rows, while the row number is represented by the related 16 address bits of MOSI as described in the SPI section.

6.1.6 Programming

The ISD5008 device is also ideal for playback-only applications, where single- or multiple-message playback is controlled through the SPI port. Once the desired message configuration is created, duplicates can easily be generated via a third-party programmer. For more information on available application tools and programmers, please see the Nuvoton website at www.Nuvoton-usa.com.

TABLE 2: EXTERNAL CLOCK INPUT

Duration (Minutes)	Sample Rate (kHz)	Required Clock (kHz)
4	8.0	1024
5	6.4	819.2
6	5.3	682.7
8	4.0	512

TABLE 3: INTERNAL SAMPLING RATE / FILTER EDGE

FLD1	FLD0	Sample Rate (kHz)	Filter Pass Band (kHz)
0	0	8	3.4
0	1	6.4	2.7
1	0	5.3	2.3
1	1	4	1.7

6.2 ANALOG FUNCTIONAL PINS

6.2.1 Mic+, Mic-

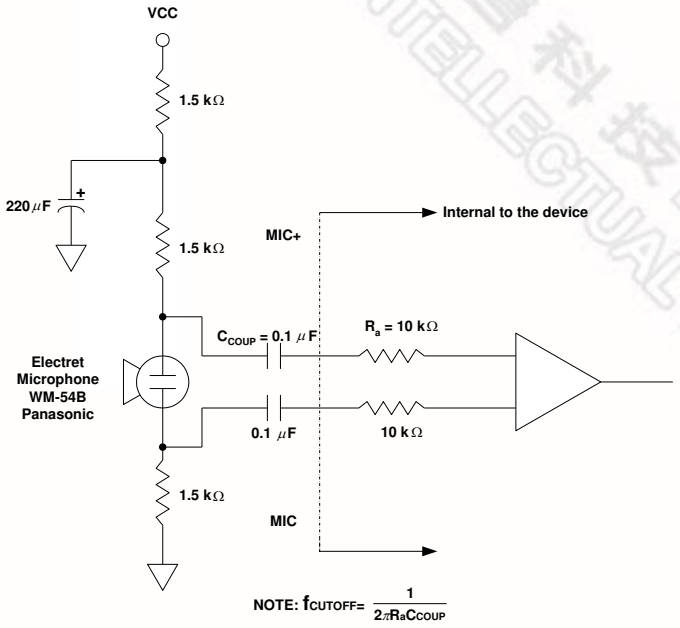
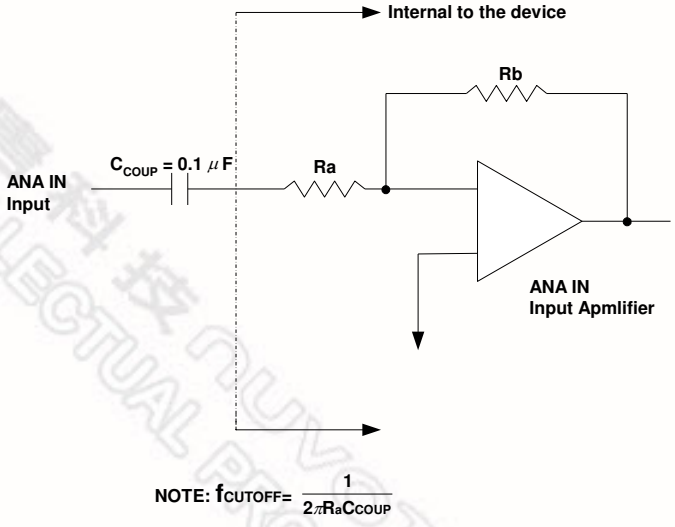


FIGURE 1: MICROPHONE INPUT

6.2.2 ANA IN (Analog Input)



Gain Setting	Resistor Ratio (Rb/Ra) kΩ/kΩ	Gain	Gain [2] (dB)
00	63.9/102	0.625	-4.1
01	77.9/88.1	0.88	-1.1
10	92.3/73.8	1.25	1.9
11	106/60	1.77	4.9

FIGURE 2: ANA IN INPUT MODES

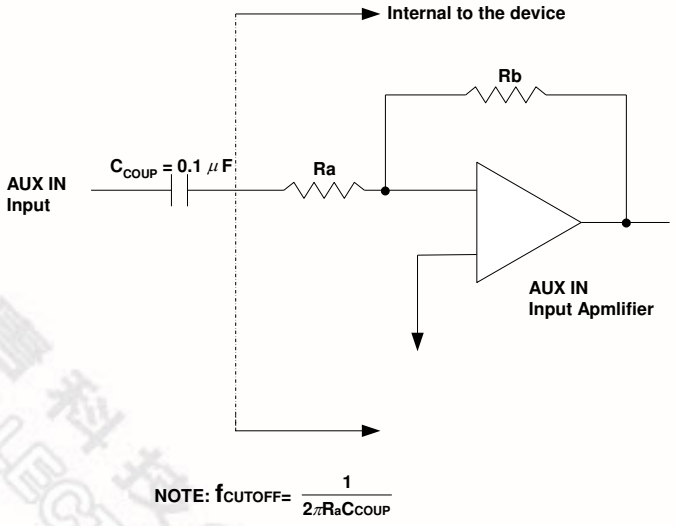
TABLE 4: ANA IN AMPLIFIER GAIN SETTINGS

Setting (1)	0TLP Input V_{PP} (3)	CFG0		Gain (2)	Array In/Out V_{PP}	Speaker Out V_{PP} (4)
		AIG1	AIG0			
6 dB	1.11	0	0	.625	.694	2.22
9 dB	.785	0	1	.883	.694	2.22
12 dB	.555	1	0	1.250	.694	2.22
15 dB	.393	1	1	1.767	.694	2.22

NOTES:

1. Gain from ANA IN to SP+ / _
2. Gain from ANA In to ARRAY IN
3. 0TLP Input is the reference Transmission Level Point that is used for testing. This level is typically 3 dB below clipping.
4. Speaker Out gain set to 1.6 (High). (Differential)

6.2.3 AUX IN (Auxillary Input)



Gain Setting	Resistor Ratio (Rb/Ra) kΩ/kΩ	Gain	Gain [2] (dB)
00	40.1/40.1	1	0
01	47.0/33.2	1.414	3
10	53.5/26.7	2	6
11	58.2/21.0	2.82	9

FIGURE 3: AUX IN INPUT MODES

TABLE 5: AUXIN AMPLIFIER GAIN SETTINGS

Setting (1)	0TLP Input V_{PP} (3)	CFG0		Gain (2)	Array In/Out V_{PP}	ANA OUT V_{PP} (4)
		AXG1	AXG0			
0 dB	.694	0	0	1.00	.694	.694
3 dB	.491	0	1	1.41	.694	.694
6 dB	.347	1	0	2.00	.694	.694
9 dB	.245	1	1	2.82	.694	.694

NOTES:

1. Gain from AUX IN to ANA OUT
2. Gain from AUX IN to ARRAY IN
3. 0TLP Input is the reference Transmission Level Point that is used for testing. This level is typically 3 dB below clipping.
4. Differential

6.2.4 ACAP (AGC Capacitor)

This pin provides the capacitor connection for setting the parameters of the microphone AGC circuit. It should have a 4.7 μF capacitor connected to ground. It cannot be left floating. This is because the capacitor is also used for the AutoMute circuit. This circuit reduces the amount of noises present in the output during quiet pauses. Tying this pin to ground gives maximum gain; to V_{CCA} gives minimum gain for the AGC amplifier but will cancel the AutoMute function.

6.3 INTERNAL FUNCTIONAL BLOCKS

FIGURE 7: MICROPHONE AMPLIFIER

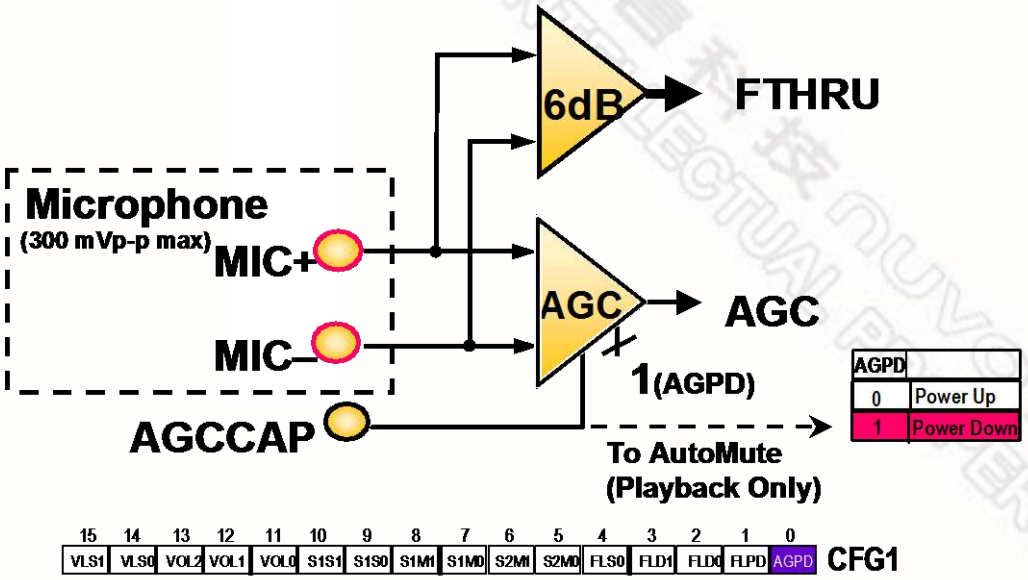


FIGURE 7: ANA IN and AUX IN

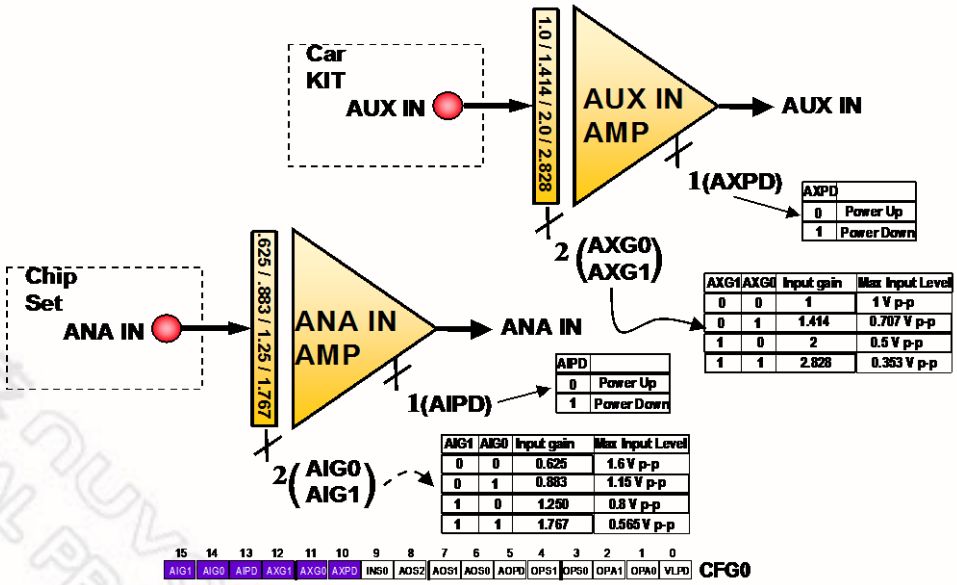


FIGURE 7: ISD5008 CORE (LEFT HALF)

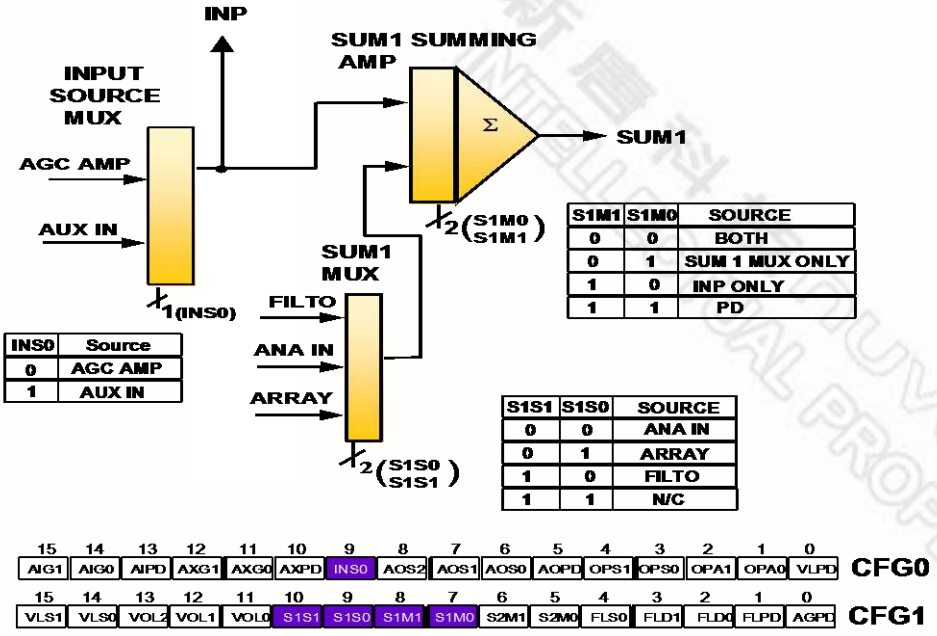


FIGURE 8: ISD5008 CORE (RIGHT HALF)

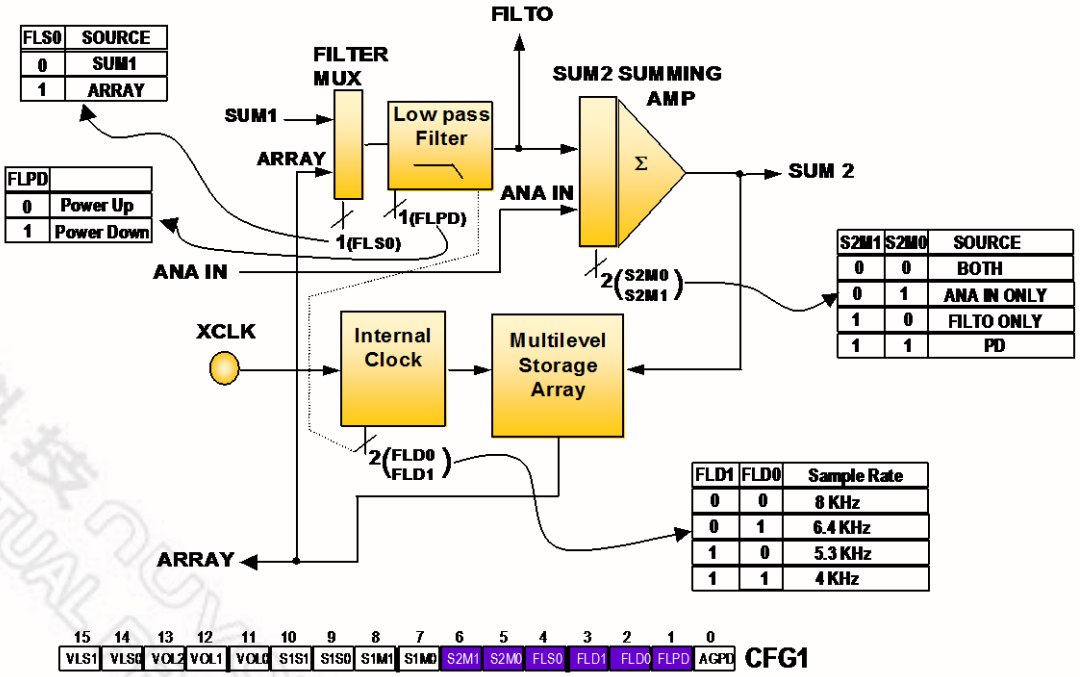


FIGURE 9: VOLUME CONTROL

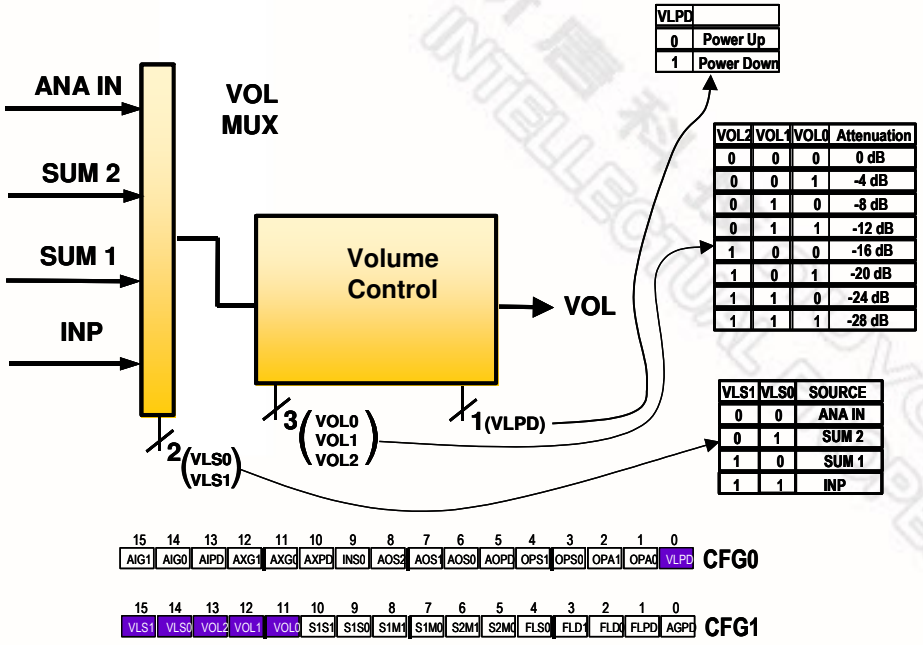


FIGURE 10: SPEAKER and AUX OUT

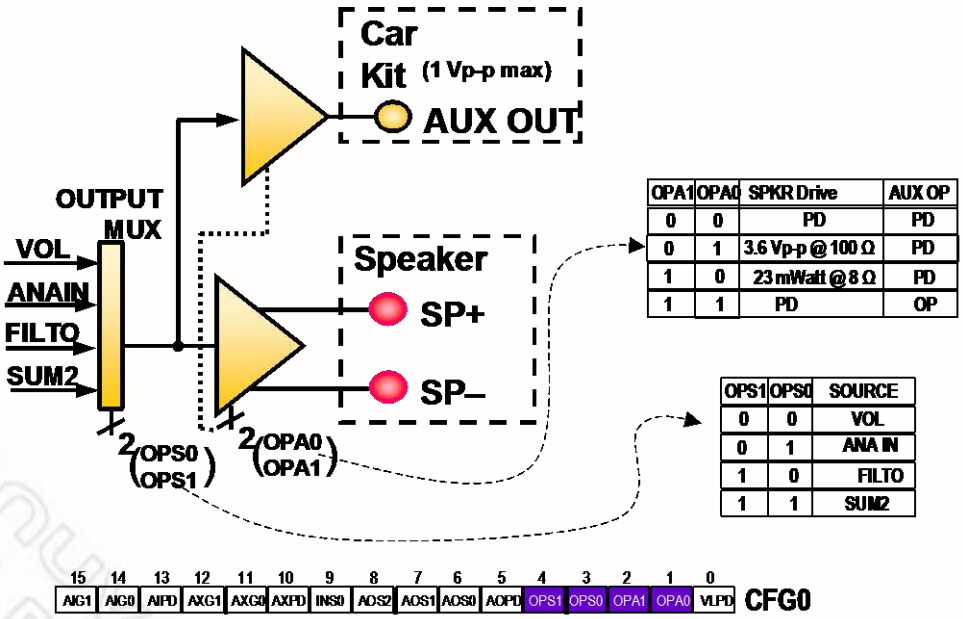
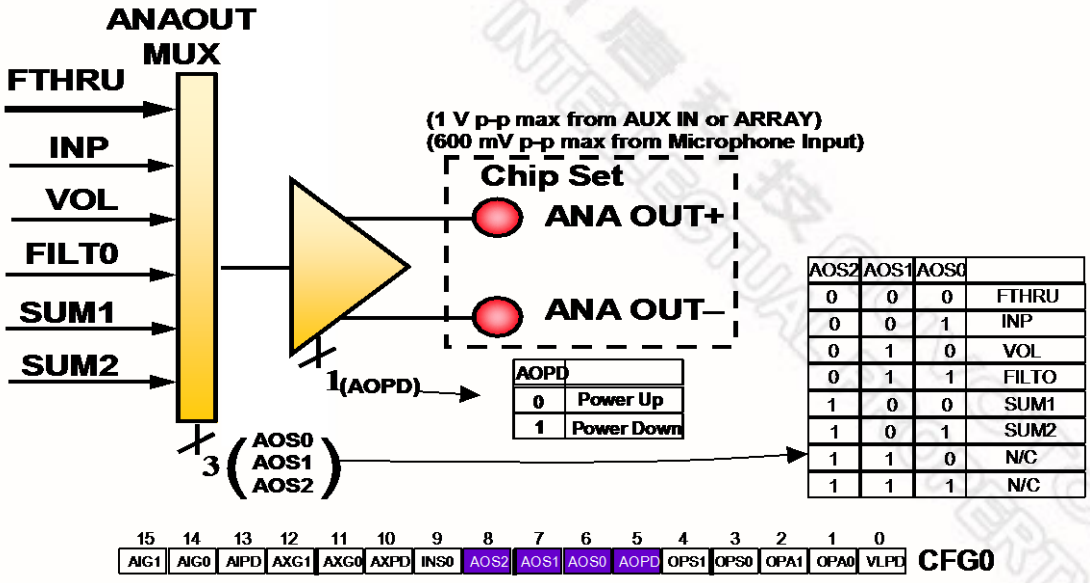


FIGURE 11: ANA OUT Output



6.4 SERIAL PERIPHERAL INTERFACE (SPI) DESCRIPTION

The ISD5008 product operates from a SPI serial interface, which operates with the following protocol:

The data transfer protocol assumes that the microcontroller's SPI shift registers are clocked on the falling edge of the SCLK. However, for the ISD5008, data is clocked into the MOSI pin at the rising clock edge, while data is clocked out onto the MISO pin at the falling clock edge.

1. All serial data transfers begin with the falling edge of SS pin.
2. SS is held LOW during all serial communications and held HIGH between instructions.
3. Data is clocked in on the rising clock edge and data is clocked out on the falling clock edge.
4. Play and Record operations are initiated by enabling the device by asserting the SS pin LOW, shifting in an opcode and an address field to the ISD5008 device (refer to the Opcode Summary of Table 6).
5. The opcodes and address fields are as follows: <8 control bits> and <16 address bits>.
6. Each operation that ends in an EOM or Overflow will generate an interrupt, including the Message Cueing cycles. The Interrupt will be cleared the next time an SPI cycle is completed.
7. As Interrupt data is shifted out of the ISD5008 MISO pin, control and address data is simultaneously being shifted into the MOSI pin. Care should be taken such that the data shifted in is compatible with current system operation. It is possible to read interrupt data and start a new operation within the same SPI cycle.
8. A record or playback operation begins with the RUN bit set and the operation ends with the RUN bit reset.
9. All operations begin with the rising edge of SS.

6.4.1 Message Cuing

Message cueing allows the user to skip through messages, without knowing the actual physical location of the message. This operation is used during playback. In this mode, the messages are skipped 1600 times faster than in normal playback mode. It will stop when an EOM marker is reached. Then, the internal address counter will point to the next message.

6.4.2 Opcodes

TABLE 6: OPCODE SUMMARY

Instruction	Opcode <8 bits> [1] Address <16 bits>	Operational Summary
POWERUP	0110 0000	Power-Up: Power-Up the device
LOADCFG0 [2]	01X0 0010 <D15-D0>	Loads a 16-bit value into Configuration Register 0
LOADCFG1	01X0 0100 <D15-D0>	Loads a 16-bit value into Configuration Register 1
SETPLAY	1110 0000 <A15-A0>	Initiates Playback from address <A15-A0>
PLAY	1111 0000	Playback from current address (until EOM or OVF)
SETREC	1010 0000 <A15-A0>	Initiates Record at address <A15-A0>
REC	1011 0000	Records from current address until OVF is reached
SETMC	1110 1000 <A15-A0>	Initiates Message Cueing (MC) from address <A15-A0>
MC	1111 1000	Performs a Message Cue. Proceeds to the end of the current message (EOM) or enters OVF condition if it reaches the end of the array.
STOP	0111 0000	Stops current operation
STOPWRDN	0101 0000	Stops current operation and enters stand-by (power-down) mode.
RINT	0111 0000	Read interrupt status bits: OVF and EOM.

NOTES:

[1] X = Don't Care.

[2] Changes in CFG0 are not recognized until CFG1 is loaded. The changes will occur at the rising edge of $\overline{SS}$ during the cycle that CFG1 is loaded.

6.4.3 Power-Up Sequence

The ISD5008 will be ready for an operation after T_{PUD} (25 ms approximately for 8 kHz sample rate). The user needs to wait T_{PUD} before issuing an instruction. Below are suggested playback and record examples for references.

6.4.3.1 Record Mode

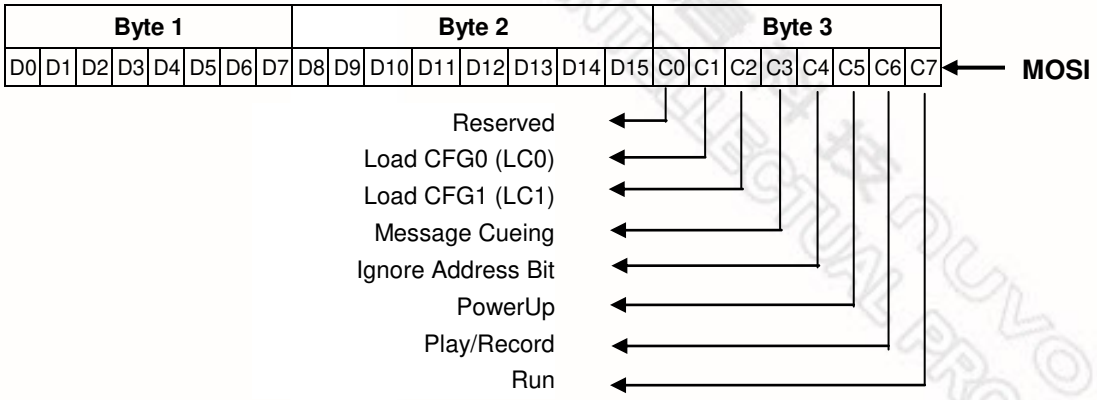
1. Send POWERUP command.
2. Wait T_{PUD} (power-up delay).
3. Send POWERUP command.
4. Wait 2 x T_{PUD} (power-up delay).
5. Load CFG0 and CFG1 for desired operation.
6. Wait $T_{PUD.}$
7. Send SETREC command with address xx, or send REC command.
8. Send STOP to halt the record operation or when the end of memory (OVF) is reached, then record stops automatically.
9. Wait $T_{Stop/Pause.}$.

6.4.3.2 Playback Mode

1. Send POWERUP command.
2. Wait T_{PUD} (power-up delay).
3. Load CFG0 and CFG1 for desired operation.
4. Wait $T_{PUD.}$
5. Send SETPLAY command with address xx, or send PLAY command.
6. Send STOP to halt the playback operation or wait until an EOM is reached, then playback stops automatically.
7. Wait $T_{Stop/Pause.}$.

6.4.4 SPI Port

The following diagram describes the SPI port and the control bits associated with it.



6.4.5 SPI Control Register

The SPI control register provides control of individual device functions such as Play, Record, Message Cueing, Power-Up and Power-Down, Start and Stop operations, Ignore Address Pointers and Load Configuration Registers.

TABLE 7: SPI CONTROL REGISTER

Control Register	Bit	Device Function
RUN		Enable or Disable an operation
=	1	Start
=	0	Stop
P/$\overline{R}$		Selects Play or Record operation
=	1	Play
=	0	Record
MC		Enable or Disable Message Cueing
=	1	Enable Message Cueing
=	0	Disable Message Cueing
LC0		
=	1	Load Configuration Reg 0
=	0	No Load

Control Register	Bit	Device Function
PU		Master power control
=	1	Power-Up
=	0	Power-Down
IAB		Ignore address control bit
=	1	Ignore input address register (A15-A0)
=	0	Use the input address register contents for an operation (A15-A0)
A15-A0		Output of the row pointer register
D15-D0		Input control and address register
LC1		
=	1	Load Configuration Reg 1
=	0	No Load

TABLE 8: CONFIGURATION REGISTER 0

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	CFGO
AIG1	AIG0	AIPD	AXG1	AXG0	AXPD	INS0	AOS2	AOS1	AOS0	AOPD	OPS1	OPS0	OPA1	OPA0	VLPD	
ANA IN AMP Gain SET (2 bits)		ANA IN Power Down	AUX IN AMP Gain SET (2 bits)		AUX IN Power Down	INPUT SOURCE MUX Select (1 bit)	ANA OUT MUX Select (3 bits)			ANA OUT Power Down	OUTPUT MUX Select (2 bits)		SPKR & AUX OUT Control (2 bits)		Volume Control Power Down	

NOTE: See details on following pages

TABLE 9: CONFIGURATION REGISTER 1

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	CFG1
VLS1	VLS0	VOL2	VOL1	VOL0	S1S1	S1S0	S1M1	S1M0	S2M1	S2M0	FLSO	FLD1	FLD0	FLPD	AGPD	
VOLUME CONT. MUX Select (2 bits)		VOLUME CONTROL (3 bits)			SUM 1 MUX Select (2 bits)		SUM 1 SUMMING AMP Control (2 bits)		SUM 2 SUMMING AMP Control (2 bits)		FILTER MUX Select	SAMPLE RATE (& Filter) Set Up (2 bits)		Filter Power Down	AGC AMP Power Down	

NOTE: See details on following pages

Detail of Configuration Register 0		
Volume Control Power Bit	Bit 0 (VLPD)	0 = Power ON 1 = Power OFF
SPEAKER and AUX OUT Control Bits	Bits 2,1 (OPA1, OPA0)	00 = Power down SPKR and AUX 01 = SPKR ON, HIGH GAIN, AUX Power down 10 = SPKR ON, LOW GAIN, AUX Power down 11 = SPKR Powered down, AUX ON
OUTPUT MUX Con trol Bits	Bits 4,3 (OPS1, OPS0)	00 = Source is VOL CONTROL (VOL) 01 = Source is ANA IN Input (ANA IN AMP) 10 = Source is LOW PASS FILTER (FILT0) 11 = Source is SUM2 SUMMING AMP (SUM2)
ANA OUT Power Bit	Bit 5 (AOPD)	0 = Power ON 1 = Power OFF
ANA OUT MUX Con trol Bits	Bits 8,7,6 (AOS2, AOS1, AOS0)	000 = Source is MICROPHONE AMP (FTHRU) 001 = Source is INPUT MUX (INP) 010 = Source is VOLUME CONTROL (VOL) 011 = Source is LOW PASS FILTER (FILT0) 100 = Source is SUM1 SUMMING AMP (SUM1) 101 = Source is SUM2 SUMMING AMP (SUM2) 110 = Unused 111 = Unused
INPUT SOURCE MUX Control Bit	Bit 9 (INS0)	0 = Source is Microphone AGC AMP (AGC) 1 = Source is AUX IN Input (AUX IN AMP)
AUX IN AMP Power Bit	Bit 10 (AXPD)	0 = Power ON 1 = Power OFF
AUX IN AMP Control Bits	Bits 12,11 (AXG1, AXG0)	00 = Input Gain = 1, OTLP input Level = 0.694 01 = Input Gain = 1.414, OTLP input Level = 0.491 10 = Input Gain = 2, OTLP input Level = 0.347 11 = Input Gain = 2.828, OTLP input Level = 0.245
ANA IN AMP Power Bit	Bit 13 (AIPD)	0 = Power ON 1 = Power OFF
ANA IN AMP Control Bits	Bits 15,14 (AIG1, AIG0)	00 = Input Gain = 0.625, OTLP input Level = 1.11 01 = Input Gain = 0.883, OTLP input Level = 0.7I85 10 = Input Gain = 1.250, OTLP input Level = 0.555 11 = Input Gain = 1.767, OTLP input Level = 0.393

Detail of Configuration Register 1		
AGC Power Control Bit	Bit 0 (AGPD)	0 = Power ON 1 = Power OFF
LOW PASS FILTER Power Control Bit	Bit 1 (FLPD)	0 = Power ON 1 = Power OFF
SAMPLE RATE and LOW PASS FILTER Control Bits	Bits 3,2 (FLD1, FLD0)	00 = Sample Rate = 8 KHz, FPB = 3.4 KHz 01 = Sample Rate = 6.4 KHz, FPB = 2.7 KHz 10 = Sample Rate = 5.3 KHz, FPB = 2.3 KHz 11 = Sample Rate = 4 KHz, FPB = 1.7 KHz
FILTER MUX Control bits	Bit 4 (FLS0)	0 = Source is SUM1 SUMMING AMP (SUM1) 1 = Source is Analog Memory Array (ARRAY)
SUM 2 SUMMING AMP Control Bits	Bits 6,5 (S2M1, S2M0)	00 = Source is both ANA IN AMP and FILT0 01 = Source is ANA IN Input (ANA IN AMP) ONLY 10 = Source is LOW PASS FILTER (FILT0) ONLY 11 = Power Down SUM2 SUMMING AMP
SUM1 SUMMING AMP Control Bits	Bit 8,7 (S1M1, S1M0)	00 = Source is both SUM1 and INP 01 = Source is SUM1 SUMMING AMP (SUM1) ONLY 10 = Source is INPUT MUX (INP) ONLY 11 = Power Down SUM1 SUMMING AMP
SUM1MUX Control Bits	Bit 10,9 (S1S1, S1S0)	00 = Source is ANA IN Input (ANA IN AMP) 01 = Source is Analog Memory Array (ARRAY) 10 = Source is LOW PASS FILTER (FILT0) 11 = UNUSED
VOLUME CONTROL Control Bits	Bits 13,12,11 (VOL2, VOL1, VOL0)	000 = Attenuation = 0 dB 001 = Attenuation = 4 dB 010 = Attenuation = 8 dB 011 = Attenuation = 12 dB 100 = Attenuation = 16 dB 101 = Attenuation = 20 dB 110 = Attenuation = 24 dB 111 = Attenuation = 28 dB
VOL MUX Control Bits	Bit 15,14 (VLS1, VLS0)	00 = Source is ANA IN Input (ANA IN AMP) 01 = Source is SUM2 SUMMING AMP (SUM2) 10 = Source is SUM1 SUMMING AMP (SUM1) 11 = Source is INPUT MUX (INP)

Configuration Register Notes

1. ***Important***: All changes to the internal settings of the ISD5008 are synchronized with the load of Configuration Register 1. A command to load Configuration Register 1 immediately transfers the input data to the internal settings of the device and the changes take place immediately at the end of the command when $\overline{SS}$ goes HIGH. A load to Configuration Register 0 sends the new data to