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# ISD Cortex™-M0 ChipCorder

# ISD9160 Technical Reference Manual



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***Table of Contents-***

# 1 GENERAL DESCRIPTION

The ISD9160 is a system-on-chip product optimized for low power, audio record and playback with an embedded ARM® Cortex™-M0 32-bit microcontroller core.

The ISD9160 embeds a Cortex™-M0 core running up to 50 MHz with 145K-byte of non-volatile flash memory and 12K-byte of embedded SRAM. It also comes equipped with a variety of peripheral devices, such as Timers, Watchdog Timer (WDT), Real-time Clock (RTC), Peripheral Direct Memory Access (PDMA), a variety of serial interfaces (UART, SPI/SSP, $I^2C$, $I^2S$), PWM modulators, GPIO, Analog Comparator, Low Voltage Detector and Brown-out detector.

The ISD9160 comes equipped with a rich set of power saving modes including a Deep Power Down (DPD) mode drawing less than 1μA. A micro-power 16KHz oscillator can periodically wake up the device from deep power down to check for other events. A Standby Power Down (SPD) mode can maintain a real time clock function at less than 10 μA.

For audio functionality the ISD9160 includes a Sigma-Delta ADC with 92dB SNR performance coupled with a Programmable Gain Amplifier (PGA) capable of a maximum gain of 61dB to enable direct connection of a microphone. Audio output is provided by a Differential Class D amplifier (DPWM) that can deliver 1W of power to an 8Ω speaker.

The ISD9160 provides eight analog enabled general purpose IO pins (GPIO). These pins can be configured to connect to an analog comparator, can be configured as analog current sources or can be routed to the SDADC for analog conversion. They can also be used as a relaxation oscillator to perform capacitive touch sensing.

# 2 FEATURES

- Core
  - ARM® Cortex™-M0 core runs up to 50MHz.
  - One 24-bit System tick timer for operating system support.
  - Supports a variety of low power sleep and power down modes.
  - Single-cycle 32-bit hardware multiplier.
  - NVIC (Nested Vector Interrupt Controller) for 32 interrupt inputs, each with 4-levels of priority.
  - Serial Wire Debug (SWD) supports with 2 watchpoints/4 breakpoints.
- Power Management
  - Wide operating voltage range from 2.4V to 5.5V.
  - Power management Unit (PMU) providing four levels of power control.
  - Deep Power Down (DPD) mode with sub micro-amp leakage (<1μA).
  - Wakeup from Deep Power Down via dedicated WAKEUP pin or timed operation from internal low power 16KHz oscillator.
  - Standby mode with limited RAM retention and RTC operation (<10μA).
  - Wakeup from Standby can be from any GPIO interrupt, RTC or BOD.
  - Sleep mode with minimal dynamic power consumption.
  - 3V LDO for operation of external 3V devices such as serial flash.
- Flash EPROM Memory
  - 145K bytes Flash EPROM for program code and data storage.
  - 4KB of flash can be configured as boot sector for ISP loader.
  - Support In-system program (ISP) and In-circuit program (ICP) application code update
  - 1K byte page erase for flash
  - Configurable boundary to delineate code and data flash.
  - Support 2 wire In-circuit Programming (ICP) update from SWD ICE interface
- SRAM Memory
  - 12K bytes embedded SRAM.
- Clock Control
  - One high speed and two low speed oscillators providing flexible selection for different applications. No external components necessary.
  - Built-in trimmable oscillator with range of 16-50MHz. Factory trimmed within 1% to settings of 49.152MHz and 32.768MHz. User trimmable with in-built frequency measurement block (OSCFM) using reference clock of 32kHz crystal or external reference source.
  - Ultra-low power (<1uA) 16KHz oscillator for watchdog and wakeup from power-down or sleep operation.
  - External 32kHz crystal input for RTC function and low power system operation.
- GPIO
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable.
  - I/O pin can be configured as interrupt source with edge/level setting.
  - Switchable pull-up.
- Audio Analog to Digital converter
  - Sigma Delta ADC with configurable decimation filter and 16 bit output.
  - 92dB Signal-to-Noise (SNR) performance.
  - Programmable gain amplifier with 32 steps from -12 to 35.25dB in 0.75dB steps.
  - Boost gain stage of 26dB, giving maximum total gain of 61dB.
  - Input selectable from dedicated MIC pins or analog enabled GPIO.
  - Programmable biquad filter to support multiple sample rates from 8-32kHz.

- DMA support for minimal CPU intervention.

- Differential Audio PWM Output (DPWM)
  - Direct connection of speaker
  - 1W drive capability into 8Ω load.
  - High efficiency 88%
  - Configurable up-sampling to support sample rates from 8-32kHz.
  - DMA support for minimal CPU intervention.

- Timers
  - Two timers with 8-bit pre-scaler and 24-bit resolution.
  - Counter auto reload.

- Watch Dog Timer
  - Default ON/OFF by configuration setting
  - Multiple clock sources
  - 8 selectable time out period from micro seconds to seconds (depending on clock source)
  - WDT can wake up power down/sleep.
  - Interrupt or reset selectable on watchdog time-out.

- RTC
  - Real Time Clock counter (second, minute, hour) and calendar counter (day, month, year)
  - Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Time tick and alarm interrupts.
  - Device wake up function.
  - Supports software compensation of crystal frequency by compensation register (FCR)

- PWM/Capture
  - Built-in up to two 16-bit PWM generators provide two PWM outputs or one complementary paired PWM outputs.
  - The PWM generator equipped with a clock source selector, a clock divider, an 8-bit pre-scaler and Dead-Zone generator for complementary paired PWM.
  - PWM interrupt synchronous to PWM period.
  - 16-bit digital Capture timers (shared with PWM timers) provide rising/falling capture inputs.
  - Support Capture interrupt

- UART
  - UART ports with flow control (TX, RX, CTS and RTS)
  - 8-byte FIFO.
  - Support IrDA (SIR) and LIN function
  - Programmable baud-rate generator up to 1/16 of system clock.

- SPI
  - Master up to 20 Mbps / Slave up to 10 Mbps.
  - Support MICROWIRE/SPI master/slave mode (SSP)
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - 2 slave/device select lines when used in master mode.
  - Hardware CRC calculation module available for CRC calculation of data stream.
  - DMA support for burst transfers.

- I2C
  - Master/Slave up to 1Mbit/s
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master).
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus

  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
  - Programmable clock allowing versatile rate control.
  - I2C-bus controller supports multiple address recognition.

- $I^2S$
  - Interface with external audio CODEC.
  - Operate as either master or slave.
  - Capable of handling 8, 16, 24 and 32 bit word sizes
  - Mono and stereo audio data supported
  - $I^2S$ and MSB justified data format supported
  - Two 8 word FIFO data buffers are provided, one for transmit and one for receive
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports DMA requests, for transmit and receive

- Brown-out detector
  - With 8 levels: 2.1V, 2.2V, 2.4V, 2.5V, 2.625V, 2.8V, 3.0V, and 4.6V
  - Supports time-multiplex operation to minimize power consumption.
  - Supports Brownout Interrupt and Reset option

- Built in Low Dropout Voltage Regulator (LDO)
  - Capable of delivering 30mA load current.
  - Configurable for output voltage of 1.8V, 2.4V, 3.0V and 3.3V
  - Eight GPIO (GPIOA<7:0>) operate from LDO voltage domain allowing direct interface to, for example, 3V SPI Flash.
  - Can be bypassed and voltage domain supplied directly from system power.

- Additional Features
  - Over temperature alarm. Can generate interrupt if device exceeds safe operating temperature.
  - Temperature proportional voltage source which can be routed to ADC for temperature measurements.
  - Digital Microphone interface.

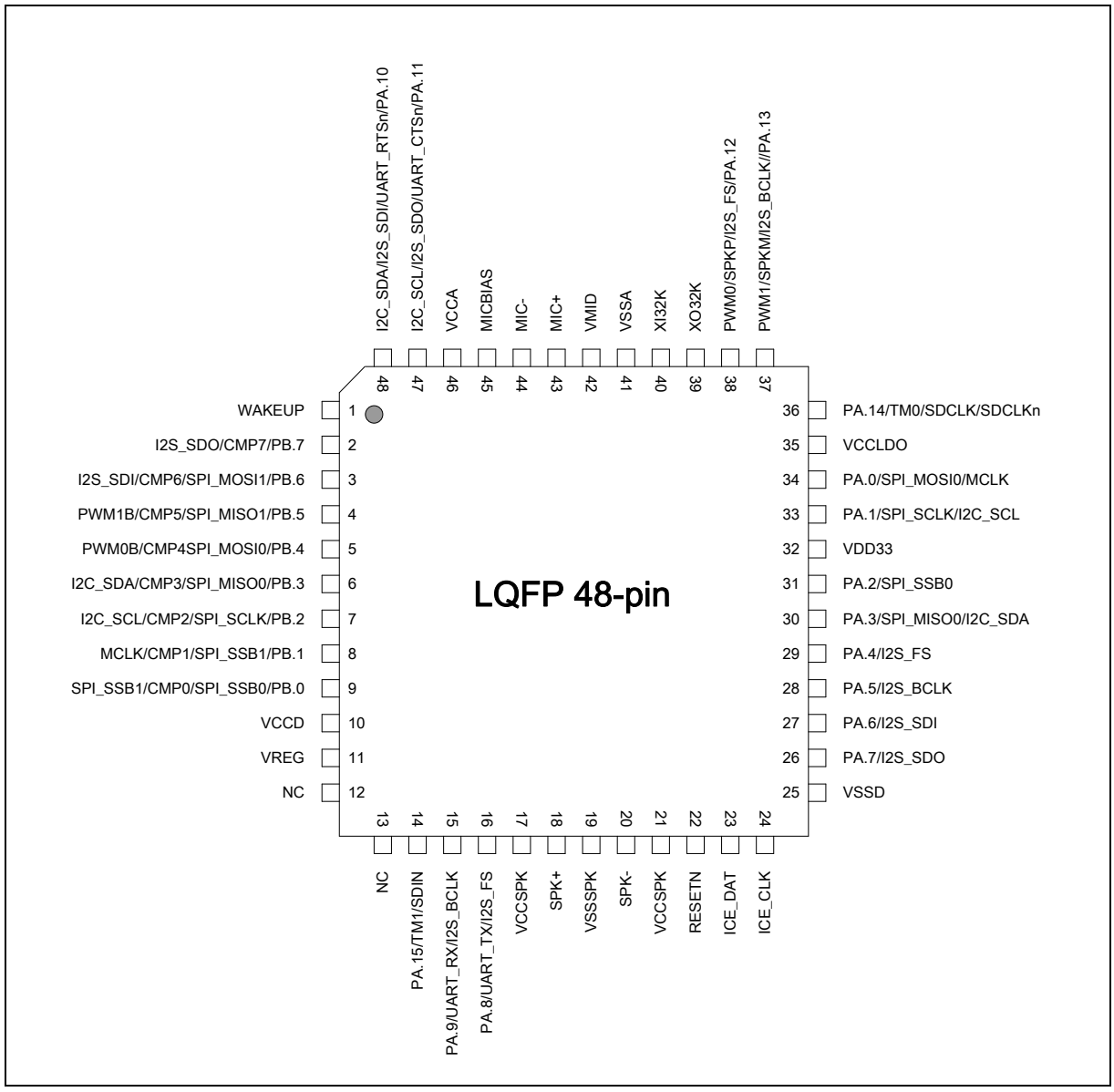
- Operating Temperature: -40C~85C

- Package:
  - All Green package (RoHS)
    - LQFP 48-pin

# 3 PART INFORMATION AND PIN CONFIGURATION

## 3.1 Pin Configuration

### 3.1.1 ISD9160 LQFP 48 pin




### 3.1.2 Pin Description

The ISD9160 is a low pin count device where many pins are configurable to alternative functions. All General Purpose Input/Output (GPIO) pins can be configured to alternate functions as described in the table below and also in **Error! Reference source not found.** and **Error! Reference source not found.**.

| Pin No. LQFP 48 | Pin Name | Pin Type | Alt CFG | Description |
|---|---|---|---|---|

| Pin No. LQFP 48 | Pin Name | Pin Type | Alt CFG | Description |
|---|---|---|---|---|
| 1 | WAKEUP | **I** | | Pull low to wake part from deep power down |
| 2 | PB.7 | **A/I/O** | 0 | General purpose input/output pin, analog capable; Port B, bit 7 |
| | I2S_SDO | **O** | 1 | Serial Data Output for I2S interface |
| | CMP7 | **AIO** | 2 | Configure as relaxation oscillator for capacitive touch sensing |
| 3 | PB.6 | **A/I/O** | 0 | General purpose input/output pin, analog capable; Port B, bit 6 |
| | I2S_SDI | **I** | 1 | Serial Data Input for I2S interface |
| | CMP6 | **AIO** | 2 | Configure as relaxation oscillator for capacitive touch sensing |
| | SPI_MOSI1 | **O** | 3 | Master Out, Slave In channel 1 for SPI interface |
| 4 | PB.5 | **A/I/O** | 0 | General purpose input/output pin, analog capable; Port B, bit 5 |
| | PWM1B | **O** | 1 | PWM channel 1 complementary output pin |
| | CMP5 | **AIO** | 2 | Configure as relaxation oscillator for capacitive touch sensing |
| | SPI_MISO1 | **I** | 3 | Master In, Slave Out channel 1 for SPI interface |
| 5 | PB.4 | **A/I/O** | 0 | General purpose input/output pin, analog capable; Port B, bit 4 |
| | PWM0B | **O** | 1 | PWM channel 0 complementary output pin |
| | CMP4 | **AIO** | 2 | Configure as relaxation oscillator for capacitive touch sensing |
| | SPI_MOSI0 | **O** | 3 | Master Out, Slave In channel 0 for SPI interface |
| 6 | PB.3 | **A/I/O** | 0 | General purpose input/output pin, analog capable; Port B, bit 3 |
| | I2C_SDA | **I/O** | 1 | Serial Data, I2C interface |
| | CMP3 | **AIO** | 2 | Configure as relaxation oscillator for capacitive touch sensing |
| | SPI_MISO0 | **I** | 3 | Master In, Slave Out channel 0 for SPI interface |
| 7 | PB.2 | **A/I/O** | 0 | General purpose input/output pin, analog capable; Port B, bit 2 |
| | I2C_SCL | **I/O** | 1 | Serial Clock, I2C interface |
| | CMP2 | **AIO** | 2 | Configure as relaxation oscillator for capacitive touch sensing |
| | SPI_SCLK | **I/O** | 3 | Serial Clock for SPI interface |
| 8 | PB.1 | **A/I/O** | 0 | General purpose input/output pin, analog capable; Port B, bit 1. Triggers external interrupt 1 (EINT1/IRQ3) |
| | MCLK | **O** | 1 | Master clock output for synchronizing external device |
| | CMP1 | **AIO** | 2 | Configure as relaxation oscillator for capacitive touch sensing |
| | SPI_SSB1 | **O** | 3 | Slave Select Bar 1 for SPI interface |
| 9 | PB.0 | **A/I/O** | 0 | General purpose input/output pin, analog capable; Port B, bit 0. Triggers external interrupt 0 (EINT0/IRQ2) |
| | SPI_SSB1 | **O** | 3 | Slave Select Bar 1 for SPI interface |

| Pin No. LQFP 48 | Pin Name | Pin Type | Alt CFG | Description |
|---|---|---|---|---|
| | CMP0 | **AIO** | 2 | Configure as relaxation oscillator for capacitive touch sensing |
| | SPI_SSB0 | **I/O** | 3 | Slave Select Bar 0 for SPI interface |
| 10 | VCCD | **P** | | Main Digital Supply for Chip. Supplies all IO except analog, Speaker Driver and PA<7:0> |
| 11 | VREG | **P** | | Logic regulator output decoupling pin. A 1µF capacitor returning to VSSD must be placed on this pin. |
| 12 | NC | | | Should remain unconnected. |
| 13 | NC | | | Should remain unconnected. |
| 14 | PA.15 | **I/O** | 0 | General purpose input/output pin; Port A, bit 15 |
| | TM1 | **I** | 1 | External input to Timer 1 |
| | SDIN | **I** | 2 | Sigma Delta bit stream input for digital MIC mode |
| 15 | PA.9 | **I/O** | 0 | General purpose input/output pin; Port A, bit 9 |
| | UART_RX | **I** | 1 | Receive channel of UART |
| | I2S_BCLK | **I/O** | 2 | Bit Clock for I2S interface |
| 16 | PA.8 | **I/O** | 0 | General purpose input/output pin; Port A, bit 8 |
| | UART_TX | **O** | 1 | Transmit channel of UART |
| | I2S_FS | **I/O** | 2 | Frame Sync Clock for I2S interface |
| 17 | VCCSPK | **P** | | Power Supply for PWM Speaker Driver |
| 18 | SPK+ | **O** | | Positive Speaker Driver Output |
| 19 | VSSSPK | **P** | | Ground for PWM Speaker Driver |
| 20 | SPK- | **O** | | Negative Speaker Driver Output |
| 21 | VCCSPK | **P** | | Power Supply for PWM Speaker Driver |
| 22 | RESETN | **I** | | External reset input. Pull this pin low to reset device to initial state. Has internal weak pull-up. |
| 23 | ICE_DAT | **I/O** | | Serial Wire Debug port data pin. Has internal weak pull-up. |
| 24 | ICE_CLK | **I** | | Serial Wire Debug port clock pin. Has internal weak pull-up. |
| 25 | VSSD | **P** | | Digital Ground. |
| 26 | PA.7 | **I/O** | 0 | General purpose input/output pin; Port A, bit 7 |
| | I2S_SDO | **O** | 1 | Serial Data Out for I2S interface |
| 27 | PA.6 | **I/O** | 0 | General purpose input/output pin; Port A, bit 6 |
| | I2S_SDI | **I** | 1 | Serial Data In for I2S interface |
| 28 | PA.5 | **I/O** | 0 | General purpose input/output pin; Port A, bit 5 |
| | I2S_BCLK | **I/O** | 1 | Bit Clock for I2S interface |

| Pin No. LQFP 48 | Pin Name | Pin Type | Alt CFG | Description |
|---|---|---|---|---|
| 29 | PA.4 | **I/O** | 0 | General purpose input/output pin; Port A, bit 4 |
| | I2S_FS | **I/O** | 1 | Frame Sync Clock for I2S interface |
| 30 | PA.3 | **I/O** | 0 | General purpose input/output pin; Port A, bit 3 |
| | SPI_MISO0 | **I** | 1 | Master In, Slave Out channel 0 for SPI interface |
| | I2C_SDA | **I/O** | 2 | Serial Data, I2C interface |
| 31 | PA.2 | **I/O** | 0 | General purpose input/output pin; Port A, bit 2 |
| | SPI_SSB0 | **I/O** | 1 | Slave Select Bar 0 for SPI interface |
| 32 | VDD33 | **P** | | LDO Regulator Output. If used, a 1µF capacitor must be placed to ground. If not used then tie to VCCD. |
| 33 | PA.1 | **I/O** | 0 | General purpose input/output pin; Port A, bit 1 |
| | SPI_SCLK | **I/O** | 1 | Serial Clock for SPI interface |
| | I2C_SCL | **I/O** | 2 | Serial Clock, I2C interface |
| 34 | PA.0 | **I/O** | 0 | General purpose input/output pin; Port A, bit 2 |
| | SPI_MOSI0 | **O** | 1 | Master Out, Slave In channel 0 for SPI interface |
| | MCLK | **O** | 2 | Master clock output. |
| 35 | VCCLDO | **P** | | Power Supply for LDO, should be connected to VCCD |
| 36 | PA.14 | **I/O** | 0 | General purpose input/output pin; Port A, bit 14 |
| | TM0 | **I** | 1 | External input to Timer 0 |
| | SDCLK | **O** | 1 | Clock output for digital microphone mode. |
| | SDCLKn | **O** | 2 | Inverse Clock output for digital microphone mode. |
| 37 | PA.13 | **I/O** | 0 | General purpose input/output pin; Port A, bit 13 |
| | PWM1 | **O** | 1 | PWM1 Output. |
| | SPKM | **O** | 2 | Equivalent to SPK-. |
| | I2S_BCLK | **I/O** | 3 | Bit Clock for I2S interface |
| 38 | PA.12 | **I/O** | 0 | General purpose input/output pin; Port A, bit 12 |
| | PWM0 | **O** | 1 | PWM0 Output. |
| | SPKP | **O** | 2 | Equivalent to SPK+ |
| | I2S_FS | **I/O** | 3 | Frame Sync Clock for I2S interface |
| 39 | XO32K | **O** | | 32.768kHz Crystal Oscillator Output |
| 40 | XI32K | **I** | | 32.768kHz Crystal Oscillator Input. Max Voltage 1.8V |
| 41 | VSSA | **AP** | | Ground for analog circuitry. |
| 42 | VMID | **O** | | Mid rail reference. Connect 4.7µF to VSSA. |

| Pin No. LQFP 48 | Pin Name | Pin Type | Alt CFG | Description |
|---|---|---|---|---|
| 43 | MIC+ | **AI** | | Positive microphone input. |
| 44 | MIC- | **AI** | | Negative microphone input. |
| 45 | MICBIAS | **AO** | | Microphone bias output. |
| 46 | VCCA | **AP** | | Analog power supply. |
| 47 | PA.11 | **I/O** | 0 | General purpose input/output pin; Port A, bit 11 |
| | I2C_SCL | **I/O** | 1 | Serial Clock, I2C interface |
| | I2S_SDO | **O** | 2 | Serial Data Out I2S interface |
| | UART_CTSn | **I** | 3 | UART Clear to Send Input. |
| 48 | PA.10 | **I/O** | 0 | General purpose input/output pin; Port A, bit 10 |
| | I2C_SDA | **I/O** | 1 | Serial Data, I2C interface |
| | I2S_SDI | **I** | 2 | Serial Data In I2S interface |
| | UART_RTSn | **O** | 3 | UART Request to Send Output. |

Note:

1. Pin Type I=Digital Input, O=Digital Output; AI=Analog Input; P=Power Pin; AP=Analog Power

# 4 BLOCK DIAGRAM

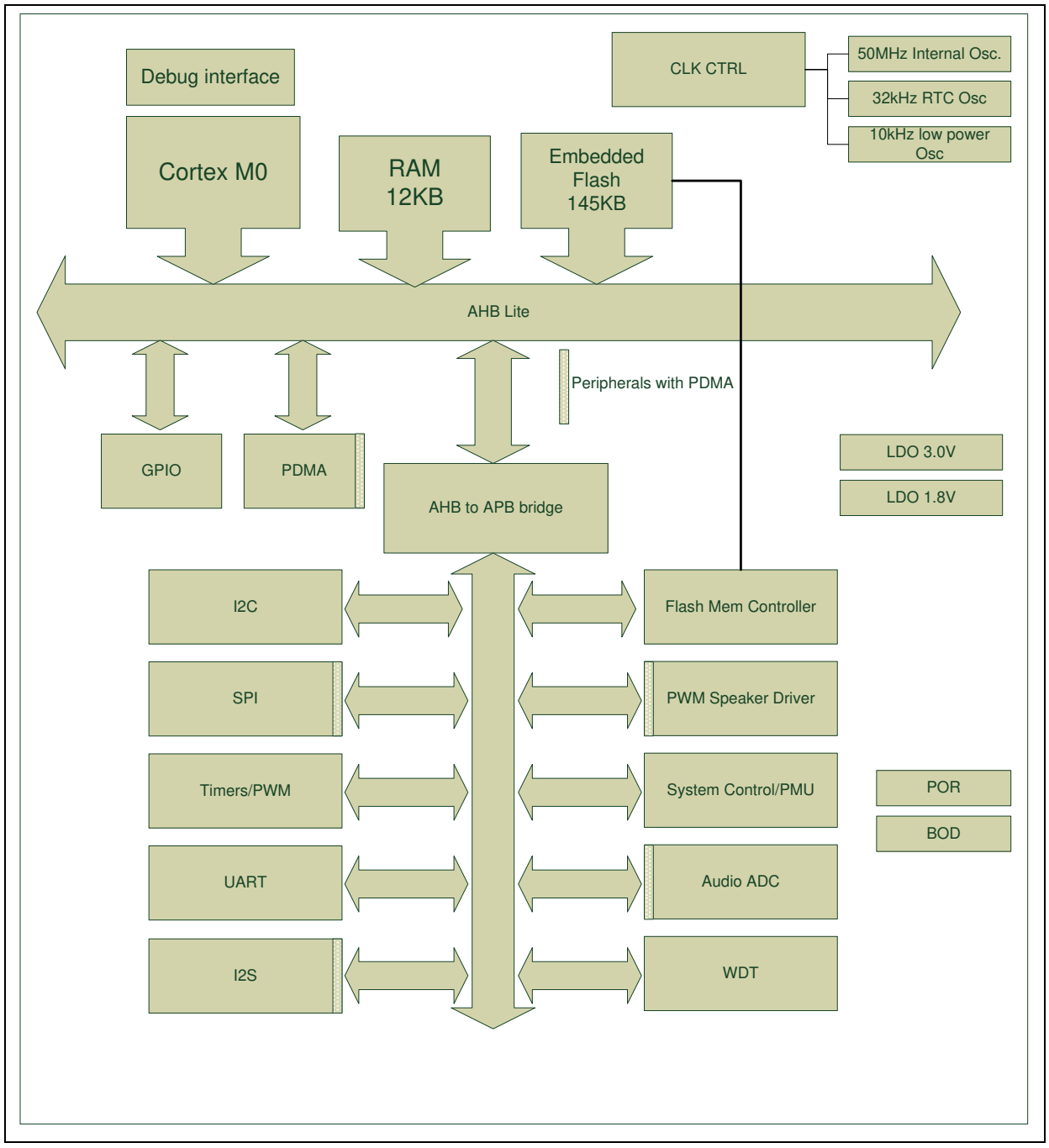



Figure 4-1 ISD9160 Block Diagram

# 5 FUNCTIONAL DESCRIPTION

## 5.1 ARM® Cortex™-M0 core

The Cortex™-M0 processor is a multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex-M profile processor.

Figure 5-1 shows the functional blocks of processor.

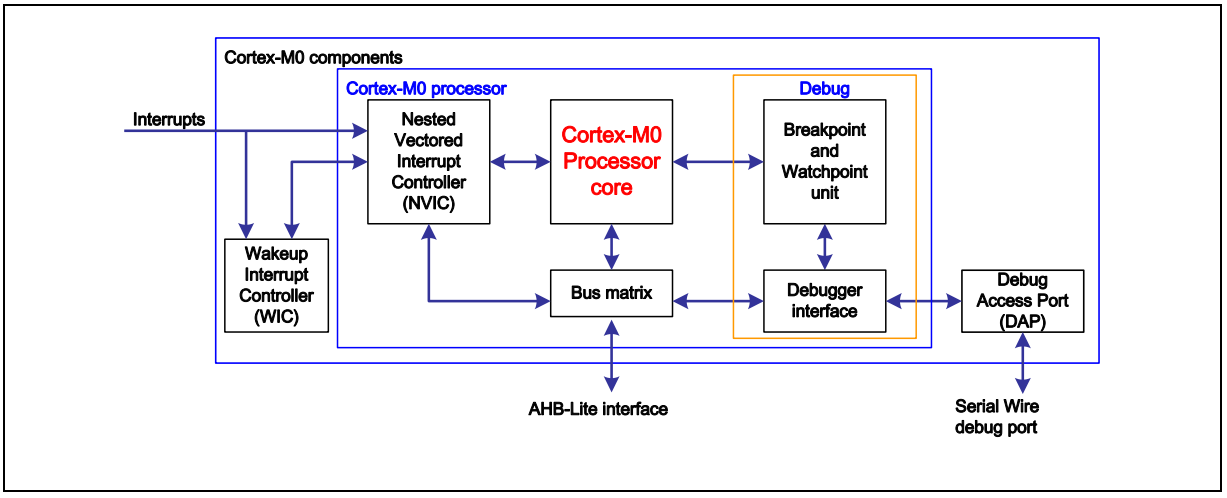



Figure 5-1 Functional Block Diagram

The implemented device provides:

- A low gate count processor that features:
  - The ARMv6-M Thumb® instruction set.
  - Thumb-2 technology.
  - ARMv6-M compliant 24-bit SysTick timer.
  - A 32-bit hardware multiplier.
  - The system interface supports little-endian data accesses.
  - The ability to have deterministic, fixed-latency, interrupt handling.
  - Load/store-multiples that can be abandoned and restarted to facilitate rapid interrupt handling.
  - C Application Binary Interface compliant exception model.
    This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers.
  - Low power sleep-mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature.
- NVIC that features:
  - 32 external interrupt inputs, each with four levels of priority.
  - Dedicated non-Maskable Interrupt (NMI) input.
  - Support for both level-sensitive and pulse-sensitive interrupt lines
  - Wake-up Interrupt Controller (WIC), providing ultra-low power sleep mode support.
- Debug support
  - Four hardware breakpoints.
  - Two watchpoints.
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling.

- Single step and vector catch capabilities.

- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
  - Single 32-bit slave port that supports the DAP (Debug Access Port).

## 5.2 System Manager

### 5.2.1 Overview

The following functions are included in system manager section

- System Memory Map
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System management registers for product ID
- System management registers for chip and module functional reset and multi-function pin control
- Brown-Out and chip miscellaneous Control Register
- Combined peripheral interrupt source identify

### 5.2.2 System Reset

The system reset includes one of the list below event occurs. For these reset event flags can be read by SYS_RSTSTS register.

- The Power-On Reset
- The low level on the RESETN pin
- Watchdog Time Out Reset
- Low Voltage Reset
- Cortex-M0 MCU Reset
- PMU Reset – for details of wakeup events, also examine CLK_PWRCTL register.
- SWD Debug interface.

A power-on reset (POR) will occur if the main external supply rail ramps from 0V or the voltage of the main supply drops below reset threshold. A low voltage reset monitors the regulated core logic (1.8V) supply and will assert if the voltage on this rail drops below reliable logic threshold.

### 5.2.3 System Power Distribution

The ISD9160 implements several power domains:

- Analog power from VCCA and VSSA provides the power for analog module operation.
- Digital power from VCCD and VSSD supplies the power to the IO ring and the internal regulator which provides 1.8V power for digital operation.
- VCCLDO supplies the LDO regulator whose output is available on pin VDD33. This supply powers the IO ring for GPIOA<7:0>.
- An internal Standby reference (SB REG) generates a 1.8V rail to part of the logic including the IO ring, Standby RAM and RTC during standby mode for low power operation.

The outputs of internal voltage regulators; VREG and VDD33, require external decoupling capacitors which should be located close to the corresponding pin. The following diagram shows the power distribution of this device.

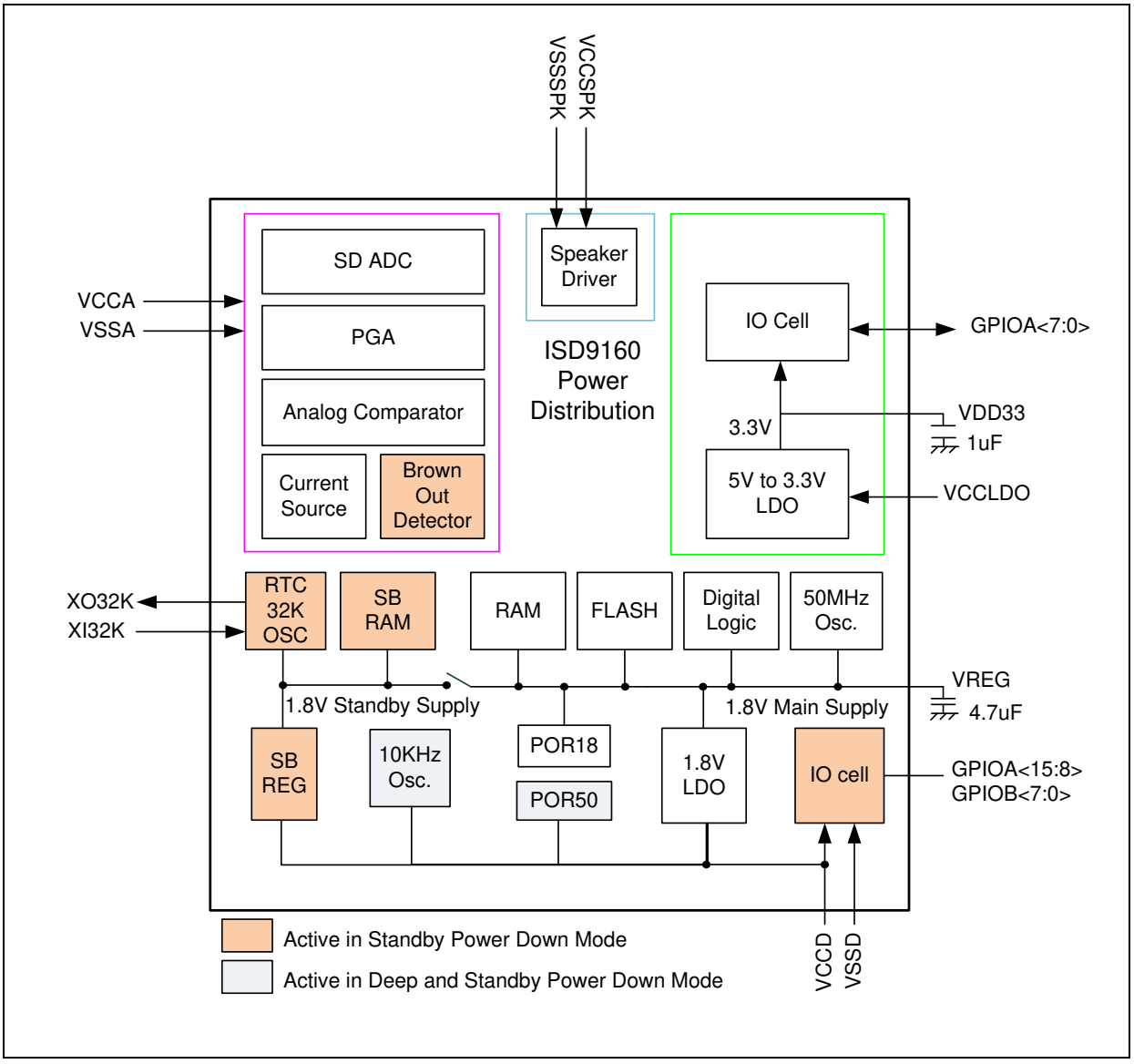



Figure 5-2 ISD9160 Power Distribution Diagram

### 5.2.4 System Memory Map

The ISD9160 provides 4G-byte address space. The memory locations assigned to each on-chip module is shown in Table 5-1. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip module. The ISD9160 supports little-endian data format.

Table 5-1 Address Space Assignments for On-Chip Modules

| Address Space | Token | Modules | Reference |
|---|---|---|---|
| **Flash & SRAM Memory Space** | | | |
| 0x0000_0000 – 0x0002_33FF | FLASH_BA | FLASH Memory Space (141KB) | |
| 0x0000_0000 – 0x0002_43FF | FLASH_BA | FLASH Memory Space (145KB) | |
| 0x2000_0000 – 0x2000_2FFF | SRAM_BA | SRAM Memory Space (12KB) | |
| **AHB Modules Space (0x5000_0000 – 0x501F_FFFF)** | | | |
| 0x5000_0000 – 0x5000_01FF | SYS_BA | System Global Control Registers | 5.2.5 |
| 0x5000_0200 – 0x5000_02FF | CLK_BA | Clock Control Registers | 5.3.5 |
| 0x5000_0300 – 0x5000_03FF | INT_BA | Interrupt Multiplexer Control Registers | 0 |
| 0x5000_4000 – 0x5000_7FFF | GPIO_BA | GPIO Control Registers | 5.4.3 |
| 0x5000_8000 – 0x5000_BFFF | PDMA_BA | SRAM_APB DMA Control Registers | 5.15 |
| 0x5000_C000 – 0x5000_FFFF | FMC_BA | Flash Memory Control Registers | 6.3 |
| **APB1 Modules Space (0x4000_0000 ~ 0x400F_FFFF)** | | | |
| 0x4000_4000 – 0x4000_7FFF | WDT_BA | Watch-Dog Timer Control Registers | 5.11 |
| 0x4000_8000 – 0x4000_BFFF | RTC_BA | Real Time Clock (RTC) Control Register | 5.8 |
| 0x4001_0000 – 0x4001_3FFF | TIMER0_BA | Timer0/Timer1 Control Registers | 5.10 |
| 0x4002_0000 – 0x4002_3FFF | I2C0_BA | I2C0 Interface Control Registers | 5.6 |
| 0x4003_0000 – 0x4003_3FFF | SPI0_BA | SPI0 Serial Interface Control Registers | 5.9 |
| 0x4004_0000 – 0x4004_3FFF | PWM_BA | PWM0/1 Control Registers | 5.7 |
| 0x4005_0000 – 0x4005_3FFF | UART0_BA | UART0 Control Registers | 5.12 |
| 0x4007_0000 – 0x4007_3FFF | DPWM_BA | Differential Audio PWM Speaker Driver | 7.2 |
| 0x4008_0000 – 0x4008_3FFF | ANA_ BA | Analog Block Control Registers | 0 |
| 0x4008_4000 – 0x4008_7FFF | BODTALM_BA | Brown Out Detector Control Registers | 5.5.1 |

| | | | |
|---|---|---|---|
| 0x4009_0000 – 0x4009_7FFF | CRC_BA | CRC Block Control Registers | 5.14 |
| 0x400A_0000 - 0x400A_FFFF | I2S_BA | I2S Interface Control registers | 5.13 |
| 0x400B_0000 - 0x400B_FFFF | BIQ_BA | Biquad Filter Control Registers | 7.6 |
| 0x400D_0000 – 0x400D_3FFF | ACMP_BA | Analog Comparator Control Registers | 0 |
| 0x400E_0000 – 0x400E_FFFF | ADC0_BA | Analog-Digital-Converter (ADC) Registers | 7.1 |
| 0x400F_0000 – 0x400F_7FFF | SBRAM_BA | Standby RAM Block Address space | |
| **System Control Space (0xE000_E000 ~ 0xE000_EFFF)** | | | |
| 0xE000_E010 – 0xE000_E0FF | SYSTICK_BA | System Timer Control Registers | 5.2.6 |
| 0xE000_E100 – 0xE000_ECFF | SCS_BA | External Interrupt Controller Control Registers | 5.2.7 |
| 0xE000_ED00 – 0xE000_ED8F | SYSINFO_BA | System Control Registers | 5.2.8 |

### 5.2.5 System Manager Control Registers

| Register | Offset | R/W | Description | Reset Value |
|---|---|---|---|---|
| SYS Base Address:<br>SYS_BA = 0x5000_0000 | | | | |
| **SYS_RSTSTS** | SYS_BA+0x04 | R/W | System Reset Source Register | 0x0000_00XX |
| **SYS_IPRST0** | SYS_BA+0x08 | R/W | IP Reset Control Resister1 | 0x0000_0000 |
| **SYS_IPRST1** | SYS_BA+0x0C | R/W | IP Reset Control Resister2 | 0x0000_0000 |
| **SYS_PASMTEN** | SYS_BA+0x30 | R/W | GPIOA input type control register | 0x0000_0000 |
| **SYS_PBSMTEN** | SYS_BA+0x34 | R/W | GPIOB input type control register | 0x0000_0000 |
| **SYS_GPA_MFP** | SYS_BA+0x38 | R/W | GPIOA multiple function control register | 0x0000_0000 |
| **SYS_GPB_MFP** | SYS_BA+0x3C | R/W | GPIOB multiple function control register | 0x0000_0000 |
| **SYS_WKCTL** | SYS_BA+0x54 | R/W | WAKEUP pin control register | 0x0000_0006 |
| **SYS_REGLCTL** | SYS_BA+0x100 | R/W | Register Lock Key Address register | 0x0000_0000 |
| **SYS_IRCTCTL** | SYS_BA+0x110 | R/W | Oscillator Frequency Adjustment control register | 0xXXXX_XXXX |

### System Reset Source Register (SYS_RSTSTS)

This register provides specific information for software to identify this chip's reset source from last operation.

| Register | Offset | R/W | Description | Reset Value |
|---|---|---|---|---|
| SYS_RSTSTS | SYS_BA+0x04 | R/W | System Reset Source Register | 0x0000_00XX |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Reserved | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CPURF | PMURSTF | SYSRF | Reserved | Reserved | WDTRF | Reserved | CORERSTF |

Table 5-2 System Reset Source Register (SYS_RSTSTS, address 0x5000_0004) Bit Description.

| Bits | Description | |
|---|---|---|
| [31:8] | Reserved | Reserved |
| [7] | CPURF | **Reset Source From CPU**<br>The CPURF flag is set by hardware if software writes SYS_IPRST0.CPURST with a "1" to reset Cortex-M0 CPU kernel and Flash memory controller (FMC).<br>0= No reset from CPU<br>1= The Cortex-M0 CPU kernel and FMC has been reset by software setting CPURST to 1.<br>This bit is cleared by writing 1 to itself. |
| [6] | PMURSTF | **Reset Source From PMU**<br>The PMURSTF flag is set if the PMU.<br>0= No reset from PMU<br>1= PMU reset the system from a power down/standby event.<br>This bit is cleared by writing 1 to itself. |

| | | |
|---|---|---|
| **[5]** | **SYSRF** | **Reset Source From MCU**<br>The SYSRF flag is set if the previous reset source originates from the Cortex_M0 kernel.<br>0= No reset from MCU<br>1= The Cortex_M0 MCU issued a reset signal to reset the system by software writing 1 to bit SYSCTL_AIRCTL.SYSRESTREQ, Application Interrupt and Reset Control Register) in system control registers of Cortex_M0 kernel.<br>This bit is cleared by writing 1 to itself. |
| **[4:3]** | Reserved | Reserved |
| **[2]** | **WDTRF** | **Reset Source From WDT**<br>The WDTRF flag is set if pervious reset source originates from the Watch-Dog module.<br>0= No reset from Watch-Dog<br>1= The Watch-Dog module issued the reset signal to reset the system.<br>This bit is cleared by writing 1 to itself. |
| **[1]** | Reserved | Reserved |
| **[0]** | **CORERSTF** | **Reset Source From CORE**<br>The CORERSTF flag is set if the core has been reset. Possible sources of reset are a Power-On Reset (POR), RESETn Pin Reset or PMU reset.<br>0= No reset from CORE<br>1= Core was reset by hardware block.<br>This bit is cleared by writing 1 to itself. |

### IP Reset Control Register1 (SYS_IPRST0)

| Register | Offset | R/W | Description | Reset Value |
|---|---|---|---|---|
| SYS_IPRST0 | SYS_BA+0x08 | R/W | IP Reset Control Resister1 | 0x0000_0000 |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Reserved | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | PDMARST | CPURST | CHIPRST |

Table 5-3 IP Reset Control Register 1 (SYS_IPRST0 address 0x5000_0008) Bit Description.

| Bits | Description | |
|---|---|---|
| [31:3] | Reserved | Reserved |
| [2] | PDMARST | **PDMA Controller Reset**<br>Set “1” will generate a reset signal to the PDMA Block. User needs to set this bit to “0” to release from the reset state<br>0= Normal operation<br>1= PDMA IP reset |
| [1] | CPURST | **CPU Kernel One Shot Reset**<br>Setting this bit will reset the CPU kernel and Flash Memory Controller(FMC), this bit will automatically return to “0” after the 2 clock cycles<br>This bit is a protected bit, to program first issue the unlock sequence (see Protected Register Lock Key Register (SYS_REGLCTL))<br>0= Normal<br>1= Reset CPU |
| [0] | CHIPRST | **CHIP One Shot Reset**<br>Set this bit will reset the whole chip, this bit will automatically return to “0” after the 2 clock cycles.<br>CHIPRST has same behavior as POR reset, all the chip modules are reset and the chip configuration settings from flash are reloaded.<br>This bit is a protected bit, to program first issue the unlock sequence (see Protected Register Lock Key Register (SYS_REGLCTL))<br>0= Normal<br>1= Reset CHIP |

### IP Reset Control Register2 (SYS_IPRST1)

Setting these bits "1" will generate an asynchronous reset signal to the corresponding peripheral block. The user needs to set bit to "0" to release block from the reset state.

| Register | Offset | R/W | Description | Reset Value |
|---|---|---|---|---|
| SYS_IPRST1 | SYS_BA+0x0C | R/W | IP Reset Control Resister2 | 0x0000_0000 |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| Reserved | ANARST | I2S0RST | EADCRST | Reserved | Reserved | Reserved | Reserved |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Reserved | ACMPRST | Reserved | PWM0RST | CRCRST | BIQRST | Reserved | UART0RST |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | Reserved | DPWMRST | SPI0RST | Reserved | Reserved | Reserved | I2C0RST |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TMR1RST | TMR0RST | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

Table 5-4 IP Reset Control Register 2 (SYS_IPRST1 address 0x5000_000C) Bit Description.

| Bits | Description | |
|---|---|---|
| [30] | ANARST | **Analog Block Control Reset**<br>0 = Normal Operation<br>1 = Reset |
| [29] | I2S0RST | **I2S Controller Reset**<br>0 = Normal Operation<br>1 = Reset |
| [28] | EADCRST | **ADC Controller Reset**<br>0 = Normal Operation<br>1 = Reset |
| [22] | ACMPRST | **Analog Comparator Reset**<br>0 = Normal Operation<br>1 = Reset |
| [20] | PWM0RST | **PWM10 controller Reset**<br>0 = Normal Operation<br>1 = Reset |
| [19] | CRCRST | **CRC Generation Block Reset**<br>0 = Normal Operation<br>1 = Reset |