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40V Precision Low Power Operational Amplifiers

ISL28117, ISL28217, ISL28417, ISL28417SEH

The ISL28117, ISL28217, ISL28417 and ISL28417SEH are a family of very high precision amplifiers featuring low noise vs power consumption, low offset voltage, low bias current and low temperature drift making them the ideal choice for applications requiring both high DC accuracy and AC performance. The combination of precision, low noise and small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision active filters, medical and analytical instrumentation, precision power supply controls and industrial controls.

The ISL28117 single and ISL28217 dual are offered in 8 Ld SOIC, MSOP and TDFN packages. The ISL28417 is offered in 14 Ld SOIC, 14 Ld TSSOP packages. All devices are offered in standard pin configurations and operate over the extended temperature range from -40°C to +125°C.

The ISL28417SEH is offered in a 14 Ld Hermetic Ceramic Flatpack package. The device is offered in an industry standard pin configuration and operates over the extended temperature range from -55°C to +125°C.

Related Literature

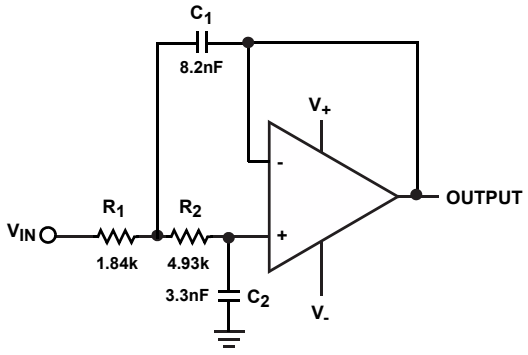
- AN1508 "ISL281X7SOICEVAL1Z Evaluation Board User's Guide"
- AN1509 "ISL282X7SOICEVAL2Z Evaluation Board User's Guide"

Features

- Low input offset voltage . . . . . ±50µV, maximum
  ISL28417SEH ±110µV, maximum
- Superb offset voltage TC . . . . . 0.6µV/°C, maximum
  ISL28417SEH 1µV/°C, maximum
- Input bias current . . . . . ±1nA, maximum
  ISL28417SEH ±5nA, maximum
- Input bias current TC . . . . . ±5pA/°C, maximum
- Low current consumption 440µA
- Voltage noise 8nV/Hz
- Wide supply range . . . . . 4.5V to 40V
- Operating temperature range. . . . . -40°C to +125°C
  ISL28417SEH -55°C to +125°C
- Small package offerings in single, dual and quad
- Pb-free (RoHS compliant)
- No phase reversal

Applications

- Precision instruments
- Medical instrumentation
- Power supply control
- Active filter blocks
- Thermocouples and RTD reference buffers
- Data acquisition



SALLEN-KEY LOW PASS FILTER (10kHz)

FIGURE 1. TYPICAL APPLICATION

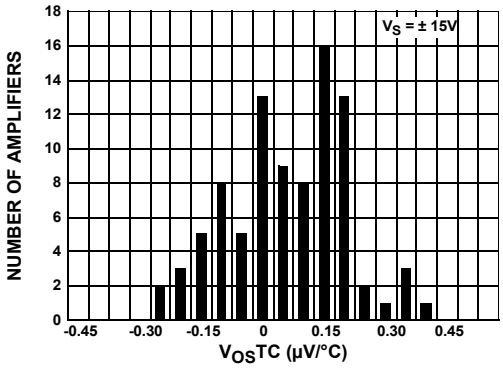


FIGURE 2. V_{OS} TEMPERATURE COEFFICIENT ($V_{OS}TC$)

Table of Contents

Ordering Information

PART NUMBER	PART MARKING	V_{OS} (MAX) (µV)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL28117FBBZ (Notes 1, 4, 6)	28117 FBZ	50 (B Grade)	8 Ld SOIC	M8.15E
ISL28117FBZ (Notes 1, 4, 6)	28117 FBZ -C	100 (C Grade)	8 Ld SOIC	M8.15E
ISL28117FUBZ (Notes 3, 4, 6)	8117Z	70 (B Grade)	8 Ld MSOP	M8.118B
ISL28117FUZ (Notes 3, 4, 6)	8117Z -C	150 (C Grade)	8 Ld MSOP	M8.118B
ISL28117FRTBZ (Notes 2, 4, 6)	8117	75 (B Grade)	8 Ld TDFN	L8.3x3K
ISL28117FRTZ (Notes 1, 4, 6)	-C 8117	150 (C Grade)	8 Ld TDFN	L8.3x3K
ISL28217FBBZ (Notes 1, 4, 6)	28217 FBZ	50 (B Grade)	8 Ld SOIC	M8.15E
ISL28217FBZ (Notes 1, 4, 6)	28217 FBZ -C	100 (C Grade)	8 Ld SOIC	M8.15E
ISL28217FUZ (Notes 1, 4, 6)	8217Z -C	150 (C Grade)	8 Ld MSOP	M8.118B
ISL28217FRTBZ (Notes 1, 4, 6)	8217	70 (B Grade)	8 Ld TDFN	L8.3x3K
ISL28217FRTZ (Notes 1, 4, 6)	-C 8217	150 (C Grade)	8 Ld TDFN	L8.3x3K
ISL28417FBBZ (Notes 1, 4, 6)	28417 FBZ	120 (B Grade)	14 Ld SOIC	MDP0027
ISL28417FBZ (Notes 1, 4, 6)	28417 FBZ -C	200 (C Grade)	14 Ld SOIC	MDP0027
ISL28417FVBZ (Notes 1, 4, 6)	28417 FVZ	120 (B Grade)	14 Ld TSSOP	M14.173
ISL28417FVZ (Notes 1, 4, 6)	28417 FVZ-C	200 (C Grade)	14 Ld TSSOP	M14.173
ISL28417SEHMF (Note 5)	ISL28417SEHMF	110 (B Grade)	14 Ld Flatpack	K14.A
ISL28417SEHF/PROTO (Note 5)	ISL28417SEHF/PROTO	110 (B Grade)	14 Ld Flatpack	K14.A
ISL28417SEHMX (Note 5)		110 (B Grade)	DIE	
ISL28417SEHX/SAMPLE (Note 5)		110 (B Grade)	DIE	
ISL28117SOICEVAL1Z	Evaluation Board			
ISL28217SOICEVAL2Z	Evaluation Board			

NOTES:

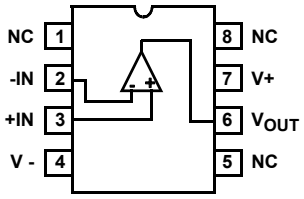
1. Add “-T13” suffix for 2.5k unit, -T7” suffix for 1k,“-T7A” suffix for 250 unit Tape and Reel options. Please refer to TB347 for details on reel specifications.
2. Add “-T13” suffix for 6k unit, -T7” suffix for 1k,“-T7A” suffix for 250 unit Tape and Reel options. Please refer to TB347 for details on reel specifications.
3. Add “-T13” suffix for 2.5k unit, -T7” suffix for 1.5k,“-T7A” suffix for 250 unit Tape and Reel options. Please refer to TB347 for details on reel specifications.
4. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
5. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
6. For Moisture Sensitivity Level (MSL), please see device information page for ISL28117, ISL28217, ISL28417. For more information on MSL please see techbrief TB363.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

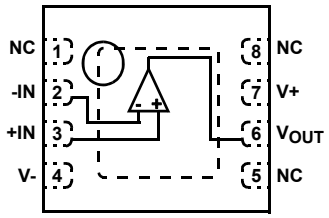
PART NUMBER	NUMBER OF DEVICES	PACKAGE	OPERATING TEMPERATURE RANGE
ISL28117	1	8 Ld SOIC	-40°C to +125°C
ISL28217	2	8 Ld SOIC	-40°C to +125°C
ISL28417	4	14 Ld SOIC	-40°C to +125°C
ISL28417SEH	4	14 Ld Flatpack	-55°C to +125°C

Pin Configurations

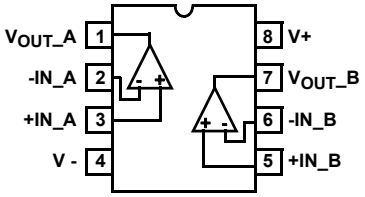
ISL28117
(8 LD SOIC, MSOP)
TOP VIEW



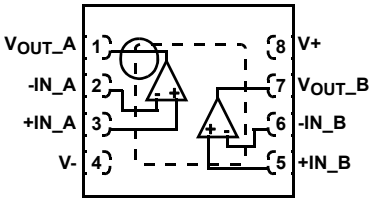
ISL28117
(8 LD TDFN)
TOP VIEW



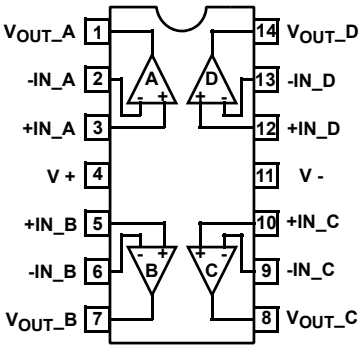
ISL28217
(8 LD SOIC, MSOP)
TOP VIEW



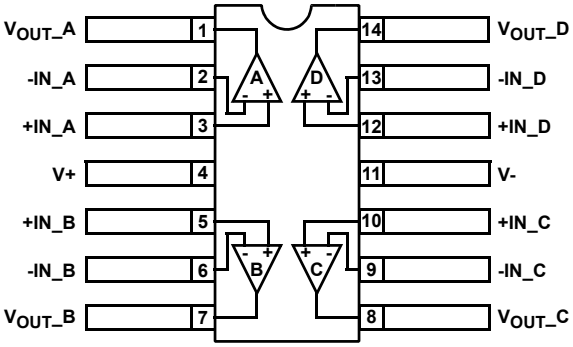
ISL28217
(8 LD TDFN)
TOP VIEW



ISL28417
(14 LD SOIC, TSSOP)
TOP VIEW

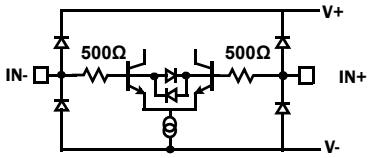


ISL28417SEH
(14 LD FLATPACK)
TOP VIEW

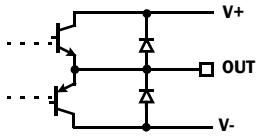


Pin Descriptions

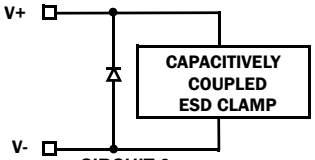
ISL28117 (8 Ld SOIC, MSOP, TDFN)	ISL28217 (8 Ld SOIC, MSOP, TDFN)	ISL28417/SEH (14 Ld SOIC, TSSOP) (14 Ld FLATPACK)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	-	-	+IN	Circuit 1	Amplifier noninverting input
-	3	3	+IN_A		
-	5	5	+IN_B		
-	-	10	+IN_C		
-	-	12	+IN_D		
4	4	11	V-	Circuit 3	Negative power supply
2	-	-	-IN	Circuit 1	Amplifier inverting input
-	2	2	-IN_A		
-	6	6	-IN_B		
-	-	9	-IN_C		
-	-	13	-IN_D		
7	8	4	V+	Circuit 3	Positive power supply
6	-	-	V_{OUT}	Circuit 2	Amplifier output
-	1	1	V_{OUT}_A		
-	7	7	V_{OUT}_B		
-	-	8	V_{OUT}_C		
-	-	14	V_{OUT}_D		
1, 5, 8	-	-	NC	-	No internal connection
PD	PD	-	PD	-	Thermal Pad - TDFN package only. Connect thermal pad to ground or most negative potential.



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Absolute Maximum Ratings

Maximum Supply Voltage 42V
Maximum Supply Voltage ISL28417SEH (Note 13) 40V
Maximum Differential Input Current 20mA
Maximum Differential Input Voltage 42V
Maximum Differential Input Voltage (ISL28417SEH) 20V
Min/Max Input Voltage . . . . . V- - 0.5V to V+ + 0.5V
Max/Min Input Current for Input Voltage >V+ or <V- . . . . . ±20mA
Output Short-Circuit Duration (1 output at a time). . . . . Indefinite
ESD Rating
Human Body Model
ISL28117, ISL28417 . . . . . 6kV
ISL28217 . . . . . 4.5kV
ISL28217 MSOP 5.5kV
ISL28417SEH 2kV
Charged Device Model
ISL28117, ISL28217 . . . . . 1.5kV
ISL28217 (MSOP), ISL28417 . . . . . 2kV
ISL28417SEH 1kV
Machine Model
ISL28117, ISL28217 (MSOP) 300V
ISL28217 . . . . . 500V
ISL28417, ISL28417SEH 450V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC ISL28117 (Notes 7, 10)	120	60
8 Ld SOIC ISL28217 (Notes 7, 10)	105	50
8 Ld MSOP ISL28117 (Notes 7, 10)	155	50
8 Ld MSOP ISL28217 (Notes 7, 10)	160	55
8 Ld TDFN ISL28117 (Notes 8, 9)	48	7
8 Ld TDFN ISL28217 (Notes 8, 9)	43	2
14 Ld SOIC (Notes 8, 10)	73	45
14 Ld TSSOP (Notes 7, 10)	90	32
14 Ld Flatpack (Notes 11, 12)	105	15

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature (T_{JMAX}) . . . . . +150°C
Pb-Free Reflow Profile (Non-Hermetic Packages Only) . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature Range (T_A)
ISL28117, ISL28217, ISL28417 . . . . . -40°C to +125°C
ISL28417SEH . . . . . -55°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

7. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
8. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
9. For θJC, the “case temp” location is the center of the exposed metal pad on the package underside.
10. For θJC, the “case temp” location is taken at the package top center.
11. θJA is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
12. For θJC, the "case temp" location is the center of the ceramic on the package underside.
13. No destructive single-event effects at effective LET of 73.9MeV • cm^2/mg up to a supply of ±20V. Reference manufacturers SEE report.

Electrical Specifications ISL28117, ISL28217, ISL28417(V_S ± 15V) V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
V_{OS}	Input Offset Voltage, SOIC, TSSOP Package	ISL28x17 B Grade	-50	8	50	µV
			-110		**110**	µV
		ISL28x17 C Grade	-100	4	100	µV
			-190		**190**	µV
		ISL28417 B Grade	-70	10	70	µV
			-120		**120**	µV
		ISL28417 C Grade	-110	10	110	µV
		T_A = -40°C to +85°C	-160		160	µV
		T_A = -40°C to +125°C	**-200**		**200**	µV
	Input Offset Voltage, MSOP Package	ISL28117 B Grade	-70	-10	70	µV
			-150		**150**	µV
		ISL28117 C Grade	-150	4	150	µV
			-250		**250**	µV
		ISL28217 C Grade	-150	10	150	µV
			-250		**250**	µV
	Input Offset Voltage, TDFN Package	ISL28117 B Grade	-75	-10	75	µV
			-160		**160**	µV
		ISL28217 B Grade	-70	10	70	µV
			-140		**140**	µV
		ISL28x17 C Grade	-150	10	150	µV
			-250		**250**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient; SOIC, TSSOP Package	ISL28x17 B Grade	**-0.6**	0.14	**0.6**	µV/°C
		ISL28x17 C Grade	**-0.9**	0.14	**0.9**	µV/°C
		ISL28417 B Grade	**-0.75**	0.20	**0.75**	µV/°C
		ISL28417 C Grade	**-0.9**	0.3	**0.9**	µV/°C
	Input Offset Voltage Temperature Coefficient; MSOP Package	ISL28117 B Grade	**-0.8**	0.1	**0.8**	µV/°C
		ISL28117 C Grade	**-1**	0.14	**1**	µV/°C
		ISL28217 C Grade	**-1**	0.14	**1**	µV/°C
	Input Offset Voltage Temperature Coefficient; TDFN Package	ISL28117 B Grade	**-0.9**	0.1	**0.9**	µV/°C
		ISL28217 B Grade	**-0.7**	0.1	**0.7**	µV/°C
		ISL28x17 C Grade	**-1**	0.1	**1**	µV/°C
I_B	Input Bias Current		-1	0.08	1	nA
			-1.5		1.5	nA
TCI_B	Input Bias Current Temperature Coefficient		-5	1	5	pA/°C
I_{OS}	Input Offset Current		-1.50	0.08	1.50	nA
			-1.85		**1.85**	nA
TCI_{OS}	Input Offset Current Temperature Coefficient		**-3**	0.42	**3**	pA/°C
		ISL28417 SOIC, TSSOP B and C Grade	**-4.00**	0.45	**4.00**	pA/°C
V_{CM}	Input Voltage Range	Guaranteed by CMRR test	**-13**		**13**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = -13V to +13V	120	145		dB
			120			dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±20V	120	145		dB
			120			dB

Electrical Specifications ISL28117, ISL28217, ISL28417(V_S ± 15V) V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
A_{VOL}	Open-Loop Gain	V_O = -13V to +13V, R_L = 10kΩ to ground	130	143		dB
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	13.5	13.7		V
			13.2			V
		R_L = 2kΩ to ground	13.30	13.55		V
			13.1			V
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground		-13.7	-13.5	V
					-13.2	V
		R_L = 2kΩ to ground		-13.55	-13.30	V
					-13.1	V
I_S	Supply Current/Amplifier			0.44	0.53	mA
					0.68	mA
I_{SC}	Short-Circuit			43		mA
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	**±2.25**		**±20**	V
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_V = 1k, R_L = 2kΩ		1.5		MHz
e_{nVp-p}	Voltage Noise V_{P-P}	0.1Hz to 10Hz		0.25		μV_{P-P}
e_n	Voltage Noise Density	f = 10Hz		10		nV/√Hz
		f = 100Hz		8.2		nV/√Hz
		f = 1kHz		8		nV/√Hz
		f = 10kHz		8		nV/√Hz
in	Current Noise Density	f = 1kHz		0.1		pA/√Hz
THD + N	Total Harmonic Distortion	1kHz, G = 1, $V_O = 3.5V_{RMS}$, R_L = 2kΩ		0.0009		%
		1kHz, G = 1, $V_O = 3.5V_{RMS}$, R_L = 10kΩ		0.0005		%
TRANSIENT RESPONSE						
SR	Slew Rate, V_{OUT} 20% to 80%	A_V = 11, R_L = 2kΩ, $V_O = 4V_{P-P}$		0.5		V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = 1, $V_{OUT} = 50mV_{P-P}$, R_L = 10kΩ to V_{CM}		130		ns
	Fall Time 90% to 10% of V_{OUT}	A_V = 1, $V_{OUT} = 50mV_{P-P}$, R_L = 10kΩ to V_{CM}		130		ns
t_s	Settling Time to 0.1% 10V Step; 10% to V_{OUT}	A_V = -1, $V_{OUT} = 10V_{P-P}$, R_L = 5kΩ to V_{CM}		21		µs
	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	A_V = -1, $V_{OUT} = 10V_{P-P}$, R_L = 5kΩ to V_{CM}		24		µs
	Settling Time to 0.1% 4V Step; 10% to V_{OUT}	A_V = -1, $V_{OUT} = 4V_{P-P}$, R_L = 5kΩ to V_{CM}		13		µs
	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	A_V = -1, $V_{OUT} = 4V_{P-P}$, R_L = 5kΩ to V_{CM}		18		µs
t_{OL}	Output Positive Overload Recovery Time	A_V = -100, $V_{IN} = 0.2V_{P-P}$, R_L = 2kΩ to V_{CM}		5.6		µs
	Output Negative Overload Recovery Time	A_V = -100, $V_{IN} = 0.2V_{P-P}$, R_L = 2kΩ to V_{CM}		10.6		µs

Electrical Specifications ISL28117, ISL28217, ISL28417 (V_S ± 5V)

V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
V_{OS}	Input Offset Voltage, SOIC, TSSOP Package	ISL28x17 B Grade	-50	8	50	µV
			-110		**110**	µV
		ISL28x17 C Grade	-100	4	100	µV
			-190		**190**	µV
		ISL28417 B Grade	-70	10	70	µV
			-120		**120**	µV
		ISL28417 C Grade	-110	10	110	µV
		T_A = -40°C to +85°C	-160		160	µV
		T_A = -40°C to +125°C	**-200**		**200**	µV
	Input Offset Voltage, MSOP Package	ISL28117 B Grade	-70	-10	70	µV
			-150		**150**	µV
		ISL28117 C Grade	-150	4	150	µV
			-250		**250**	µV
		ISL28217 C Grade	-150	10	150	µV
			-250		**250**	µV
	Input Offset Voltage, TDFN Package	ISL28117 B Grade	-75	-10	75	µV
			-160		**160**	µV
		ISL28217 B Grade	-70	10	70	µV
			-140		**140**	µV
		ISL28x17 C Grade	-150	10	150	µV
			-250		**250**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient; SOIC, TSSOP Package	ISL28x17 B Grade	**-0.60**	0.14	**0.60**	µV/°C
		ISL28x17 C Grade	**-0.90**	0.14	**0.90**	µV/°C
		ISL28417 B Grade	**-0.75**	0.20	**0.75**	µV/°C
		ISL28417 C Grade	**-0.9**	0.3	**0.9**	µV/°C
	Input Offset Voltage Temperature Coefficient; MSOP Package	ISL28117 B Grade	**-0.8**	0.1	**0.8**	µV/°C
		ISL28117 C Grade	**-1**	0.14	**1**	µV/°C
		ISL28217 C Grade	**-1**	0.14	**1**	µV/°C
	Input Offset Voltage Temperature Coefficient; TDFN Package	ISL28117 B Grade	**-0.9**	0.1	**0.9**	µV/°C
		ISL28217 B Grade	**-0.7**	0.1	**0.7**	µV/°C
		ISL28x17 C Grade	**-1**	0.1	**1**	µV/°C
I_B	Input Bias Current		-1	0.18	1	nA
			-1.5		**1.5**	nA
TCI_B	Input Bias Current Temperature Coefficient		**-5**	1	**5**	pA/°C
I_{OS}	Input Offset Current		-1.5	0.3	1.5	nA
			-1.85		**1.85**	nA
TCI_{OS}	Input Offset Current Temperature Coefficient		-3	0.42	3	pA/°C
		ISL28417 SOIC, TSSOP B and C Grade	**-4.00**	0.45	**4.00**	pA/°C
V_{CM}	Input Voltage Range		**-3**		**3**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = -3V to +3V	120	145		dB
			120			dB

Electrical Specifications ISL28117, ISL28217, ISL28417 (V_S ± 5V)

V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±5V	120	145		dB
			120			dB
A_{VOL}	Open-Loop Gain	V_O = -3.0V to +3.0V, R_L = 10kΩ to ground	130	143		dB
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	3.5	3.7		V
			3.2			V
		R_L = 2kΩ to ground	3.30	3.55		V
			3.1			V
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground		-3.7	-3.5	V
					-3.2	V
		R_L = 2kΩ to ground		-3.55	-3.30	V
					-3.1	V
I_S	Supply Current/Amplifier			0.44	0.53	mA
					0.68	mA
I_{SC}	Short-Circuit			43		mA
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_V = 1k, RL = 2kΩ		1.5		MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz		0.25		μV_{P-P}
e_n	Voltage Noise Density	f = 10Hz		12		nV/√Hz
		f = 100Hz		8.6		nV/√Hz
		f = 1kHz		8		nV/√Hz
		f = 10kHz		8		nV/√Hz
in	Current Noise Density	f = 1kHz		0.1		pA/√Hz
TRANSIENT RESPONSE						
SR	Slew Rate, V_{OUT} 20% to 80%	A_V=11, R_L = 2kΩ V_O = $4V_{P-P}$		0.5		V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = 1, V_{OUT} = $50mV_{P-P}$, R_L = 10kΩ to V_{CM}		130		ns
	Fall Time 90% to 10% of V_{OUT}	A_V = 1, V_{OUT} = $50mV_{P-P}$, R_L = 10kΩ to V_{CM}		130		ns
t_s	Settling Time to 0.1% 4V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = $4V_{P-P}$, R_L = 5kΩ to V_{CM}		12		µs
	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	AV = -1, V_{OUT} = $4V_{P-P}$, R_L = 5kΩ to V_{CM}		19		µs
t_{OL}	Output Positive Overload Recovery Time	A_V = -100, V_{IN} = $0.2V_{P-P}$ R_L = 2kΩ to V_{CM}		7		µs
	Output Negative Overload Recovery Time	A_V = -100, V_{IN} = $0.2V_{P-P}$ R_L = 2kΩ to V_{CM}		5.8		µs

Electrical Specifications ISL28417SEH (V_S ±15V)

V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the -55°C to +125°C operating temperature range. The limits also define room temperature post-irradiation performance following ^{60}Co irradiation at 0.01rad(Si)/s to a total dose of 50krad(Si) wafer-by-wafer acceptance.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
V_{OS}	Input Offset Voltage			10	85	µV
					110	µV
TCV_{OS}	Offset Voltage Drift			0.1	**1**	µV/°C
I_{IB}	Input Bias Current		-2.5	0.08	2.5	nA
		T_A = -55°C, +125°C	-5		5	nA
		T_A = +25°C, post radiation	-15		15	nA
TCI_{IB}	Input Bias Current Temperature Coefficient		**-5**	**1**	**5**	pA/°C
I_{OS}	Input Offset Current		-2.50	0.08	2.50	nA
		T_A = -55°C, +125°C	-3		3	nA
		T_A = +25°C, post radiation	-6		6	nA
TCI_{OS}	Input Offset Current Temperature Coefficient		**-3**	**0.42**	**3**	pA/°C
V_{CM}	Input Voltage Range	Guaranteed by CMRR test	**-13**		**13**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = -13V to +13V	120	145		dB
			120			dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±20V	120	145		dB
			120			dB
A_{VOL}	Open-Loop Gain	V_O = -13V to +13V, R_L = 10kΩ to ground	3,000	14,000		V/mV
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	13.5	13.7		V
			13.2			V
		R_L = 2kΩ to ground	13.30	13.55		V
			13.0			V
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground		-13.7	-13.5	V
					-13.2	V
		R_L = 2kΩ to ground		-13.55	-13.30	V
					-13.0	V
I_S	Supply Current/Amplifier			0.44	0.53	mA
					0.68	mA
I_{SC}	Short-Circuit Current			43		mA
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	**±2.25**		**±20**	V
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_V = 1k, R_L = 2kΩ		1.5		MHz
e_{nVp-p}	Voltage Noise V_{P-P}	0.1Hz to 10Hz		0.25		$µV_{P-P}$
e_n	Voltage Noise Density	f = 10Hz		10		nV/√Hz
		f = 100Hz		8.2		nV/√Hz
		f = 1kHz		8		nV/√Hz
		f = 10kHz		8		nV/√Hz

Electrical Specifications ISL28417SEH (V_S ±15V) V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the -55°C to +125°C operating temperature range. The limits also define room temperature post-irradiation performance following ^{60}Co irradiation at 0.01rad(Si)/s to a total dose of 50krad(Si) wafer-by-wafer acceptance. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
in	Current Noise Density	f = 1kHz		0.1		pA/√Hz
THD + N	Total Harmonic Distortion	1kHz, G = 1, V_O = 3.5VRMS, R_L = 2kΩ		0.0009		%
		1kHz, G = 1, V_O = 3.5VRMS, R_L = 10kΩ		0.0005		%
TRANSIENT RESPONSE						
SR	Slew Rate, V_{OUT} 20% to 80%	A_V = 11, R_L = 2kΩ, V_O = $4V_{P-P}$	0.3	0.5		V/µs
			0.2			V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = 1, V_{OUT} = $50mV_{P-P}$, R_L = 10kΩ to V_{CM}		130	450	ns
					625	ns
	Fall Time 90% to 10% of VOUT	A_V = 1, V_{OUT} = $50mV_{P-P}$, R_L = 10kΩ to V_{CM}		130	600	ns
					700	ns
t_s	Settling Time to 0.1% 10V Step; 10% to V_{OUT}	AV = -1, V_{OUT} = $10V_{P-P}$, R_L = 5kΩ to V_{CM}		21		µs
	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = $10V_{P-P}$, R_L = 5kΩ to V_{CM}		24		µs
	Settling Time to 0.1% 4V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = $4V_{P-P}$, R_L = 5kΩ to V_{CM}		13		µs
	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = $4V_{P-P}$, R_L = 5kΩ to V_{CM}		18		µs
t_{OL}	Output Positive Overload Recovery Time	A_V = -100, V_{IN} = $0.2V_{P-P}$, R_L = 2kΩ to V_{CM}		5.6		µs
	Output Negative Overload Recovery Time	A_V = -100, V_{IN} = $0.2V_{P-P}$, R_L = 2kΩ to V_{CM}		10.6		µs
OS+	Positive Overshoot	A_V = 1, V_{OUT} = $10V_{P-P}$, R_f = 0Ω R_L = 2kΩ to V_{CM}		15		%
					33	%
OS-	Negative Overshoot	A_V = 1, V_{OUT} = $10V_{P-P}$, R_f = 0Ω R_L = 2kΩ to V_{CM}		15		%
					33	%

Electrical Specifications ISL28417SEH (V_S ±5V) V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the -55°C to +125°C operating temperature range. The limits also define room temperature post-irradiation performance following ^{60}Co irradiation at 0.01rad(Si)/s to a total dose of 50krad(Si) wafer-by-wafer acceptance.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
V_{OS}	Input Offset Voltage			10	150	µV
					250	µV
TCV_{OS}	Offset Voltage Drift			0.1	**1**	µV/°C
I_{IB}	Input Bias Current		-2.50	0.18	2.50	nA
		T_A = -55°C, +125°C	-5		5	nA
		T_A = +25°C, post radiation	-15		15	nA
TCI_{IB}	Input Bias Current Temperature Coefficient		**-5**	**1**	**5**	pA/°C
I_{OS}	Input Offset Current		-2.5	0.3	2.5	nA
		T_A = -55°C, +125°C	-3		3	nA
		T_A = +25°C, post radiation	**6**	**0.42**	**6**	nA

Electrical Specifications ISL28417SEH (V_S ±5V) V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the -55°C to +125°C operating temperature range. The limits also define room temperature post-irradiation performance following ^{60}Co irradiation at 0.01rad(Si)/s to a total dose of 50krad(Si) wafer-by-wafer acceptance. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
TCI_{OS}	Input Offset Current Temperature Coefficient		**-3**	**0.42**	**3**	pA/°C
V_{CM}	Input Voltage Range		**-3**		**3**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = -3V to +3V	120	145		dB
			120			dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±5V	120	145		dB
			120			dB
A_{VOL}	Open-Loop Gain	V_O = -3.0V to +3.0V R_L = 10kΩ to ground	3,000	14,000		V/mV
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	3.5	3.7		V
			3.2			V
		R_L = 2kΩ to ground	3.300	3.550		V
			3.0			V
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground		-3.7	-3.5	V
					-3.2	V
		R_L = 2kΩ to ground		-3.55	-3.30	V
					-3.0	V
I_S	Supply Current/Amplifier			0.44	0.53	mA
					0.68	mA
I_{SC}	Short-Circuit Current			43		mA
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_V = 1k, R_L = 2kΩ		1.5		MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz		0.25		μV_{P-P}
e_n	Voltage Noise Density	f = 10Hz		12		nV/√Hz
		f = 100Hz		8.6		nV/√Hz
		f = 1kHz		8		nV/√Hz
		f = 10kHz		8		nV/√Hz
in	Current Noise Density	f = 1kHz		0.1		pA/√Hz
TRANSIENT RESPONSE						
SR	Slew Rate, V_{OUT} 20% to 80%	A_V = 11, R_L = 2kΩ, VO = $4V_{P-P}$		0.5		V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	AV = 1, V_{OUT} = $50mV_{P-P}$, R_L = 10kΩ to V_{CM}		130		ns
	Fall Time 90% to 10% of V_{OUT}	A_V = 1, V_{OUT} = $50mV_{P-P}$, R_L = 10kΩ to V_{CM}		130		ns
t_s	Settling Time to 0.1% 4V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = $4V_{P-P}$, R_L = 5kΩ to V_{CM}		12		µs
	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = $4V_{P-P}$, R_L = 5kΩ to V_{CM}		19		µs

Electrical Specifications ISL28417SEH (V_S ±5V) V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the -55°C to +125°C operating temperature range. The limits also define room temperature post-irradiation performance following ^{60}Co irradiation at 0.01rad(Si)/s to a total dose of 50krad(Si) wafer-by-wafer acceptance. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
t_{OL}	Output Positive Overload Recovery Time	A_V = -100, V_{IN} = 0.2V_{P-P} R_L = 2kΩ to V_{CM}		7		µs
	Output Negative Overload Recovery Time	A_V = -100, V_{IN} = 0.2V_{P-P} R_L = 2kΩ to V_{CM}		5.8		µs
OS+	Positive Overshoot	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		15		%
OS-	Negative Overshoot	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		15		%

NOTE:

14. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified.

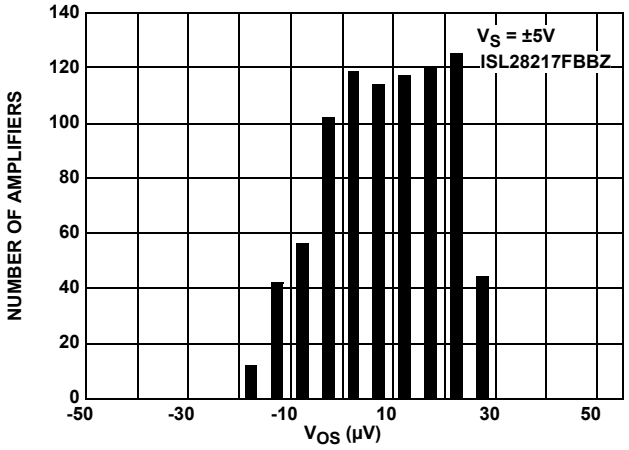


FIGURE 3. V_{OS} DISTRIBUTION FOR GRADE B

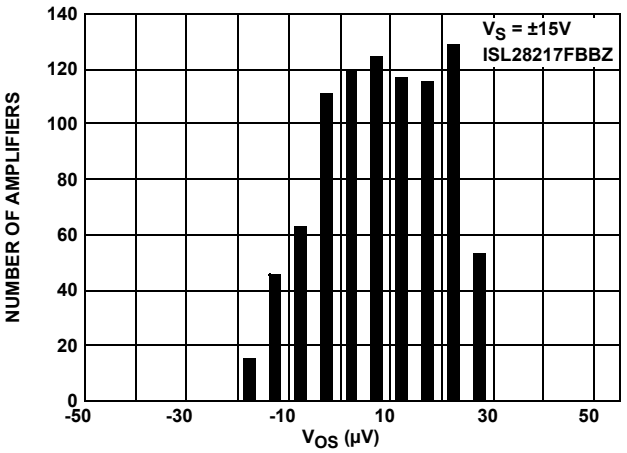


FIGURE 4. V_{OS} DISTRIBUTION FOR GRADE B

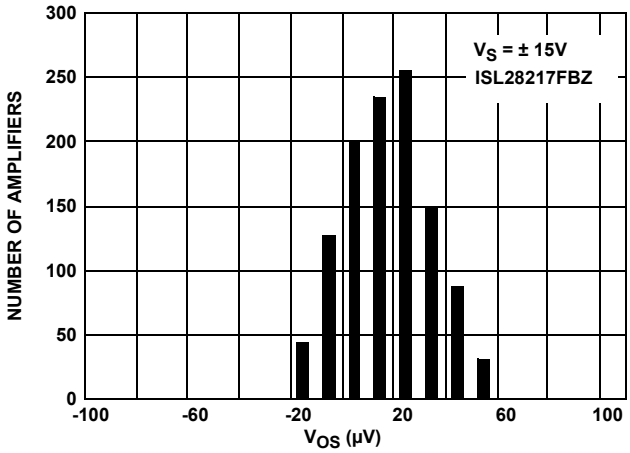


FIGURE 5. V_{OS} DISTRIBUTION FOR GRADE C

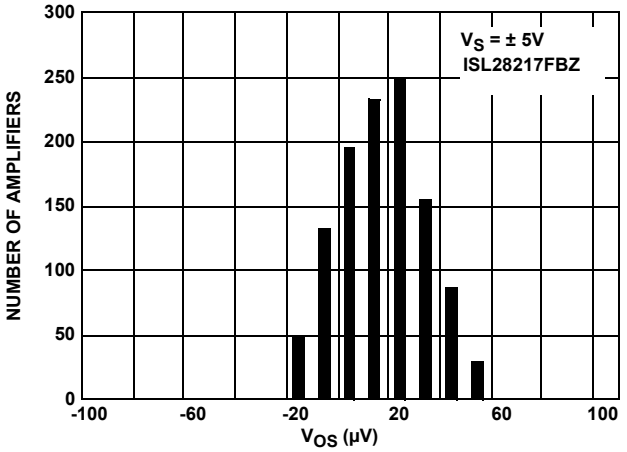


FIGURE 6. V_{OS} DISTRIBUTION FOR GRADE C

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

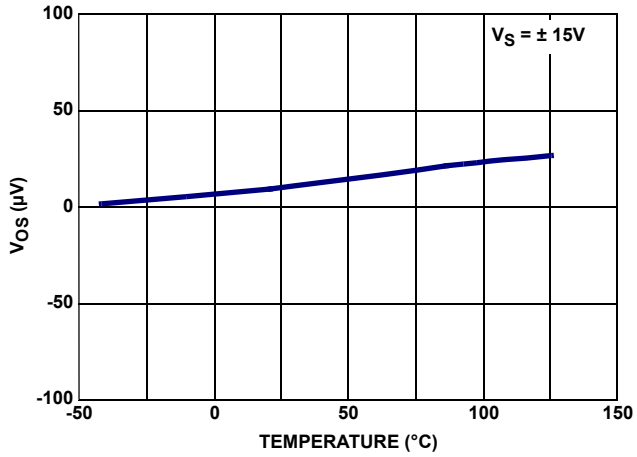


FIGURE 7. V_{OS} RANGE vs TEMPERATURE

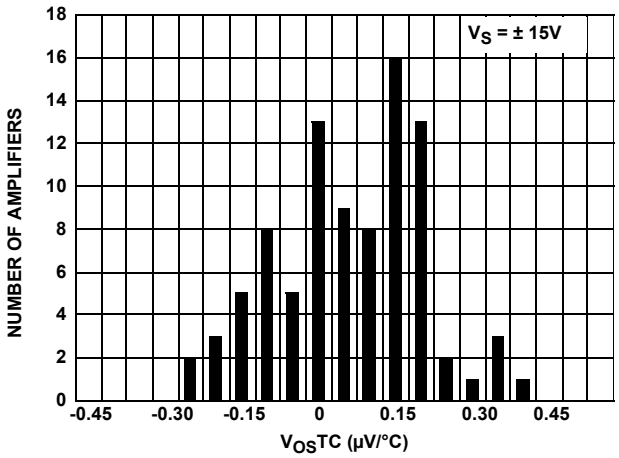


FIGURE 8. TCV_{OS} vs NUMBER OF AMPLIFIERS

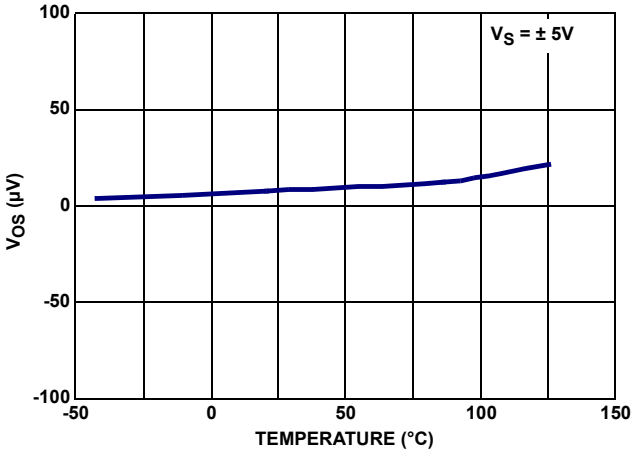


FIGURE 9. V_{OS} RANGE vs TEMPERATURE

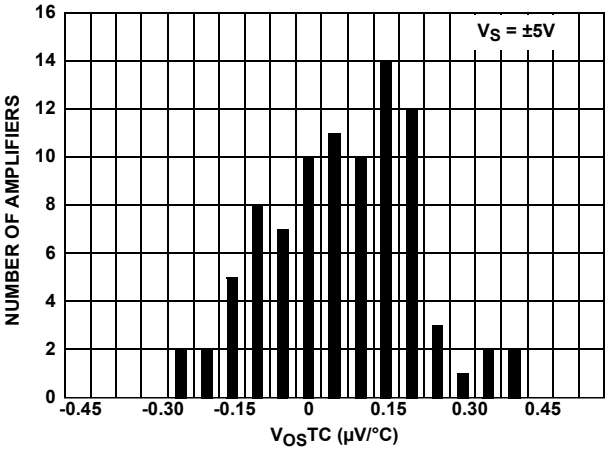


FIGURE 10. TCV_{OS} vs NUMBER OF AMPLIFIERS

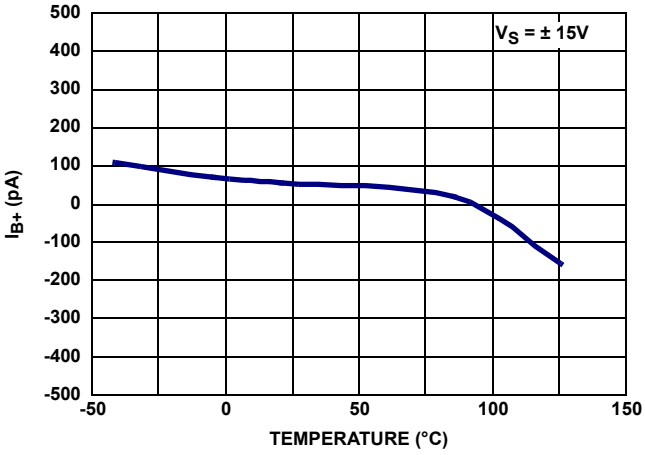


FIGURE 11. I_{B+} RANGE vs TEMPERATURE

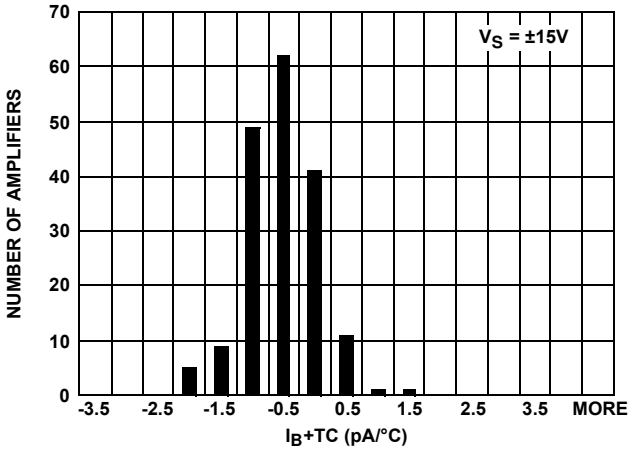


FIGURE 12. TCI_{B+} vs NUMBER OF AMPLIFIERS

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

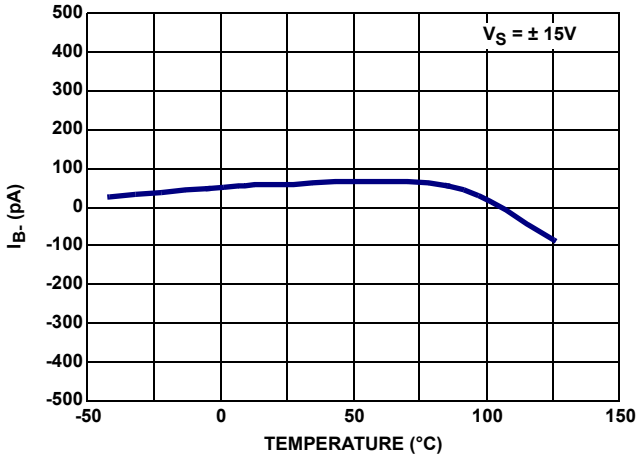


FIGURE 13. I_{B-} RANGE vs TEMPERATURE

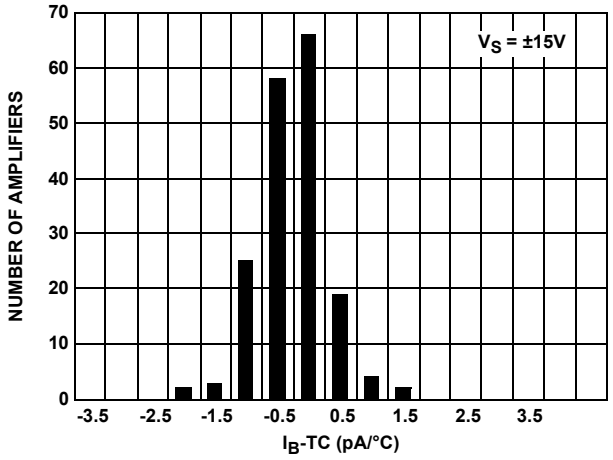


FIGURE 14. TCI_{B-} vs NUMBER OF AMPLIFIERS

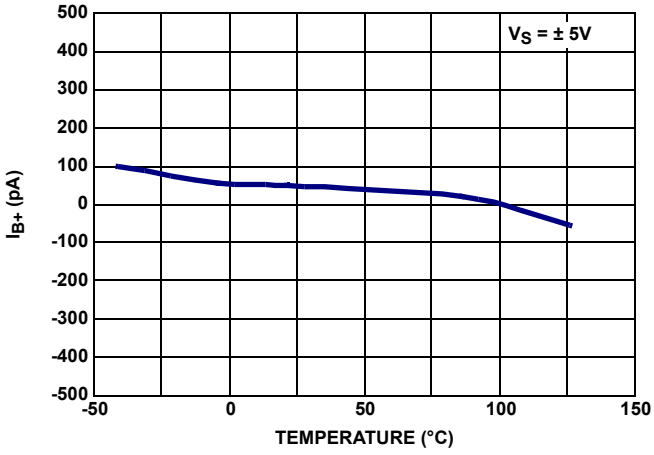


FIGURE 15. I_{B+} RANGE vs TEMPERATURE

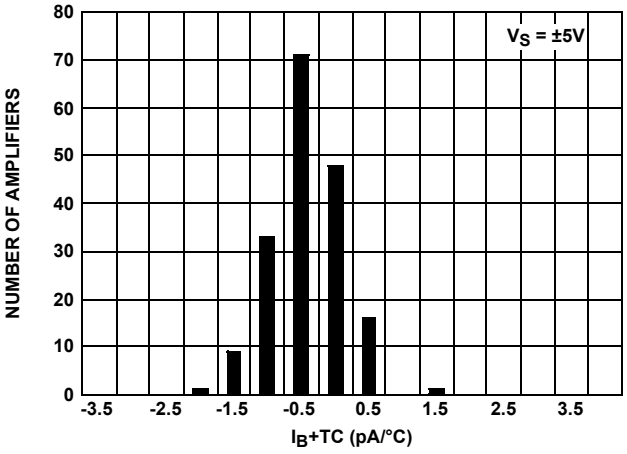


FIGURE 16. TCI_{B+} vs NUMBER OF AMPLIFIERS

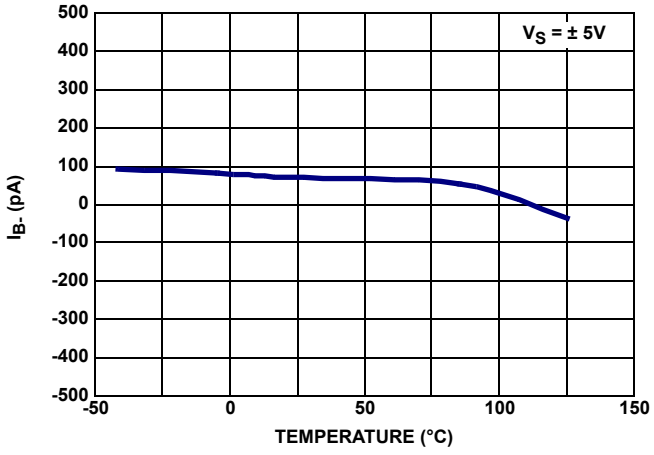


FIGURE 17. I_{B-} RANGE vs TEMPERATURE

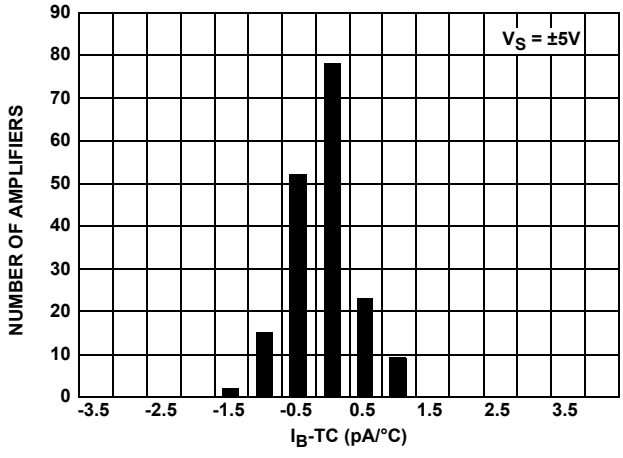


FIGURE 18. TCI_{B-} vs NUMBER OF AMPLIFIERS

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

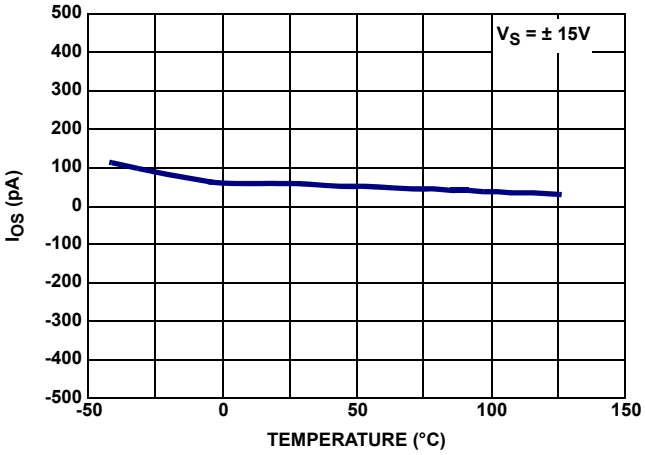


FIGURE 19. I_{OS} RANGE vs TEMPERATURE

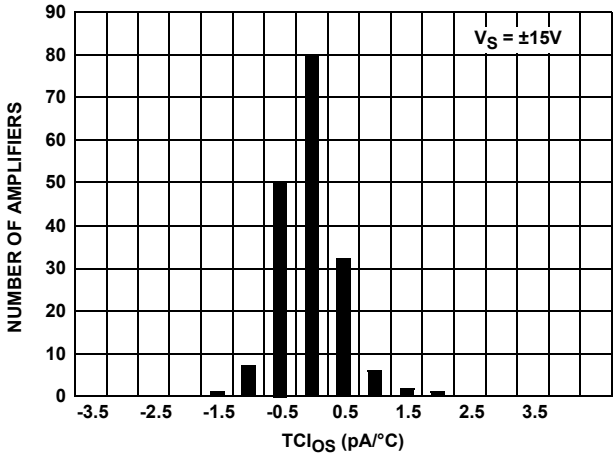


FIGURE 20. $I_{OS}TC$ vs NUMBER OF AMPLIFIERS

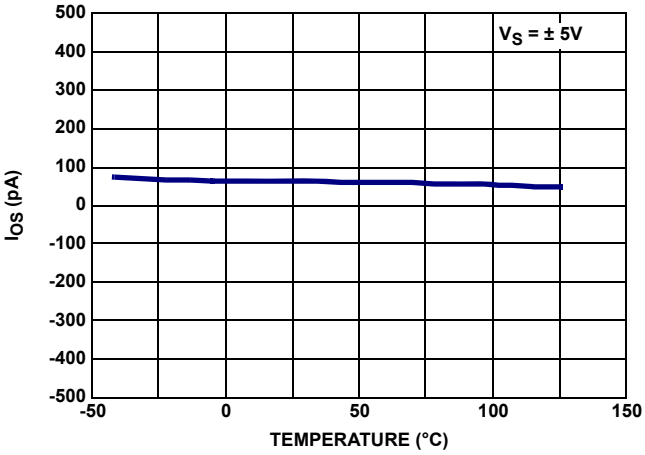


FIGURE 21. I_{OS} RANGE vs TEMPERATURE

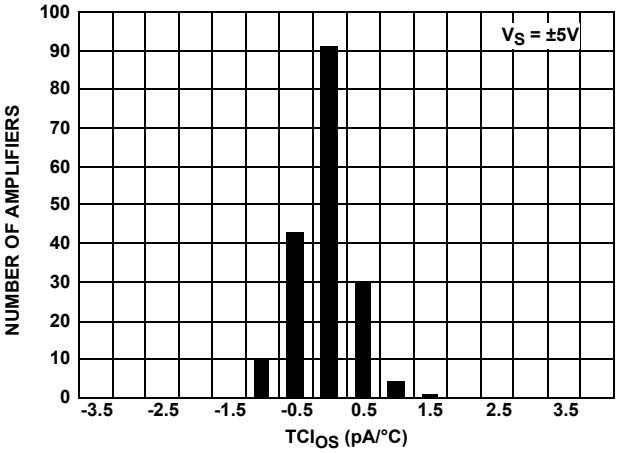


FIGURE 22. $I_{OS}TC$ vs NUMBER OF AMPLIFIERS

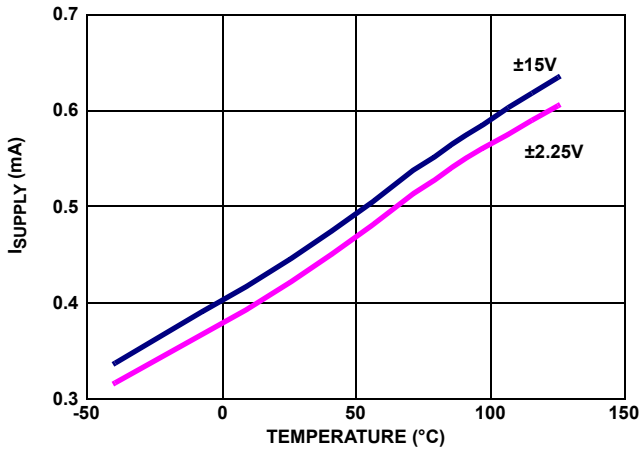


FIGURE 23. SUPPLY CURRENT PER AMPLIFIERS vs TEMPERATURE

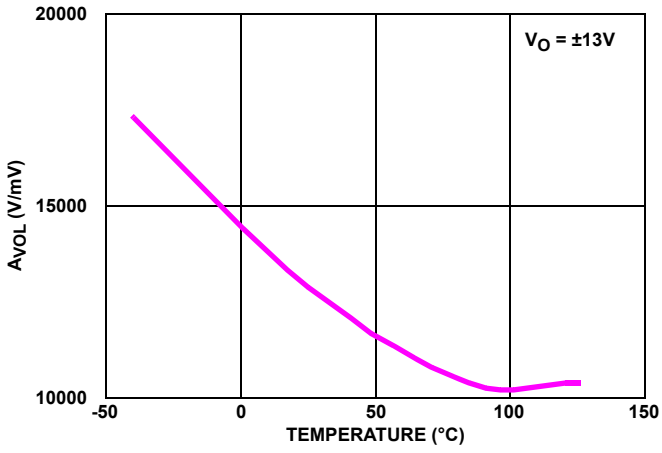


FIGURE 24. A_{VOL} vs TEMPERATURE

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

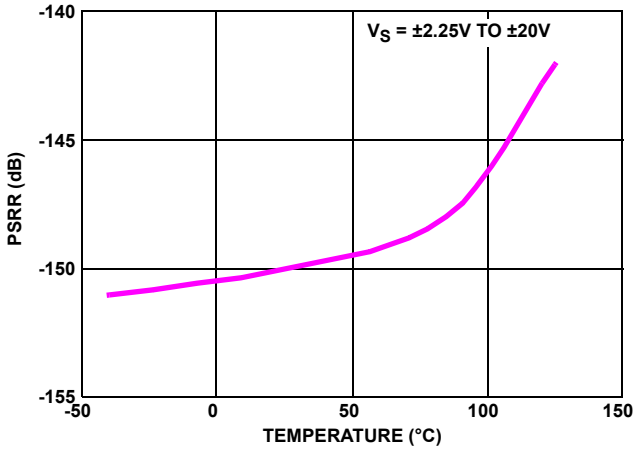


FIGURE 25. PSRR vs TEMPERATURE

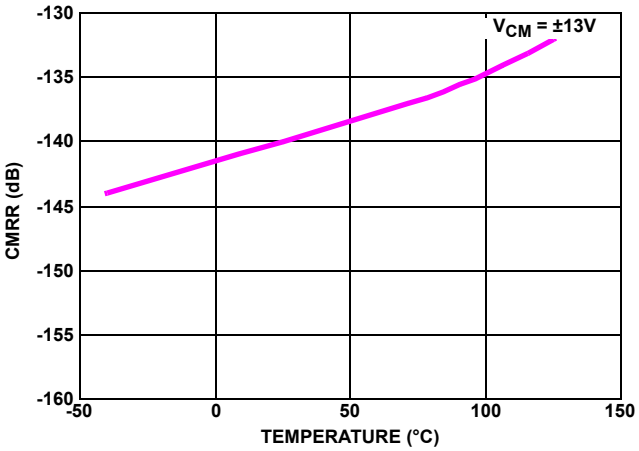


FIGURE 26. CMRR vs TEMPERATURE

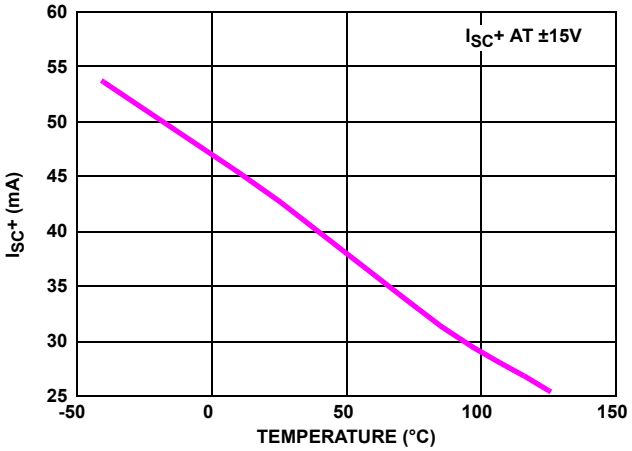


FIGURE 27. POSITIVE SHORT-CIRCUIT CURRENT vs TEMPERATURE

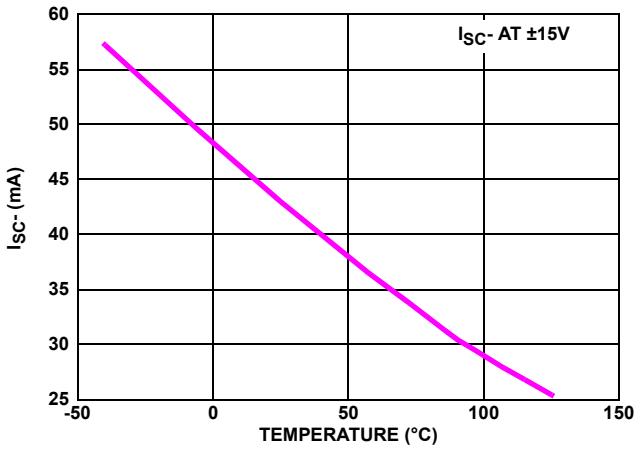


FIGURE 28. NEGATIVE SHORT-CIRCUIT CURRENT vs TEMPERATURE

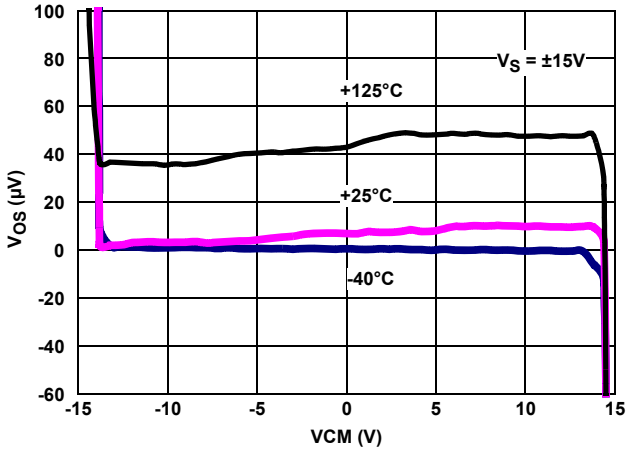


FIGURE 29. INPUT V_{OS} vs INPUT COMMON-MODE VOLTAGE, V_S = ±15

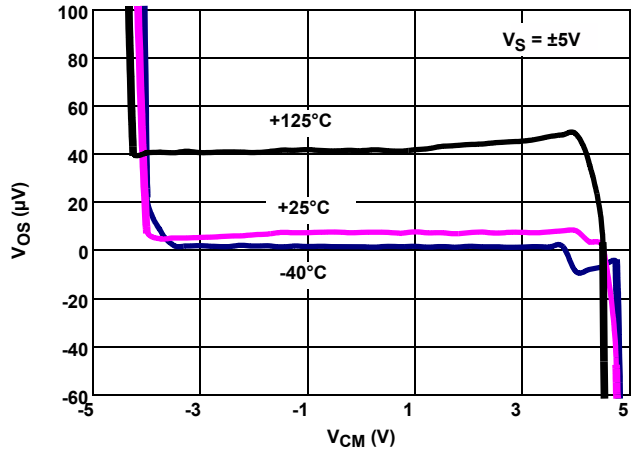


FIGURE 30. INPUT V_{OS} vs INPUT COMMON-MODE VOLTAGE, V_S = ±5V

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

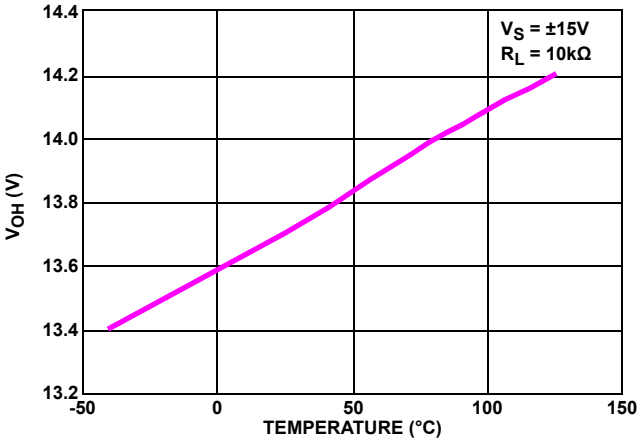


FIGURE 31. V_{OH} vs TEMPERATURE

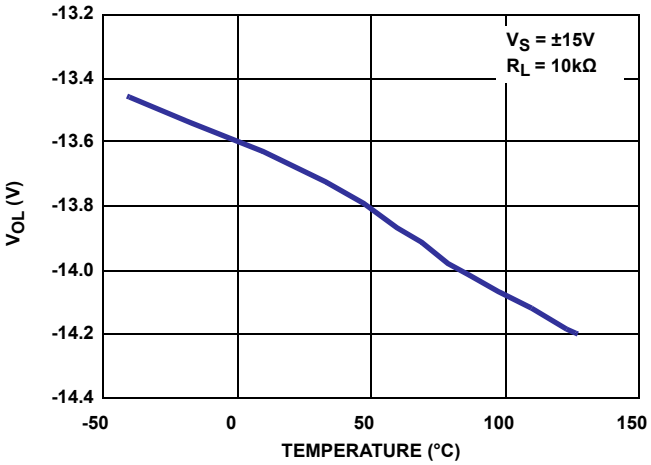


FIGURE 32. V_{OL} vs TEMPERATURE,

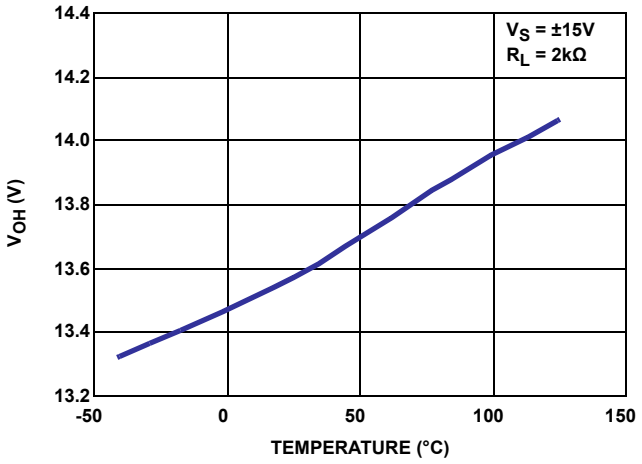


FIGURE 33. V_{OH} vs TEMPERATURE

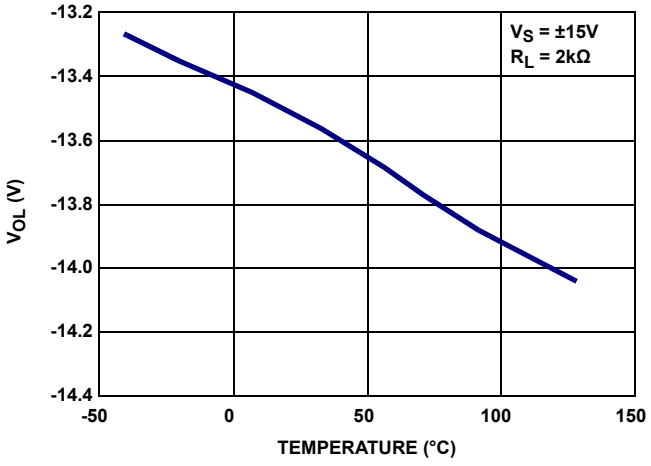


FIGURE 34. V_{OL} vs TEMPERATURE

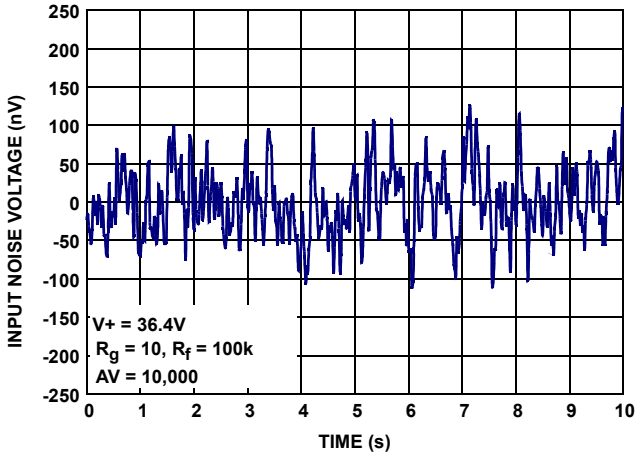


FIGURE 35. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz

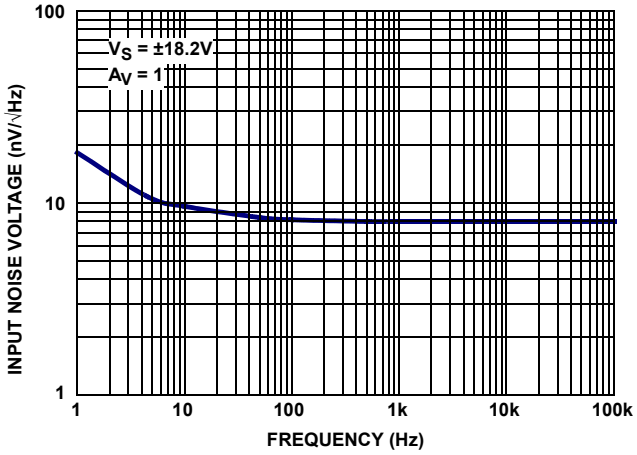


FIGURE 36. INPUT NOISE VOLTAGE SPECTRAL DENSITY

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

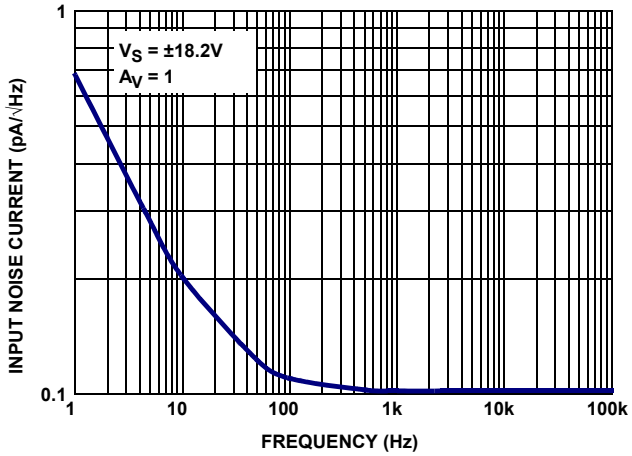


FIGURE 37. INPUT NOISE CURRENT SPECTRAL DENSITY

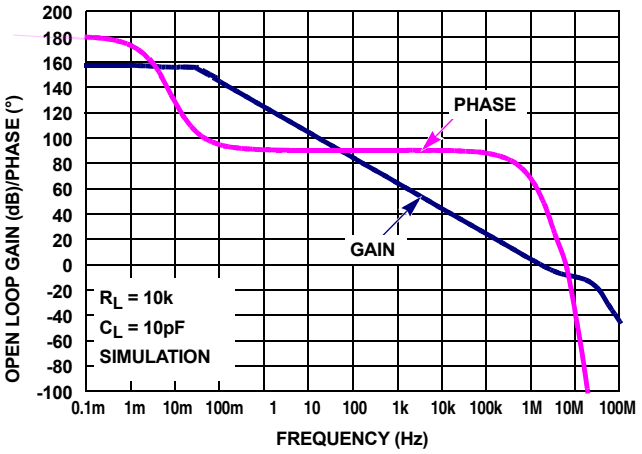


FIGURE 38. OPEN-LOOP GAIN, PHASE vs FREQUENCY, R_L = 10kΩ, C_L = 10pF

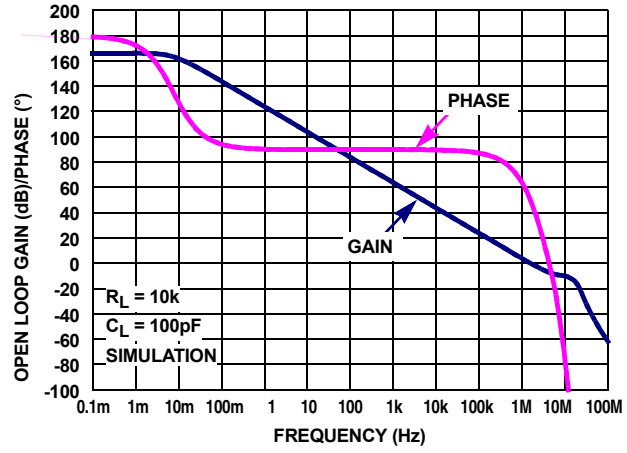


FIGURE 39. OPEN-LOOP GAIN, PHASE vs FREQUENCY, R_L = 10kΩ, C_L = 100pF

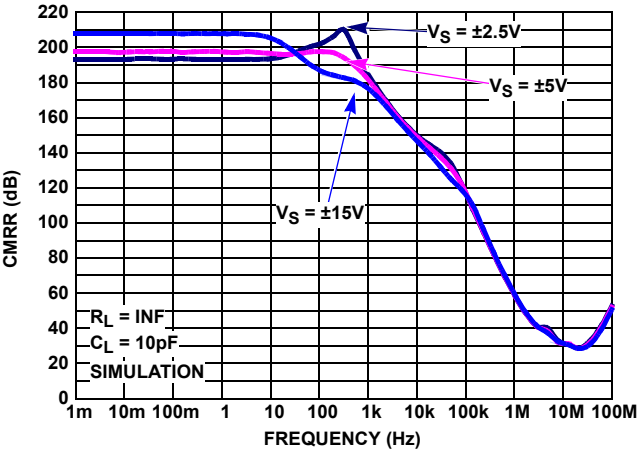


FIGURE 40. CMRR vs FREQUENCY, V_S = ±2.25, ±5V, ±15V

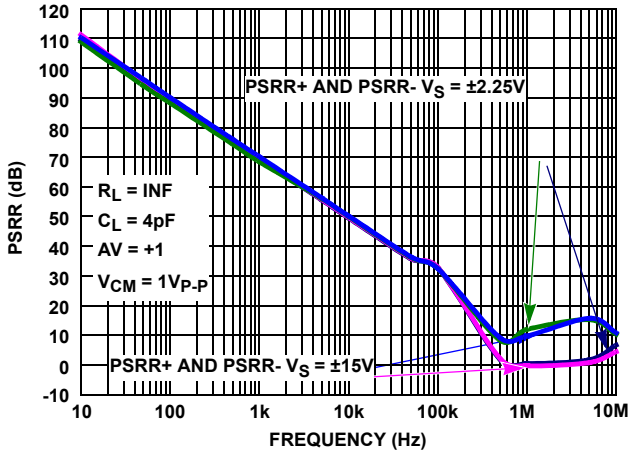


FIGURE 41. PSRR vs FREQUENCY, V_S = ±5V, ±15V

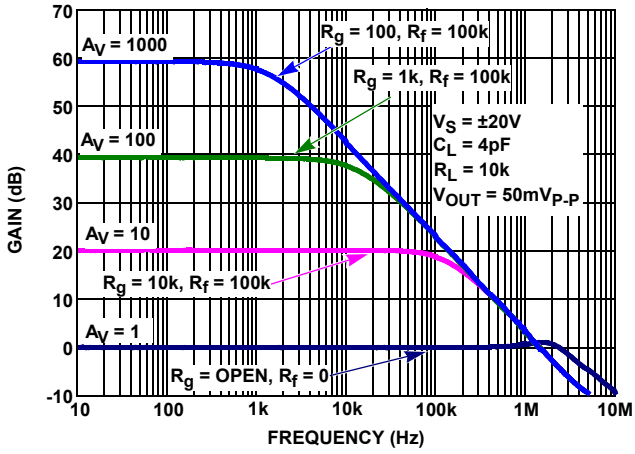


FIGURE 42. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

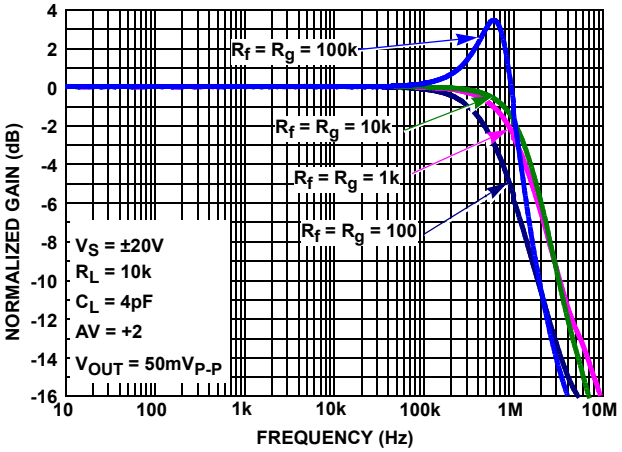


FIGURE 43. FREQUENCY RESPONSE vs FEEDBACK RESISTANCE R_f/R_g

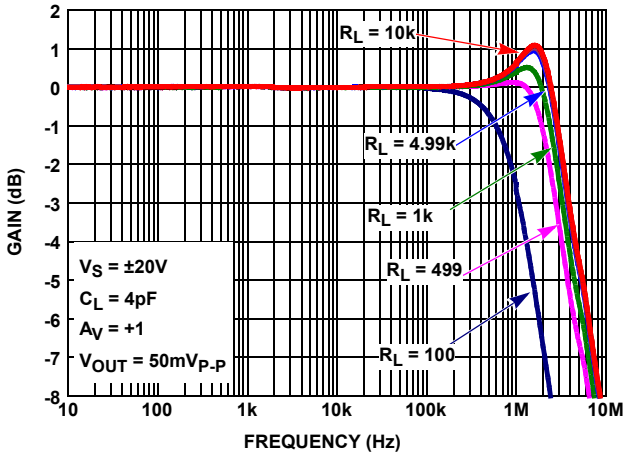


FIGURE 44. GAIN vs FREQUENCY vs R_L

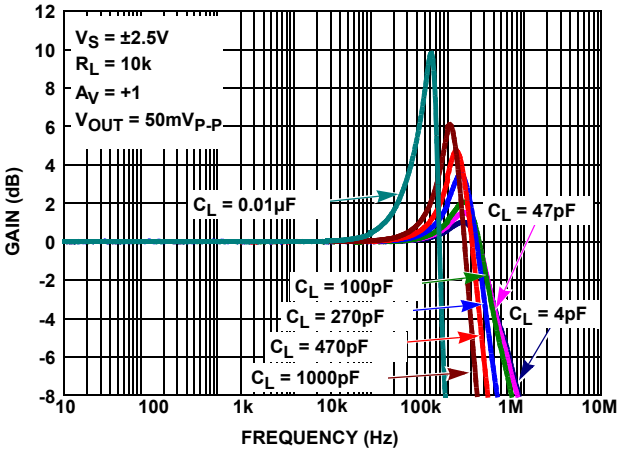


FIGURE 45. GAIN vs FREQUENCY vs C_L

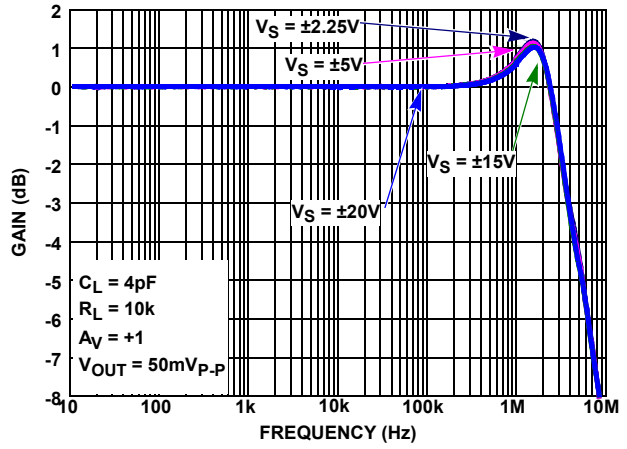


FIGURE 46. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

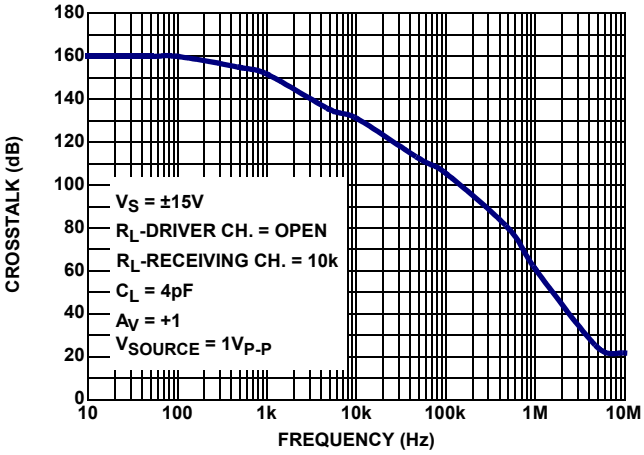


FIGURE 47. CROSSTALK, V_S = ±15V

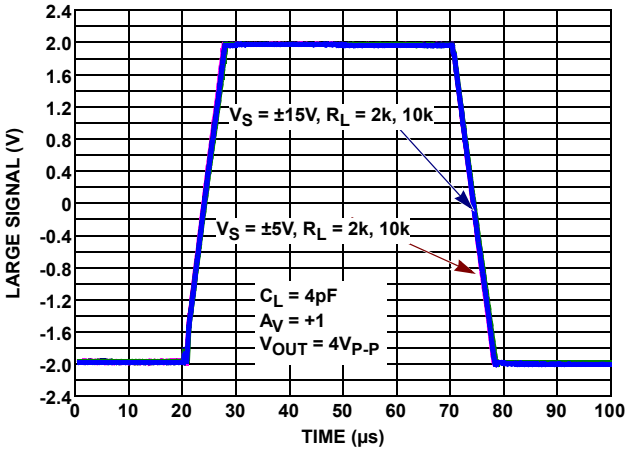


FIGURE 48. LARGE SIGNAL TRANSIENT RESPONSE vs R_L V_S = ±5V, ±15V

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

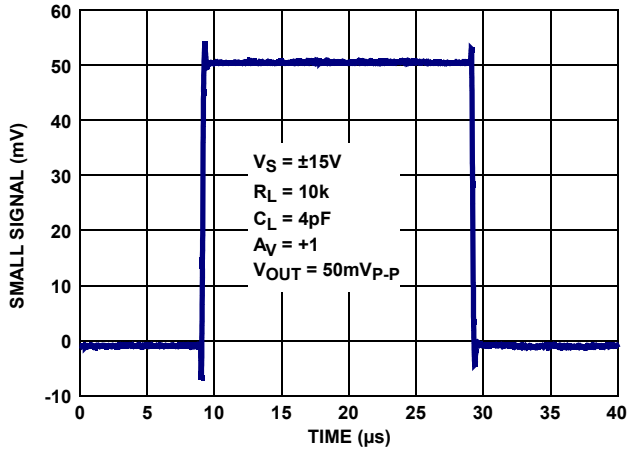


FIGURE 49. SMALL SIGNAL TRANSIENT RESPONSE, V_S = ±5V, ±15V

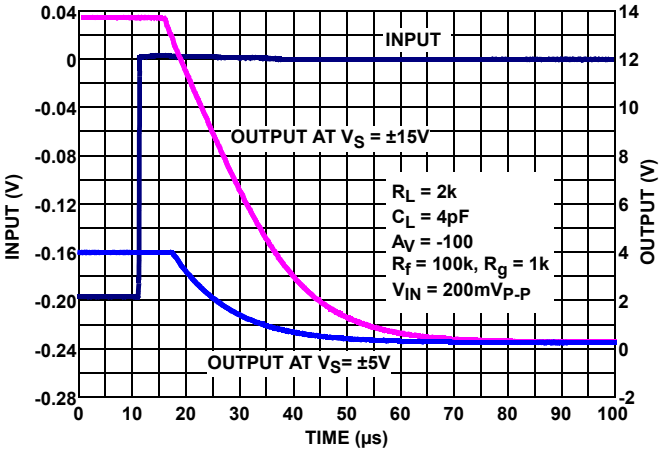


FIGURE 50. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±5V, ±15V

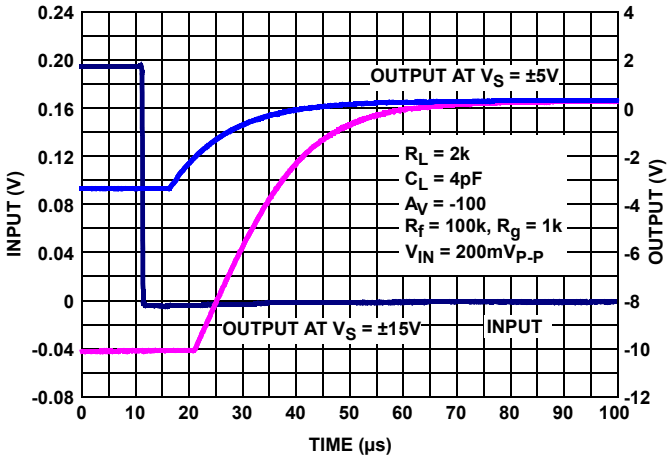


FIGURE 51. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±5V, ±15V

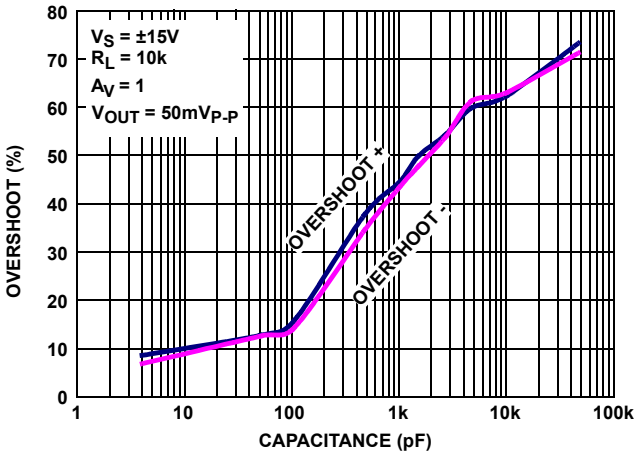


FIGURE 52. % OVERSHOOT vs LOAD CAPACITANCE, V_S = ±15V

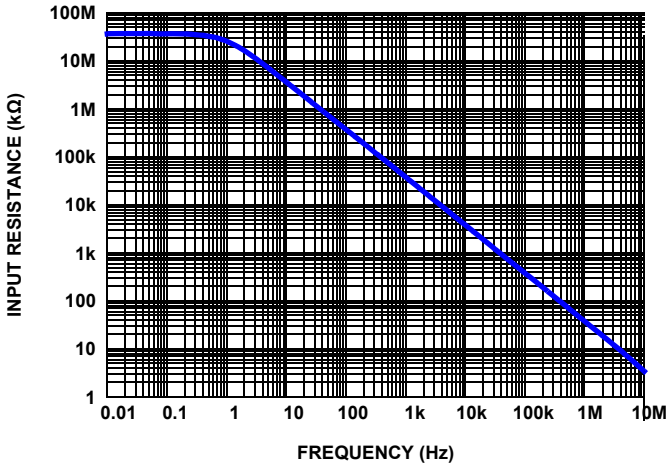


FIGURE 53. COMMON-MODE INPUT IMPEDANCE

Applications Information

Functional Description

The ISL28117, ISL28217, ISL28417 and ISL28417SEH are single, dual and quad, low noise precision op amps. Both devices are fabricated in a new precision 40V complementary bipolar DI process. A super-beta NPN input stage with input bias current cancellation provides low input bias current (180pA typical), low input offset voltage (13µV typical), low input noise voltage (8nV/√Hz) and low 1/f noise corner frequency (~8Hz). These amplifiers also feature high open loop gain (18kV/mV) for excellent CMRR (145dB) and THD+N performance (0.0005% at $3.5V_{RMS}$, 1kHz into 2kΩ). A complimentary bipolar output stage enables high capacitive load drive without external compensation.

Operating Voltage Range

The devices are designed to operate over the 4.5V (±2.25V) to 40V (±20V) range and are fully characterized at 10V (±5V) and 30V (±15V). The Power Supply Rejection Ratio typically exceeds 140dB over the full operating voltage range and 120dB minimum over the -40°C to +125°C temperature range. The worst case common-mode input voltage range over-temperature is 2V to each rail. With ±15V supplies, CMRR performance is typically >130dB over-temperature. The minimum CMRR performance over the -40°C to +125°C temperature range is >120dB for power supply voltages from ±5V (10V) to ±15V (30V).

Input Performance

The super-beta NPN input pair provides excellent frequency response while maintaining high input precision. High NPN beta (>1000) reduces input bias current while maintaining good frequency response, low input bias current and low noise. Input bias cancellation circuits provide additional bias current reduction to <1nA and excellent temperature stabilization. Figures 11 through 18 show the high degree of bias current stability at ±5V and ±15V supplies that is maintained across the -40°C to +125°C temperature range. The low bias current TC also produces very low input offset current TC, which reduces DC input offset errors in precision, high impedance amplifiers.

The +25°C maximum input offset voltage (V_{OS}) for the "B" grade is 50µV and 100µV for the "C" grade. Input offset voltage temperature coefficients ($V_{OS}TC$) are a maximum of ±0.6µV/°C for the "B" and ±0.9µV/°C for the "C" grade. Figures 3 through 6 show the typical gaussian-like distribution over the ±5V to ±15V supply range and over the full temperature range. The V_{OS} temperature behavior is smooth (Figures 7 through 10) maintaining constant TC across the entire temperature range.

Input ESD Diode Protection

The input terminals (IN+ and IN-) have internal ESD protection diodes to the positive and negative supply rails, series connected 500Ω current limiting resistors and an anti-parallel diode pair across the inputs (Figure 54).

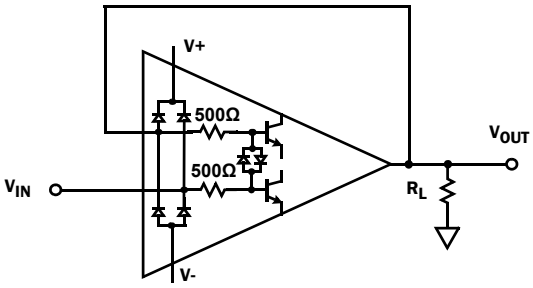


FIGURE 54. INPUT ESD DIODE CURRENT LIMITING- UNITY GAIN

The series resistors limit the high feed-through currents that can occur in pulse applications when the input dv/dt exceeds the 0.5V/µs slew rate of the amplifier. Without the series resistors, the input can forward-bias the anti-parallel diodes causing current to flow to the output resulting in severe distortion and possible diode failure. Figure 48 provides an example of distortion free large signal response using a $4V_{P-P}$ input pulse with an input rise time of <1ns. The series resistors enable the input differential voltage to be equal to the maximum power supply voltage (40V) without damage.

In applications where one or both amplifier input terminals are at risk of exposure to high voltages beyond the power supply rails, current limiting resistors may be needed at the input terminal to limit the current through the power supply ESD diodes to 20mA maximum.

Output Current Limiting

The output current is internally limited to approximately ±45mA at +25°C and can withstand a short-circuit to either rail as long as the power dissipation limits are not exceeded. This applies to only 1 amplifier at a time for the dual op amp. Continuous operation under these conditions may degrade long term reliability. Figures 27 and 28 show the current limit variation with temperature.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL28117, ISL28217, ISL28417 and ISL28417SEH are immune to output phase reversal, even when the input voltage is 1V beyond the supplies.

Unused Channels

The user must configure unused channel(s) to prevent them from oscillating. The unused channel(s) oscillates if the input and output pins are floating. This results in higher than expected supply currents and possible noise injection into the other channel(s) being used. The proper way to prevent this oscillation is to short the output to the inverting input and ground the positive input, as shown in Figure 55.

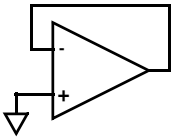


FIGURE 55. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAXTOTAL} \quad \text{(EQ. 1)}$$

Where:

- $PD_{MAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

Where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application

ISL28117, ISL28217, ISL28417, ISL28417SEH SPICE Model

Figure 56 shows the SPICE model schematic and Figure 57 shows the net list for the ISL28117, ISL28217, ISL28417 and ISL28417SEH SPICE model for a Grade “B” part. The model is a simplified version of the actual device and simulates important AC and DC parameters. AC parameters incorporated into the model are: 1/f and flatband noise, Slew Rate, CMRR, Gain and Phase. The DC parameters are VOS, IOS, total supply current and output voltage swing. The model uses typical parameters given in the “Electrical Specifications” table beginning on page 7. The AVOL is adjusted for 155dB with the dominant pole at 0.02Hz. The CMRR is set (210dB, f_{cm} = 10Hz). The input stage models the actual device to present an accurate AC representation. The model is configured for ambient temperature of +25°C.

Figures 58 through 68 show the characterization vs simulation results for the Noise Voltage, Closed Loop Gain vs Frequency, Closed Loop Gain vs RL, Large Signal Step Response, Open Loop Gain Phase and Simulated CMRR vs Frequency.

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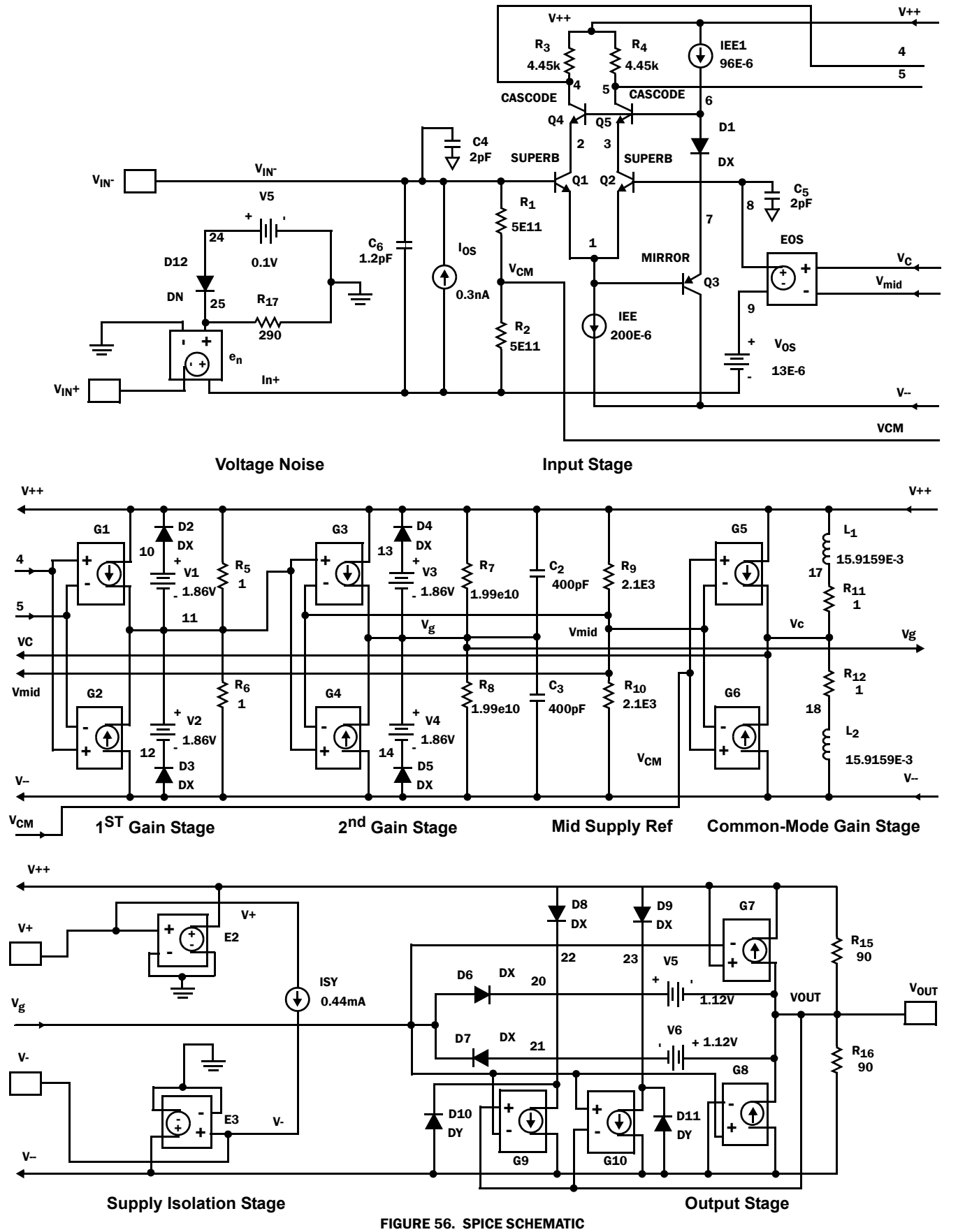

FIGURE 56. SPICE SCHEMATIC