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intersil™

40V Precision Single Supply Rail-to-Rail Output Low Power Operational Amplifiers

ISL28108, ISL28208, ISL28408

The ISL28108, ISL28208 and ISL28408 are single, dual and quad low power precision amplifiers optimized for single supply applications. These devices feature a common mode input voltage range extending to 0.5V below the V- rail, a rail-to-rail differential input voltage range for use as a comparator, and rail-to-rail output voltage swing, which make them ideal for single supply applications where input operation at ground is important.

Added features include low offset voltage, and low temperature drift making them the ideal choice for applications requiring high DC accuracy. The output stage is capable of driving large capacitive loads from rail-to-rail for excellent ADC driving performance. The devices can operate for single or dual supply from 3V (±1.5V) to 40V (±20V) and are fully characterized at ±5V and ±15V. The combination of precision, low power, and small footprint provide the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision instrumentation, data acquisition, precision power supply control, and industrial control.

The ISL28108 single is offered in 8 Ld TDFN, MSOP and SOIC packages. The ISL28208 dual amplifier is offered in 8 Ld TDFN, MSOP, and SOIC packages. The ISL28408 is offered in 14 Ld SOIC package. All devices are offered in standard pin configurations and operate over the extended temperature range of -40°C to +125°C.

Features

- Single or dual supply, rail-to-rail output and below ground (V-) input capability
- Rail-to-rail input differential voltage range for comparator applications
- Single supply range . . . . 3V to 40V
- Low current consumption (V_S = ±5V). 165µA
- Low noise voltage. . . . . 15.8nV/√Hz
- Low noise current. . . . . 80fA/√Hz
- Low input offset voltage (ISL28108) 150µV
- Superb temperature drift
  - Voltage offset TC . . . . 0.1µV/°C, Typ
- Low input bias current. . . . . -13nA Typ
- Operating temperature range. . . . . -40°C to +125°C
- No phase reversal

Applications

- Precision instruments
- Medical instrumentation
- Data acquisition
- Power supply control
- Industrial process control

Related Literature

- AN1658, "ISL28208SOICEVAL2Z Evaluation Board User Guide"

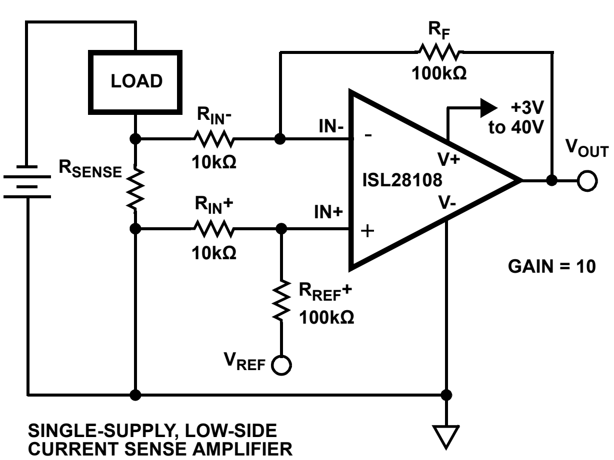


FIGURE 1. TYPICAL APPLICATION CIRCUIT

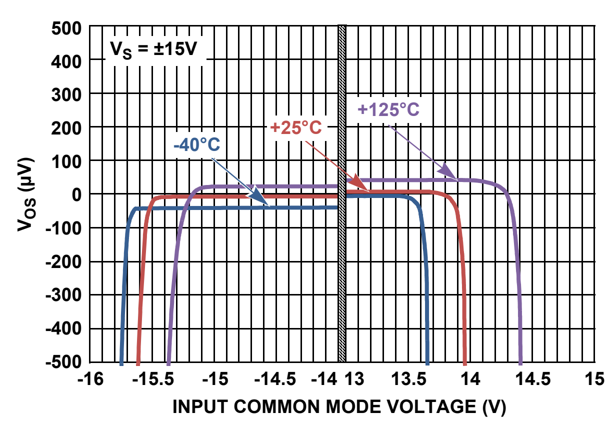


FIGURE 2. INPUT OFFSET VOLTAGE vs INPUT COMMON MODE VOLTAGE, V_S = ±15V

Table of Contents

Ordering Information

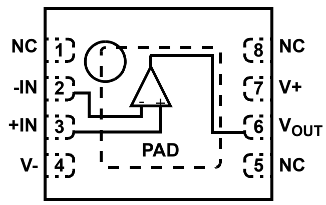
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28108FBZ	28108 FBZ	-40 to +125	8 Ld SOIC	M8.15E
ISL28108FRTZ	108Z	-40 to +125	8 Ld TDFN	L8.3x3K
Coming soon ISL28108FUZ	8108Z	-40 to +125	8 Ld MSOP	M8.118B
ISL28208FBZ	28208 FBZ	-40 to +125	8 Ld SOIC	M8.15E
ISL28208FRTZ	208F	-40 to +125	8 Ld TDFN	L8.3x3K
ISL28208FUZ	8208Z	-40 to +125	8 Ld MSOP	M8.118B
ISL28408FBZ	28408 FBZ	-40 to +125	14 Ld SOIC	M14.15
ISL28208SOICEVAL2Z	Evaluation Board			

NOTES:

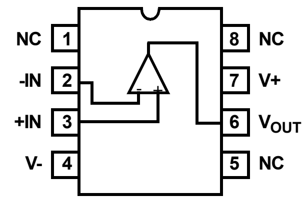
1. Add "-T*" suffix for tape and reel. Please refer to Tech Brief TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL28108, ISL28208, ISL28408. For more information on MSL please see Tech Brief TB363.

Pin Configurations

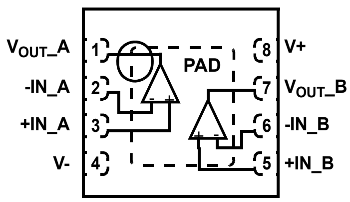
ISL28108
(8 LD TDFN)
TOP VIEW



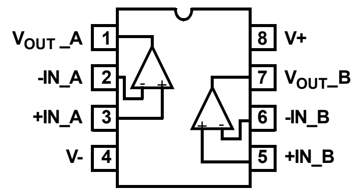
ISL28108
(8 LD MSOP, SOIC)
TOP VIEW



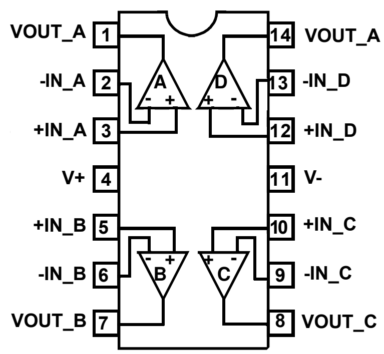
ISL28208
(8 LD TDFN)
TOP VIEW



ISL28208
(8 LD MSOP, SOIC)
TOP VIEW

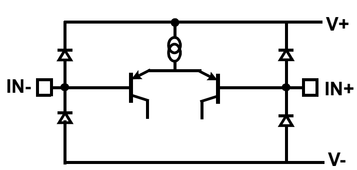


ISL28408
(14 LD SOIC)
TOP VIEW

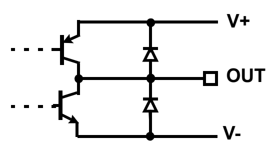


Pin Descriptions

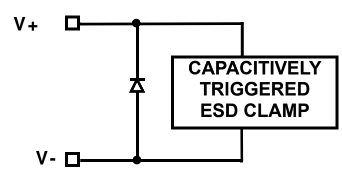
ISL28108 (8 Ld SOIC, MSOP, TDFN)	ISL28208 (8 Ld SOIC, MSOP, TDFN)	ISL28408 (14 Ld SOIC)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	-	-	+IN	Circuit 1	Amplifier non-inverting input
-	3	3	+IN_A		
-	5	5	+IN_B		
-	-	10	+IN_C		
-	-	12	+IN_D		
4	4	11	V-	Circuit 3	Negative power supply
2	-	-	-IN	Circuit 1	Amplifier inverting input
-	2	2	-IN_A		
-	6	6	-IN_B		
-	-	9	-IN_C		
-	-	13	-IN_D		
7	8	4	V+	Circuit 3	Positive power supply
6	-	-	V_{OUT}	Circuit 2	Amplifier output
-	1	1	V_{OUT}_A		
-	7	7	V_{OUT}_B		
-	-	8	V_{OUT}_C		
-	-	14	V_{OUT}_D		
1, 5, 8	-	-	NC	-	No internal connection
PAD	PAD	-	PAD	-	Thermal Pad - TDFN package only. Connect thermal pad to ground or most negative potential.



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Absolute Maximum Ratings

Maximum Supply Voltage 42V
Maximum Differential Input Voltage . . . . 42V or V_- - 0.5V to V_+ + 0.5V
Min/Max Input Voltage . . . . 42V or V_- - 0.5V to V_+ + 0.5V
Max/Min Input Current . . . . ±20mA
Output Short-Circuit Duration (1 output at a time) . . . . Indefinite
ESD Tolerance (ISL28208, ISL28408)
- Human Body Model (Tested per JESD22-A114F) 6kV
- Machine Model (Tested per JESD22-A115-C) 400V
- Charged Device Model (Tested per JESD22-C110D) 2kV

ESD Tolerance (ISL28108)
- Human Body Model (Tested per JESD22-A114F) 5.5kV
- Machine Model (Tested per JESD22-A115-C) 300V
- Charged Device Model (Tested per JESD22-C110D) 2kV

ESD Tolerance (ISL28108 MSOP package only)
- Human Body Model (Tested per JESD22-A114F) 3kV
- Machine Model (Tested per JESD22-A115-C) 300V
- Charged Device Model (Tested per JESD22-C110D) 2kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC Package (208, Notes 4, 7)	120	55
8 Ld SOIC Package (108, Notes 4, 7)	120	60
8 Ld TDFN Package (208, Notes 5, 6)	47	6
8 Ld TDFN Package (108, Notes 5, 6)	45	3.5
8 Ld MSOP Package (208, Notes 4, 7)	150	50
8 Ld MSOP Package (108, Notes 4, 7)	165	57
14 Ld SOIC Package (408, Notes 4, 7)	71	37

Storage Temperature Range . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Ambient Operating Temperature Range . . . . -40°C to +125°C
Maximum Operating Junction Temperature . . . . +150°C
Supply Voltage . . . . 3V (±1.5V) to 40V (±20V)

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
7. For θ_{JC}, the "case temp" location is taken at the package top center.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications, V_S ±15

V_{CM} = 0, V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface entries apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
V_{OS}	Input Offset Voltage	ISL28208 ISL28408	-230	25	230	µV
			-330		**330**	µV
		ISL28108 SOIC, TDFN	-150	10	150	µV
			-270		**270**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient	ISL28208 SOIC -40°C to +125°C		**0.1**	**1.1**	µV/°C
		ISL28208 MSOP -40°C to +125°C		**0.2**	**1.5**	µV/°C
		ISL28208 TDFN ISL28408 -40°C to +125°C		**0.2**	**1.4**	µV/°C
		ISL28108 SOIC, TDFN -40°C to +125°C		**0.2**	**1.2**	µV/°C
ΔV_{OS}	Input Offset Voltage Match (ISL28208 only)	ISL28208 SOIC, TDFN	-300	5	300	µV
			-400		**400**	µV
		ISL28208 MSOP	**-420**		**420**	µV
I_B	Input Bias Current		-43	-13		nA
			-63			nA
TCI_B	Input Bias Current Temperature Coefficient			**0.07**		nA/°C

Electrical Specifications, V_S ±15 V_{CM} = 0, V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface entries apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
I_{OS}	Input Offset Current	ISL28208	-3	0	3	nA
			-4		**4**	nA
		ISL28108 SOIC, TDFN ISL28408	-4	0	4	nA
			-5		**5**	nA
CMRR	Common-Mode Rejection Ratio	V_{CM} = V_- -0.5V to V_+ -1.8V		119		dB
		V_{CM} = V_- -0.2V to V_+ -1.8V		123		dB
				102		dB
		V_{CM} = V_- to V_+ -1.8V	105	123		dB
			102	**115**		dB
V_{CMIR}	Common Mode Input Voltage Range	Guaranteed by CMRR test	V_- - 0.5		V_+ - 1.8	V
			V_-		**V_+ - 1.8**	V
PSRR	Power Supply Rejection Ratio	V_S = 3V to 40V, V_{CMIR} = Valid Input Voltage	110	128		dB
			109	**124**		dB
A_{VOL}	Open-Loop Gain	V_O = -13V to +13V, R_L = 10kΩ to ground	117	126		dB
			100			dB
V_{OL}	Output Voltage Low, V_{OUT} to V_-	R_L = 10kΩ		52	85	mV
					145	mV
V_{OH}	Output Voltage High, V_+ to V_{OUT}	R_L = 10kΩ		70	110	mV
					150	mV
I_S	Supply Current/Amplifier	R_L = Open		185	250	µA
				270	**350**	µA
I_{SC+}	Output Short Circuit Source Current	R_L = 10Ω to V_-		19		mA
I_{SC-}	Output Short Circuit Sink Current	R_L = 10Ω to V_+		30		mA
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	**3**		**40**	V
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_{CL} = 101, V_O = 100mV_{P-P}, R_L = 2kΩ		1.2		MHz
e_{np-p}	Noise Voltage	0.1Hz to 10Hz; V_S = ±18V		580		nVP-P
e_n	Noise Voltage Density	f = 10Hz; V_S = ±18V		18		nV/√Hz
e_n	Noise Voltage Density	f = 100Hz; V_S = ±18V		16		nV/√Hz
e_n	Noise Voltage Density	f = 1kHz; V_S = ±18V		15.8		nV/√Hz
e_n	Noise Voltage Density	f = 10kHz; V_S = ±18V		15.8		nV/√Hz
i_n	Noise Current Density	f = 10kHz; V_S = ±18V		80		fA/√Hz
THD + N	Total Harmonic Distortion + Noise	1kHz, A_V = 1, V_O = 3.5V_{RMS}, R_L =10kΩ		0.00042		%
TRANSIENT RESPONSE						
SR	Slew Rate, V_{OUT} 20% to 80%	A_V = 1, R_L = 2kΩ, V_O = 10V_{P-P}		0.45		V/µs
t_r, t_f, Small Signal	Rise Time, V_{OUT} 10% to 90%	A_V = 1, V_{OUT} = 100mV_{P-P}, R_f = 0Ω, R_L = 2kΩ to V_{CM}		264		ns
	Fall Time, V_{OUT} 90% to 10%	A_V = 1, V_{OUT} = 100mV_{P-P}, R_f = 0Ω, R_L = 2kΩ to V_{CM}		254		ns
t_s	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = 10V_{P-P}, R_g = R_f =10k, R_L = 2kΩ to V_{CM}		27		µs

Electrical Specifications, V_S ±5V V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface entries apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
V_{OS}	Input Offset Voltage	ISL28208 ISL28408	-230	25	230	µV
			-330		**330**	µV
		ISL28108 SOIC, TDFN	-150	10	150	µV
			-270		**270**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient	ISL28208 SOIC **-40°C to +125°C**		**0.1**	**1.1**	µV/°C
		ISL28208 MSOP **-40°C to +125°C**		**0.2**	**1.5**	µV/°C
		ISL28208 TDFN ISL28408 **-40°C to +125°C**		**0.2**	**1.4**	µV/°C
		ISL28108 SOIC, TDFN **-40°C to +125°C**		**0.2**	**1.2**	µV/°C
ΔV_{OS}	Input Offset Voltage Match (ISL28208 only)		-300	3	300	µV
			-400		**400**	µV
I_B	Input Bias Current		-43	-15		nA
			-63			nA
TCI_B	Input Bias Current Temperature Coefficient	**-40°C to +125°C**		**-0.067**		nA/°C
I_{OS}	Input Offset Current	ISL28208	-3	0	3	nA
			-4		**4**	nA
		ISL28108 SOIC, TDFN ISL28408	-4	0	4	nA
			-5		**5**	nA
CMRR	Common-Mode Rejection Ratio	V_{CM} = V_- -0.5V to V_+ -1.8V		101		dB
		V_{CM} = V_- -0.2V to V_+ -1.8V		123		dB
				89		dB
		V_{CM} = V_- to V_+ -1.8V ISL28108, ISL28208	105	123		dB
			100	**112**		dB
		V_{CM} = V_- to V_+ -1.8V ISL28408	105	123		dB
			97	**112**		dB
V_{CMIR}	Common Mode Input Voltage Range	Guaranteed by CMRR test	V_- - 0.5		V_+ - 1.8	V
			V_-		**V_+ - 1.8**	V
PSRR	Power Supply Rejection Ratio	V_S = 3V to 10V, V_{CMIR} = Valid Input Voltage All except ISL28208 MSOP	110	126		dB
			109	**123**		dB
		ISL28208 MSOP V_S = 3V to 10V, V_{CMIR} = Valid Input Voltage	109	126		dB
			107	**123**		dB
A_{VOL}	Open-Loop Gain	V_O = -3V to +3V, R_L = 10kΩ to ground	117	124		dB
			99			dB
V_{OL}	Output Voltage Low, V_{OUT} to V_-	R_L = 10kΩ		23	38	mV
					48	mV
V_{OH}	Output Voltage High, V_+ to V_{OUT}	R_L = 10kΩ		30	65	mV
					70	mV

Electrical Specifications, V_S ±5V

V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface entries apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
I_S	Supply Current/Amplifier	R_L = Open		165	250	µA
				240	**350**	µA
I_{SC+}	Output Short Circuit Source Current	R_L = 10Ω to V_-		14		mA
I_{SC-}	Output Short Circuit Sink Current	R_L = 10Ω to V_+		22		mA
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product	A_{CL} = 101, V_O = 100mV_{P-P}, R_L = 2kΩ		1.2		MHz
e_{np-p}	Noise Voltage	0.1Hz to 10Hz		600		nV_{P-P}
e_n	Noise Voltage Density	f = 10Hz		18		nV/√Hz
e_n	Noise Voltage Density	f = 100Hz		16		nV/√Hz
e_n	Noise Voltage Density	f = 1kHz		15.8		nV/√Hz
e_n	Noise Voltage Density	f = 10kHz		15.8		nV/√Hz
i_n	Noise Current Density	f = 10kHz		90		fA/√Hz
TRANSIENT RESPONSE						
SR	Slew Rate, V_{OUT} 20% to 80%	A_V = 1, R_L = 2kΩ, V_O = 4V_{P-P}		0.4		V/µs
t_r, t_f, Small Signal	Rise Time, V_{OUT} 10% to 90%	A_V = 1, V_{OUT} = 100mV_{P-P}, R_f = 0Ω, R_L = 2kΩ to V_{CM}		264		ns
	Fall Time, V_{OUT} 90% to 10%	A_V = 1, V_{OUT} = 100mV_{P-P}, R_f = 0Ω, R_L = 2kΩ to V_{CM}		254		ns
t_s	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = 4V_{P-P}, R_g = R_f =10k, R_L = 2kΩ to V_{CM}		14.4		µs

NOTE:

8. Compliance to data sheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified.

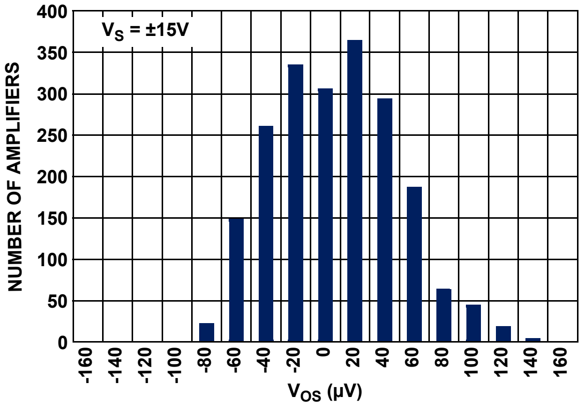


FIGURE 3. ISL28408 SOIC INPUT OFFSET VOLTAGE DISTRIBUTION, V_S = ±15V

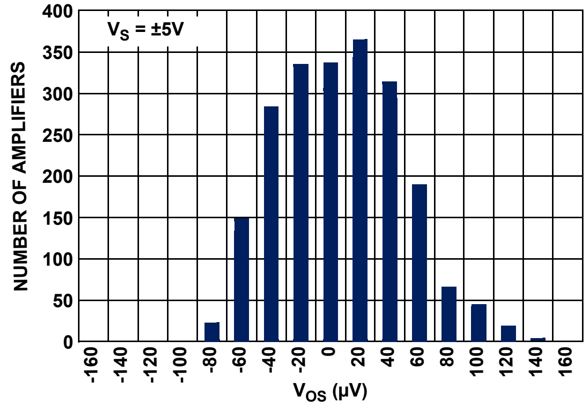


FIGURE 4. ISL28408 SOIC INPUT OFFSET VOLTAGE DISTRIBUTION, V_S = ±5V

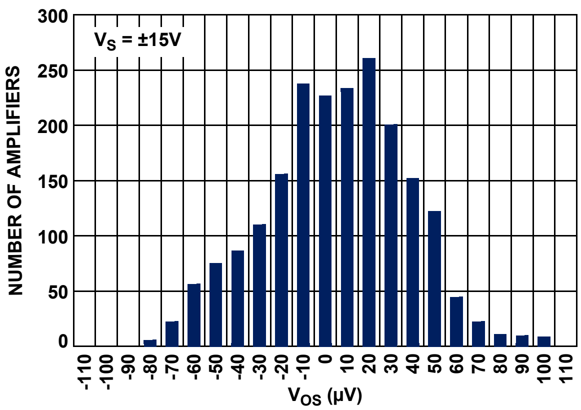


FIGURE 5. ISL28208 INPUT OFFSET VOLTAGE DISTRIBUTION, V_S = ±15V

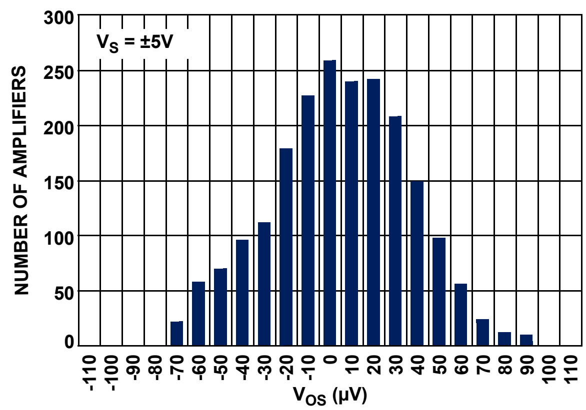


FIGURE 6. ISL28208 INPUT OFFSET VOLTAGE DISTRIBUTION, V_S = ±5V

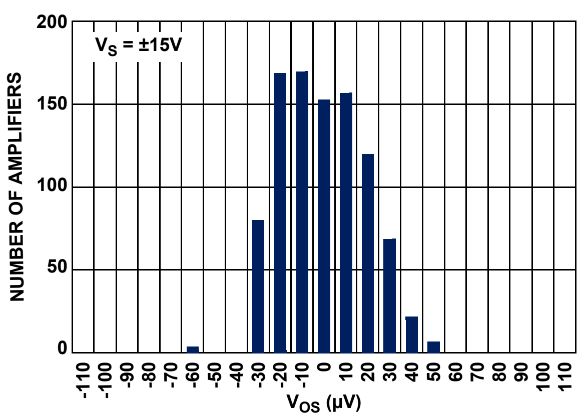


FIGURE 7. ISL28108 SOIC INPUT OFFSET VOLTAGE DISTRIBUTION, V_S = ±15V

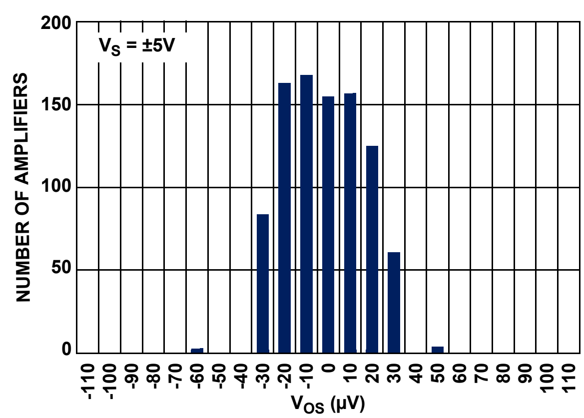


FIGURE 8. ISL28108 SOIC INPUT OFFSET VOLTAGE DISTRIBUTION, V_S = ±5V

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

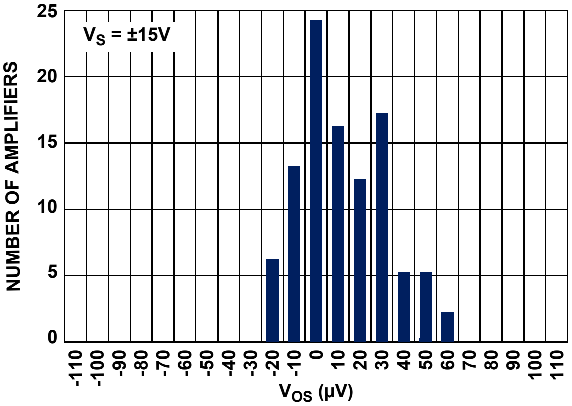


FIGURE 9. ISL28108 TDFN INPUT OFFSET VOLTAGE DISTRIBUTION, V_S = ±15V

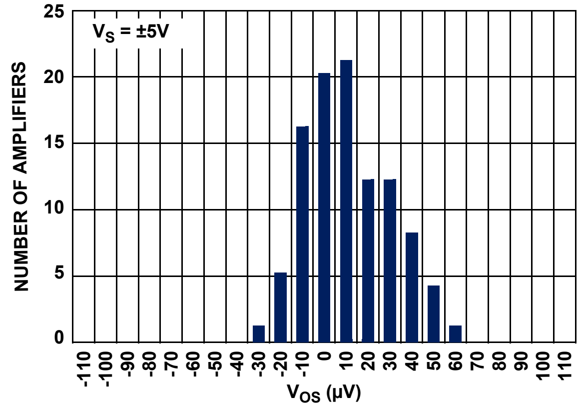


FIGURE 10. ISL28108 TDFN INPUT OFFSET VOLTAGE DISTRIBUTION, V_S = ±5V

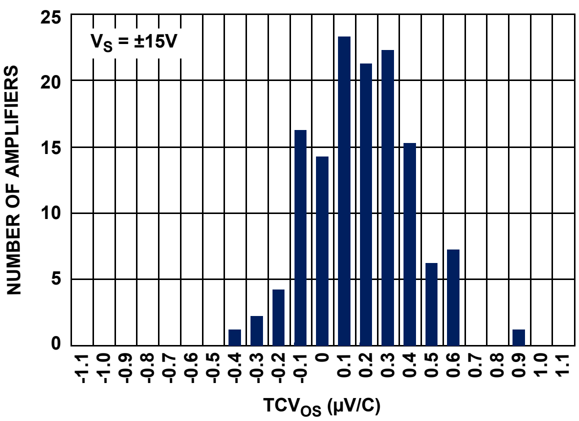


FIGURE 11. ISL28408 SOIC TCV_{OS} vs NUMBER OF AMPLIFIERS, V_S = ±15V

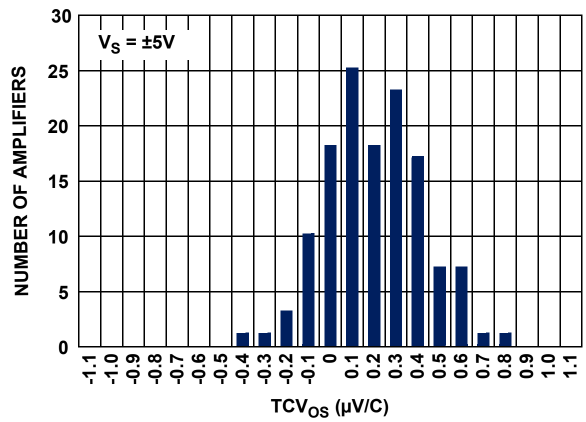


FIGURE 12. ISL28408 SOIC TCV_{OS} vs NUMBER OF AMPLIFIERS, V_S = ±5V

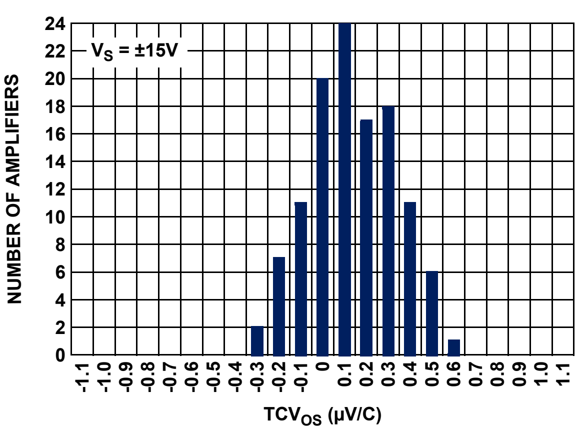


FIGURE 13. ISL28208 SOIC TCV_{OS} vs NUMBER OF AMPLIFIERS, V_S = ±15V

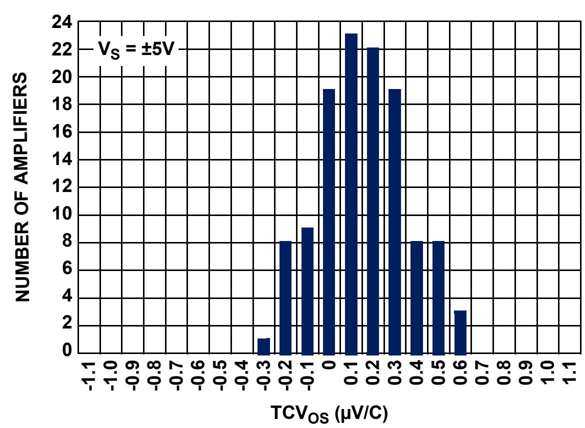


FIGURE 14. ISL28208 SOIC TCV_{OS} vs NUMBER OF AMPLIFIERS, V_S = ±5V

Typical Performance Curves $V_S = \pm 15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. **(Continued)**

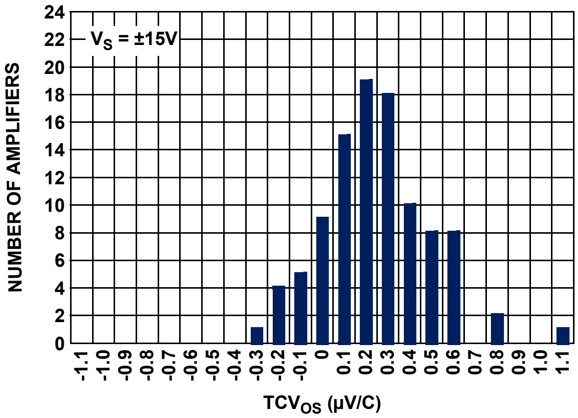


FIGURE 15. ISL28208 TDFN AND MSOP TCV_{OS} vs NUMBER OF AMPLIFIERS, $V_S = \pm 15V$

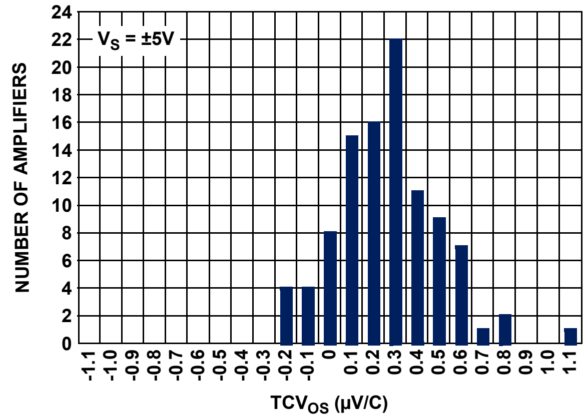


FIGURE 16. ISL28208 TDFN AND MSOP TCV_{OS} vs NUMBER OF AMPLIFIERS, $V_S = \pm 5V$

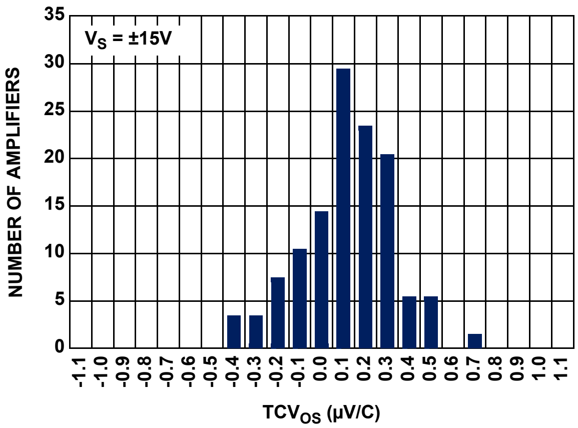


FIGURE 17. ISL28108 SOIC TCV_{OS} vs NUMBER OF AMPLIFIERS, $V_S = \pm 15V$

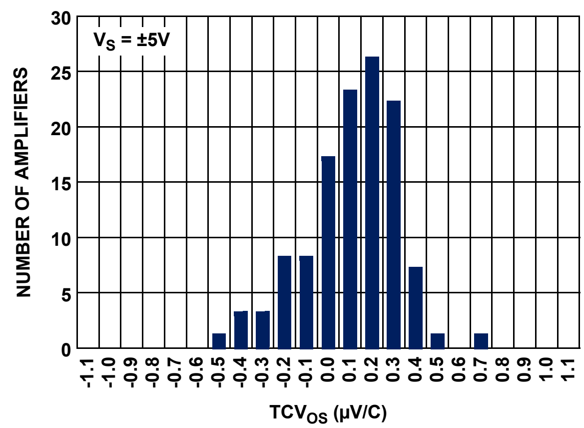


FIGURE 18. ISL28108 SOIC TCV_{OS} vs NUMBER OF AMPLIFIERS, $V_S = \pm 5V$

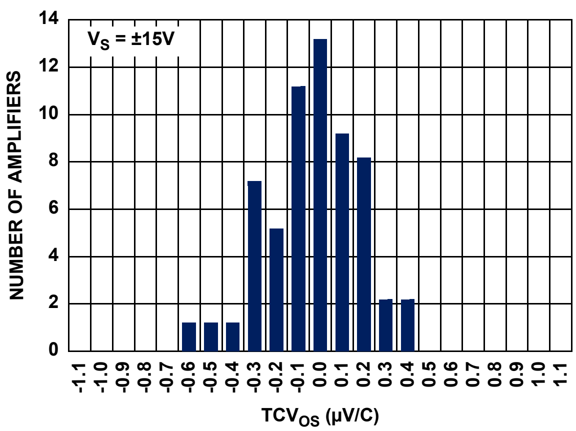


FIGURE 19. ISL28108 TDFN TCV_{OS} vs NUMBER OF AMPLIFIERS, $V_S = \pm 15V$

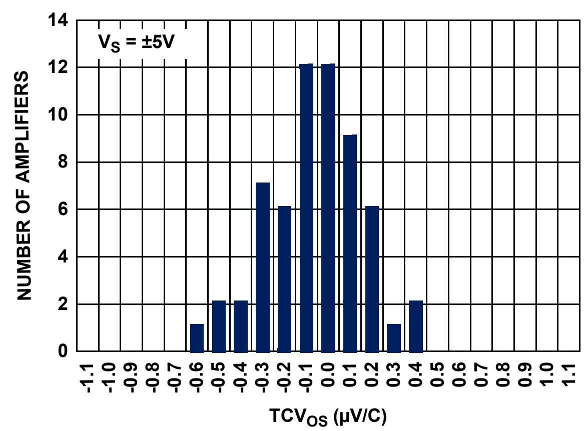


FIGURE 20. ISL28108 TDFN TCV_{OS} vs NUMBER OF AMPLIFIERS, $V_S = \pm 5V$

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

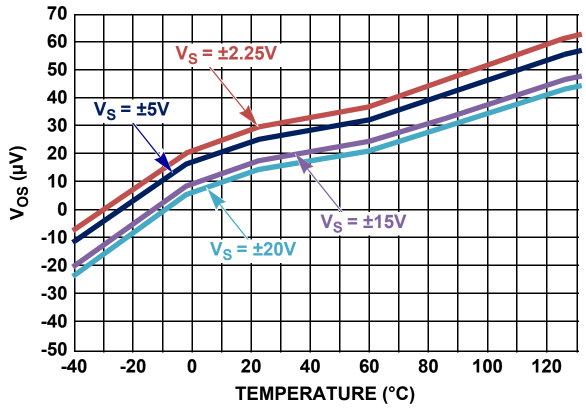


FIGURE 21. V_{OS} vs TEMPERATURE

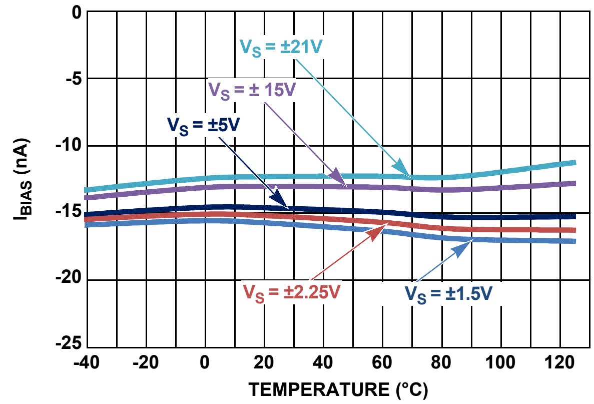


FIGURE 22. I_{BIAS} vs TEMPERATURE vs SUPPLY

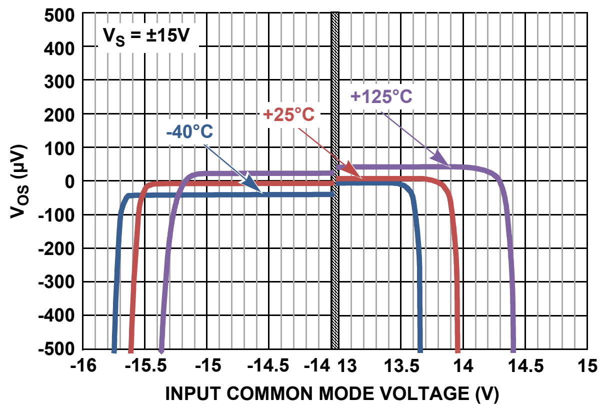


FIGURE 23. INPUT OFFSET VOLTAGE vs INPUT COMMON MODE VOLTAGE, V_S = ±15V

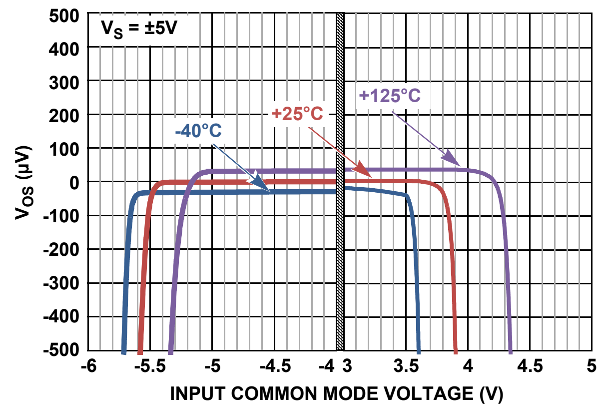


FIGURE 24. INPUT OFFSET VOLTAGE vs INPUT COMMON MODE VOLTAGE, V_S = ±5V

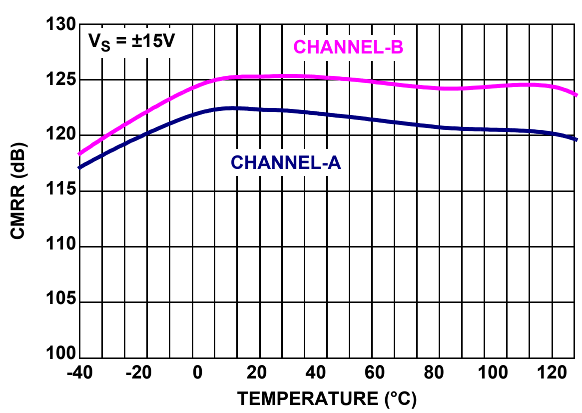


FIGURE 25. CMRR vs TEMPERATURE, V_S = ±15V

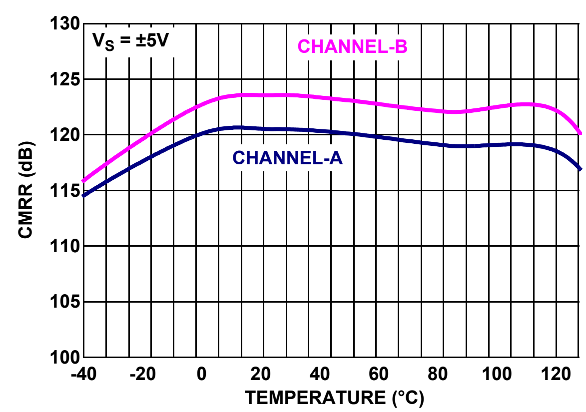


FIGURE 26. CMRR vs TEMPERATURE, V_S = ±5V

Typical Performance Curves
V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

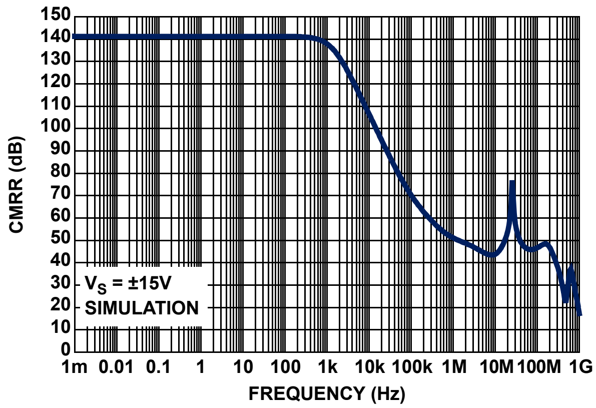


FIGURE 27. CMRR vs FREQUENCY, V_S = ±15V

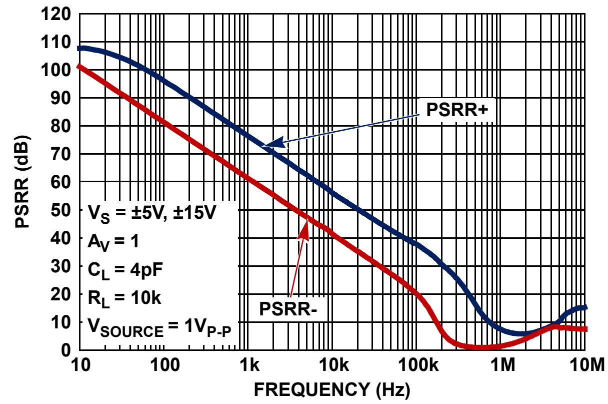


FIGURE 28. PSRR vs FREQUENCY, V_S = ±5V AND ±15V

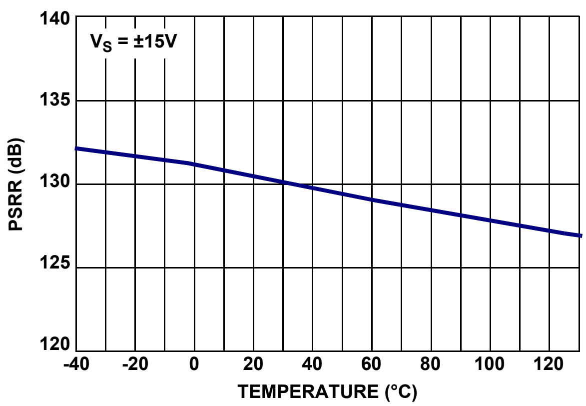


FIGURE 29. PSRR (DC) vs TEMPERATURE, V_S = ±15V

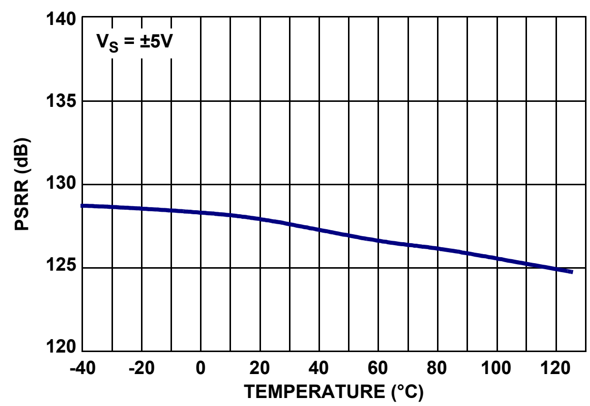


FIGURE 30. PSRR (DC) vs TEMPERATURE, V_S = ±5V

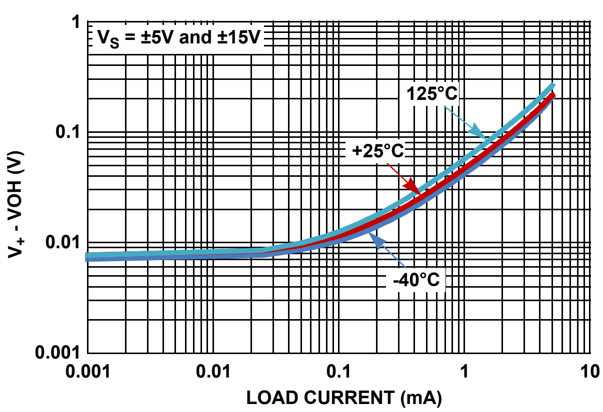


FIGURE 31. OUTPUT OVERHEAD VOLTAGE HIGH vs LOAD CURRENT, V_S = ±5V AND ±15V

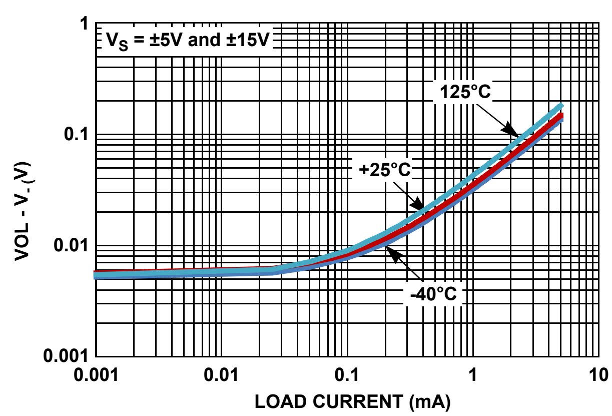


FIGURE 32. OUTPUT OVERHEAD VOLTAGE LOW vs LOAD CURRENT, V_S = ±5V AND ±15V

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

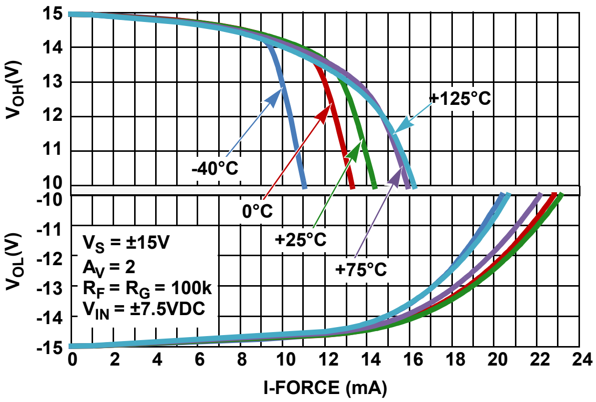


FIGURE 33. ISL28208 OUTPUT VOLTAGE SWING vs LOAD CURRENT V_S = ±15V

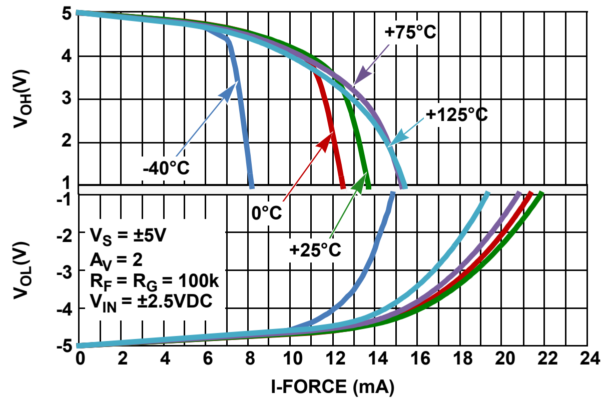


FIGURE 34. ISL28208 OUTPUT VOLTAGE SWING vs LOAD CURRENT V_S = ±5V

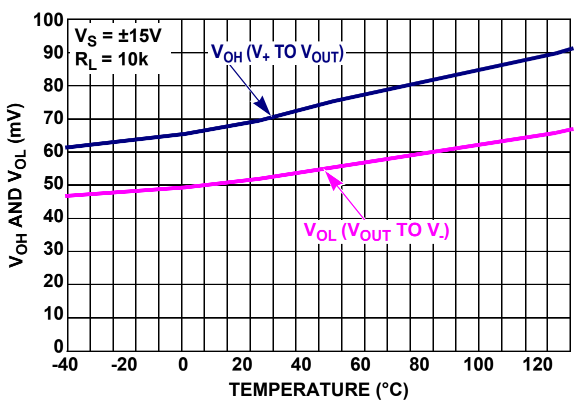


FIGURE 35. V_{OUT} HIGH AND LOW vs TEMPERATURE, V_S = ±15V, R_L = 10k

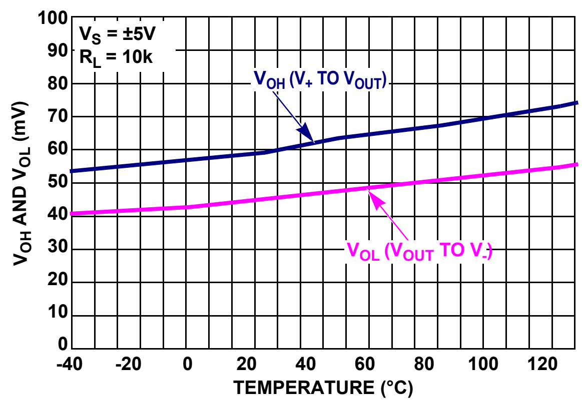


FIGURE 36. V_{OUT} HIGH AND LOW vs TEMPERATURE, V_S = ±5V, R_L = 10k

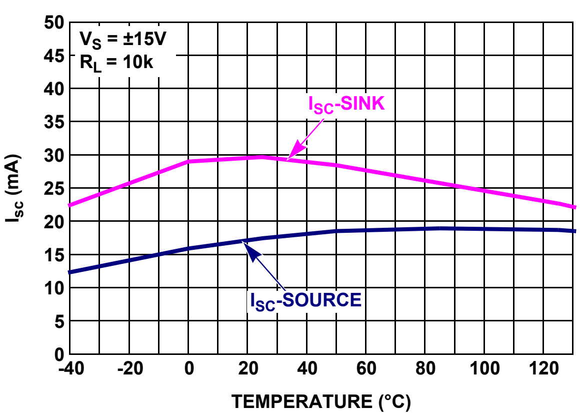


FIGURE 37. SHORT CIRCUIT CURRENT vs TEMPERATURE, V_S = ±15V

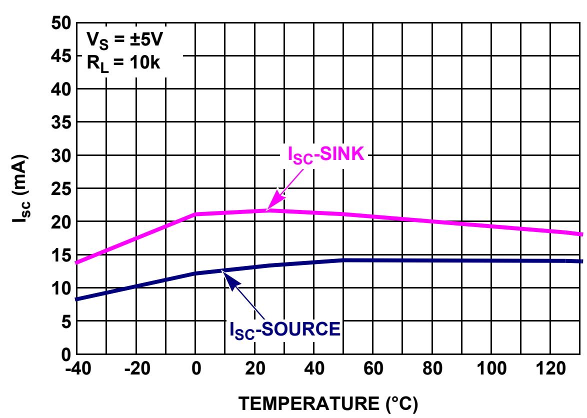


FIGURE 38. SHORT CIRCUIT CURRENT vs TEMPERATURE, V_S = ±5V

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

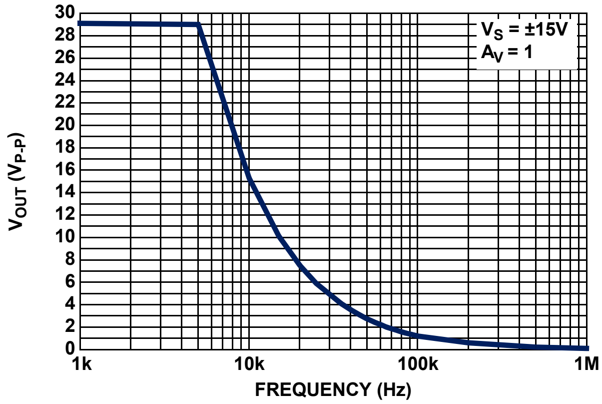


FIGURE 39. MAX OUTPUT VOLTAGE vs FREQUENCY

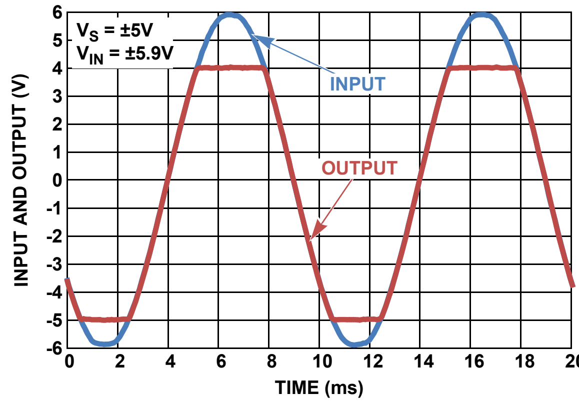


FIGURE 40. NO PHASE REVERSAL

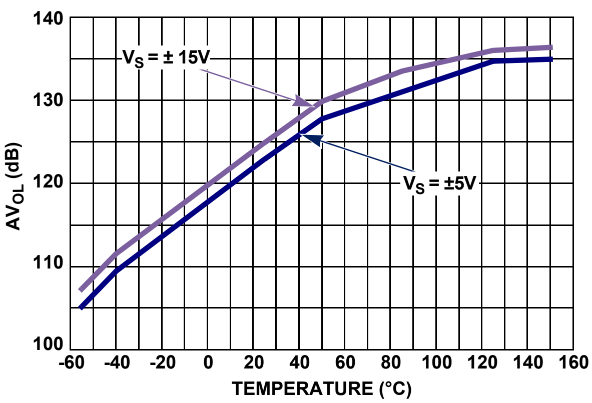


FIGURE 41. AV_{OL} vs TEMPERATURE

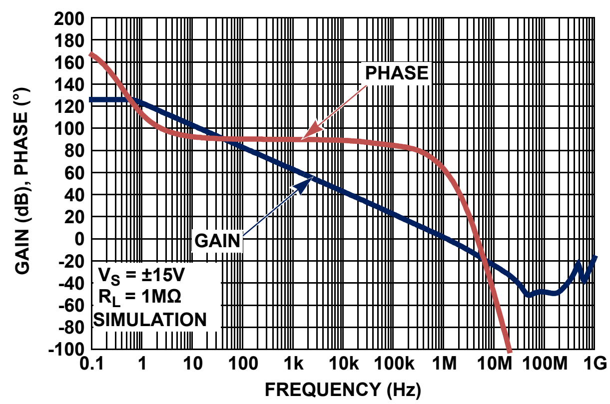


FIGURE 42. OPEN-LOOP GAIN, PHASE vs FREQUENCY, V_S = ±15V

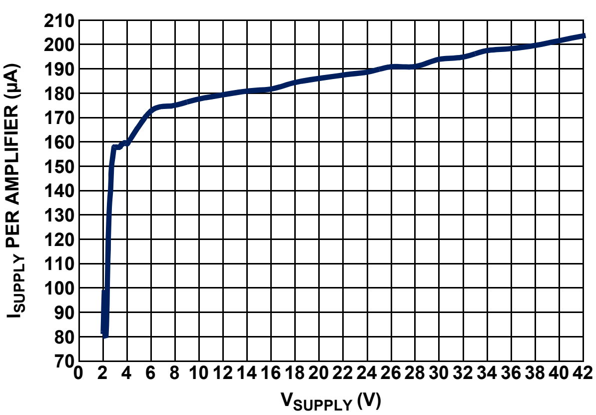


FIGURE 43. SUPPLY CURRENT vs SUPPLY VOLTAGE

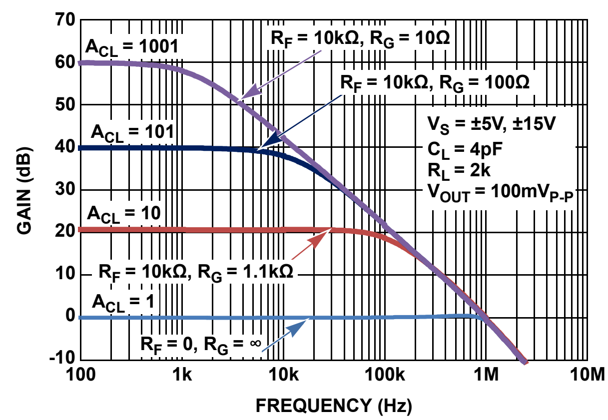


FIGURE 44. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

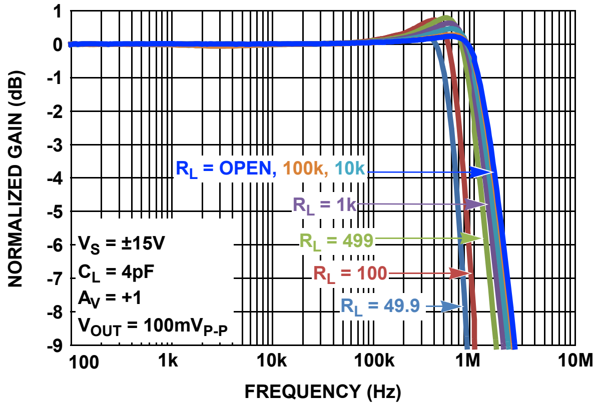


FIGURE 45. GAIN vs FREQUENCY vs R_L, V_S = ±15V

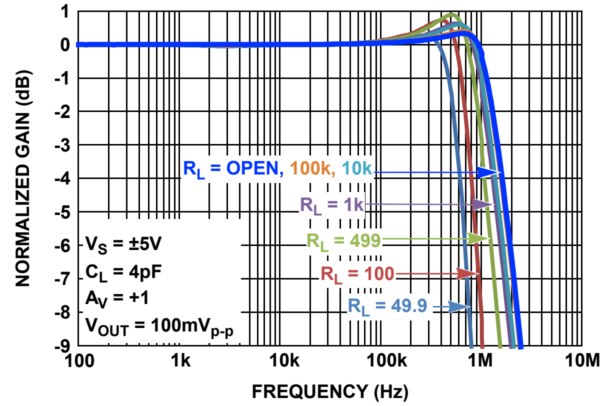


FIGURE 46. GAIN vs FREQUENCY vs R_L, V_S = ±5V

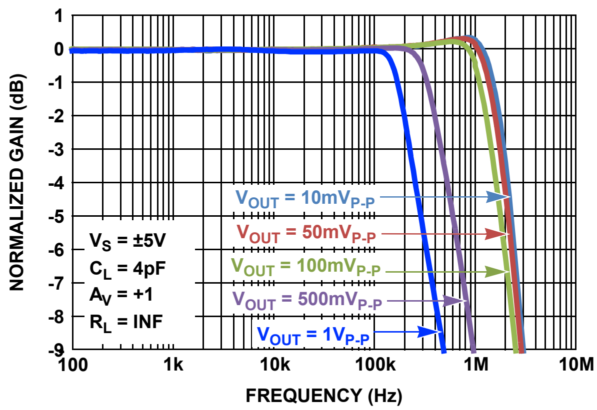


FIGURE 47. GAIN vs FREQUENCY vs OUTPUT VOLTAGE

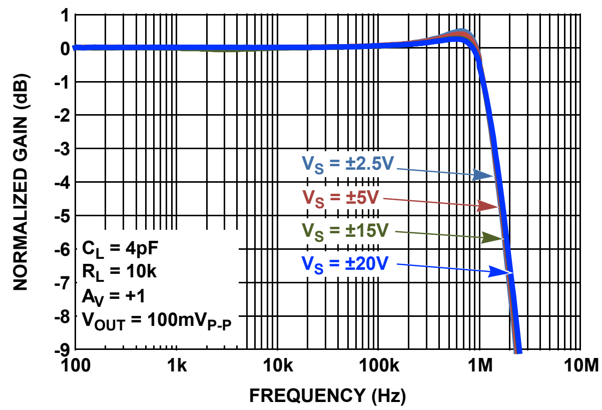


FIGURE 48. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

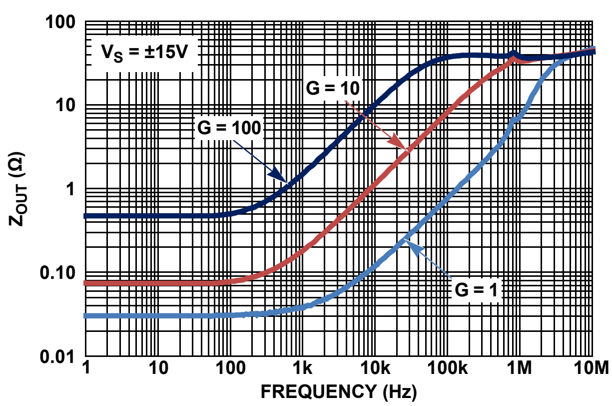


FIGURE 49. OUTPUT IMPEDANCE vs FREQUENCY, V_S = ±15V

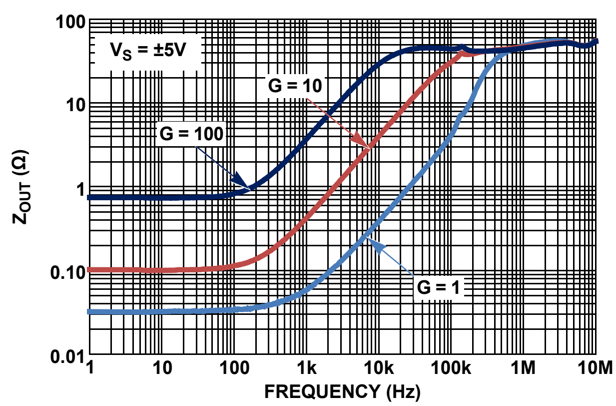


FIGURE 50. OUTPUT IMPEDANCE vs FREQUENCY, V_S = ±5V

Typical Performance Curves $V_S = \pm15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. (Continued)

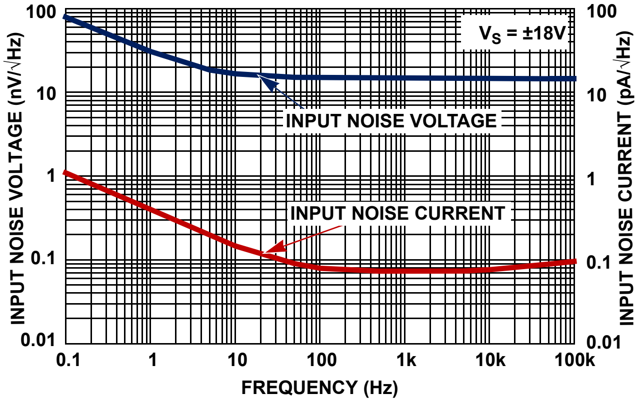


FIGURE 51. INPUT NOISE VOLTAGE (en) AND CURRENT (in) vs FREQUENCY, $V_S = \pm18V$

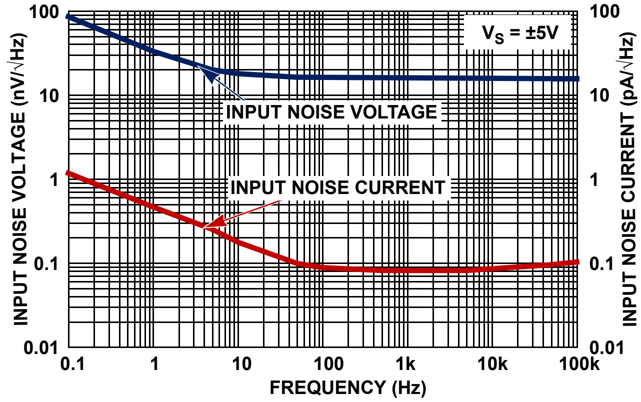


FIGURE 52. INPUT NOISE VOLTAGE (en) AND CURRENT (in) vs FREQUENCY, $V_S = \pm5V$

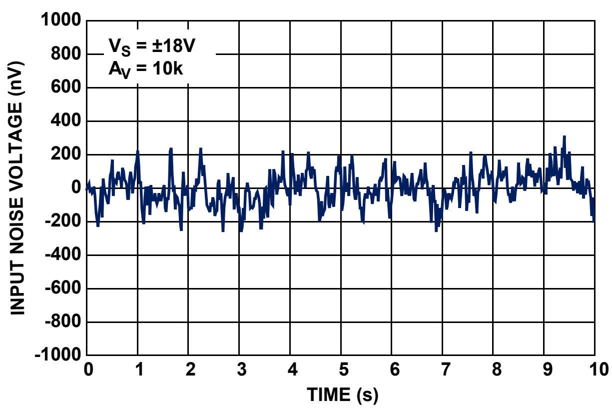


FIGURE 53. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz, $V_S = \pm18V$

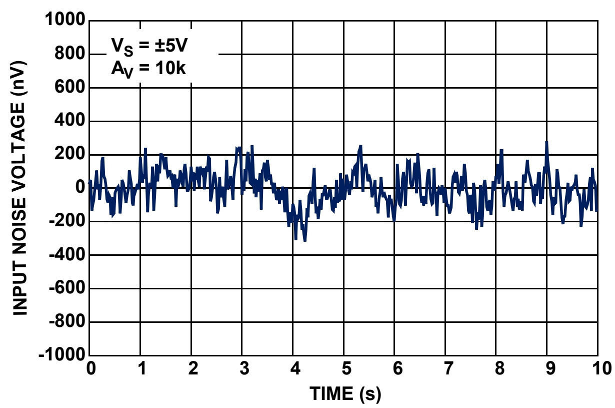


FIGURE 54. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz, $V_S = \pm5V$

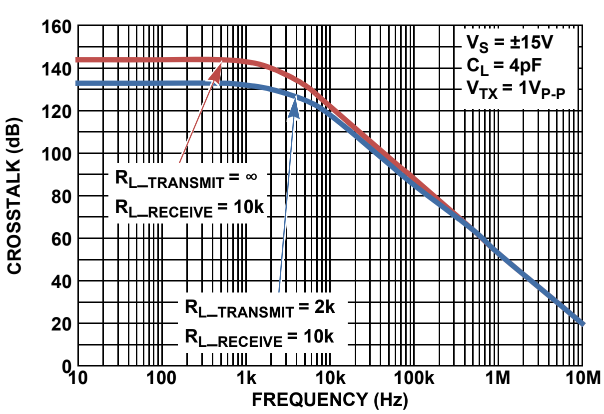


FIGURE 55. ISL28208 CHANNEL SEPARATION vs FREQUENCY, $V_S = \pm5V, \pm15V$

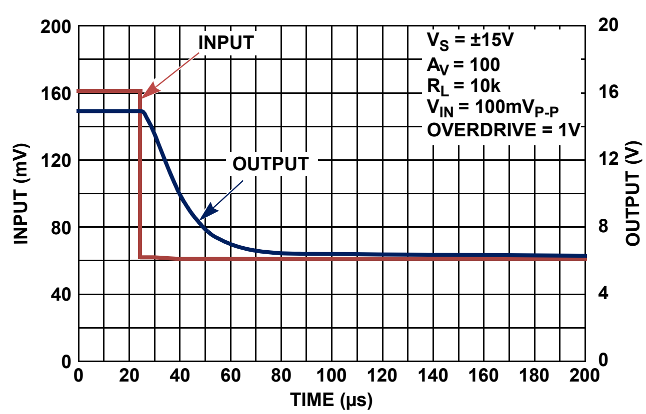


FIGURE 56. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, $V_S = \pm15V$

Typical Performance Curves
V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

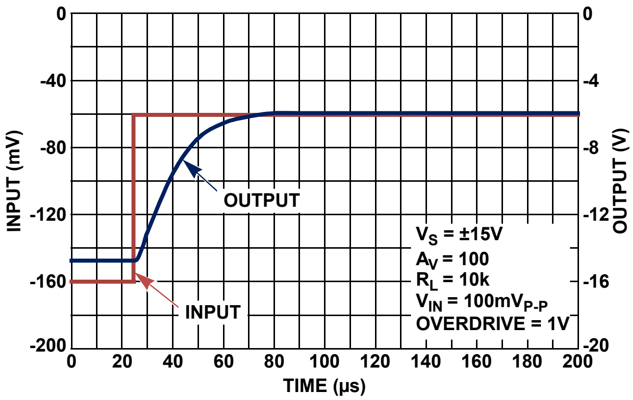


FIGURE 57. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±15V

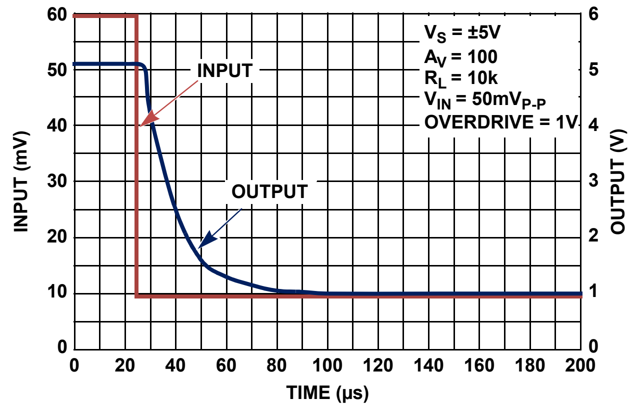


FIGURE 58. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±5V

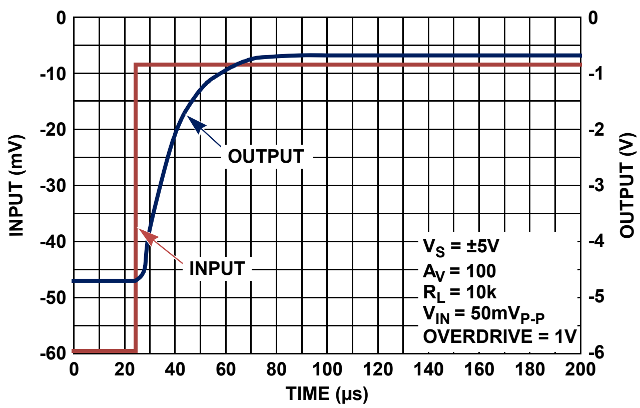


FIGURE 59. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±5V

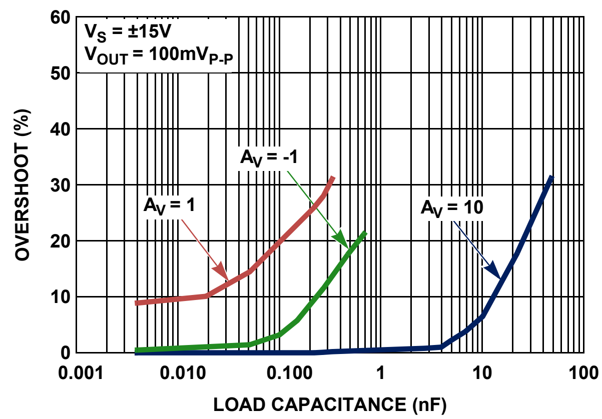


FIGURE 60. OVERSHOOT vs CAPACITIVE LOAD, V_S = ±15V

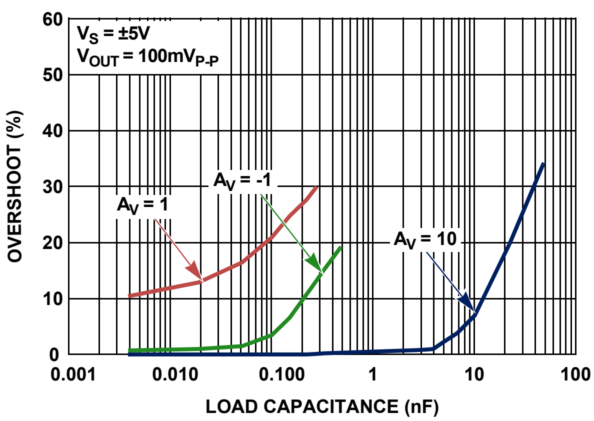


FIGURE 61. OVERSHOOT vs CAPACITIVE LOAD, V_S = ±5V

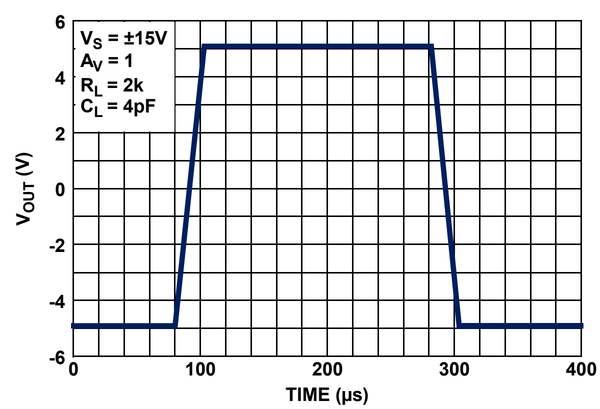


FIGURE 62. LARGE SIGNAL 10V STEP RESPONSE, V_S = ±15V

Typical Performance Curves
V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

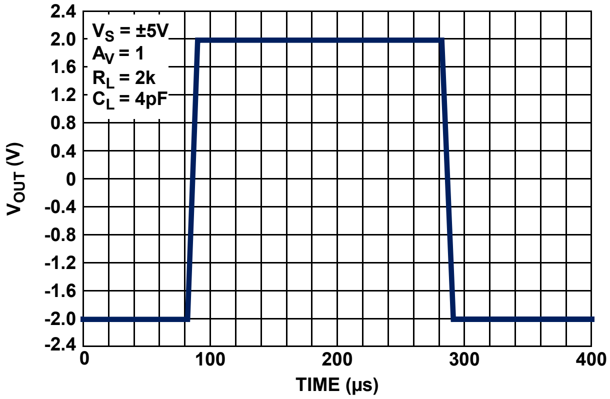


FIGURE 63. LARGE SIGNAL 4V STEP RESPONSE, V_S = ±5V

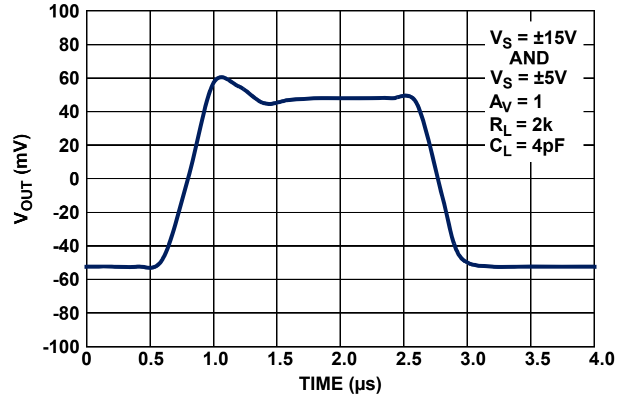


FIGURE 64. SMALL SIGNAL TRANSIENT RESPONSE V_S = ±5V, ±15V

Applications Information

Functional Description

The ISL28108, ISL28208, and ISL28408 are single, dual and quad, 1.2MHz, single supply rail-to-rail output amplifiers with a common mode input voltage range extending to a range of 0.5V below the V- rail. Their input stages are optimized for precision sensing of ground referenced signals in low voltage, single supply applications. The input stage has the capability of handling large input differential voltages without phase inversion making them suitable for high voltage comparator applications. Their bipolar design features high open loop gain and excellent DC input and output temperature stability. These op amps feature low quiescent current of 165µA, and a maximum temperature drift ranging from 1.1µV/°C for the ISL28208 and ISL28408 in the SOIC package to 1.4µV/°C for the ISL28208 in the TDFN package and the ISL28408 in the SOIC package (see Figures 11 through 20). All devices are fabricated in a new precision 40V complementary bipolar DI process and immune from latch-up.

Operating Voltage Range

The devices are designed to operate over the 3V (±1.5V) to 40V (±20V) range and are fully characterized at ±5V and ±15V. Both DC and AC performance remain virtually unchanged over the ±5V to ±15V operating voltage range. Parameter variation with operating voltage is shown in the "Typical Performance Curves" beginning on page 10.

Input Stage Performance

The PNP input stage has a common mode input range extending up to 0.5V below ground at +25°C (see Figures 23 and 24). Full amplifier performance is guaranteed down to ground (V-) over the -40°C to +125°C temperature range. For common mode voltages down to -0.5V the amplifiers are fully functional, but performance degrades slightly over the full temperature range. This feature provides excellent CMRR, AC performance and DC accuracy when amplifying low level ground referenced signals.

The input stage has a maximum input differential voltage equal to a diode drop greater than the supply voltage (max 42V) and does not contain the back-to-back input protection diodes found on many similar amplifiers. This feature enables the device to function as a precision comparator by maintaining very high input impedance for high voltage differential input comparator voltages. The high differential input impedance also enables the device to operate reliably in large signal pulse applications without the need for anti-parallel clamp diodes required on MOSFET and most bipolar input stage op amps. Thus, input signal distortion caused by nonlinear clamps under high slew rate conditions are avoided.

In applications where one or both amplifier input terminals are at risk of exposure to voltages beyond the supply rails, current limiting resistors may be needed at each input terminal (see Figure 65, $R_{IN}+$, $R_{IN}-$) to limit current through the power supply ESD diodes to 20mA.

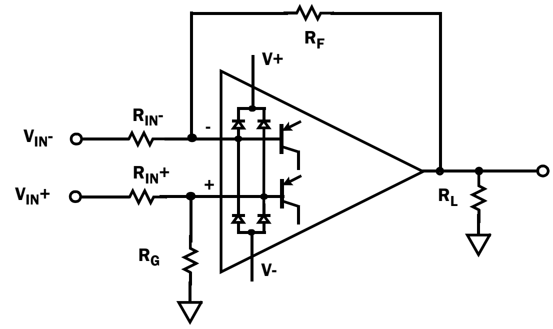


FIGURE 65. INPUT ESD DIODE CURRENT LIMITING

Output Drive Capability

The bipolar rail-to-rail output stage features low saturation levels that enable an output voltage swing to less than 10mV when the total output load (including feedback resistance) is held below 50µA (Figures 31 and 32). With ±15V supplies this can be achieved by using feedback resistor values >300kΩ. The low input bias and offset currents (-43nA and ±3nA +25°C max respectively) minimize DC offset errors at these high resistance values. For example, a balanced 4 resistor gain circuit (Figure 65) with 1MΩ feedback resistors (R_F, R_G) generates a worst case input offset error of only ±3mV. Furthermore, the low noise current reduces the added noise associated with high feedback resistance.

The output stage is internally current limited. Output current limit over-temperature is shown in Figures 37 and 38. The amplifiers can withstand a short circuit to either rail as long as the power dissipation limits are not exceeded. This applies to only one amplifier at a time for the dual op amp. Continuous operation under these conditions may degrade long-term reliability.

The amplifiers perform well driving capacitive loads (Figures 60 and 61). The unity gain, voltage follower (buffer) configuration provides the highest bandwidth, but is also the most sensitive to ringing produced by load capacitance found in BNC cables. Unity gain overshoot is limited to 30% at capacitance values to 0.33nF. At gains of 10 and higher, the device is capable of driving more than 10nF without significant overshoot.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. These devices are immune to output phase reversal, out to 0.5V beyond the rail ($V_{ABS\ MAX}$) limit (see Figure 40).

Unused Channels

If the application requires only one channel, the user must configure any unused channel to prevent it from oscillating. Unused channels can oscillate if the input and output pins are floating. This will result in higher-than-expected supply currents and possible noise injection into the channel being used. The proper way to prevent oscillation is to short the output to the inverting input, and ground the positive input (Figure 66).

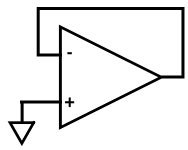


FIGURE 66. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAXTOTAL} \quad \text{(EQ. 1)}$$

where:

- $PD_{MAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

ISL28108, ISL28208, ISL28408 SPICE Model

Figure 67 shows the SPICE model schematic and Figure 68 shows the net list for the SPICE model. The model is a simplified version of the actual device and simulates important AC and DC parameters. AC parameters incorporated into the model are: 1/f and flat band noise voltage, Slew Rate, CMRR, Gain and Phase. The DC parameters are I_{OS}, total supply current and output voltage swing. The model uses typical parameters given in the “Electrical Specifications” Table beginning on page 6. The AVOL is adjusted for 122dB with the dominant pole at 1Hz. The CMRR is set 128dB, f = 6kHz. The input stage models the actual device to present an accurate AC representation. The model is configured for ambient temperature of +25°C.

Figures 69 through 83 show the characterization vs simulation results for the Noise Voltage, Open Loop Gain Phase, Closed Loop Gain vs Frequency, Gain vs Frequency vs R_L, CMRR, Large Signal 10V Step Response, Small Signal 0.05V Step and Output Voltage Swing ±15V supplies.

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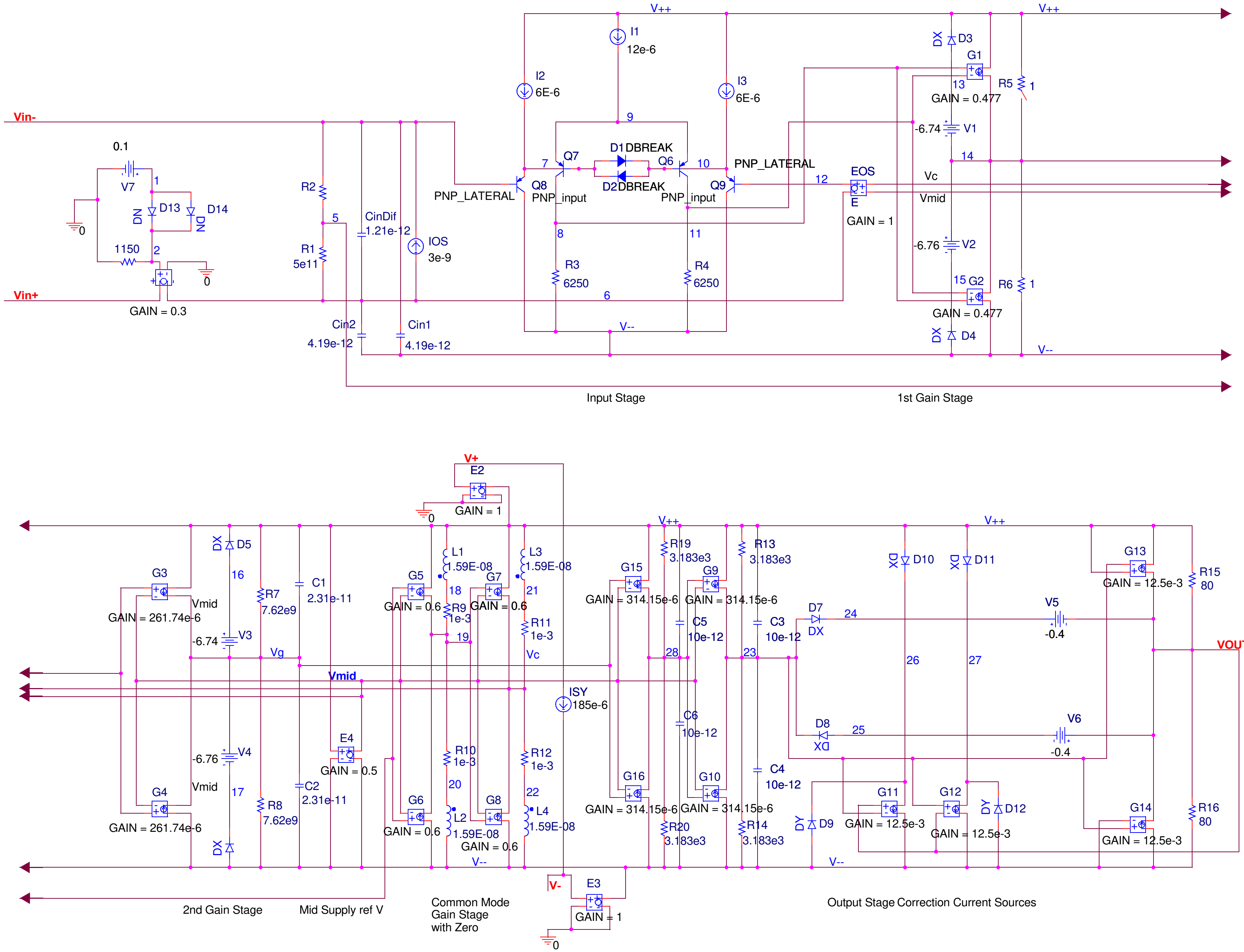

FIGURE 67. SPICE MODEL SCHEMATIC

```
*ISL28108_208 Macromodel - covers following
*products
*ISL28108
*ISL28208
*ISL28408
*
*Revision History:
* Revision B, LaFontaine January 22 2014
* Model for Noise, supply currents, CMRR
*128dB f=6kHz ,AVOL 122dB f=1Hz
* SR = 0.45V/us, GBWP 1.2MHz.
*Copyright 2011 by Intersil Corporation
*Refer to data sheet "LICENSE STATEMENT"
*Use of this model indicates your acceptance
*with the terms and provisions in the License
*Statement.
*
*Intended use:
*This Pspice Macromodel is intended to give
*typical DC and AC performance characteristics
*under a wide range of external circuit
*configurations using compatible simulation
*platforms – such as iSim PE.
*
*Device performance features supported by this
*model
*Typical, room temp., nominal power supply
*voltages used to produce the following
*characteristics:
*Open and closed loop I/O impedances,
*Open loop gain and phase,
*Closed loop bandwidth and frequency
*response,
*Loading effects on closed loop frequency
*response,
*Input noise terms including 1/f effects,
*Slew rate,
*Input and Output Headroom limits to I/O
*voltage swing,
*Supply current at nominal specified supply
*voltages.
*
*Device performance features NOT supported
*by this model:
*Harmonic distortion effects,
*Output current limiting (current will limit at
*40mA),
*Disable operation (if any),
*Thermal effects and/or over temperature
*parameter variation,
*Limited performance variation vs. supply
*voltage is modeled,
*Part to part performance variation due to
*normal process parameter spread,
*Any performance difference arising from
*different packaging source,
*Load current reflected into the power supply
*current.

*
* Connections:       +input
*                      |   -input
*                      |    |   +Vsupply
*                      |    |    |   -Vsupply
*                      |    |    |    |   output
*                           |    |    |    |
.subckt ISL28108_208 Vin+ Vin-V+ V- VOUT
* source ISL28118_218_subckt_check_0
*
*Voltage Noise
E_En        VIN+ 6 2 0 0.3
D_D13       1 2 DN
D_D14       1 2 DN
V_V7        1 0 0.1
R_R17       2 0  1150
*
*Input Stage
Q_Q6        11 10 9 PNP_input
Q_Q7        8 7 9 PNP_input
Q_Q8        V-- VIN- 7 PNP_LATERAL
Q_Q9        V-- 12 10 PNP_LATERAL
I_I1        V++ 9 DC 12e-6
I_I2        V++ 7 DC 6E-6
I_I3        V++ 10 DC 6E-6
I_IOS       6 VIN- DC 3e-9
D_D1        7 10 DBREAK
D_D2        10 7 DBREAK
R_R1        5 6  5e11
R_R2        VIN- 5  5e11
R_R3        V-- 8  6250
R_R4        V-- 11  6250
C_Cin1      V-- VIN-  4.19e-12
C_Cin2      V-- 6  4.19e-12
C_CinDif    6 VIN-  1.21E-12
*
*1st Gain Stage
G_G1        V++ 14 8 11 0.4779867
G_G2        V-- 14 8 11 0.4779867
V_V1        13 14  -6.74
V_V2        14 15  -6.76
D_D3        13 V++ DX
D_D4        V-- 15 DX
R_R5        14 V++  1
R_R6        V-- 14  1
*
*2nd Gain Stage
G_G3        V++ VG 14 VMID 261.748e-6
G_G4        V-- VG 14 VMID 261.748e-6
V_V3        16 VG  -6.74
V_V4        VG 17  -6.76
D_D5        16 V++ DX
D_D6        V-- 17 DX
R_R7        VG V++  7.62283e9
R_R8        V-- VG  7.62283e9
C_C1        VG V++  2.31e-11
C_C2        V-- VG  2.31e-11
*
*Mid supply Ref
E_E2        V++ 0 V+ 0 1
E_E3        V-- 0 V- 0 1
E_E4        VMID V-- V++ V-- 0.5
I_ISY       V+ V- DC 185E-6
*
*Common Mode Gain Stage with Zero
G_G5        V++ 19 5 VMID 0.6
G_G6        V-- 19 5 VMID 0.6
G_G7        V++ VC 19 VMID 0.6
G_G8        V-- VC 19 VMID 0.6
E_EOS       12 6 VC VMID 1
L_L1        18 V++  1.59159E-08
L_L2        20 V--  1.59159E-08
L_L3        21 V++  1.59159E-08
L_L4        22 V--  1.59159E-08
R_R9        19 18  1e-3
R_R10       20 19  1e-3
R_R11       VC 21  1e-3
R_R12       22 VC  1e-3
*
*Pole Stage
G_G15       V++ 28 VG VMID 314.15e-6
G_G16       V-- 28 VG VMID 314.15e-6
R_R19       28 V++  3.18319e3
R_R20       V-- 28  3.18319e3
C_C5        28 V++  10e-12
C_C6        V-- 28  10e-12
*
G_G9        V++ 23 28 VMID 314.15e-6
G_G10       V-- 23 28 VMID 314.15e-6
R_R13       23 V++  3.18319e3
R_R14       V-- 23  3.18319e3
C_C3        23 V++  10e-12
C_C4        V-- 23  10e-12
*
*Output Stage with Correction Current Sources
G_G11       26 V-- VOUT 23 12.5e-3
G_G12       27 V-- 23 VOUT 12.5e-3
G_G13       VOUT V++ V++ 23 12.5e-3
G_G14       V-- VOUT 23 V-- 12.5e-3
D_D7        23 24 DX
D_D8        25 23 DX
D_D9        V-- 26 DY
D_D10       V++ 26 DX
D_D11       V++ 27 DX
D_D12       V-- 27 DY
V_V5        24 VOUT -0.4
V_V6        VOUT 25 -0.4
R_R15       VOUT V++  80
R_R16       V-- VOUT  80
.model PNP_LATERAL pnp(is=1e-016 bf=250
va=80
+ ik=0.138 rb=0.01 re=0.101 rc=180 kf=0 af=1)
.model PNP_input pnp(is=1e-016 bf=100
va=80
+ ik=0.138 rb=0.01 re=0.101 rc=180 kf=0 af=1)
.model DBREAK D(bv=43 rs=1)
.model DN D(KF=6.69e-9 AF=1)
.MODEL DX D(IS=1E-12 Rs=0.1)
.MODEL DY D(IS=1E-15 BV=50 Rs=1)
.ends ISL28108_208
```

FIGURE 68. SPICE NET LIST

Characterization vs Simulation Results

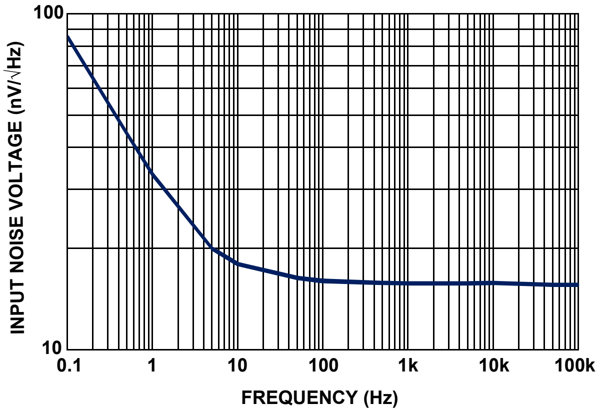

FIGURE 69. CHARACTERIZED INPUT NOISE VOLTAGE

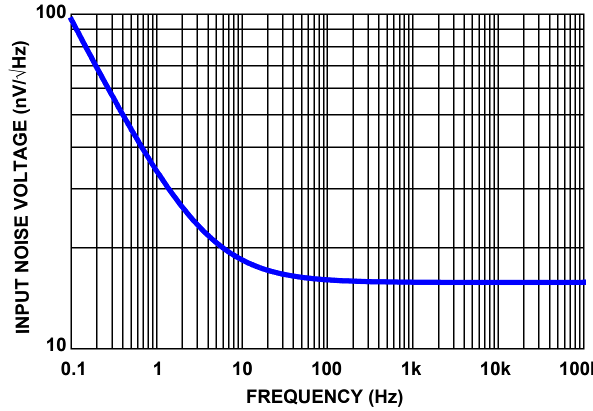

FIGURE 70. SIMULATED INPUT NOISE VOLTAGE

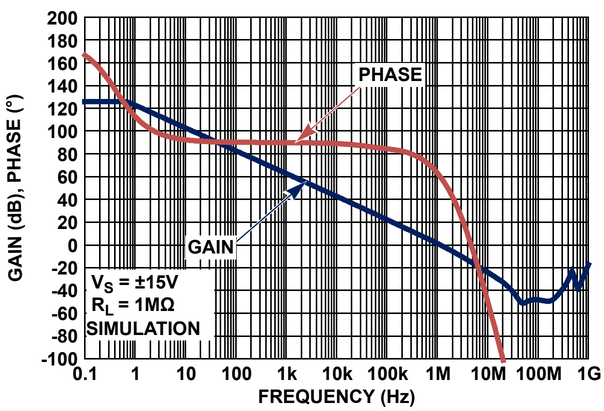

FIGURE 71. CHARACTERIZED OPEN-LOOP GAIN, PHASE vs FREQUENCY

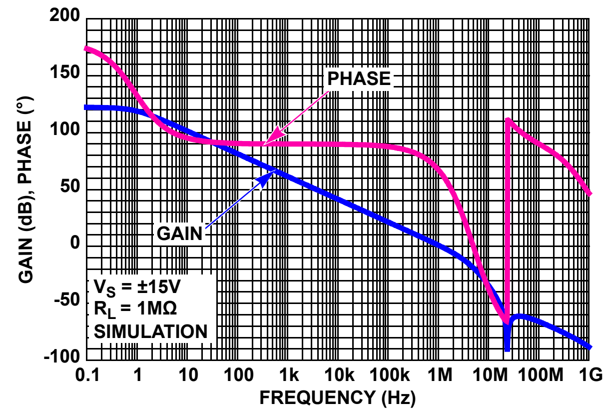

FIGURE 72. SIMULATED OPEN-LOOP GAIN, PHASE vs FREQUENCY

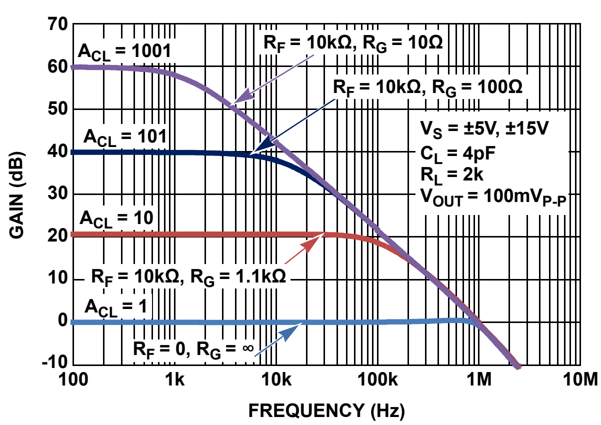

FIGURE 73. CHARACTERIZED CLOSED LOOP GAIN vs FREQUENCY

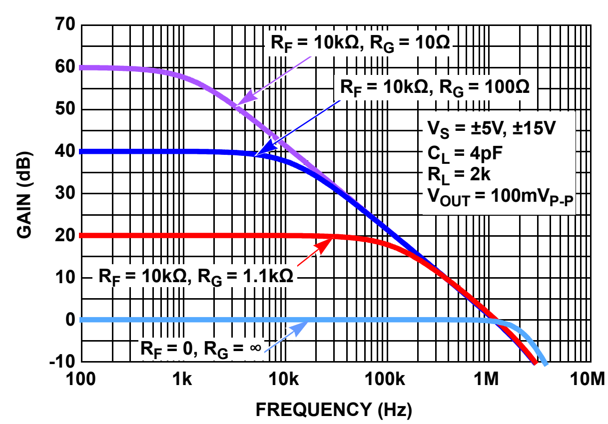

FIGURE 74. SIMULATED CLOSED LOOP GAIN vs FREQUENCY