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**Application Note** 

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#### Introduction

The ISL2827xEVAL1Z evaluation board is a design platform containing all the circuitry needed to characterize critical performance parameters of the ISL28276 and ISL28278 dual operational amplifiers, using a variety of user defined test circuits.

The ISL2827x amplifiers feature low noise, low distortion, and rail-to-rail output drive capability. They are designed to operate with single and dual supplies from +5VDC (±2.5VDC) down to +2.4VDC (±1.2VDC).

#### Reference Documents

- ISL28276 Data Sheet, FN6301
- ISL28278 Data Sheet, FN6145

## **Evaluation Board Key Features**

The ISL2827xEVAL1Z is designed to enable the IC to operate from a single supply (+2.4VDC to +5VDC), or from split supplies (±1.2VDC to ±2.5V). The board is configured for 2 independent op amps connected for differential input with a closed loop gain of 10. A single external reference voltage (VREF) pin and provisions for a user-selectable voltage divider (filter is included).

#### **Power Supplies** (Figure 1)

External power connections are made through the V+, V- and Ground connections on the evaluation board. For single supply operation, the V- and Ground pins are tied together to the power supply negative terminal. For split supplies V+ and V- terminals connect to their respective power supply terminals. De-coupling capacitors C<sub>12</sub>, C<sub>17</sub>, connect to ground through R<sub>1</sub>, R<sub>46</sub>, 0 $\Omega$  resistors. Resistors R<sub>40</sub> and R<sub>49</sub> are 0 $\Omega$  but can be changed by the user to provide

additional power supply filtering, or to reduce the voltage rate-of-rise to less than  $\pm 1 \text{V/}\mu\text{s}$ . Two additional capacitors,  $C_{10}$  and  $C_{18}$ , are connected close to the part to filter out high frequency noise. Anti-reverse diodes  $D_1$ ,  $D_2$  and zener diode  $D_3$  protect the circuit in the case of accidental polarity reversal.

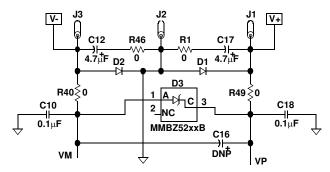
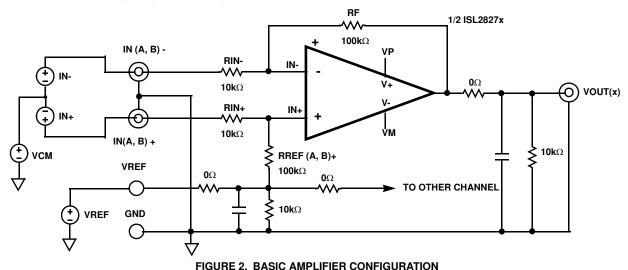


FIGURE 1. POWER SUPPLY CIRCUIT

## Amplifier Configuration (Figure 2)

The schematic of each of the 2 op amps with the components supplied is shown in Figure 2. The circuit implements a differential input amp with a closed loop gain of 10. The circuit can operate from a single 2.4VDC to +5VDC supply, or from dual supplies from ±1.2VDC to ±2.5VDC. The VREF pin can be connected to ground to establish a ground referenced input for split supply operation, or can be externally set to any reference level for single supply operation.



#### User-Selectable Options (Figures 3 to 5)

Component pads are included to enable a variety of user-selectable circuits to be added to the amplifier inputs, the VREF input, outputs and the amplifier feedback loops. The outputs (Figure 3) have additional resistor and capacitor placements for loading.

A voltage divider and filter option (Figure 4) can be added to establish a power supply-tracking common mode reference at the VREF input. The inverting and non-inverting inputs have additional resistor placements for adding input attenuation, or to establish input DC offsets through the VREF pin.

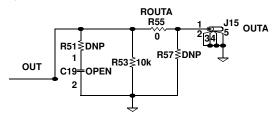
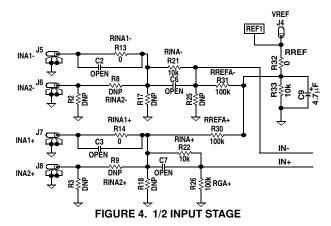


FIGURE 3. 1/2 OUTPUT STAGE



In the standard configuration (Figure5),  $R_{41}$  and  $R_{45}$  are RF feedback resistors for the two independent amplifiers, set for AV = 10. Resistors  $R_{47}$  and  $R_{48}$  connect the DUT output to the output circuit (Figure 3). The additional unpopulated components,  $R_{34}$  to  $R_{39}$ ,  $R_{42}$  to  $R_{44}$ ,  $C_{10}$ ,  $C_{11}$ ,  $C_{13}$  to  $C_{15}$  and  $C_{18}$  allow the user to configure the board for a variety of other applications such as cascaded gain stages, active feedback loops, etc.

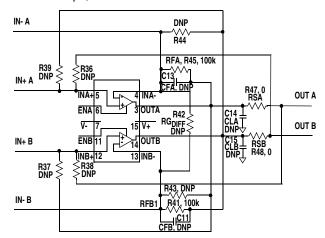
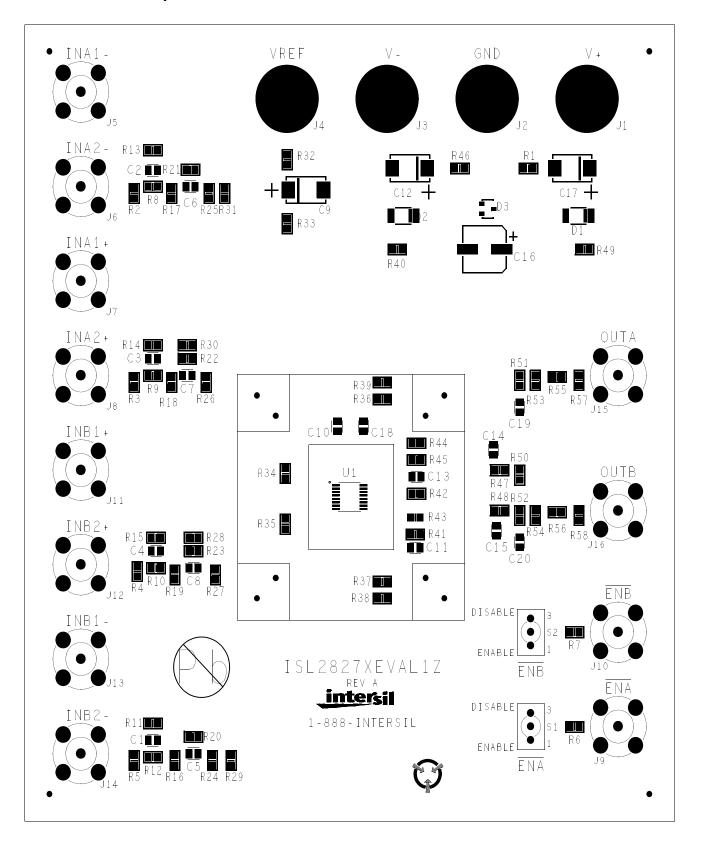


FIGURE 5. OPTICAL COMPONENTS

# ISL2827xEVAL1Z Components Parts List

DEVICE NUMBER	DESCRIPTION	COMMENTS
C9, C12, C17	CAP-TANTALUM, SMD, D, 4.7μF, 50V, 10%, LOW ESR, ROHS	Power supply decoupling
C10, C18	CAP, SMD, 0603, 0.1μF, 25V, 10%, X7R, ROHS	Power supply decoupling
C6-C25	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS	User selectable capacitors - not populated
D1, D2	DIODE-RECTIFIER, SMD, SOD-123, 2P, 40V, 0.5A, ROHS	Reverse power protection
D3	DIODE-ZENER, SMD, OD-123, 2P, 5.1V, 350mV, ROHS	Reverse power protection
U1 (ISL28276EVAL1Z)	ISL28276FAZ, IC-RAIL-TO-RAIL PRECISION OP AMP, 16P, QSOP, ROHS	
U1 (ISL28278EVAL1Z)	ISL28278FAZ, IC-RAIL-TO-RAIL PRECISION OP AMP, 16P, QSOP, ROHS	
R2-R5, R8-R10, R12, R16-R19, R24-R27, R29, R31, R34-R39, R42-R44, R50-R52, R57, R58	RESISTOR, SMD, 0603, 0.1%, MF, DNP-PLACE HOLDER	User selectable resistors - not populated
R1, R11, R13-R15, R24,R25, R32, R40, R46-R49, R55, R56	RES, SMD, 0603, $0\Omega$ , 1/10W, TF, ROHS	$0\Omega$ user selectable resistors
R6, R7, R20-R23, R33, R53, R54	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	RG gain resistors
R28, R30, R41, R45	RES, SMD, 0603, 100k, 1/10W, 1%, TF, ROHS	RF gain resistors

#### ISL2827xEVAL1Z Top View



#### ISL2827xEVAL1Z Schematic Diagram R<sub>INA1-</sub>(R13) (0) (C2) DNP INA1- (O R<sub>INA2- DNP</sub> R<sub>INA-</sub>(R21) (10 k) INA2- (0) R<sub>REFA-</sub>(R31) DNP DNP (R8) >(R2) (C6) DNP **}** R<sub>GA-</sub> (R25) DNP **<**(R17) DNP $^{4}$ R<sub>INA1+</sub> (R14) (0) R<sub>REFA+</sub>(R30) (100 k) DNP R<sub>INA2+ DNP</sub> R<sub>INA+</sub> (R22) (10 k) INA2+ (R44) (R55) (0) R<sub>OUTA</sub> (R9) $\gtrsim_{(R3)}$ R<sub>FA1</sub> (R45) (100 k) (R51) DNP< DNP R<sub>GA+</sub> (R26) -√√-**∠**(R18) \(\begin{align\*} \text{CR36} \\ \text{DNP} \end{align\*} $\varphi$ (R39) ∑ (R53) C13) C<sub>FA</sub> DNP DNP (10 k) (R57) DNP **→**DNP $^{4}$ (R47) (0) R<sub>SA</sub> (C19) DNP INA-INA+ (R6) (10 k) (R34) DNP $\Diamond$ ENA (O) OUTA (C14) C<sub>LA</sub> **ENA** (R42) >\ >RG<sub>DIFF</sub> DNP $\mathsf{R}_\mathsf{OUTAB}$ (R50) DNP DNP 🕂 15 V+ V-ENB (O ENB OUTB (R7) (10 k) (R35) DNP (C15) L C<sub>LB</sub> DNP 士(C18) (C10) R<sub>SB</sub> (R48)(0) INB-INB+ 13 $\Diamond$ $\Diamond$ $R_{INB1+}(R15)$ (0) $\leq$ (R38) (R37) DNP (R56)(0)INB1+ (o-DNP $R_{\text{OUTB}}$ R<sub>REFB+</sub>(R28)(100 k) (C4) DNP € OUTB (R43) DNP R<sub>FB1</sub>(R41) (100 k) R<sub>INB2+ DNP</sub> (R52) R<sub>INB+</sub>(R23) (10 k) DNP (R54) INB2+ (10 k) (R58) DNP ŲDNP. (R10) (C11) (C20) + DNP $\downarrow$ $\geq_{(R4)}$ (C8) C<sub>FB</sub> DNP DNP R<sub>GB+</sub> (R27) DNP >(R19) DNP (10 k) (R33) DNP R<sub>INB1-</sub>(R11)(0) V+ INB1- (0-) (C16) R<sub>REFB-</sub>(R29) DNP (C9) (CD3) (C1) DNP (10 k) (R20) 4.7uF (0) (0) $R_{INB2-}\,DNP$ 5.1V R<sub>INB</sub>-(R32) R<sub>REF</sub> \*(R40) (R49) >(0) INB2- O √V \-(R12) (R46) (C12) (D2) (D1) **\**\\\( (0) (R5) DNP $\varphi$ (C5) 4.7uF (R16) DNP $R_{GB}$ (R24) DNP DNP **VREF** GND $^{\uparrow}$

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