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Data Sheet June 29, 2005 FN6165.0.0

Octal 2.488Gbps to 3.187Gbps/ Lane Retimer

Features

- 8 Lanes of Clock & Data Recovery and Retiming; 4 in Each Direction
- Differential Input/Output
- Wide Operating Data Rate Range: 2.488Gbps to 3.1875Gbps, and 1.244Gbps to 1.59325Gbps
- Ultra Low-Power Operation (163mW typical per lane, 1300mW typical total consumption, LX4 mode)
- Low Power Version Available for LX4 Applications
- 17mm Square Low Profile 192 pin 1.0mm Pitch EBGA-B Package
- Compliant to the IEEE 802.3 10GBASE-LX4(WWDM), 10GBASE-CX4, and XAUI Specifications
- Reset Jitter Domain
- Meets 802.3ae and 802.3ak Jitter Requirements with Significant Margin
- Received Data Aligned to Local Reference Clock for Retransmission
- Increase Driving Distance
- LX4: Up to 40 inches of FR-4 Traces or 500 Meters of MMF Fiber at 3.1875Gbps
- CX4: Over 15 meters of Compatible Cable
- Deskewing and Lane-to-Lane Alignment
- 0.13mm Pure-Digital CMOS Technology
- 1.5V Core Supply, Control I/O 2.5V Tolerant
- Clock Compensation
- Tx/Rx Rate Matching via IDLE Insertion/Deletion up to ±100ppm Clock Difference
- Receive Signal Detect and 16 Levels of Receiver Equalization for Media Compensation
- CML CX4 Transmission Output with 16 Settable Levels of Pre-Emphasis, Eight on XAUI Side
- Single-Ended or Differential Input Lower-Speed Reference Clock
- Ease of Testing
- Complete Suite of Ingress-Egress Loopbacks
- Full 802.3ae Pattern Generation and Test, including CJPAT & CRPAT
- PRBS (both 2^{23}-1 and 13458 byte) Built-In Self Tests, Error Flags and Count Output
- JTAG and AC-JTAG Boundary Scan
- Long Run Length (512 bit) Frequency Lock Ideal for Proprietary Encoding Schemes
- Extensive Configuration and Status Reporting via 802.3 Clause 45 Compliant MDC/MDIO Serial Interface
- Automatic Load of ISL35822 Control and all XENPAK Registers from EEPROM or DOM Circuit

Figure 1. FUNCTIONAL BLOCK DIAGRAM

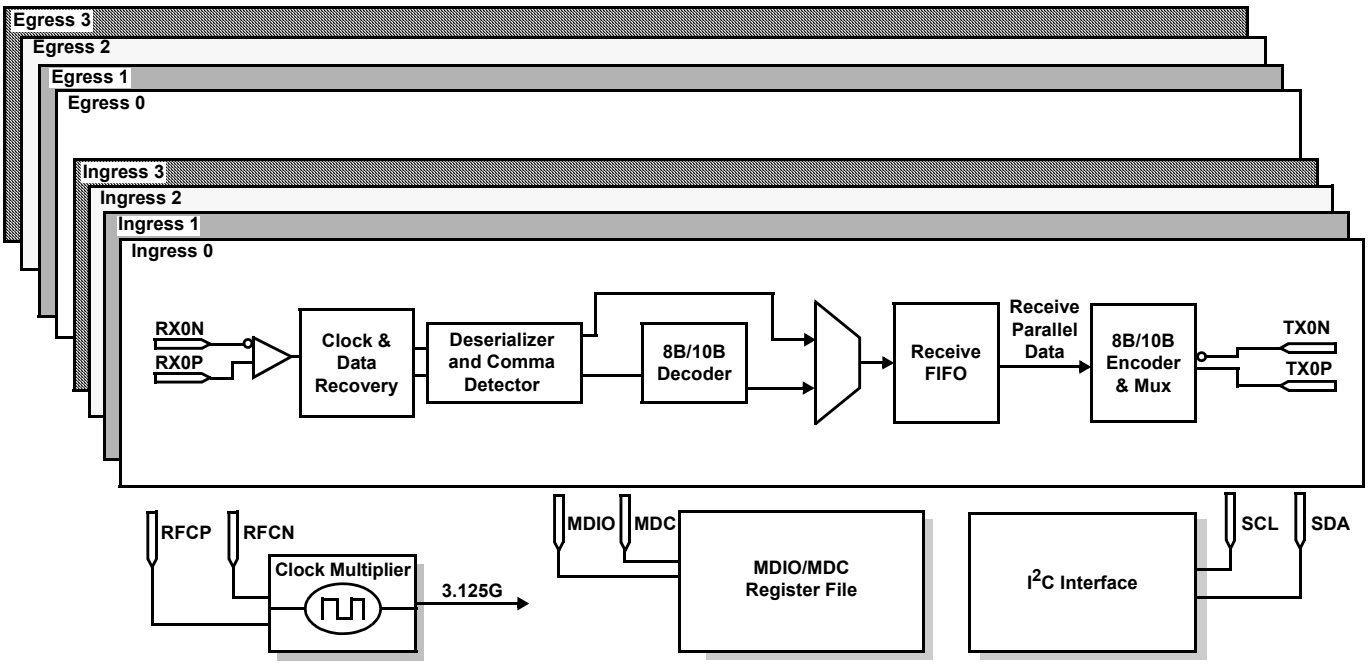

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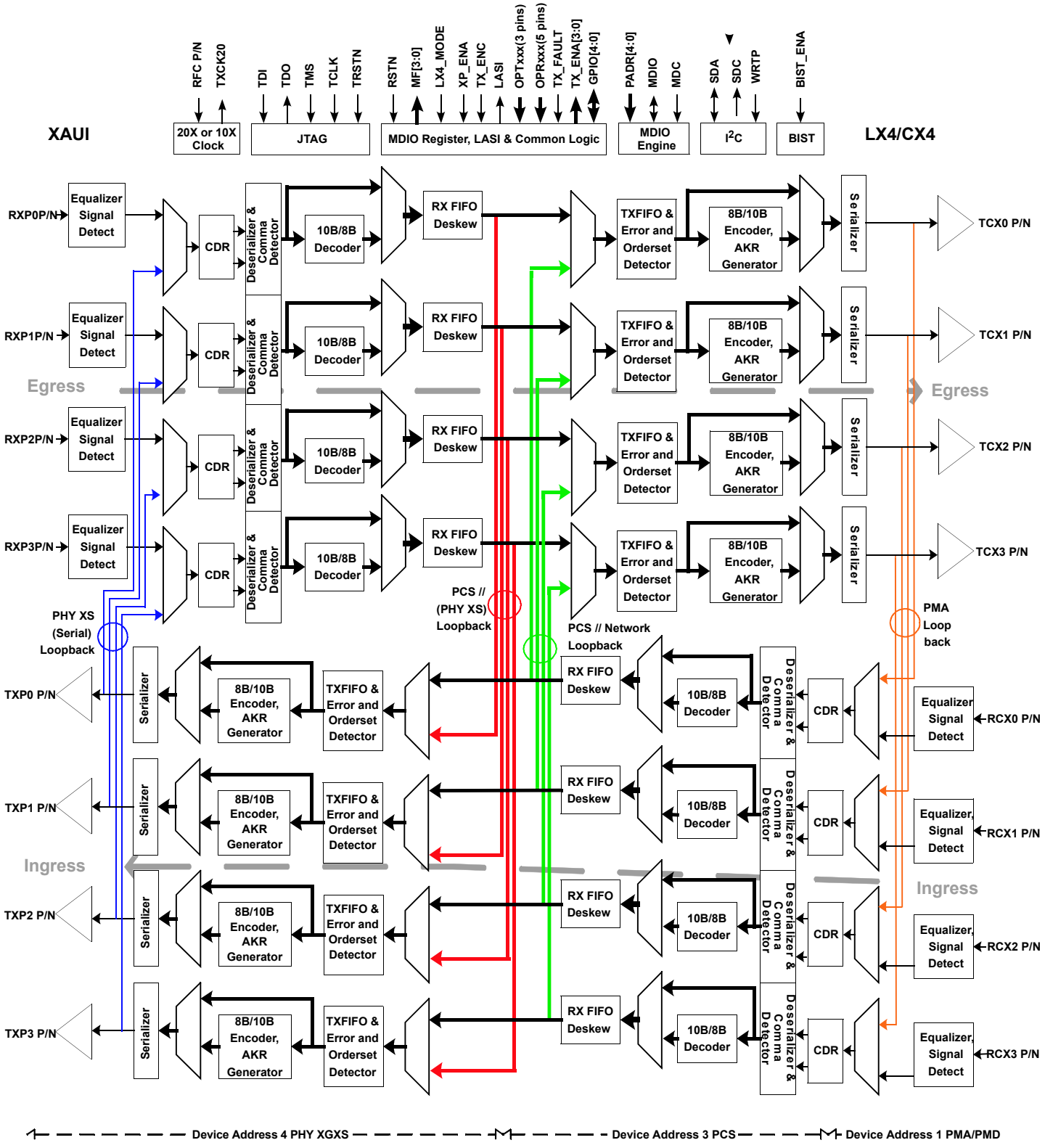
FIGURE 2. DETAILED FUNCTIONAL BLOCK DIAGRAM (BIST OMITTED)

(See also Figure 4 & Figure 5 for MDIO and LASI blocks and Figure 6 for BIST operation)



General Description

The ISL35822 is a fully integrated octal 2.488Gbps to 3.1875Gbps Clock and Data Recovery (CDR) circuit and Retimer ideal for high bandwidth serial electrical or optical communications systems. It extracts timing information and data from serial inputs at 2.488Gbps to 3.1875Gbps, covering 10 Gigabit Fiber Channel (10GFC) and IEEE 802.3 specified 10 Gigabit Ethernet eXtended Attachment Unit Interface (XAUI) rates.

Each ISL35822 accepts two sets of four high-speed differential serial signals, re-times them with a local Reference Clock, reduces jitter, and delivers eight clean high-speed signals. The ISL35822 provides a full-function XAUI-to-10GBASE-CX4 PMA/PMD (compatible with the IEEE 802.3ak specification), and also can be configured to provide the electrical portion of a XAUI-to-10GBASE-LX4 PMA/PMD, needing only laser drivers and photo detectors to be added. In both these applications, the XAUI side can be configured to implement the XENPAK MSA_R3.0 specification, including full NVR and DOM support. The XPAK and X2 specifications currently all reference the XENPAK specification, and are supported in exactly the same manner. The ISL35822 can also be used to enhance a single full-duplex 10 Gigabit XAUI link, extending the driving distance of the high-speed (2.488Gbps to 3.1875Gbps) differential traces to 40 inches of FR4 PCB (assuming a proper impedance-controlled layout).

Each lane can operate independently with a data transfer rate of within ±100ppm of either 20x or 10x the local Reference Clock. The reference clock should be 156.25MHz for 10 Gigabit Ethernet XAUI applications, and 159.375MHz for 10 Gigabit Fiber Channel. Other reference frequencies can be used for proprietary rates. For other applications, each of the 8 lanes can be operated independently, within the same data rate and clock restrictions.

The ISL35822 contains eight clock & data recovery units, 8B/10B decoders and encoders, and elastic buffers which provide the user with a simple interface for transferring data serially and recovering it on the receive side. When recovering an 8B/10B stream, a receive FIFO aligns all incoming serial data to the local reference clock domain, adding or removing IDLE sequences as required. This simplifies implementation of an upstream ASIC by removing the requirement to deal with multiple clock domains. The Retimer can also be configured to operate as eight non-encoded 10-bit Retimers. Allowing long strings of consecutive 1's or 0's (up to 512 bits), the ISL35822 has the capacity to accommodate proprietary encoded data links at any data rate between 2.488Gbps and 3.1875Gbps (and for half rate operation from 1.244Gbps to 1.59375Gbps).

The device configuration can be done through the use of the two line Management Data Input/Output (MDIO) Interface specified in IEEE 802.3 Clause 45. The ISL35822 supports a 5-bit Port Address, and DEVice ADdresses (DEVAD) 1, 3 & 4. The initial values of the registers default to values controlled, where appropriate, by external configuration pins, and set to optimize the initial configuration for XAUI, CX4, and XENPAK/XPAK/X2 use. Optionally, the ISL35822 configuration can be loaded at power-on or reset from the NVR EEPROM or DOM used for the XENPAK/XPAK/X2 registers.

A full suite of loopback configurations is provided, including the (802.3ae required) XAUI-transmit to XAUI-receive loopback, and also the (802.3ae optional) PHY XGXS loopback (effectively CX4/LX4-receive to CX4/LX4 transmit). Lane-by-lane diagnostic loopback is available through vendor-specific MDIO registers.

The ISL35822 is a version of the BBT3821 for operation as a lower-power LX4 device. Power consumption can be reduced further at lowered supply voltages.

Functions

The ISL35822 serves three main functions:

- Pre-emphasize the output and equalize the input in order to "re-open" the data eye, thus allowing CX4 operation, and also increasing the available driving distance of the high-speed traces in XAUI links.
- Clock compensation by insertion and deletion of IDLE characters when 8B/10B encoding and decoding is enabled.
- Automatic Byte and Lane Alignment, using both disparities of /K/ for Byte alignment and either ||A|| or IDLE to DATA transitions for lane alignment.

Receiver Operations

Loss of Signal Detection, Termination & Equalization

Each receiver lane detects and recovers the serial clock from the received data stream. An equalizer has been added to each receiver input buffer, which boosts high frequency edge response. The boost factor can be selected from 16 values (none to full) through the MDIO Registers, (see Table 43 for the PMA/PMD and Table 87 for the PHY XS).

A nominally 100Ω on-chip transmission line terminating resistor is integrated with the input equalizer. This eliminates the requirement of external termination resistors. It greatly improves the effectiveness of the termination, providing the best signal integrity possible.

There are also signal detect functions on each input lane, whose "Loss Of Signal" (LOS) and "Signal Detect" (SIG_DET) outputs appear in the MDIO Vendor-Specific registers at address 1.C00A'h (Table 44) and 4.C00A'h (Table 90). The LOS indication reflects the standard XAUI specification, while the SIG_DET indication (CX4 inputs only) implements the CX4 function. These signals can also

be routed to the MF[3:0] pins (see Table 81 and Table 99). The PMA configuration determines which of these signals will be reflected in the IEEE PMD Receive signal detect register at 1.10 (see Table 12), and contribute to the RX_FAULT bit in the IEEE Status Register 2 at address 1.8 (see Table 10) and the LOCAL_FLT bit in the IEEE PMA/PMD Status 1 Register, at address 1.1, (see Table 6). The PHY XGXS LOS will be reflected in the IEEE Status Registers at addresses 4.8 and 4.1 (see Table 77 and Table 76). The threshold of the LOS detectors is controlled via the 'LOS_TH' bits in the MDIO registers at 1.C001'h, see Table 39, for the PMA/PMD, and for the PHY XS at 4.C001'h, see Table 81.

Clock and Data Recovery

When the 8B/10B coding is used, the line rate receive clock is extracted from the transition rich 10-bit coded serial data stream independently on each lane. When 8B/10B coding is not used, longer run length (up to 512 1's and 0's) can be supported. The data rate of the received serial bit stream must be within ±100ppm of the nominal bit rate (strictly within ±200 ppm of the multiplied local reference clock) to guarantee proper reception. The receive clock locks to the input within 2µs after a valid input data stream is applied. The received data is de-serialized and byte aligned.

Byte Alignment (Code-Group Alignment)

Unless the CDET bits of the MDIO Registers at address 3.C000'h (for PCS, see Table 63) or 4.C000'h (for PHY XS, see Table 80) are turned off, the respective Byte Alignment Units are activated. Each Byte Alignment Unit searches the coded incoming serial stream for a sequence defined in IEEE 802.3-2002 Clause 36 as a "comma". A comma is the sequence "0011111" or "1100000" depending on disparity, and is uniquely located in a valid 8B/10B coded data stream, appearing as the start of some control symbols, including the /K/ IDLE (K28.5). Comma disparity action can be controlled via the same CDET bits of the registers [3:4].C000'h (see Table 63 and Table 80). Any proprietary encoding scheme used should either incorporate these codes, or arrange byte alignment differently.

Upon detection of a comma, the Byte Alignment Unit shifts the incoming data to align the received data properly in the 10-bit character field. Two possible algorithms may be used for byte alignment. The default is that specified in the IEEE802.3ae-2002 clause 48 specification, and is very robust. This algorithm relies on the 10b/8b decoder, and should not be used with proprietary encoding/decoding schemes. The alternative is to byte-align on any comma pattern. Although quick to align, and normally quite reliable, this method is susceptible to realignment on certain single bit errors or on successive K28.7 characters, but could be preferable for proprietary coding schemes, or during debug. The algorithm selection is controlled via MDIO register PCS_SYNC_EN bits, for the PCS at address 3.C000'h (Table 63), for the PHY XS at address 4.C000'h (Table 80), unless overridden by the respective XAUI_EN bits in the [3,4].C001'h registers (Table 64 and Table 81). Up to a full code group may be deleted or modified while aligning the "comma" code group correctly to the edges of the RefClock. A comma received at any odd or even byte location, but at the proper byte boundary, will not cause any byte re-alignment.

8b/10b Decoding

The internal 10b decoding specified in the IEEE802.3-2002 specification, section 36.2.4 in Tables 36-1 & 36-2, and discussed in more detail in "8b/10b Coding and Decoding" page 12, is enabled by default in the PCS and PHY XS through the setting of the respective CODECENA bits to 1'b, and may be disabled through the MDIO registers [3,4].C000'h (Table 63 and Table 80) by setting the respective bit to 0'b. Note that the transmit encoding will also be disabled. Although Comma detection will still operate normally, the PCS_SYNC engine (see above) may not operate correctly on a proprietary coding scheme, unless byte sync is performed on K28.5 characters, and no code violations are to be expected in the proprietary data, and so should normally be disabled if the 8b/10b coding is turned off. The 'fallback' byte sync operations described above can still be used, if the encoding scheme meets the "comma" rules; otherwise they should be disabled also via the CDET bits, and the user should expect unsynchronized 10-bit data to be forwarded to the transmitter. No clock compensation is then possible, and a synchronous reference clock should be used throughout.

Receive FIFO

The Receive FIFO performs two functions:

1. Lane to Lane Alignment
2. Clock Compensation

Deskew (Lane to Lane) Alignment

Trunking, also known as deskewing, means the alignment of packet data across multiple lanes. 8 bytes of RXFIFO are dedicated for this lane to lane alignment in each direction.

During high-speed transmission, different active and passive elements in the links may impart varying delays in the four lanes. In trunking mode, multiple lanes share the same clock (the local reference clock), which is used to transfer data for output on the serial transmitter.

Deskewing is accomplished by monitoring the contents of the FIFOs to detect either an /A/ code-group on every lane (an ||A|| Ordered_Set), or the boundary between IDLE sequences and any non-IDLE data (see Table 1); the latter boundary defines the beginning of the packet. The choice of which alignment markers to use can be controlled by the A_ALIGN_DIS bits in MDIO [3,4].C000'h (see for PCS Table 63 and for PHY XS Table 80), unless overridden by the respective XAUI_EN bits in the [3,4].C001'h registers (Table 64 and Table 81) to align on ||A||. When this alignment

data is detected in all four lanes within the span of the Alignment FIFO, the deskewing (lane to lane) alignment operation is performed, and will be held until another ||A|| or IDLE-to- non-IDLE transition is detected again on the lanes. During this alignment, up to four code groups may be deleted on any lane. For correct operation, the XAUI Lane 0 signals should be connected to the ISL35822 Lane 0 pins.

The deskew algorithm state machines (each implemented according to IEEE 802.3ae) are enabled by setting the DSKW_SM_EN bits (Address [3,4].C000'h, see Table 63 and/or Table 80) to 1 or overriding them with the respective XAUI_EN bits in the [3,4].C001'h registers (Table 64 and Table 81). Note that when one side's DSKW_SM_EN is set to 1, the same side CAL_EN bit (Address [3,4].C000'h, Table 63/Table 80) is ignored. When a DSKW_SM_EN bit is set to 0, lane deskew can still be enabled by setting CAL_EN, but the deskew action will be carried out without hysteresis.

The user has the option to disable trunking, or to enable trunking across each set of 4 lanes, in the PCS (device 3) and PHY XGXS (device 4), under control of the respective PSYNC bits in registers [3,4].C000h. In trunking mode, the lanes may have phase differences, but they are expected to be frequency synchronous. In non-trunking mode, each received serial stream need only be within ±100ppm of the nominal bit rate (2.488Gbps to 3.1875Gbps in full-speed mode or 1.244Gbps to 1.59375Gbps in half-speed mode). Setting the PSYNC bits high will enable the trunking mode, so that all transmitted data will be synchronized to the same clock. Note that trunking mode is only possible if 8B/10B Coding is activated, and all lanes have the same half-rate setting (See Table 71).

Clock Compensation

In addition to deskew, the Receive FIFOs also compensate for clock differences. Since the received serial streams can, under worst case conditions, be off by up to ±200ppm from the local clock domain, the received data must be adjusted to the local reference clock frequency.

Another 8 bytes of RXFIFO are dedicated for clock compensation. The FIFOs achieve clock tolerance by identifying any of the IDLE patterns (/K/, /A/ or /R/ as defined by the IEEE 802.3ae standard) in the received data and then adding or dropping IDLEs as needed. The Receive FIFO does not store the actual IDLE sequences received but generates the number of IDLEs needed to compensate for clock tolerance differences. The IDLE patterns retransmitted will be determined according to the IEEE 802.3ae algorithm if the appropriate AKR_SM_EN bit is set in Registers [3,4].C001'h (see Table 64 and Table 81).

Transmitter Operations

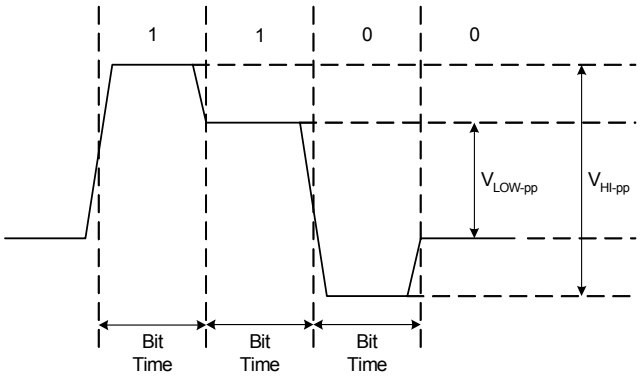
8b/10b Encoding

The internal 10b encoding specified in the IEEE802.3-2002 specification, section 36.2.4 in Tables 36-1 & 36-2, and discussed in more detail in "8b/10b Coding and Decoding" page 12, is enabled by default in the PCS and PHY XS through the setting of the respective CODECENA bits to 1'b, and may be disabled through the MDIO registers [3,4].C000'h (see Table 63 and Table 80) by setting the respective bit to 0'b. Note that the receive decoding will also be disabled. The (decoded, synchronized and aligned) data is transferred via the transmit FIFOs, (normally) encoded, serialized and re-transmitted on the Serial Output pins, whose effective output impedance is nominally 100Ω differential.

Pre-Emphasis

In order to compensate for the loss of the high frequency signal component through PCB traces or the CX4 Cable Assembly, sixteen levels of programmable pre-emphasis have been provided on the CX4/LX4 PMA serial transmit lanes, and eight levels on the XAUI PHY XS serial transmit lanes. The output signal is boosted immediately after any transition (see Figure 3). This maximizes the data eye opening at the receiver inputs and enhances the bit error rate performance of the system. The MDIO Registers at Addresses [1,4].C005'h (see Table 41 and Table 85) control the level of pre-emphasis for the PMA/PMD (sixteen levels) and PHY XGXS (eight levels) respectively, settable from none to the maximum. The initial default values of the PMA/PMD register depend on the LX4_MODE configuration pin, and are set to the optimum values for CX4 or XAUI (assumed best for LX4 drivers). The PMA side has an additional set of Pre-emphasis enabling bits, in 1.C00B.5:2 that enable or disable the predriver/pre-emphasis. In LX4 mode these default to disabled, to reduce the power consumption. All these three registers may be auto-loaded (see Auto-Configuring Control Registers page 16) from an NVR EEPROM on start-up or RESET.

FIGURE 3. PRE-EMPHASIS OUTPUT ILLUSTRATION



8b/10b Coding and Decoding

8 Bit Mode

If 8B/10B encoding/decoding is turned on, the ISL35822 expects to receive a properly encoded serial bit stream. The serial bit stream must be ordered “abcdeifghj” with “a” being the first bit received and “j” the last. If the received data contains an error, the Retimer will re-transmit it as an ERROR or /E/ character. The character transmitted may be controlled via the ERROR code Registers [3,4].C002’h, Table 66 and Table 82. The internal decoding into, and encoding from, the FIFOs is listed in Table 1 below. If the TRANS_EN bit or XAUI_EN bit (MDIO Registers at addresses [3,4].C001’h, see Table 64 and Table 81 are set, all incoming XAUI or CX4/LX4 IDLE patterns will be converted to the (internal) XGMII IDLE pattern set by the respective PCS or PHY XS control registers at addresses [3,4].C003’h, with a default value 107’h, the standard XGMII IDLE code (see Table 67 and Table 83) in the internal FIFOs. The first full column of IDLES after any column containing a non-IDLE will be stored in the respective elasticity FIFO, and all subsequent full IDLE columns will repeat this pattern, until another column containing a non-idle is received. If in addition either of the AKR_SM_EN or XAUI_EN bits in the respective MDIO registers at Addresses [3,4].C001’h is set (see Table 64 and Table 81, these IDLEs will be sequenced on transmission into a pseudo-random pattern of ||A||, ||K||, and ||R|| codes according to the IEEE 802.3ae specified algorithm. If neither of the AKR_SM_EN and XAUI_EN bits are set, the internal IDLEs will all be transmitted as /K/ codes. Elasticity will be achieved by adding or deleting columns of internal IDLEs.

If neither the TRANS_EN bit nor the XAUI_EN bit is set (for either the PCS or the PHY XS), the incoming XAUI IDLE codes will all be decoded to the appropriate XGMII control code values in the respective internal FIFO. If the AKR_EN or XAUI_EN bits are set, they will be sequenced into a pseudo-random pattern of ||A||, ||K||, and ||R|| codes and retransmitted, if not, the Inter Packet Gap (IPG) will be retransmitted as the same XAUI codes as in the first full IDLE column.

For most applications, the XAUI_EN bit high configuration is the most desirable, and is the default.

Table 1. VALID 10b/8b DECODER & ENCODER PATTERNS

RECEIVING SERDES		INTERNAL DATA			TRANSMITTING SERDES			NOTES
SERIAL CODE, CHARACTER	TRANS_EN BIT(4)	E-BIT	K-BIT	INTERNAL FIFO DATA	AKR_SM_EN(4)	SERIAL CHARACTER	SERIAL CODE	DESCRIPTION
Valid Data	X	0	0	0-FF’h	X	See 802.3 Table	Valid Data	Same Data Value as Received
/K/ (Sync) K28.5	1	0	1	07’h (2)	1	/A/ /K/ /R/		IEEE802.3ae algorithm
	0	0	1	BC (1)	0	/K/	K28.5	Comma (Sync)
/A/ (Align) K28.3	1	0	1	07’h (2)	1	/A/ /K/ /R/		IEEE802.3ae algorithm
	0	0	1	7C (1)	0	/A/	K28.3	Align
/R/ (Skip) K28.0	1	0	1	07’h (2)	1	/A/ /K/ /R/		IEEE802.3ae algorithm
	0	0	1	1C (1)	0	/R/	K28.0	Alternate Idle (Skip)
/S/ K27.7	X	0	1	FB	1	/S/	K27.7	Start
/T/ K29.7	X	0	1	FD	0	/T/	K29.7	Terminate
K28.1	X	0	1	3C	X		K28.1	Extra comma
/F/ K28.2	X	0	1	5C	X	/F/	K28.2	Signal Ordered_Set
/Q/ K28.4	X	0	1	9C	X	/Q/	K28.4	Sequence Ordered_Set
K28.6	X	0	1	DC	X		K28.6	
K28.7	X	0	1	FC	X		K28.7	Repeat has False Comma
K23.7	X	0	1	F7	X		K23.7	
/E/ K30.7	X	1	1	FE	X	/E/	K30.7	Error Code
Any other	X	1	= ERROR reg.(3)		X	Invalid code		Error Code

Note (1): First incoming IDLE only, subsequent IDLEs in that block repeat first received code.
Note (2): Default value, actually set by ‘Internal Idle’ register, [3:4].C003’h, see Table 67 and Table 83.
Note (3): Value set by ‘ERROR Code’ register, [3:4].C002’h, see Table 66 and Table 66. The XAUI_EN bit forces it to 1FE’h.
Note (4): If the XAUI_EN bit is set, the ISL35822 acts as though both the TRANS_EN and AKR_EN bits are set.

10 Bit Mode

If a PCS or PHY XS 8B/10B codec is inactive (the respective XAUI_EN AND CODECENA bits are disabled, see Table 63/Table 64 & Table 80/Table 81), no 8b/10b coding or decoding is performed. The incoming bits will be arbitrarily split into 10 bit bundles in the internal FIFO, optionally based on any commas received, but otherwise not checked, and must be retransmitted in the same clock domain, since no elasticity is possible. Therefore the local reference clock must be frequency synchronous with the data source. Only the jitter domain will be reset. System designers must ensure that the data stream is adequately DC-balanced and contains sufficient transition density for proper operation, including synchronization.

Error Indications

An equivalent schematic of the various IEEE-defined and Vendor Specific Fault and Status registers in the ISL35822 is shown in Figure 4. Those register signals that also contribute to the LASI system are indicated (see Figure 5).

Loss of Signal

If the reference clock is missing or at an out-of-range frequency, the PLL in the CMU will fail to lock. This is the only possible internal cause of a PMA 'TX Local Fault ' indication in bit 1.8.11 (Table 10), and will cause 'RX Local Fault' in bit 1.8.10 and other consequent fault indications (see Table 6, Table 27 and Table 28).

Loss of the input signal may be caused by poor connections, insufficient voltage swings, or excessive channel loss. If any of these conditions occurs, the Loss Of Signal (LOS) and (CX4) SIG_DET detector outputs on the lane will indicate the fault, and may be monitored via the MDIO system (see Table 6, Table 10, Table 27, Table 28, Table 76 and Table 77). See also the section on "Loss of Signal Detection, Termination & Equalization" on page 9 above. In addition, the MDIO MF_SEL and MF_CTRL register bits (address 4.C001'h, see Table 81) may be set to provide the LOS/SIG_DET indication on the MF[3:0] pins.

Byte or Lane Synchronization Failure

The MDIO system can indicate a failure to achieve Byte Synchronization on any lane, in the PCS register bits 3.24.3:0 (Table 61) or in the PHY XS register bits 4.24.3:0 (Table 78), which shows the lane-by-lane Byte Sync status. A failure here, if not caused by any of the above 'Loss of Signal' conditions, would normally reflect a very high bit error rate, or incorrectly coded data.

Failure of Lane Synchronization is indicated for the PCS by register bit 3.24.12 (Table 61) or for the PHY XS by register bit 4.24.12 (Table 78), and can be caused by failure to detect /A/ characters on every lane of a channel, by excessive skew between /A/s on the lanes of a channel, or by inconsistent skews.

Channel Fault Indications

Any of the above faults (LOS/SIG_DET, Byte Sync, or Lane Align), will (by default) cause a local fault in the relevant receiver. If the PCS_SYNC_EN bit at address [3,4]C000'h (or the XAUI_EN bit at [3:4].C001'h) (see Table 63 to Table 65 and/or Table 80 to Table 81) is set, the internal FIFOs will propagate the local fault indication specified in the IEEE802.3ae-2002 specification (Sections 46.3.4 and 48.2.4.2) as the Sequence Ordered_Set ||LF|| (see Table 48-4), /K28.4/D0.0/D0.0/D1.0/, which will be transmitted as the appropriate XAUI or LX4/CX4 TX output. The ISL35822 lanes 0-3 must be connected to XAUI and LX4/CX4 lanes 0-3 in strict order. Any Sequence Ordered_Set (including ||LF|| and ||RF||) received on an input channel will be retransmitted unchanged on the appropriate output channel.

Coding Violation, Disparity & FIFO Errors

The 8b/10b decoder will detect any code violation, and replace the invalid character by the error character /E/. In the case of a disparity error, the error may be propagated and only flagged at the end of a packet (according to the IEEE 802.3 rules). The ISL35822 will handle this according to those rules. In addition, the MDIO system includes a flag, in registers [3,4].C007'h on bits 11:8 (see Table 69 and Table 88). Similarly, an error in the PCS or PHY XS Elastic (clock compensation) FIFOs will be flagged in bits 7:4 of the same registers. The FIFO errors may also be flagged on the MF[3:0] pins via the MDIO MF_SEL and MF_CTRL register bits (address 4.C001'h, see Table 81).

If a PCS or PHY XS 8B/10B codec is inactive, disparity error and coding violation errors do not apply, and the FIFOs have no active error source.

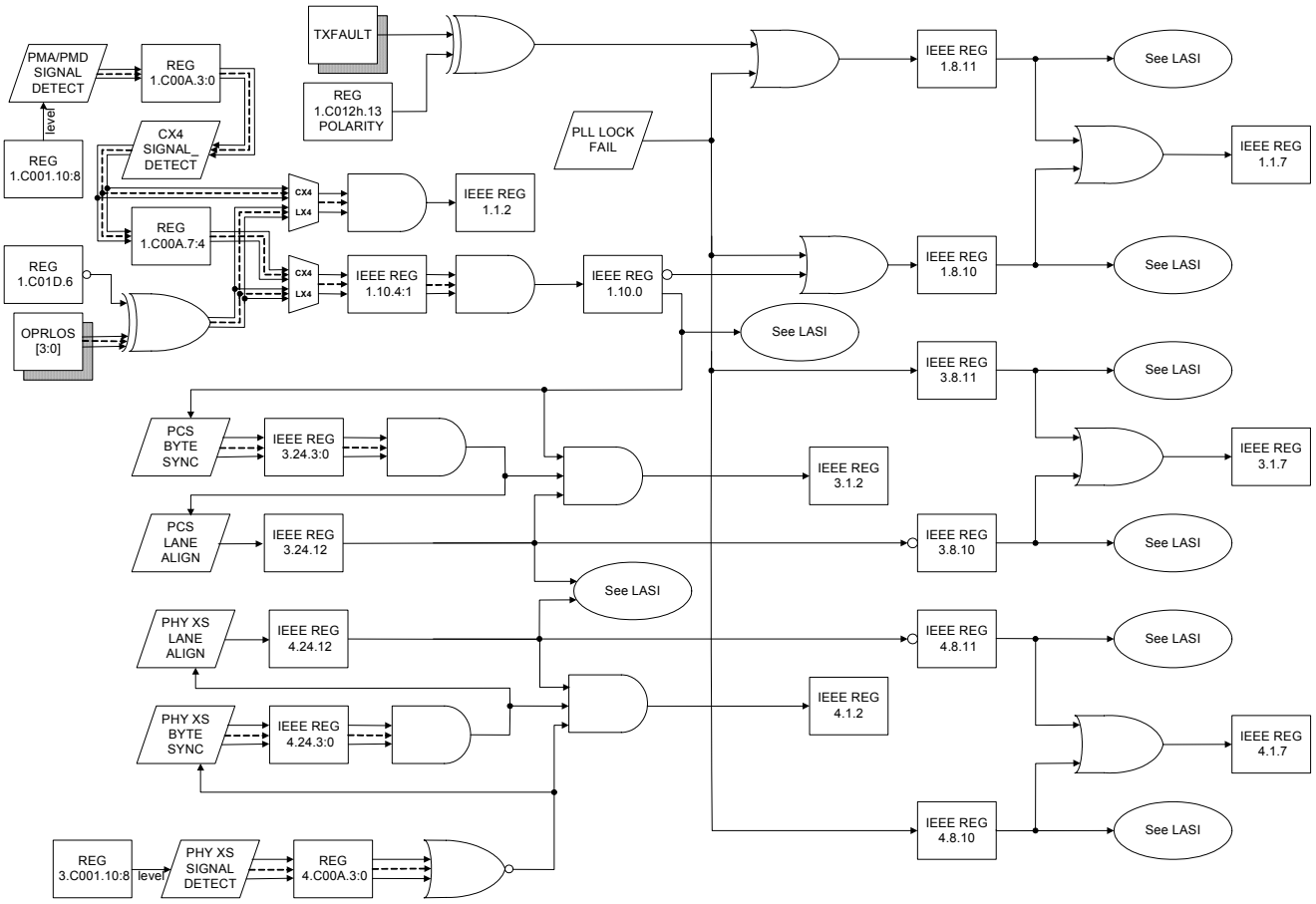
Loopback Modes

In addition to the IEEE 802.3ae-required loopback modes, the ISL35822 provides a number of additional modes. Each mode is described in detail below, by reference to the Detailed Functional Block Diagram in Figure 2, together with the register bits controlling it.

PMA Loopback (1.0.0 & 1.C004.[11:8])

The PMA loopback is implemented from the output of the TCX[3:0] serializers to the input multiplexers in front of the RCX[3:0] CDRs. All four lanes are controlled by bit 1.0.0, while the individual lanes can be controlled (one at a time) by the 1.C004'h.[11:8] bits. Assuming that this is the only loopback enabled, and that the BIST and test pattern generation features are not enabled, the signal flow is from the RXP[3:0][P/N] pins through almost all the 'egress' channel to the input of the (still active) TCX[3:0] output drivers, then (bypassing the RCX[3:0][P/N] inputs, the equalizers and LOS detectors) back from the CDRs through almost all the 'ingress' channel to the TXP[3:0][P/N] pins.

FIGURE 4. IEEE AND VENDOR SPECIFIC FAULT AND STATUS REGISTERS (EQUIVALENT SCHEMATIC)



PHY XS (Serial) Loopback (4.0.14 & 4.C004.[11:8])

The PHY XS loopback is implemented from the output of the TXP[3:0] serializers to the input multiplexers in front of the RXP[3:0] CDRs. All four lanes are controlled by bit 4.0.14, while the individual lanes can be controlled (one at a time) by the 4.C004'h.[11:8] bits. Assuming that this is the only loopback enabled, and that the BIST and test pattern generation features are not enabled, the signal flow is from the RCX[3:0][P/N] pins through almost all the 'ingress' channel to the input of the (still active) TXP[3:0] output drivers, then (bypassing the RXP[3:0][P/N] inputs, the equalizers and LOS detectors) back from the CDRs through almost all the 'egress' channel to the TCX[3:0][P/N] pins.

PCS Parallel Network Loopback (3.C004.[3:0])

This loopback is implemented (at the internal XGMII-like level) from the output of the RXFIFOs in the 'ingress' channel to the input of the TXFIFOs in the 'egress' channel. The individual lanes can be controlled (one at a time) by the 3.C004'h.[3:0] bits. Assuming that this is the only loopback enabled, and that the BIST and test pattern generation features are not enabled, the signal flow is from the RCX[3:0][P/N] pins through the PMA/PMD and PCS and again PMA/PMD to the TCX[3:0][P/N] pins. This could also be seen as a 'short' loopback at the XGMII input of the PHY XS.

PCS (Parallel) Loopback (4.C004.[3:0] & Optionally 3.0.14)

This loopback is implemented (at the internal XGMII-like level) from the output of the RXFIFOs in the 'egress' channel to the input of the TXFIFOs in the 'ingress' channel. The individual lanes can be controlled (one at a time) by the 4.C004'h.[3:0] bits. If the enable bit in 3.C001.7 (Table 64) is set, all four lanes can be controlled by bit 3.0.14. Since the latter is specifically excluded by subclause 45.2.3.1.2 of the IEEE 802.3ae-2002 specification for a 10GBASE-X PCS, the default is to NOT enable this loopback bit, and if it is enabled, the ISL35822 does not conform to the IEEE specification. A maintenance request has been submitted to the IEEE to enable this loopback bit as optional, and to allow a 'PCS Loopback Capability' bit in register bit 3.24.10 (see http://www.ieee802.org/3/maint/requests/maint_1113.pdf), but this has so far been rejected, and may never be approved. Assuming that this is the only loopback enabled, and that the BIST and test pattern generation features are not enabled, the signal flow is from the RXP[3:0][P/N] pins through the full PHY XS via the internal XGMII to the TXP[3:0][P/N] pins. This could also be seen as a 'short' loopback at the XGMII input of the PCS.

Serial Test Loopbacks (1.C004.12 & 4.C004.12)

In addition to the above loopbacks, the ISL35822 also offers two serial loopbacks directly between the serial inputs and outputs. These loopbacks use the recovered clock as the timing for the outputs (instead of the multiplied reference clock), so do not reset the jitter or clock domains, and in addition do NOT provide any pre-emphasis on the outputs. Furthermore, on the PMA/PMD side (1.C004.12) the lanes are internally swapped (so the Lane 3 output is from the Lane 0 input, etc.). Because of their limited utility, they are not illustrated in Figure 2 or Figure 6. They are mainly useful for debugging an otherwise intractable system problem. The reference clock still needs to be within locking range of the input frequency. The remainder of the signal path will remain active (as normal), so that if for example 1.C004.12 is set, data coming in on RCX[3:0], in addition to emerging on TCX[0:3] without retiming, etc., will also emerge from TXP[3:0] retimed, as usual.

Serial Management Interface

The ISL35822 implements the MMD Management Interface defined in IEEE 802.3-2002 Clauses 22 & enhanced in IEEE 802.3ae-2002 Clause 45. This two-pin interface allows serial read/write of the internal control registers and consists of the MDC clock and MDIO data terminals. The PADR[4..0] pins are used to select the ‘Port address’ to which a given ISL35822 device responds. The ISL35822 will ignore Clause 22 format frames (on a frame-by-frame basis), based on the second ST (start) bit value. The two formats are shown in Table 3, together with the references to the respective IEEE 802.3 specifications.

MDIO Register Addressing

The PADR[4..0] hardware address pins control the PRTAD (Port Address) value, each port normally consisting of a series of MDIO Managed Devices (MMDs). Each Port may include up to 31 different devices, of which the current specification defines 8 types, and allows vendor specification of two others. The ISL35822 device corresponds to the PMA/PMD, PCS and PHY XGXS defined types, so responds to DEVAD values of 1, 3 and 4 respectively. The Clause 45-accessible registers are listed for each Device Address in the tables referenced in Table 2. Many of these register addresses are IEEE-defined; the ‘Vendor Defined’ registers are arranged to be as DEVAD independent as possible.

Table 2. DEVAD DEVICE ADDRESS TABLE

DEVAD VALUE	IEEE DEFINITION	REGISTER LIST TABLE
DEVAD = 1 (00001’b)	PMA/PMD Device	Table 4, page 19
DEVAD = 3 (00011’b)	PCS Device	Table 56, page 38
DEVAD = 4 (00100’b)	PHY XS (XGXS) Device	Table 74, page 45

Each individual device may have up to 2^{16} (65,536) registers. The ISL35822 implements all the defined registers for 10GBASE PMA/PMD, 10GBASE-X PCS and PHY XS devices, and a few Vendor Specific registers for each DEVAD respectively. The latter have been placed in the blocks beginning at D.C000’h so as to avoid the areas currently defined as for use by the XENPAK module and similar MSA devices, to facilitate use of the ISL35822 in such modules and systems.

Table 3. MDIO MANAGEMENT FRAME FORMATS

CLAUSE 22 FORMAT (FROM TABLE 22-10 IN IEEE STD 802.3-2002 EDITION, FOR REFERENCE)								
OPERN	**PRE**	**ST**	**OP**	**PHYAD**	**REGAD**	**TA**	**DATA**	**IDLE**
Read	1….1	01	10	PPPPP	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write	1….1	01	01	PPPPP	RRRRR	10	DDDDDDDDDDDDDDDD	Z
CLAUSE 45 FORMAT (FROM TABLE 45-64 IN IEEE 802.3.ae-2002)								
OPERN	**PRE(1)**	**ST**	**OP**	**PRTAD**	**DEVAD**	**TA**	**ADDRESS/DATA**	**IDLE**
Addrs	1….1	00	00	PPPPP	DDDDD	10	AAAAAAAAAAAAAAAA	Z
Write	1….1	00	01	PPPPP	DDDDD	10	DDDDDDDDDDDDDDDD	Z(2)
Read	1….1	00	11	PPPPP	DDDDD	Z0	DDDDDDDDDDDDDDDD	Z
Read Inc	1….1	00	10	PPPPP	DDDDD	Z0	DDDDDDDDDDDDDDDD	Z

Note (1): The ‘Preamble’ consists of at least 32 bits. After a software reset, a few extra preamble bits may be needed, depending on the MDC clock rate. See timing diagrams in Figure 15 and Figure 17.

Note (2): The actual register will not be updated until up to three additional MDC cycles have been received. See Figure 15.

I²C Space Interface

In addition to the standard MDIO registers discussed above, the ISL35822 implements the register addresses specified in the XENPAK MSA specification for the NVR, DOM and LASI blocks. The built-in I²C controller can be configured to load these registers with the MSA-specified data on start-up or reset or on demand from an I²C EEPROM (frequently included as part of a DOM circuit) and/or one or four DOM circuits (see below). Optionally, a portion of the NVR space may be used to autoload the various ISL35822 control registers at start-up or reset. These operations are discussed in more detail below.

NVR Registers & EEPROM

If the XP_ENA pin is asserted enabled (high), at the end of hardware RESET or power-up the ISL35822 will attempt to load the NVR area by initiating a NVR-block read through the 1.32768 (1.8000'h) control register (Table 15). See Figure 18. The same will occur if the appropriate command value is written into this register. The I²C interface will attempt to read the A0.00:FF'h I²C space into the 1.8007:8106'h MDIO register space. The Command Status bits in the 1.32768 (1.8000'h) Control register will reflect the status of this operation. Failure may occur if the expected ACK is not received from any address after the number of attempts set in control register 1.32273 (1.8005'h), default 63 (Table 20), or if a collision is detected on the I²C bus. The timing sequence of this Block Read operation is shown in Figure 20. The host can check the checksums against the values at 1.807D, and optionally 1.80AD and 1.8106, and take appropriate action. As soon as the XENPAK MDIO space is loaded, the STA MDIO device may interrogate it. Note that the ISL35822 merely stores the values read from the EEPROM or other device at A0.00-FF'h, and, with a few exceptions, does not interpret them in any way. The exceptions are listed explicitly in Table 22, together with the other uninterpreted groups, and are:

- The Package OUI at 1.32818:32821 (1.8032:5'h), which will be mirrored in the IEEE-defined 1.14:15 (1.E:F'h) space, as required by section 10.8.2 of the XENPAK spec; the allowable values here are specified by the XENPAK, XPAK and X2 specifications;
- The DOM Capability byte at 1.32890 (1.807A), see the DOM Registers section, page 16;
- The Auto-configure size and pointer bytes at 1.33028:9(1.8104:5); (see Auto-Configuring Control Registers, page 16).
- If the Auto-configure operation is enabled, the block of bytes so specified will be written into the ISL35822 control registers, (see Auto-Configuring Control Registers on page 16 and Table 92).

Other registers may be interpreted in future versions of the ISL35822.

Auto-Configuring Control Registers

If the XP_ENA pin is asserted, and the I²C controller can successfully read the I²C NVR space into the MDIO NVR space, the ISL35822 will examine the Auto-configure Pointer value at 1.33029 (1.8105'h). If this is neither 00'h or FF'h, the ISL35822 will use that value (*S* below) as an offset pointer into the A0.00:FF'h I²C space already copied into the MDIO NVR space, and the number of bytes given in the Auto-configure Size register 1.33028 (1.8104) value (N below) to load *N* bytes from the NVR data starting from location *S* into the various ISL35822 configuration control registers. The loading sequence and the correspondence between the NVR block and the control registers is listed in Table 92. The auto-configure engine will behave benignly if the *S* and *N* values are misconfigured, so that if $S + N \geq 252$ (for example), the auto-configure block will stop at an $S + N$ value of 252, and not use *S*, *N* , or the Checksum value to load a configuration control register. (Hence the exclusion of FF'h as a value for *S* is no limitation). Similarly, values of $N >$ 40 will be ignored.

Note that in a XENPAK/XPAK/X2 module, the value of *S* should not be between 00'h and 76'h, since this would start the loading from within the MSA-defined region. (Hence the exclusion of 00'h as a value for *S* is normally no limitation). If the value of *S* lies between 77'h and A6'h, that portion of the auto-configure data within that band can be overwritten as part of the Customer Writable area defined by the MSA specifications; if this is undesirable, that range of values should also be excluded. On the other hand, this could be used to allow some customization for specific end-user configuration values. If the block overlaps the boundary between the 'Customer Writable' and 'Vendor Specific' areas, the first part would be customer-writable, and the second part not. The order of the configuration registers has been arranged to place those most likely to be useful in such a customer-configuration environment at the beginning of the block. The 'Customer Area Checksum' would be part of the auto-configure block, and some other byte in the 'Customer Writeable Area' would need to be adjusted to make the Checksum and the desired configuration value coincide.

The Command Status bits in the NVR Command register (Table 15) at 1.32768.3:2 (1.8000'h.3:2) will reflect the success of both the NVR and (if called for) the auto-configure loading operations.

DOM Registers

If the NVR load operation succeeds, the (newly read-in) XENPAK register at 1.32890 (1.807A'h) is examined, and if the DOM Capability bit is set (bit 6, see Table 23), the I²C interface will attempt to read the DOM values from the I²C device address space specified in the same register (bits 2:0), normally 001'b pointing to A2'h. See Note (2) to Table 23 for details. A full block of data will be read from this space (normally A2.00:FF'h) into the 1.40960:41215 (1.A000: A0FF'h) MDIO register DOM space. See Figure 18 and Figure 20 for details. The DOM control register is implemented in the ISL35822 at

1.41216 (1.A100'h), so that one-time or (by default) periodic updates of the DOM information can be loaded into the MDIO DOM space by writing the appropriate values into it, as shown in Table 38, page 33. The actual automatic update rates selectable in this XENPAK-defined register are controlled by the DOM Control register in the ISL35822 vendor-specific register space at 1.49176 (1.C018'h), which also controls other actions of the DOM interface (see Table 51). In particular, since many available DOM circuits can handle only one lane, bit 2 enables or disables indirect access to separate DOM circuits on the four lanes. If the bit is 0'b, the DOM circuit is directly addressed at Ax.00:FF'h, and is assumed to provide the full four lane data, including the determination of which data is to be treated as the 'furthest out of range' or the 'representative value', as specified in Note 1 to Table 27 in section 11.2.6 of the XENPAK R3.0 specification, to be returned in the XENPAK-defined 1.A060:A06D'h space for a WDM module. If bit 2 of 1.C018'h is set to 1'b, the DOM data is polled from four devices attached to the I^2C serial bus, getting 10 bytes from each of them. The 40 bytes of data are stored in the four lane register blocks starting from 1.A0C0'h, 1.A0D0'h, 1.A0E0'h and 1.A0F0'h respectively. The device addresses of these four DOM devices on the 2-wire bus are configured by registers 1.C01B'h and 1.C01C'h (Table 54); the starting memory addresses by registers 1.C019'h and 1.C01A'h (Table 53). Since the ISL35822 has no mechanism to determine out-of-range data, it chooses one of these four 10-byte long groups of data to copy into 1.A060'h:A069'h according to bits 1:0 of 1.C018'h (the 'representative' lane per the above-mentioned XENPAK Note). In addition, the Alarm and Status flags (Table 36 and Table 37) will be loaded from this lane into 1.A070:A075'h.

The ISL35822 assumes that the DOM circuit(s) will have these A/D values and flags at the same relative offsets as those specified in the XENPAK R3.0 and the SFF-8472 specifications.

General Purpose (GPIO) Pins

The ISL35822 includes some flexibly configurable General Purpose Input-Output (GPIO) pins, which may be configured to be inputs or outputs. As inputs, their level may be read directly via the MDIO system, but also they may be configured (again via MDIO registers, see Table 47 through Table 50) to optionally trigger the LASI on either a high or low level. The GPIO pins may also individually be used as outputs, and set high or low, under MDIO control. The GPIO control registers are among those that can be auto-configured on start-up.

LASI Registers & I/O

The ISL35822 implements the Link Alarm Status Interrupt (LASI) interface defined in section 10.13 of the XENPAK specification. The source and nature of these is described above under "Error Indications" on page 13 and in Figure 4. In addition to these specification-defined inputs, the ISL35822 incorporates a number of additional inputs, related to the possible byte alignment and 8b/10b code violations, which may be used to trigger a LASI. The available inputs depend on the LX4/CX4 select LX4_MODE pin (Table 99), and are detailed in Table 27 and Table 28, and include:

1. Various status bits within the ISL35822, derived from its operations; in particular, the LOS indications, Byte Sync and EFIFO errors, the Fault bits [1,3,4].8.10:11, etc.
2. The Optical Interface Status pins (in LX4 mode), see Table 99.
3. The Alarm flags in 1.A070:1 (Table 36). These bits are gated with the enable bits in 1.9006:7 (Table 30 and Table 31) and the LX4/CX4 LX4_MODE pin (Table 99) to drive bits 1.9004.1 & 1.9003.1 (Table 28 & Table 27).
4. The GPIO pins (Table 100). If configured as inputs, they may be used to optionally trigger the LASI on either a high or low level. See above.

These status inputs can all be read via the LASI Status registers (1.9003 to 1.9005, see Table 27 to Table 29). Any of these inputs, if enabled via the LASI Control Registers, 1.9000 to 1.9002 (Table 24 to Table 26), can drive the LASI pin.

Figure 5 shows an equivalent schematic for the LASI system (an expansion of Figure 21 in the XENPAK specification).

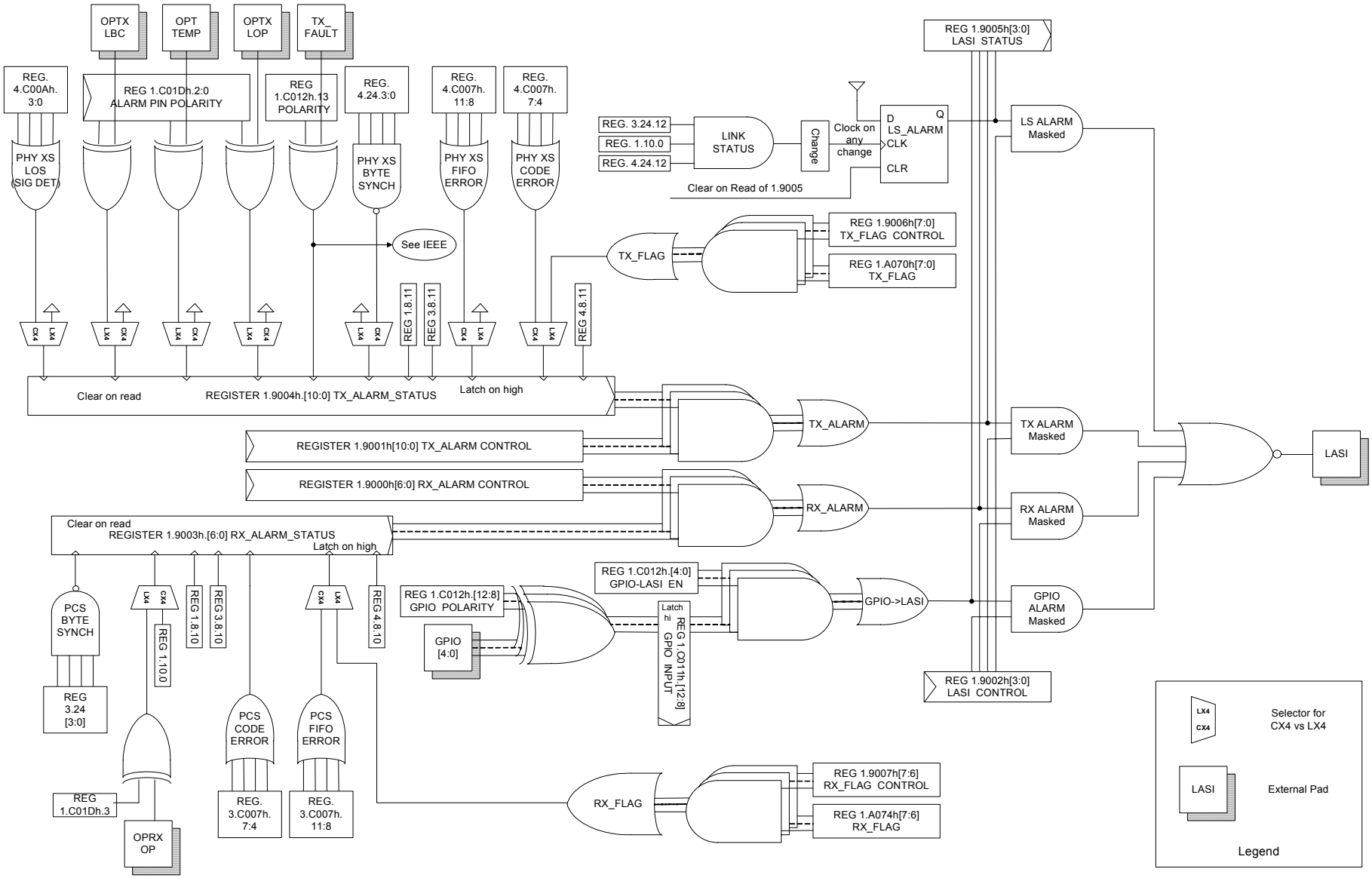
Reading Additional EEPROM Space Via the I^2C Interface

The I^2C interface will allow single-byte reads from any possible I^2C address. The device address and memory address are written into the 1.32769 (1.8001'h) and 1.32770 (1.8002'h) registers respectively (see Table 16 and Table 17), and on issuing a 'Read one byte' command (write 0002'h to 1.32768 = 1.8000'h) the data will be read from the I^2C space in the MDIO register at 1.32771 (1.8003'h, see Table 18). For timing sequence, see Figure 22. Note that a 16-bit addressable EEPROM (or equivalent) device on the I^2C bus may be read by setting the Long Memory bit 1.32773.8 (1.8005.8'h) to a '1', and writing a full 16-bit memory address value into 1.32770 (1.8002'h). This in principle allows access to almost a full 8MB of I^2C space, excluding only the NVR and (optional) DOM device address portions. This 16-bit operation MUST NOT be used on an 8-bit device, since the register address setting operation will attempt to write the low byte of the address into the register at the high byte address. Such a 16-bit memory address device should be located at a device address not used by the NVR or DOM system.

These one-byte operations could be used to read other types of data from (multiple) DOM devices (such as limit lookup tables), or for expanded informational areas. It also facilitates the use of I^2C-based DCP (Digital Control Potentiometer) devices for Laser Current control, and other similar setup and monitoring uses.

FIGURE 5. LASI EQUIVALENT SCHEMATIC

(See Also Figure 4)



Writing EEPROM Space through the I²C Interface

The ISL35822 permits two methods for writing the requisite values into EEPROM or other I²C devices from the MDIO space into the I²C register space. Many DOM circuits protect their important internal data through some form of password protection, and in general the ISL35822 will allow this to be done without a problem.

BLOCK WRITES TO EEPROM SPACE

The first method is applicable only to the NVR space (I²C address space A0.00:FF'h). If the WRTP (Write Protect) pin is inactive (low), and the NVR Write Size bit (1.32773.7 = 1.8005.7'h) is set to a '1', then issuing a 'Write All NVR' command (write 0023'h to 1.32768 = 1.8000'h) will write the current contents of MDIO registers 1.8007:8106'h into the NVR space. The 'NVR Write Page Size' bits in 1.32773.1:0 (1.8005.1:0'h) control the block size used for the write operation. See Figure 21 for the sequence timing. Normally this operation is only useful for initialization of a module EEPROM space, but it could be used for field upgrades or the like. If the WRTP (Write Protect) pin is high (active, normal condition), OR the Write Size bit (1.32773.7 = 1.8005.7'h) is cleared to a '0', then issuing a 'Write All NVR' command (write 0023'h to 1.32768 = 1.8000'h) will write only the current contents of the MDIO register block within 1.807F:80AE'h to the XENPAK-defined Customer Area, A0.77:A6'h. The actual block write will occur one byte at a time. The block write size controls cannot be used here, since the Customer Area block boundaries do not lie on page-write boundaries of the EEPROM, a feature of the XENPAK specification.

BYTE WRITES TO EEPROM SPACE

The second method is applicable to any part of the I²C space. The write operation is performed one byte at a time. The device address and memory address are written into the 1.32769 (1.8001'h) and 1.32770 (1.8002'h) registers respectively (see Table 16 and Table 17), and the data to be written into the 1.32772 (1.8004'h) register. On issuing a 'Write one byte' command (write 0022'h to 1.32768 = 1.8000'h) the data will be written into the I²C space. See Figure 23 for the timing sequence. Note that if the WRTP (Write Protect) pin is high, or the Write Size bit (1.32773.7 = 1.8005.7'h) is cleared to a '0', writes to any part of the basic NVR space outside the XENPAK-defined Customer Area will be ignored. Also note that a 16-bit addressable EEPROM (or equivalent) device on the I²C bus may be written by setting the Long Memory bit 1.32773.8 (1.8005.8'h) to a '1', and writing a full 16-bit memory address value into 1.32770 (1.8002'h). Note that this 16-bit operation MUST NOT be used on an 8-bit device.

These one-byte operations could be used to load modified Device Address values or protective passwords into multiple DOM devices, or for loading other types of data into them. They are also useful for writing data into I²C interface DCP devices for setting laser currents, etc.

MDIO Registers

In the following tables, the addresses are given in the table headers both in decimal (as used in the IEEE 802.3ae and 802.3ak documents) and in hexadecimal form. Where the registers coincide in structure and meaning, but the Device Addresses differ, the underlying register bits are the same, and may be read or written indiscriminately via any relevant Device Address. For instance a full RESET may be initiated by writing any one of 1.0.15, 3.0.15, or 4.0.15. While the reset is active, reading any of these bits would return a '1' (except that the reset lasts less than the MDIO preamble plus frame time). When the reset operation is complete, reading any of them will return a '0'. Note that extra preambles may be required after such a software RESET (see Figure 17).

Table 4. MDIO PMA/PMD DEVAD 1 REGISTERS

PMA/PMD DEVICE 1 MDIO REGISTERS							
ADDRESS		NAME	DESCRIPTION	DEFAULT	AC (5)	R/W	DETAILS
DEC	HEX						
1.0	1.0	PMA/PMD Control 1	Reset, Enable serial loop back mode.	2040'h		R/W	Table 5
1.1	1.1	PMA/PMD Status 1	Local Fault and Link Status	0004'h (2)		RO/LL	Table 6
1.2:3	1.2:3	ID Code	Manufacturer OUI & Device ID	01839C6V'h		RO	See (1)
1.4	1.4	Speed Ablty	PMA/PMD Speed Ability	0001'h		RO	Table 7
1.5	1.5	Dev in Pkg.	Devices in Package, Clause 22.	001A'h		RO	Table 8
1.6	1.6	Vend Sp Dev	Vendor Specific Devices in Package	0000'h		RO	Table 8
1.7	1.7	PMA/PMD Control 2	PMA/PMD type Selection	P (4)		RO (6)	Table 9
1.8	1.8	PMA/PMD Status 2	Fault Summary, Device Ability	B311'h (2)		RO (LH)	Table 10
1.9	1.9	PMD TX Dis	Disable PMD Transmit	0000'h		R/W	Table 11
1.10	1.A	PMD Sig Det	PMD Signal Detect	001F'h (2)		RO	Table 12

Table 4. MDIO PMA/PMD DEVAD 1 REGISTERS (Continued)

PMA/PMD DEVICE 1 MDIO REGISTERS							
ADDRESS		NAME	DESCRIPTION	DEFAULT	AC (5)	R/W	DETAILS
DEC	HEX						
1.11	1.B	PMD Ext Ca	PMD Extended Capability	0001'h		RO	Table 13
1.14:15	1E:F	Pkg OUI	PMD Package OUI, etc.	00000000'h (3)		R/W	Table 14
1.32768	1.8000	NVR Cntrl	NVR Control & Status Register	0003'h		R/W	Table 15
1.32769	1.8001	I^2C Dev Ad	1-Byte Operation Device Addr.	A2'h		R/W	Table 16
1.32770	1.8002	I^2C Mem Ad	1-Byte Operation Memory Addr.	0000'h		R/W	Table 17
1.32771	1.8003	I^2C RD Data	1-Byte Operation Read Data	0000'h		RO	Table 18
1.32772	1.8004	I^2C WR Data	1-Byte Operation Write Data	0000'h		R/W	Table 19
1.32773	1.8005	I^2C Op Ctl	I^2C Operation Control	004D'h		R/W	Table 20
1.32774	1.8006	I^2C Op Stts	I^2C Operation Status	0000'h		RO/LH	Table 21
1.32775: 33030	1.8007: 8106	NVR Copy Registers	XENPAK NVR Register Copies	Set by EEPROM		R/W	Table 22
1.36864	1.9000	RX Al Ctrl	RX ALARM Control	See Table (4)	A	R/W	Table 24
1.36865	1.9001	TX Al Ctrl	TX ALARM Control	See Table (4)	A	R/W	Table 25
1.36866	1.9002	LASI Ctrl	LASI Control	0000'h	A	R/W	Table 26
1.36867	1.9003	RX Al Stts	RX ALARM Status	0000'h (2)		RO	Table 27
1.36868	1.9004	TX Al Stts	TX ALARM Status	0000'h (2)		RO	Table 28
1.36869	1.9005	LASI Stts	LASI Status	0000'h (2)		RO	Table 29
1.36870	1.9006	DOM TX	DOM TX_Flag Control	0000'h	A	R/W	Table 30
1.36871	1.9007	DOM RX	DOM RX_Flag Control	0000'h	A	R/W	Table 31
1.40960: 41215	1.A000 :A0FF	DOM Copy Registers	Alarm & Warning Thresholds, A/D Values, (cf SFF-8472)	Set by DOM devices		RO	Table 32: Table 37
1.41216	1.A100	DOM Ctrl	DOM Control & Status	0000'h		R/W	Table 38
1.49153	1.C001	PMA Ctrl2	PMA Control 2	0000'h	A	R/W	Table 39
1.49156	1.C004	PMA LB	PMA Loopback Control	0000'h	A	R/W	Table 40
1.49157	1.C005	PMA Pre	PMA Pre-emphasis Control	See Table (4)	A	R/W	Table 41
1.49158	1.C006	PMA Eql	PMA Equalizer Boost Control	See Table (4)	A	R/W	Table 43
1.49162	1.C00A	SIG_DET	Signal Detect Flags	0000'h (2)		RO	Table 44
1.49163	1.C00B	Fine Tune	Adjust pre-emphasis, amplitude	See Table (4)	A	R/W	Table 45
1.49167	1.C00F	Soft RST	Soft RESET	0000'h		R/W	Table 46
1.49168: 49171	1.C010 :C013	GPIO Cnfg	GPIO Config, Status & Alarm Registers	0000'h (2)	A	R/W	Table 47: Table 50
1.49176	1.C018	DOM Control	DOM Control Register	0000'h	A	R/W	Table 51
1.49177:8	1.C019:A	DOM Mem	DOM Indirect Start Addresses	6060'h	A	R/W	Table 53
1.49179:80	1.C01B:C	DOM Dev	DOM Indirect Device Addresses	See Tables	A	R/W	Table 54
1.49181	1.C01D	StatusPolrty	LASI Alarm Pin Polarity	0000'h	A	R/W	Table 55

Note (1): V' is a version number. See "JTAG & AC-JTAG Operations" on page 53 for a note about the version number.
Note (2): Read values depend on status signal values. Values shown indicate 'normal' operation.
Note (3): If NVR load operation succeeds, will be overwritten by value loaded, see Table 22
Note (4): Default value depends on CX4/LX4 select LX4_MODE Pin Value. IEEE 802.3ae shows as R/W, but cannot write any other value.
Note (5): For rows with "A", the default value may be overwritten by the Auto-Configure operation (See "Auto-Configuring Control Registers" on page 16 and Table 92 for details).
Note (6): IEEE 802.3 shows as R/W, but cannot write any other value than that set by LX4_MODE Pin.

IEEE PMA/PMD REGISTERS (1.0 TO 1.15/1.000F'H)

Table 5. IEEE PMA/PMD CONTROL 1 REGISTER

MDIO REGISTER ADDRESS = 1.0 (1.0000'h)					
BIT(S)	**NAME**	**SETTING**	**DEFAULT**	**R/W**	**DESCRIPTION**
1.0.15 3.0.15 4.0.15	Reset	1 = reset 0 = reset done, normal operation	0'b	R/W SC	Writing 1 to this bit will reset the whole chip, including the MDIO registers. (1)
1.0.14	Reserved		0'b		
1.0.13	Speed Select	1 = 10Gbps	1'b	RO	1 = bits 5:2 select speed
1.0.12	Reserved		0'b		
1.0.11	LOPOWER	0 = Normal Power	0'b	R/W	No Low Power Mode, writes ignored
1.0.10:7	Reserved		0'h		
1.0.6	Speed Select	1 = 10Gbps	1'b	RO	1 = bits 5:2 select speed
1.0.5:2	Speed Select	0000 = 10Gbps	0'h	RO	Operates at 10Gbps
1.0.1	Reserved		0'b		
1.0.0	PMA Loopback	1 = Enable loopback 0 = Normal operation	0'b	R/W	Enable serial loop back mode on all four lanes, XAUI in to XAUI out.

Note (1): After this RESET bit is written, the ISL35822 will not begin counting PREAMBLE bits immediately. See Figure 17 for details.

Table 6. IEEE PMA/PMD STATUS 1 REGISTER

MDIO REGISTER ADDRESS = 1.1 (1.0001'h)					
BIT	**NAME**	**SETTING**	**DEFAULT**	**R/W**	**DESCRIPTION**
1.1.15:8	Reserved		00'h		
1.1.7	Local Fault	1 = PMA Local Fault	0'b	RO	Derived from Register 1.8.11:10
1.1.6:3	Reserved		0'h		
1.1.2	Rx Link Up	1 = PMA Rx Link Up 0 = PMA/D Rx Link Down	1'b (1)	RO LL(1)	'Up' means CX4/LX4 signal level is OK, and the PLL locked
1.1.1	LoPwrAble	Low Power Ability	0'b	RO	Device does not support a low power mode
1.1.0	Reserved		0'b		

Note (1): This bit is latched low on a detected Fault condition. It is set high on being read.

Table 7. IEEE PMA/PMD, PCS, PHY XS, SPEED ABILITY REGISTER

MDIO REGISTER ADDRESSES = 1.4, 3.4 & 4.4 ([1,3,4].0004'h)					
BIT	**NAME**	**SETTING**	**DEFAULT**	**R/W**	**DESCRIPTION**
1.4.15:3 3.4.15:2 4.4.15:1	Reserved for future speeds		000'h		
1.4.2:1 3.4.1	10PASS-T2/ 2BASE-TL	EFM Ability	00'b	RO	Device cannot operate @ 2BASE-TL or 10PASS-T2
1.4.0 3.4.0 4.4.0	10GbpsAble	10Gbps Ablility	1'b	RO	Device Able to operate @ 10Gbps

Table 8. IEEE DEVICES IN PACKAGE REGISTERS

MDIO REGISTER ADDRESSES = 1.5, 3.5, 4.5 ([1,3:4].0005'h)					
BIT	**NAME**	**SETTING**	**DEFAULT**	**R/W**	**DESCRIPTION**
[1,3:4].5.15:8	Reserved		000'h		
[1,3,4].5.7	Link Partner	Link Partner PMA/PMD present	0'b	RO	Device has no Link Partner
[1,3,4].5.6	10PASS-TS tone table	10PASS-TS tone table present	0'b	RO	Device has no 10PASS-TS tone table
[1,3:4].5.5	DTE XS	DTE XS Present	0'b	RO	Device ignores DEVAD 5
[1,3:4].5.4	PHY XS	PHY XS Present	1'b	RO	Device responds to DEVAD 4
[1,3:4].5.3	PCS	PCS Present	1'b	RO	Device responds to DEVAD 3
[1,3:4].5.2	WIS	WIS Present	0'b	RO	Device ignores DEVAD 2
[1,3:4].5.1	PMD_PMA	PMD/PMA Present	1'b	RO	Device responds to DEVAD 1
[1,3:4].5.0	Cls_22	Clause 22 registers	0'b	RO	Device ignores Clause 22
MDIO REGISTER ADDRESSES = 1.6, 3.6, 4.6 ([1,3:4].0006'h)					
[1,3:4].6.15	VndrDEV2	Vendor Specific DEV2	0'b	RO	Device ignores DEVAD 31
[1,3:4].6.14	VndrDEV1	Vendor Specific DEV1	0'b	RO	Device ignores DEVAD 30
[1,3,4].6.13	Clause 22 extn.	Clause 22 extension	0'b	RO	Device has no Clause 22 extension
[1,3:4].6.12:0	Reserved		000'h		

Table 9. IEEE PMA/PMD TYPE SELECT REGISTER

MDIO REGISTER ADDRESSES = 1.7 (1.0007'h)					
BIT	**NAME**	**SETTING**	**DEFAULT**	**R/W**	**DESCRIPTION**
1.7.15:4	Reserved		000'h		
1.7.3:0	PMA/PMD Type	0100 = 10GBASE-LX4 0000 = 10GBASE-CX4	P'b(1)	RO	LX4_MODE select pin high is LX4 value, low is CX4 value

Note (1): Value depends on the current state of the LX4/CX4 select LX4_MODE pin. Although IEEE 802.3ae specifies R/W bits, only valid values may be written; since the pin controls the available valid value, no meaningful write is possible.

Table 10. IEEE PMA/PMD STATUS 2 DEVICE PRESENT & FAULT SUMMARY REGISTER

MDIO REGISTER ADDRESSES = 1.8 (1.0008'h)					
BIT	**NAME**	**SETTING**	**DEFAULT**	**R/W**	**DESCRIPTION**
1.8.15:14	Device present	10 = Device present	10'b	RO	When read as "10", it indicates that a device is present at this device address
1.8.13	TXLocalFlt Ability	1 = PMA/PMD can detect TX Fault	1'b	RO	PMA/PMD has the ability to detect a Local Fault on Transmit Path
1.8.12	RXLocalFlt Ability	1 = PMA/PMD can detect RX Fault	1'b	RO	PMA/PMD has the ability to detect a Local Fault on Receive Path
1.8.11	TXLocalFlt	1 = TX Local Fault; on Egress channel	0'b	RO LH(1)	PLL lock fail (missing REFCLK) or TX_FAULT pin active
1.8.10	RXLocalFlt	1 = RX Local Fault; on Ingress channel	0'b	RO LH(1,2)	PLL lock fail (missing REFCLK), or Loss of Signal in 1.10 (1.000A'h)
1.8.9	Ext Ability	1 = Extended Ability Register present.	1'b	RO	Device has Extended Ability Register in 1.11 (1.000B'h)
1.8.8	TX Disable	1 = Can Disable TX	1'b	RO	Device can Disable Transmitter
1.8.7	10GBASE-SR	0 = cannot perform	0'b	RO	Device cannot be 10GBASE-SR
1.8.6	10GBASE-LR	0 = cannot perform	0'b	RO	Device cannot be 10GBASE-LR

Table 10. IEEE PMA/PMD STATUS 2 DEVICE PRESENT & FAULT SUMMARY REGISTER (Continued)

MDIO REGISTER ADDRESSES = 1.8 (1.0008'h)					
BIT	**NAME**	**SETTING**	**DEFAULT**	**R/W**	**DESCRIPTION**
1.8.5	10GBASE-ER	0 = cannot perform	0'b	RO	Device cannot be 10GBASE-ER
1.8.4	10GBASE-LX4	1 = can perform	1'b	RO	Device can be 10GBASE-LX4
1.8.3	10GBASE-SW	0 = cannot perform	0'b	RO	Device cannot be 10GBASE-SW
1.8.2	10GBASE-LW	0 = cannot perform	0'b	RO	Device cannot be 10GBASE-LW
1.8.1	10GBASE-EW	0 = cannot perform	0'b	RO	Device cannot be 10GBASE-EW
1.8.0	PMA Loopback	1 = can perform	1'b	RO	Device can perform PMA loopback

Note (1): These bits are latched high on any Fault condition detected. They are reset low (cleared) on being read. They will also be reset low on reading the LASI registers 1.9003'h (bit 10, see Table 27) or 1.9004'h (bit 11, see Table 28).

Note (2): The source of 'Loss of Signal' depends on the LX4/CX4 select LX4_MODE pin (see register 1.10, 12, note (1) below).

Table 11. IEEE TRANSMIT DISABLE REGISTER

MDIO REGISTER ADDRESS = 1.9 (1.0009'h)					
BIT	**NAME**	**SETTING**	**DEFAULT**	**R/W**	**DESCRIPTION**
1.9.15:5	Reserved				
1.9.4	PMD Dis 3	Disable TX on Lane 3(1)	0'b	R/W	1 = Disable PMD Transmit on respective Lane(1) 0 = Enable PMD Transmit on respective Lane (unless TXON/OFF pin is Low)
1.9.3	PMD Dis 2	Disable TX on Lane 2(1)	0'b	R/W	
1.9.2	PMD Dis 1	Disable TX on Lane 1(1)	0'b	R/W	
1.9.1	PMD Dis 0	Disable TX on Lane 0(1)	0'b	R/W	
1.9.0	PMD Dis All	Disable TX on all 4 Lanes	0'b	R/W	

Note (1): In CX4 mode the TCXnP/N pin outputs will be disabled; in LX4 Mode only TX_ENA[n] pin is disabled.

Table 12. IEEE PMD SIGNAL DETECT REGISTER

MDIO REGISTER ADDRESS = 1.10 (1.000A'h)					
BIT	**NAME**	**SETTING**	**DEFAULT**	**R/W**	**DESCRIPTION**
1.10.15:5	Reserved				
1.10.4	PMD Rx Ln 3	PMD Signal Det'd	1'b(1)	RO	1 = PMD Signal Detected on respective Lane (Global, all Lanes) 0 = PMD Signal not detected on respective Lane (Global, any Lane)
1.10.3	PMD Rx Ln 2	PMD Signal Det'd	1'b(1)	RO	
1.10.2	PMD Rx Ln 1	PMD Signal Det'd	1'b(1)	RO	
1.10.1	PMD Rx Ln 0	PMD Signal Det'd	1'b(1)	RO	
1.10.0	PMD Rx Glob	PMD Signal Det'd	1'b(1)	RO	

Note (1): These bits reflect the OPRLOS[3:0] pins (Table 99) in LX4 mode, or the CX4 SIGNAL_DETECT function in CX4 mode, depending on the LX4_MODE select pin.

Table 13. IEEE EXTENDED PMA/PMD CAPABILITY REGISTER(1)

MDIO Register Addresses = 1.11 (1.000B'h)					
BIT	**NAME**	**SETTING**	**DEFAULT**	**R/W**	**DESCRIPTION**
1.11.15:1	Reserved		0000'h	RO	
1.11.0(1)	10GBASE-CX4	1 = can perform	1'b	RO	Device can be 10GBASE-CX4

Note (1): These values reflect the IEEE 802.3ak 10GBASE-CX4 specification.

Table 14. IEEE PACKAGE IDENTIFIER REGISTERS

MDIO REGISTER ADDRESSES = 1.14:15 (1.000E:F'h)					
BIT	**NAME**	**SETTING**	**DEFAULT**	**R/W**	**DESCRIPTION**
1.14.15:0	Package ID	Package OUI bits 3:24 & etc.	00'h	R/W	If NVR is loaded, these are copies of 1.32818:32819 (1.8032:8033'h) & 1.32820:32821 (1.8034:8035'h)
1.15.15:0	Package ID		00'h	R/W	

XENPAK-DEFINED REGISTERS (1.8000'H TO 1.8106'H)

Table 15. XENPAK NVR CONTROL & STATUS REGISTER

MDIO (XENPAK) REGISTER ADDRESS = 1.32768 (1.8000'h)					
BIT	**NAME**	**SETTING**	**DEFAULT**	**R/W**	**DESCRIPTION**
1.32768.15:6	Reserved		000'h	R/W	
1.32768.5	NVR Command(1)	1 = Write NVR 0 = Read NVR	0'b(2)	R/W	Write/Read Control for I^2C operation
1.32768.4	Reserved		0'b	RO	
1.32768.3:2	NVR Command Status(3)	Current Status of NVR Command	00'b	RO	11 = Command failed 10 = Command in progress/Queued 01 = Command completed with success 00 = Idle
1.32768.1:0	Extended NVR Command	NVR operation to be performed	11'b(2)	R/W	10 = read/write one byte(3) 11 = read/write all NVR contents(3) Other values = reserved

Note (1): User writes to these bits are not valid unless the Command Status is Idle. The Command Status will not return to Idle until read after command completion (either Succeed or Failed).

Note (2): At the end of a hardware RESET via the RSTN pin, on powerup, or on a register [1,3,4].0.15 RESET operation, and if the XP_ENA pin is asserted, the ISL35822 will automatically begin an 'all NVR read' operation.

Note (3): The single byte commands are controlled through the bits of the registers at 1.32769:32774 (1.8001:8006'h). The 'block write/read' commands are affected by register 1.32773 (1.8005'h). Additional status is available in 1.327743 (1.8006'h)

Table 16. I^2C ONE-BYTE OPERATION DEVICE ADDRESS REGISTER

MDIO REGISTER ADDRESS = 1.32769 (1.8001'h)					
BIT	**NAME**	**SETTING**	**DEFAULT**	**R/W**	**DESCRIPTION**
1.32769.15:8	Reserved		00'h	RO	
1.32769.7:0	Device Address	I^2C Device address to access	A2'h	R/W	All I^2C Device addresses are even. Bit 0 cannot be set.

Table 17. I^2C ONE-BYTE OPERATION MEMORY ADDRESS REGISTER

MDIO REGISTER, ADDRESS = 1.32770 (1.8002'h)					
BIT	**NAME**	**SETTING**	**DEFAULT**	**R/W**	**DESCRIPTION**
1.32770.15:0	Memory Address	I^2C Memory address to access	0000'h(2)	R/W	I^2C Memory Address within Device address of 1.32769 (1.8001'h)

Note (1): 8-bit-addressed I^2C devices are addressed using bits 7:0. Never set bit 1.32773.8 (1.8005'h.8) for 16-bit address operation with an 8-bit address I^2C device.

Table 18. I^2C ONE-BYTE OPERATION READ DATA REGISTER

MDIO REGISTER ADDRESS = 1.32771 (1.8003'h)					
BIT	**NAME**	**SETTING**	**DEFAULT**	**R/W**	**DESCRIPTION**
1.32771.15:8	Reserved		00'h	RO	
1.32771.7:0	Read Data	I^2C Read Data	00'h	RO	Result of I^2C 1-byte Read operation

Table 19. I²C ONE-BYTE OPERATION WRITE DATA REGISTER

MDIO Register Address = 1.32772 (1.8004'h)					
BIT	**NAME**	**SETTING**	**DEFAULT**	**R/W**	**DESCRIPTION**
1.32772.15:8	Reserved		00'h	RO	
1.32772.7:0	Write Data	I²C Write Data	00'h	R/W	Data to be written by 1-byte Write Operation

Table 20. NVR I²C OPERATION CONTROL REGISTER

MDIO REGISTER ADDRESS = 1.32773 (1.8005'h)						
BIT	**NAME**	**SETTING**	**DEFAULT**	**R/W**	**DESCRIPTION**	
1.32773.15:9	Reserved		00'h	RO		
1.32773.8	Long Memory(1)	1 =16 bit 0 = 8 bit	0'b	R/W	Length of address for I²C device selected	
1.32773.7	NVR Write Size		0'b	R/W	1 = Block write all 256 bytes to NVR(2) 0 = Write only 1.807F:AE'h to NVR(3)	
1.32773.6:4	I²C Bus Speed	Speed of I²C SCL clock(4) (derived from REF_CLOCK)	100'b	R/W	111 = 400kHz 110 = 200kHz 101 = 150kHz 100 = 100kHz	011 = 40kHz 010 = 20kHz 001 = 10kHz 000 = 4kHz
1.32773.3:2	NVR ACK Error Count	11 = 63 10 = 16 01 = 4 00 = 1	11'b	R/W	Number of ACK failures at any address before I²C Operation failure is reported	
1.32773.1:0	NVR Write Page Size(2)	11 = 32 bytes 10 = 16 bytes 01 = 8 bytes 00 = 4 byte	01'b	R/W	The I²C interface block write operation will issue a STOP and wait for the EEPROM every time after this number of bytes are sent out	

Note (1): This bit should only be set if an I²C device which needs a 16-bit address is to be addressed. The NVR and DOM spaces are all 8-bit address sections, and for these areas, this bit should be 0'b.

Note (2): Block 256-byte NVR writes will not occur unless the WRTP pin is set Low. NVR Write Page Size controls Page size for Block operations only.

Note (3): This area corresponds to the XENPAK-defined Customer Area; see XENPAK Spec R3.0 Section 10.12.22. Writes will be performed one byte at a time.

Note (4): The I²C clock speeds listed are approximate. They are derived by division from the CMU, locked to the RFCP/N inputs. At 156.25MHz, the nominal 100kHz clock will actually be 156.25/1.6kHz, just over 97.5kHz. See also the notes to Table 117.

Table 21. NVR I²C OPERATION STATUS REGISTER

MDIO REGISTER ADDRESS = 1.32774 (1.8006'h)					
BIT	**NAME**	**SETTING**	**DEFAULT**	**R/W**	**DESCRIPTION**
1.32774.15	XP_ENA	XP_ENA pin		RO	1 = XP_ENA pin high, 0 = low
1.32774.14:4	Reserved		0000'h	RO	
1.32774.3	Vendor Specific Area EXOR sum check	Error Flag	0'b	RO LH	1 = 1.8106 ! = EXOR(1.80AE:8105) 0 = 1.8106 = EXOR(1.80AE:8105) (2)
1.32774.2	Customer Write Area EXOR sum check	Error Flag	0'b	RO LH	1 = 1.80AD ! = EXOR(1.807E:80AC) 0 = 1.80AD = EXOR(1.807E:80AC) (2)
1.32774.1	Reserved		0'b	RO LH(1)	
1.32774.0	NVR Area EXOR sum check	Error Flag	0'b	RO LH	1 = 1.807D ! = EXOR(1.8007:807C) 0 = 1.807D = EXOR(1.8007:807C) (2)

Note (1): These bits are latched high on any internal error condition detected. They are reset low (cleared) on being read.

Note (2): These bits are set if the EXOR sum calculated from the indicated range is not the same as the value read into the listed checksum register. Note that this is NOT the same as the XENPAK-defined checksum calculation. Contact Intersil for a method of reconciling these two checksum calculations.