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11.1Gb/s Lane Extender

ISL36111

The ISL36111 is a settable single-channel receive-side equalizer with extended functionality for advanced protocols operating with line rates up to 11.1Gb/s, such as 10G Ethernet. The ISL36111 compensates for the frequency dependent attenuation of copper twin-axial cables, extending the signal reach up to at least 10m on 28AWG cable.

The small form factor, highly-integrated design is ideal for high-density data transmission applications including active copper cable assemblies. The equalizing filter within the ISL36111 can be set to provide optimal signal fidelity for a given media and length. The compensation level for the filter is set by two external control pins.

Operating on a single 1.2V power supply, the ISL36111 enables channel throughputs of 10Gb/s to 11.1Gb/s while supporting lower data rates including 8.5, 6.25, 5, 4.25, 3.125, 2.5 and 1 Gb/s. The ISL36111 uses current mode logic (CML) input/output and is packaged in a 3mmx3mm 16 lead QFN. The device supports LOS functionality for module applications.

Features

- Supports data rates up to 11.1Gb/s
- Low power (~110mW)
- Low latency (<500ps)
- Single channel equalizer in a 3mmx3mm QFN package for straight route-through architecture and simplified routing
- Adjustable equalizer boost
- Supports 64b/66b encoded data – long run lengths
- Line silence preservation
- 1.2V supply voltage
- Loss of Signal support

Applications

- SFP+ active copper cable modules
- QSFP active copper cable modules
- 10G Ethernet
- Fibre Channel
- High-speed active cable assemblies
- High-speed printed circuit board (PCB) traces

Benefits

- Thinner gauge cable
- Extends cable reach greater than 3x
- Improved BER

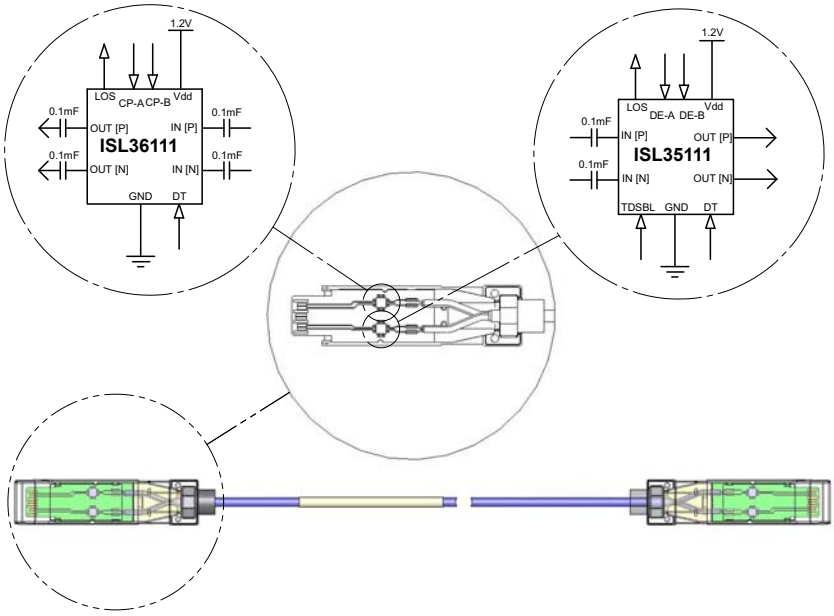


FIGURE 1. TYPICAL CABLE APPLICATION DIAGRAM

Ordering Information

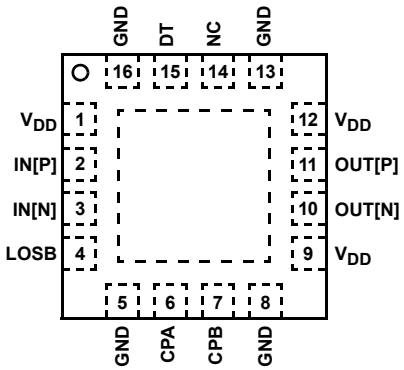
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL36111DRZ-TS	6111	0 to +85	16 Ld QFN (7'' 100 pcs.)	L16.3x3B
ISL36111DRZ-T7	6111	0 to +85	16 Ld QFN (7" 1k pcs.)	L16.3x3B

NOTES:

1. "-TS" and "-T7" suffix is for Tape and Reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL36111. For more information on MSL please see techbrief TB363.

Pin Configuration

ISL36111
(16 LD QFN)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
V_{DD}	1, 9, 12	Power supply. 1.2V supply voltage. The use of parallel 100pF and 47nF decoupling capacitors to ground is recommended for each of these pins for broad high-frequency noise suppression.
IN[P,N]	2, 3	Equalizer differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
LOSB	4	LOS BAR indicator. Low output when input signal is below DT threshold. This pin is internally pulled HIGH with an 11kΩ resistor.
CP[A,B]	6, 7	Control pins for setting equalizer boost level. Tri-state inputs. Pins are read as a 2-digit number to set the boost level. A is the MSB, and B is the LSB.
GND	5, 8, 13, 16	These pins must be grounded.
OUT[P,N]	11, 10	Equalizer differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
DT	15	Detection Threshold. Reference DC voltage threshold for input signal power detection. Data output OUT[P,N] is muted when the power of the input signal IN[P,N] falls below the threshold. Tie to ground to disable electrical idle preservation and always enable the output driver.
Exposed Pad	-	Exposed pad. For proper electrical and thermal performance, this pad should be connected to the PCB ground plane.

Absolute Maximum Ratings

Supply Voltage (V_{DD} to GND) . . . . . -0.3V to 1.5V
Voltage at All Input Pins. . . . . -0.3V to 1.5V
ESD Rating
High-Speed Pins . . . . . 1.5kV (HBM)
All Other Pins . . . . . 2kV (HBM)

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld QFN Package (Notes 4, 5)	56	10

Operating Ambient Temperature Range . . . . . 0°C to +85°C
Storage Ambient Temperature Range . . . . . -55°C to +150°C
Maximum Junction Temperature . . . . . +125°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Operating Conditions

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		1.1	1.2	1.3	V
Operating Ambient Temperature	T_A		0	25	85	°C
Bit Rate		NRZ data applied to any channel	1		11.1	Gb/s

Control Pin Characteristics

V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 600mV_{P-P}, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN (Note 14)	TYP	MAX (Note 14)	UNITS
Output LOW Logic Level	V_{OL}	LOSB	0	0	250	mV
Output HIGH Logic Level	V_{OH}	LOSB	1000		V_{DD}	mV
Input Current		Current draw on boost control pin, i.e., CP[A,B]		30	100	µA

Electrical Specifications

V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 600mV_{P-P}, unless otherwise noted.

PARAMETERS	SYMBOL	CONDITION	MIN (Note 14)	TYP	MAX (Note 14)	UNITS	NOTES
Supply Current	I_{DD}			92		mA	
Cable Input Amplitude Range	V_{IN}	Measured differentially at data source before encountering channel loss; Up to 10m 28AWG standard twin-axial cable (approx. -27dB @ 5GHz)	600		1600	mV_{P-P}	6
DC Differential Input Resistance		Measured on input channel IN[P,N]	80	100	120	Ω	
DC Single-Ended Input Resistance		Measured on input channel IN[P] or IN[N], with respect to V_{DD}.	40	50	60	Ω	
Input Return Loss Limit (Differential)	$S_{DD}11$	100MHz to 4.1GHz		Note 7		dB	7
		4.1GHz to 11.1GHz		Note 8		dB	8
Output Amplitude Range	V_{OUT}	Measured differentially at OUT[P] and OUT[N] with 50Ω load on both output pins	450	650	850	mV_{P-P}	
Differential Output Impedance		Measured on OUT[P,N]	80	105	120	Ω	
Output Return Loss Limit (Differential)	$S_{DD}22$	100MHz to 4.1GHz		Note 7		dB	7
		4.1GHz to 11.1GHz		Note 8		dB	8
Output Return Loss Limit (Common Mode)	$S_{CC}22$	100MHz to 2.5GHz		Note 9		dB	9
		2.5GHz to 11.1GHz		-3		dB	10

Electrical Specifications V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 600mV_{P-P}, unless otherwise noted. (Continued)

PARAMETERS	SYMBOL	CONDITION	MIN (Note 14)	TYP	MAX (Note 14)	UNITS	NOTES
Output Residual Jitter		10.3125Gbps; Up to 10m 28AWG standard twin-axial cable (approx. -27dB @ 5GHz)		0.35		UI	6, 11, 12
Output Transition Time	t_r, t_f	20% to 80%		32		ps	13
Propagation Delay		From IN to OUT		500		ps	

NOTES:

6. The input pins IN[P,N] are DC biased to V_{DD}. The specified cable input amplitude range is established by characterization and not production tested, and is valid so long as the voltages at the input pins IN[P,N] do not violate the voltage ranges specified in “Absolute Maximum Ratings” on page 3.
7. Maximum Reflection Coefficient given by equation SDDXX(dB) = -12 + 2*√(f), with f in GHz. Established by characterization and not production tested.
8. Maximum Reflection Coefficient given by equation SDDXX(dB) = -6.3 + 13Log10(f/5.5), with f in GHz. Established by characterization and not production tested.
9. Reflection Coefficient given by equation SCCXX(dB) < -7 + 1.6*f, with f in GHz. Established by characterization and not production tested.
10. Limits established by characterization and are not production tested.
11. Output residual jitter is the difference between the total jitter at the lane extender output and the total jitter of the transmitted signal (as measured at the input to the channel). Total jitter (T_J) is DJ_{pp} + 14.1 x RJ_{RMS}
12. Measured using a PRBS 2^{15}-1 pattern. Deterministic jitter at the input to the lane extender is due to frequency-dependent, media-induced loss only.
13. Rise and fall times measured using a 2GHz clock with a 20ps edge rate.
14. Compliance to limits is assured by characterization and design.

Typical Performance Characteristics

Performance is measured using the test setup illustrated in Figure 2. The signal from the pattern generator is launched into the twin-ax cable using an SMA adapter card. The chip evaluation board is connected to the output of the cable through another adapter card. The ISL36111 output signal is then visualized on a scope to determine signal integrity parameters such as jitter.

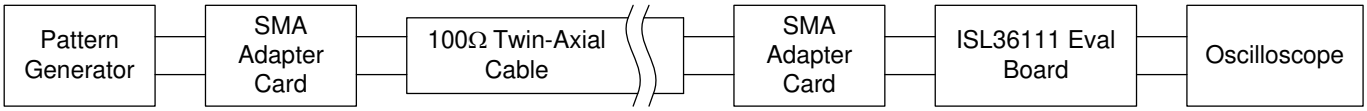


FIGURE 2. DEVICE CHARACTERIZATION SET UP

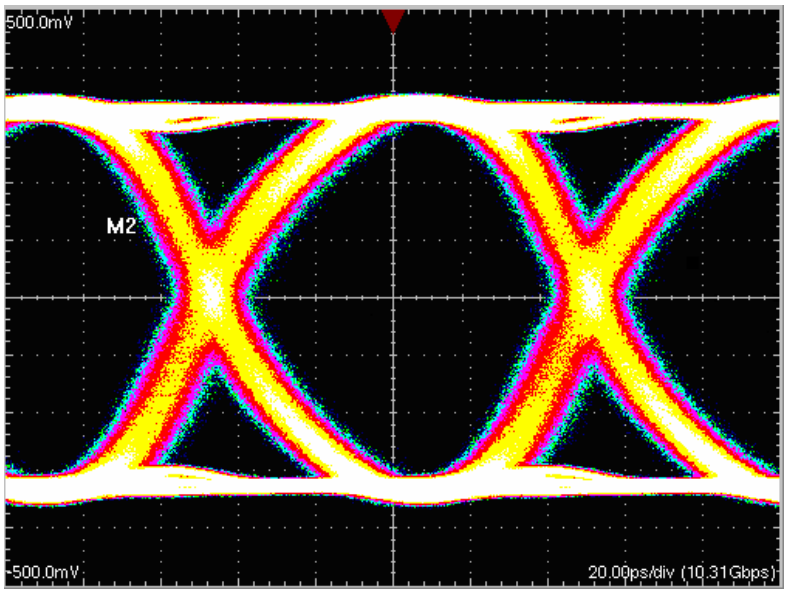


FIGURE 3. ISL36111 10.3125Gb/s OUTPUT FOR A 10M 28AWG CABLE

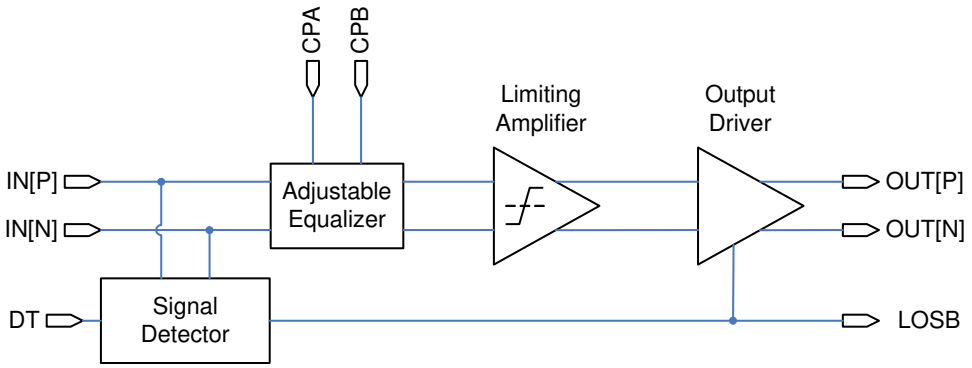


FIGURE 4. FUNCTIONAL BLOCK DIAGRAM OF THE ISL36111

Operation

The ISL36111 is an advanced lane-extender for high-speed interconnects. A functional diagram of ISL36111 is shown in Figure 4. In addition to a robust equalization filter to compensate for channel loss and restore signal fidelity, the ISL36111 contains unique integrated features to preserve special signaling protocols typically broken by other equalizers. The signal detect function is used to mute the channel output when the input signal falls below the level determined by the Detection Threshold (DT) pin voltage. This function is intended to preserve periods of line silence ("DC idle"). Furthermore, the output of the Signal Detect/DT comparator is used as a loss of signal (LOSB) indicator to indicate the absence of a received signal.

As illustrated in Figure 4, the core of the high-speed signal path in the ISL36111 is a sophisticated equalizer followed by a limiting amplifier. The equalizer compensates for skin loss, dielectric loss, and impedance discontinuities in the transmission channel. The equalizer is followed by a limiting amplification stage that provides a clean output signal with full amplitude swing and fast rise-fall times for reliable signal decoding in a subsequent receiver.

Adjustable Equalization Boost

ISL36111 features a settable equalizer for custom signal restoration. The flexibility of this adjustable compensation architecture enables signal fidelity to be optimized based on a given application, providing support for a wide variety of channel characteristics and data rates ranging from 2.5Gb/s to 11.1Gb/s. Because the boost level is externally set rather than internally adapted, the ISL36111 provides reliable communication from the very first bit transmitted. There is no time needed for adaptation and control loop convergence. Furthermore, there are no pathological data patterns that will cause the ISL36111 to move to an incorrect boost level.

Control Pin Boost Setting

The connectivity of the CP pins are used to determine the boost level of ISL36111. Table 1 defines the mapping from the 2-bit CP word to the 9 available boost levels.

TABLE 1. MAPPING BETWEEN BOOST LEVEL AND CP-PIN CONNECTIVITY

CPA	CPB	BOOST LEVEL
Float	Float	0
Float	GND	1
GND	VDD	2
Float	VDD	3
VDD	Float	4
GND	Float	5
GND	GND	6
VDD	GND	7
VDD	VDD	8

CML Input and Output Buffers

The input and output buffers for the high-speed data channel in the ISL36111 are implemented using CML. Equivalent input and output circuits are shown in Figures 5 and 6.

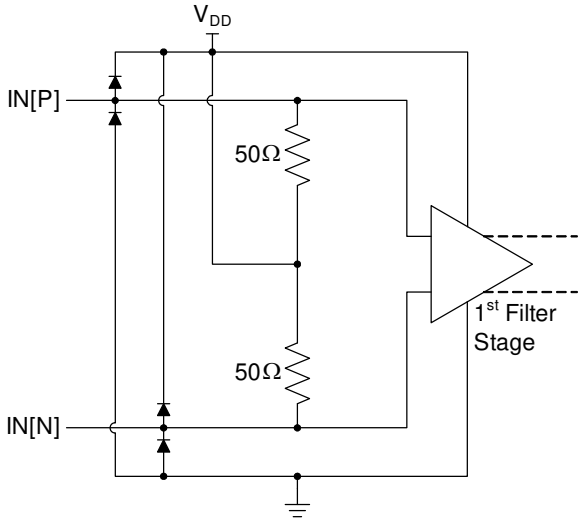


FIGURE 5. CML INPUT EQUIVALENT CIRCUIT FOR THE ISL36111

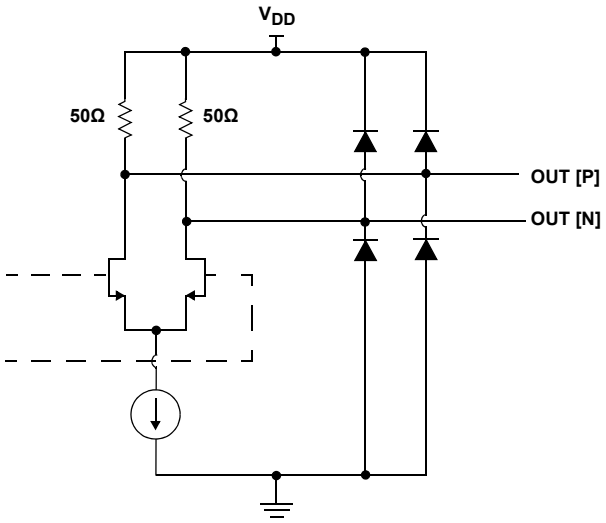


FIGURE 6. CML OUTPUT EQUIVALENT CIRCUIT FOR THE ISL36111

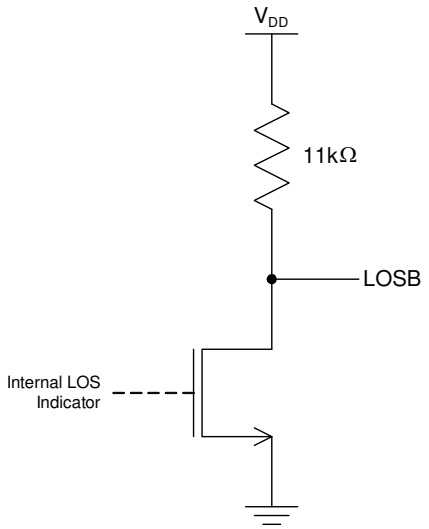


FIGURE 7. LOSB EQUIVALENT OUTPUT STRUCTURE

Line Silence/Quiescent Mode

Line silence is commonly broken by the limiting amplification in other equalizers. This disruption can be detrimental in many systems that rely on line silence as part of the protocol. The ISL36111 contains special lane management capabilities to detect and preserve periods of line silence while still providing the fidelity-enhancing benefits of limiting amplification during active data transmission. Line silence is detected by measuring the amplitude of the input signal and comparing that to a threshold set by the voltage at the DT pin. When the amplitude falls below the threshold, the output driver stage is muted.

LOS Bar Indicator

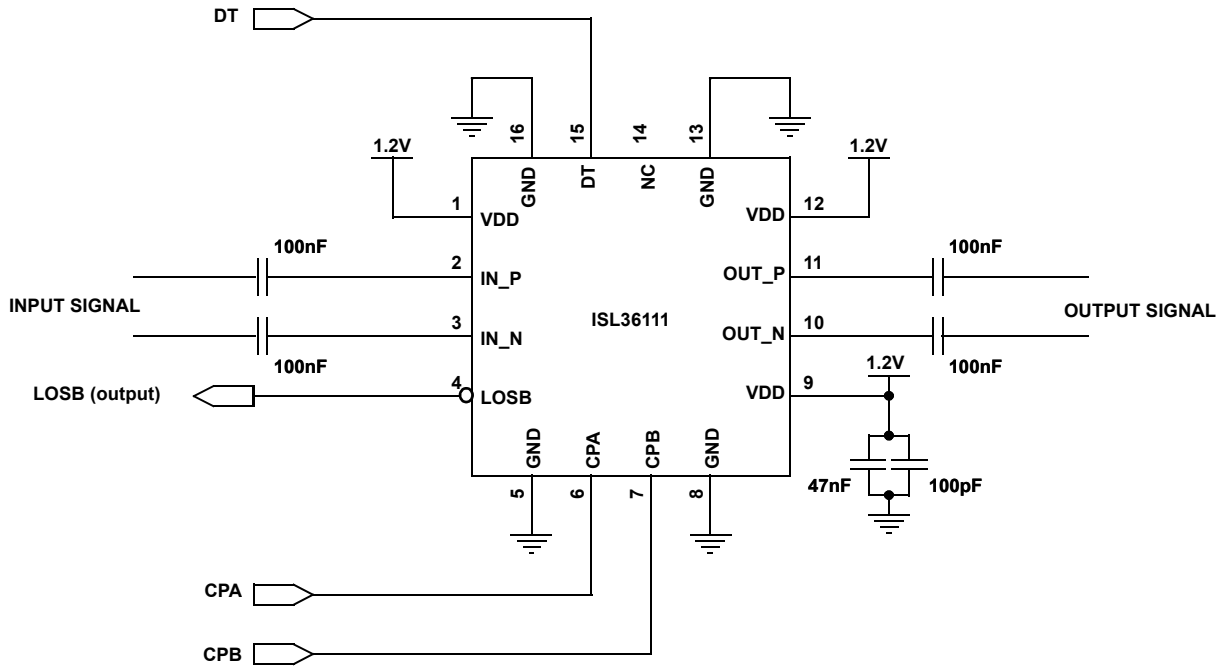
Pin 4 (LOSB) is used to output the state of the muting circuitry to serve as a loss of signal indicator for the device. This signal is directly derived from the muting signal output by the detection threshold / signal detector comparator. The LOSB signal goes LOW when the signal detector output is below the externally controlled detection threshold and HIGH when the detector output goes above this threshold. This feature is meant to be used in optical systems (e.g. SFP+) where there are no quiescent or electrical-idle states. In these cases, the detection threshold is used to determine the sensitivity of the LOSB indicator. Figure 7 shows the schematic of the LOSB equivalent output structure.

Detection Thereshold (DT) Pin Functionality

The ISL36111 is capable of maintaining periods of line silence by monitoring the channel for loss of signal (LOS) conditions and subsequently muting the output driver when such a condition is detected. A reference voltage applied to the detection threshold (DT) pin is used to set the LOS threshold of the internal signal detection circuitry. The DT voltage is set with an external pull-up resistor, R_{DT}. For typical applications, a 30kΩ resistor is recommended for channels with loss greater than 12dB at 5GHz, and a 1.8kΩ resistor is recommended for lower loss channels. Other values of the resistor may also be applicable; therefore DT settings should be verified on an application-specific basis.

Application Information

Typical application schematic for ISL36111 is shown in Figure 8.



NOTES:

14. See “Control Pin Boost Setting” on page 5 for information on how to connect the CP pins
15. See “Detection Thereshold (DT) Pin Functionality” on page 6 for details on DT pin operation.
16. Although the filtering network is shown only for one V_{DD} pin for simplicity, all the V_{DD} pins need to be connected in this way.

FIGURE 8. TYPICAL APPLICATION REFERENCE SCHEMATIC FOR ISL36111

PCB Layout Considerations

Because of the high speed of the ISL36111 signals, careful PCB layout is critical to maximize performance. The following guidelines should be adhered to as closely as possible:

- All high speed differential pair traces should have a characteristic impedance of 50Ω with respect to ground plane and 100Ω with respect to each other.
- Avoid using vias for high speed traces as this will create discontinuity in the traces characteristic impedance.
- Input and output traces need to have DC blocking capacitors (100nF). Capacitors should be placed as close to the chip as possible.
- For each differential pair, the positive trace and the negative trace need to be of same length in order to avoid intra-pair skew. Serpentine technique may be used to match trace lengths.
- Maintain a constant solid ground plane underneath the high-speed differential traces
- Each V_{DD} pin should be connected to 1.2V and also bypassed to ground through a 47nF and a 100pF capacitor in parallel. Minimize the trace length and avoid vias between the V_{DD} pin and the bypass capacitors in order to maximize the power supply noise rejection.

About Q:ACTIVE®

Intersil has long realized that to enable the complex server clusters of next generation datacenters, it is critical to manage the signal integrity issues of electrical interconnects. To address this, Intersil has developed its groundbreaking Q:ACTIVE® product line. By integrating its analog ICs inside cabling interconnects, Intersil is able to achieve unsurpassed improvements in reach, power consumption, latency, and cable gauge size as well as increased airflow in tomorrow’s datacenters. This new technology transforms passive cabling into intelligent “roadways” that yield lower operating expenses and capital expenditures for the expanding datacenter.

Intersil Lane Extenders allow greater reach over existing cabling while reducing the need for thicker cables. This significantly reduces cable weight and clutter, increases airflow, and improves power consumption.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
July 12, 2012	FN6974.2	On page 1, Column 1, changed last paragraph from: "Operating on a single 1.2V power supply, the ISL36111 enables channel throughputs of 10Gb/s to 11.1Gb/s while supporting lower data rates including 8.5, 6.25, 5, 4.25, 3.125 and 2.5Gb/s." to: "Operating on a single 1.2V power supply, the ISL36111 enables channel throughputs of 10Gb/s to 11.1Gb/s while supporting lower data rates including 8.5, 6.25, 5, 4.25, 3.125, 2.5 and 1 Gb/s." In “Electrical Specifications” on page 3 , changed Min Entry for “Bit Rate” from: "2.5Gb/s" to: "1Gb/s" Added Note 14 to MIN and MAX columns of spec tables.
October 27, 2010	FN6974.1	1. Added “Application Information” on page 7, Figure 8 on page 7, and “PCB Layout Considerations” on page 7 2. Corrected “Pin Descriptions” on page 2 for VDD pin from "and 10nF decoupling capacitors.." to “and 47nF decoupling capacitors.." 3. Corrected “Pin Descriptions” on page 2 for CP[A,B] pin from "Pins are read as a 3-digit number.." to "Pins are read as a 2-digit number.."
November 19, 2009	FN6974.0	Initial Release to web

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL36111

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

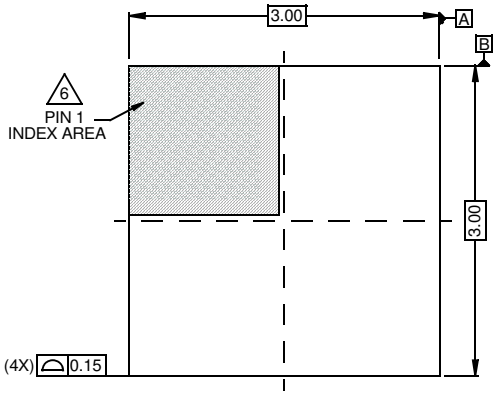
FITs are available from our website at http://rel.intersil.com/reports/search.php

Package Outline Drawing

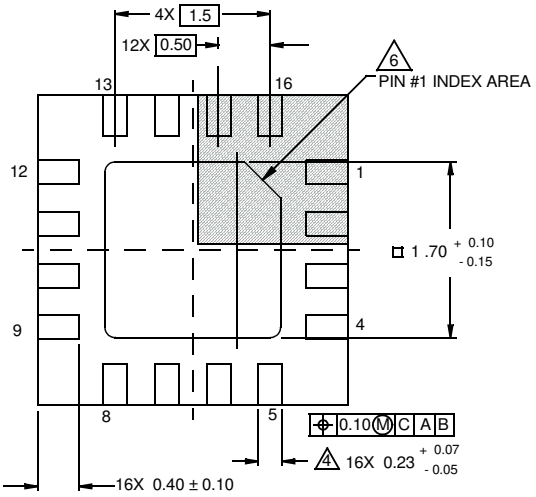
L16.3x3B

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

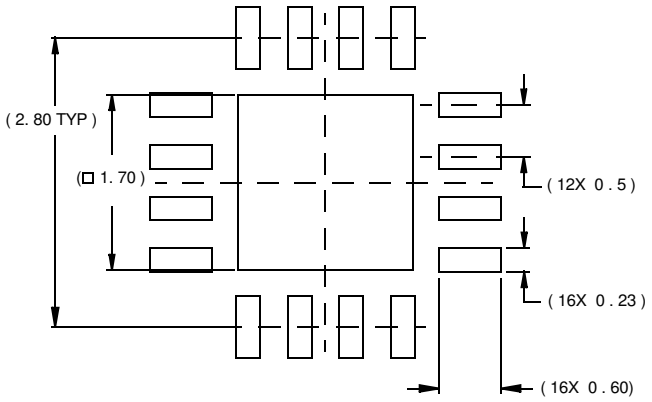
Rev 1, 4/07



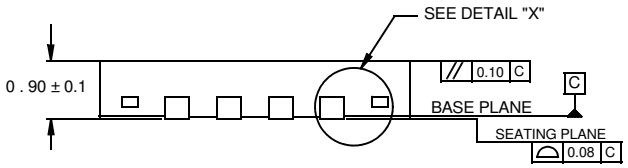
TOP VIEW



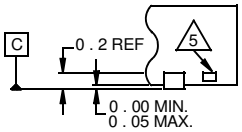
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.