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Data Sheet June 28, 2006 FN6192.1

DC-Restored Video Amplifier

The ISL4089 is complete DC-restored monolithic video amplifier sub-system. It contains a high performance video amplifier and a nulling, sample-and-hold amplifier designed to establish a programmable DC output level.

When the HOLD logic input “0” is applied the DC restore function is active. The sample-and-hold amplifier loop is closed and used to null the DC offset of the video amplifier. This can occur during sync, or, at any time that a black level is expected. When the HOLD input “1” is applied, the correcting voltage is stored on the video amplifier’s input coupling capacitor. This condition must be true during active video. The restored DC voltage level can be adjusted using an external reference voltage applied to the V_{REF} pin.

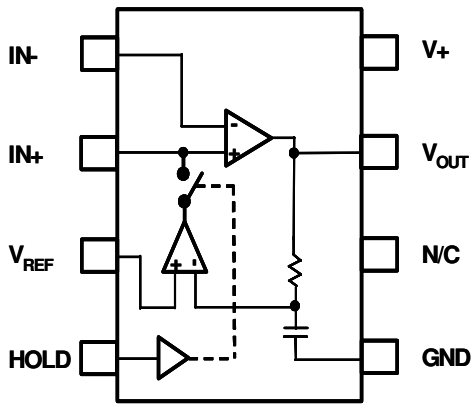
The device operates from a single +5V supply and is ideal for +5V only systems when used with a sync separator, such as the EL1883.

The ISL4089 is intended to directly replace the EL4089 only in certain applications. This direct replacement requires that the single positive supply is no higher than +5.5V and that no part of the clamped output goes below ground. The NC on pin 6 is not internally connected, so it can be connected to the -5V pin in existing EL4089 applications.

The ISL4089 is specified for operation over -40°C to +85°C temperature range.

Pinout

ISL4089
(8 Ld SOIC)
TOP VIEW



Features

- Complete video level DC-restoration system
- 0.03% differential gain and 0.05° differential phase accuracy
- 300MHz -3dB small signal bandwidth at A_V = 1
- 150MHz -3dB small signal bandwidth at A_V = 2
- 300V/µs Slew Rate
- 0.1dB flatness to 80MHz
- +5V single supply operation
- TTL/CMOS compatible hold signal
- Pb-free plus anneal available (RoHS compliant)

Applications

- Input amplifier in video equipment
- DC-restoration amplifier in video mixers

Related Documents

- AN1261: ISL4089EVAL1 User’s Guide
- AN1089: EL4089 and EL4390 DC-Restored Video Amplifier

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
ISL4089IBZ (See Note)	4089IBZ	-	8 Ld SO (Pb-free)	MDP0027
ISL4089IBZ-T7 (See Note)	4089IBZ	7”	8 Ld SO (Pb-free)	MDP0027

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and GND 5.5V
Voltage between IN+, IN-, HOLD, V_{REF} and GND
. . . . . GND -0.5;V+ +0.5V
Supply Turn-on Slew Rate 1V/µs
Digital and Analog Input Current (Note 1) 50mA
Output Current (Continuous) 60mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7). . . .3000V
Machine Model 250V

Storage Temperature Range . . . . . .-65°C to +150°C
Ambient Operating Temperature . . . . . .-40°C to +85°C
Operating Junction Temperature . . . . . .-40°C to +125°C
Power Dissipation . . . . . See Curves

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

V+ = +5V, Load = 1kΩ; T_A = +25°C

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
AMPLIFIER SECTION (HOLD = 5V)						
Ib+	IN+ Input Bias Current	V_{IN+} = 2.5V	-7		20	µA
Ib-	IN- Input Bias Current	V_{IN-} = 1.3V	-30		-1	µA
A_{VOL}	Open Loop Gain			60		dB
V_{OUT+}	High Output Level	R_L = 1k	3.5			V
V_{OUT-}	Low Output Level	IL = 0mA			5	mV
I_{SC}	Short Circuit Current			100		mA
RESTORE SECTION						
V_{OS}, Comp	Composite Input Offset Voltage	V_{REF} = 0V to +2.5V		10	15	mV
I_{OUT}	Restoring Current Available			300		µA
PSRR	Power Supply Rejection Ratio	V+ = 5V to 6V	70	90		dB
Ib V_{REF}	V_{REF} Input Bias Current	V_{REF} = +2.5V	-0.8	-0.5	-0.2	µA
V_H HOLD	HOLD Logic Input Low				0.8	V
V_L HOLD	HOLD Logic Input High		2.0			V
I_{IH}, Hold	HOLD Input Current @ Logic High	V_{HOLD} = 5V	-15		30	µA
I_{IL}, Hold	HOLD Input Current @ Logic Low	V_{HOLD} = 0V	-5		5	µA
I_S	Supply Current	V_{HOLD} = 0V	17	20	23	mA

AC Electrical Specifications

V_S = +5V, V_{REF} = 0V_{DC}, R_L = 150Ω, R_F and R_G = 475Ω; A_V = 2, T_A = +25°C.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNITS
AMPLIFIER SECTION						
SR	Slew Rate; 2V_{P-P}, 20% to 80%			300		V/µs
tr, tf	Output Rise and Fall Times	V_{OUT} = 0.2Vp-p; 10% to 90%		3.2		ns
tpd	Propagation Delay, IN+ to Output	V_{OUT} = 0.2V; 10% to 10%		0.3		ns
-3dB BW	Small Signal; Unity Gain	R_F = 0; R_G = inf.; C_L = 0.6pF, V_{OUT} = 0.2V_{P-P}		300		MHz
	Large Signal; Unity Gain	R_F = 0; R_G = inf.; C_L = 0.6pF, V_{OUT} = 2V_{P-P}		95		MHz
	Small Signal; A_V = +2	C_L = 0.6pF, V_{OUT} = 0.2V_{P-P}		150		MHz
	Large Signal; A_V = +2	C_L = 0.6pF, V_{OUT} = 2V_{P-P}		85		MHz

AC Electrical Specifications V_S = +5V, V_{REF} = 0V_{DC}, R_L = 150Ω, R_F and R_G = 475Ω; A_V = 2, T_A = +25°C. **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNITS
0.1dB BW	0.1dB Gain Flatness; Unity Gain	R_F = 0; R_G = inf.; C_L = 0.6pF V_{OUT} = 0.2V_{P-P}		70		MHz
		R_F = 0; R_G = inf.; C_L = 0.6pF V_{OUT} = 2V_{P-P}		60		MHz
	0.1dB Gain Flatness; A_V = +2	C_L = 0.6pF, V_{OUT} = 0.2V_{P-P}		80		MHz
		C_L = 0.6pF, V_{OUT} = 2V_{P-P}		50		MHz
dG	Differential Gain Error	NTC-7, Restore on sync tip		0.03		%
dP	Differential Phase Error	NTC-7, Restore on sync tip		0.05		°
RESTORE SECTION						
T_{HE}	Time to Enable Hold; 50% to 50%	HOLD input 0V to +5V		40		ns
T_{HD}	Time to Disable Hold; 50% to 50%	HOLD input 5V to 0V		20		ns

NOTE:

1. If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values

Typical Performance Curves V_S = +5V, R_L = 150Ω to GND, C_L = 0.6pF, T_A = 25°C, unless otherwise specified.

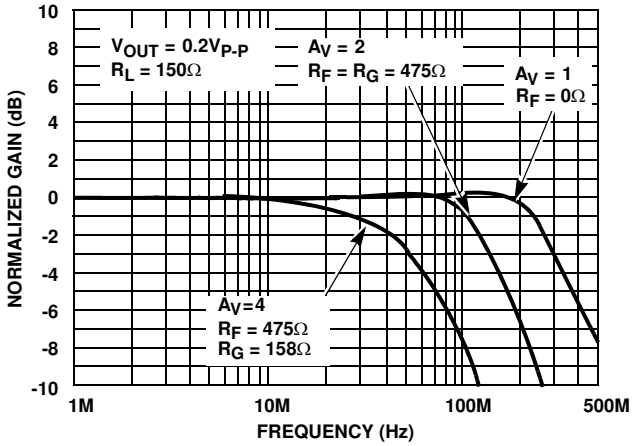


FIGURE 1. SMALL SIGNAL GAIN vs FREQUENCY for VARIOUS GAINS

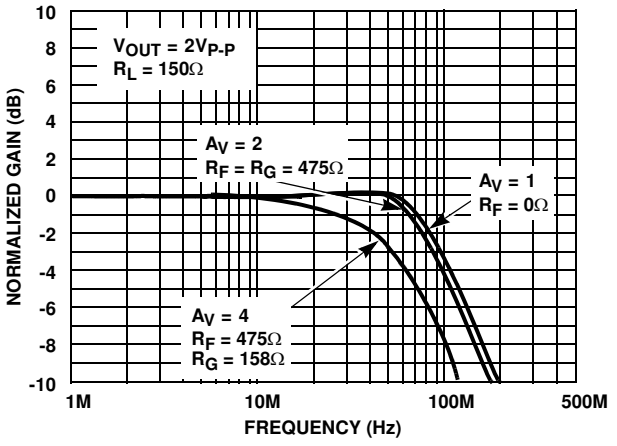


FIGURE 2. LARGE SIGNAL GAIN vs FREQUENCY for VARIOUS GAINS

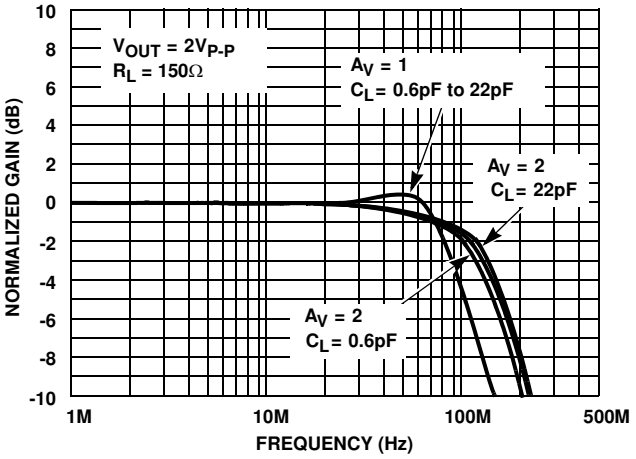


FIGURE 3. LARGE SIGNAL GAIN vs FREQUENCY vs C_L

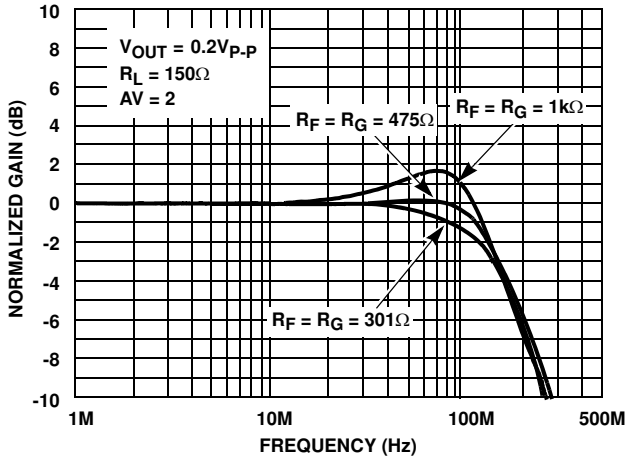


FIGURE 4. SMALL SIGNAL GAIN vs R_F, R_G

Typical Performance Curves V_S = +5V, R_L = 150Ω to GND, C_L = 0.6pF, T_A = 25°C, unless otherwise specified. **(Continued)**

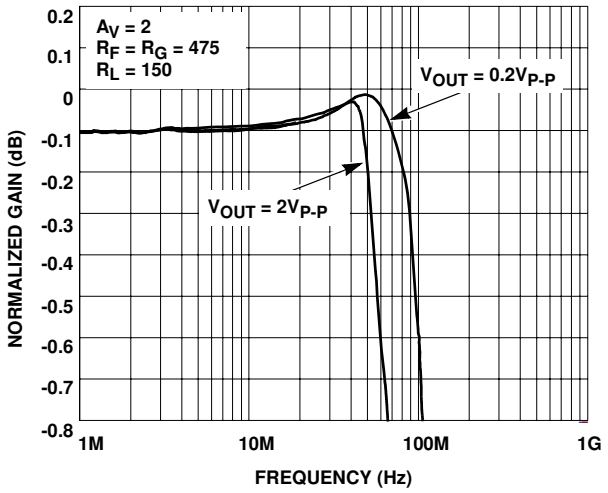


FIGURE 5. 0.1dB GAIN FLATNESS

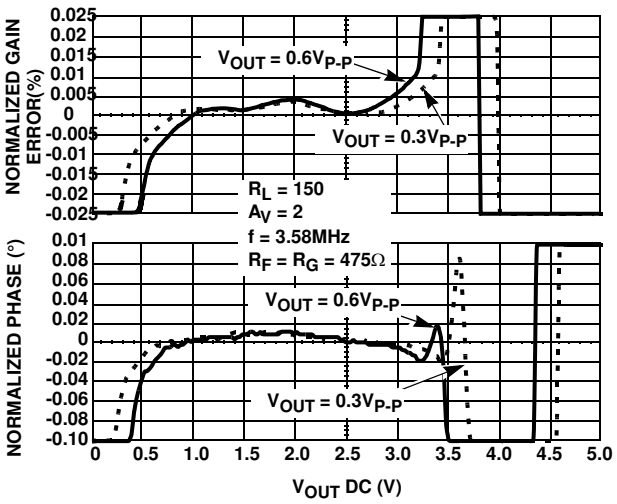


FIGURE 6. DIFFERENTIAL GAIN - PHASE

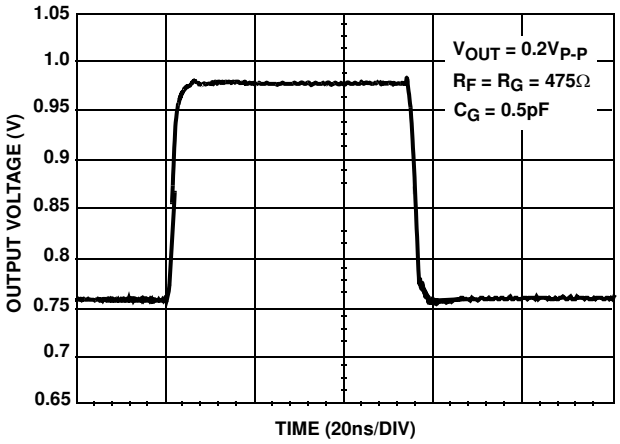


FIGURE 7. SMALL SIGNAL TRANSIENT RESPONSE; A_V = 2

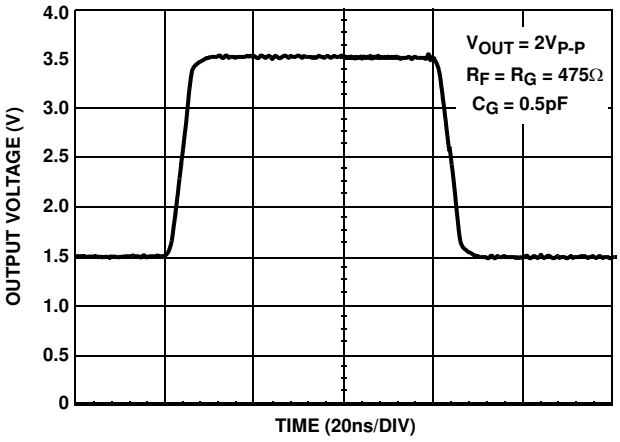


FIGURE 8. LARGE SIGNAL TRANSIENT RESPONSE; A_V = 2

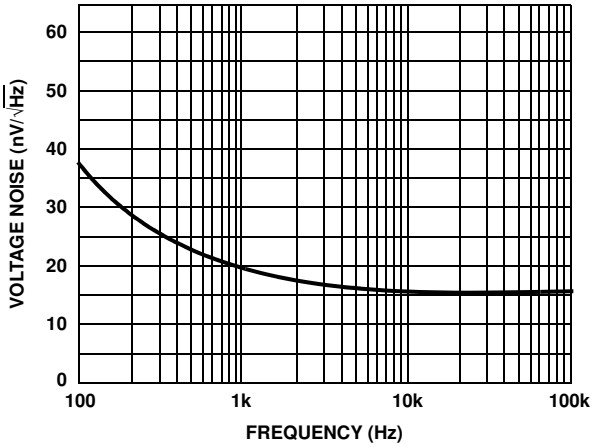


FIGURE 9. INPUT NOISE vs FREQUENCY

Typical Performance Curves V_S = +5V, R_L = 150Ω to GND, C_L = 0.6pF, T_A = 25°C, unless otherwise specified. **(Continued)**

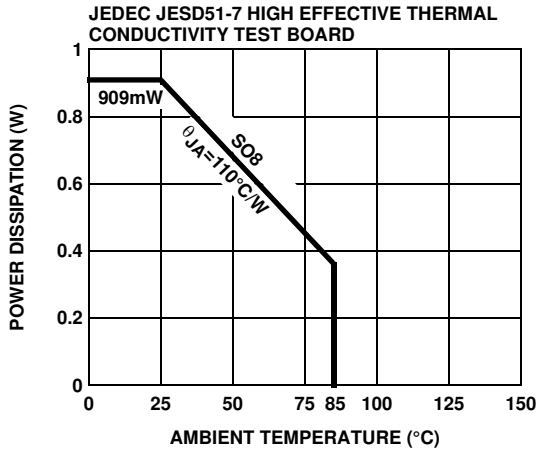


FIGURE 10. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

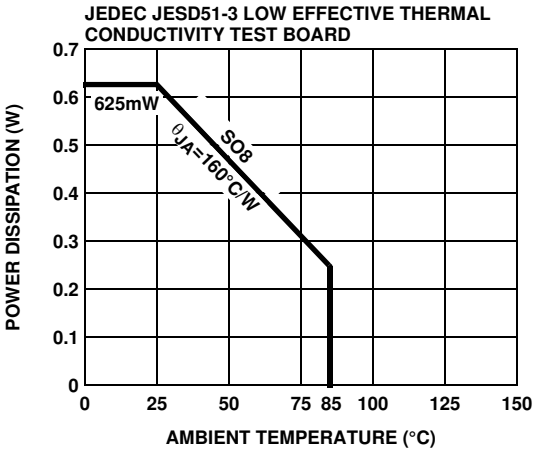
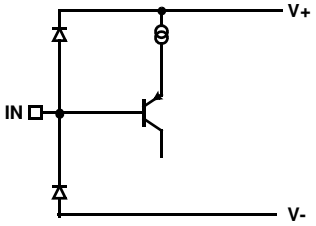
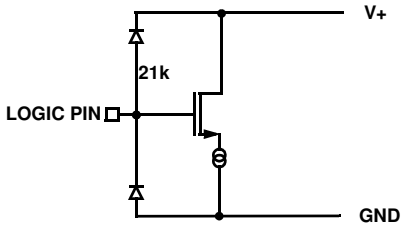


FIGURE 11. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

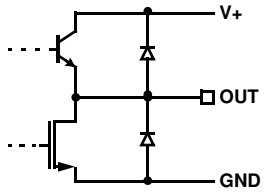
ISL4089 (8 LD SOIC)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	IN-	Circuit 1	Video amplifier inverting input
2	N+	Circuit 1	Video amplifier non-inverting input
3	V_{REF}	Circuit 1	Restore amplifier V_{REF} input
4	HOLD	Circuit 2	Hold/restore logic input. Logic “0” selects the restore state; logic “1” selects the hold state
5	GND	Circuit 4	Ground
6	NIC	Circuit 1	No internal connection
7	V_{OUT}	Circuit 3	Video amplifier output
8	V+	Circuit 4	Positive power supply



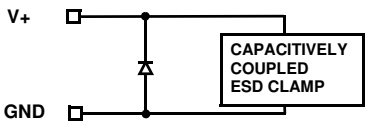
CIRCUIT 1



CIRCUIT 2



CIRCUIT 3



CIRCUIT 4

AC Test Circuits

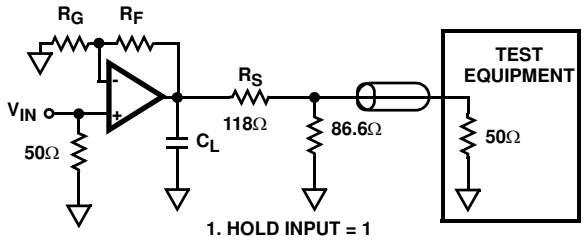


FIGURE 12A. VIDEO AMPLIFIER AC TEST CIRCUIT FOR 50Ω

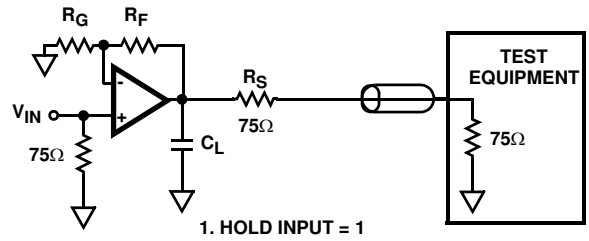


FIGURE 12B. BACKTERMINATED TEST CIRCUIT FOR VIDEO CABLE APPLICATION.

Figure 12A illustrates the AC test circuit used to operate the video amplifier into a 150Ω load while providing a 50Ω matched impedance. Figure 12B illustrates the test circuit for impedance matching to 75Ω test equipment.

Application Information

General

The ISL4089 implements the video DC-restore function using a high performance gain adjustable video amplifier and a nulling, sample-hold amplifier to establish a user defined DC reference voltage at the video amplifier output. A detailed description of the DC-restore function implemented in the ISL4089 can be found in application note AN1089, EL4089 and EL4390 DC-Restored Video Amplifier. The ISL4089 performs the same function with the exception that it is designed for single supply operation.

Video Amplifier Operation (Figure 13)

The ISL4089 video amplifier (A1) is voltage-feed, high performance video amplifier designed for +5V operation. The output stage is capable of swinging to within 10mV of the negative rail. The differential input stage contains an internal voltage reference that positions the non-inverting input DC level (V1) to ~1.2V higher than the negative supply rail. This offset ensures that the amplifier input DC level is maintained within the common mode input voltage range. The amplifier non-inverting gain is given in Equation 1.

$$V_{OUT} = (V_{IN+} - 1.2V) \bullet \left(1 + \frac{R_F}{R_G}\right) \quad \text{(EQ. 1)}$$

DC-Restore Amplifier (Figure 13)

The DC-restore circuit contains a voltage reference amplifier and an analog switch function that closes the DC-restore loop under control of the HOLD logic input. The reference amplifier uses an internal 10mV offset voltage (V2) to enable the V_{REF} input to sense down to the negative supply. The A2 amplifier output stage operates in a current-feed mode with a source/sink capability of ±300µA (Typ).

A logic “0” at the HOLD input closes switch S1 which closes the DC-restore loop. The video input AC coupling capacitor, CX1, acts as a DC hold capacitor (through the 75Ω termination resistor RX1) to average the current-source output of amplifier A2. When the DC-restore loop has reached equilibrium, the DC voltage stored on CX1 will the value required to force the output voltages at A1 (V_{OUT}) and A2 (V_{IN+}) according to the following:

$$V_{OUT}(DC) = V_{REF} + 10mV \quad \text{(EQ. 2)}$$

and; the DC voltage at the non-inverting input of the video amplifier A1 is given in Equation 3:

$$V_{IN+} = V_{OUT}(DC) + 1.2V \quad \text{(EQ. 3)}$$

Therefore, if V_{REF} is set to 0V (GND); V_{OUT} = 10mV, and the DC voltage stored on CX1 is ~1.2V.

The CX1 capacitor value is chosen from the system requirements. A typical DC-restore application using the horizontal sync to drive the HOLD pin will result in a 62µs hold time. The typical input bias current to the video amplifier is 1.2µA, so for a 62µs hold time, and a 0.01µF capacitor, the output voltage drift is 7.5mV in one line. The restore amplifier can provide a typical current of 300µA to charge capacitor CX1, so with a 1.2µs sampling time, the output can be corrected by 36mV in each line.

Using a smaller value of CX1 increases both the voltage that can be corrected, as well as the droop while being held. Likewise, using a larger value of CX1, reduces the correction and droop voltages. A sample of charging and droop rates are shown on the following table.

TABLE OF CHARGE STORAGE CAPACITOR VS DROOP CHARGING RATES (NOTE)

CAP VALUE (if)	DROOP IN 62µs (mV)	CHARGE IN 1.2µs (mV)	CHARGE IN 4µs (mV)
10	7.5	36	120
33	2.3	11	36
100	0.75	3.6	12

NOTE: Basic formulae are: V (droop) = Ib+ * (Line time - Sample time)/Capacitor and V (charge) = I_{OUT} * Sample time/Capacitor

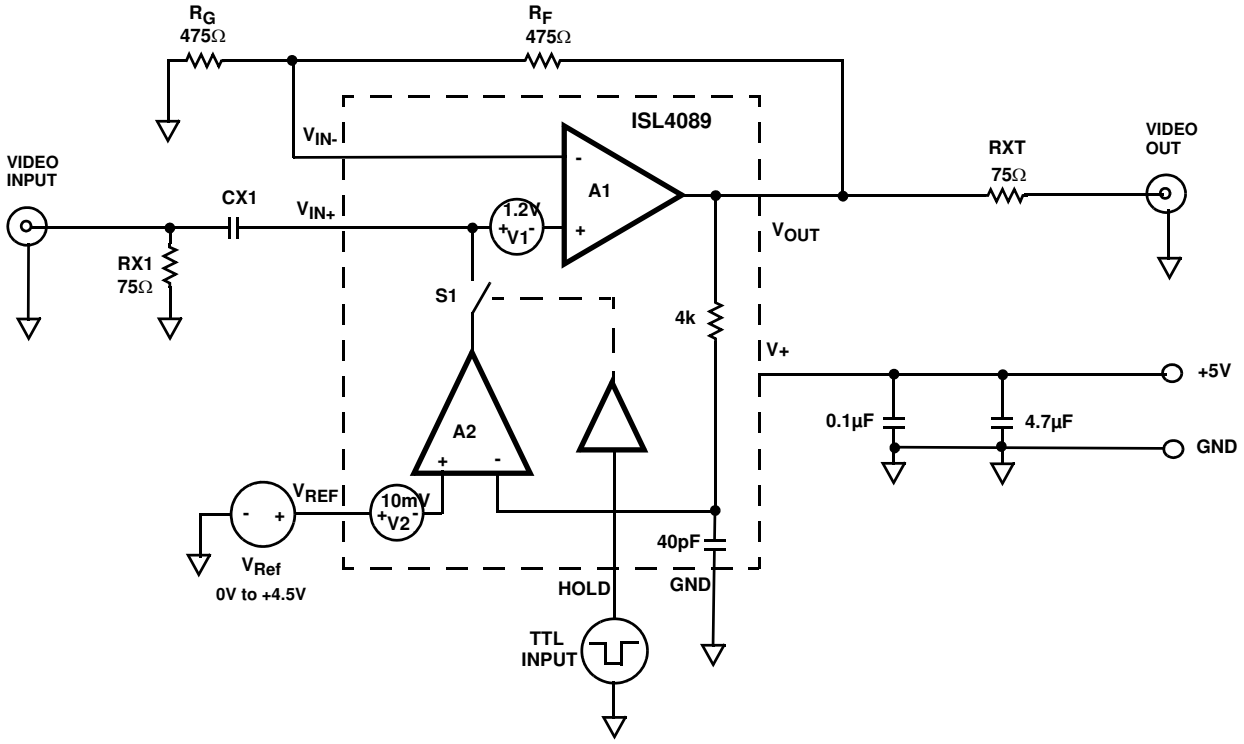


FIGURE 13. BASIC +5V APPLICATION CIRCUIT

Using the Reference Voltage Input (V_{REF})

Implementing DC-restore and amplifying composite video using a single +5V supply amplifier, requires attention to the performance of the amplifier over the minimum to maximum range of output voltage swing. The differential gain - phase plot in Figure 6 shows the amplifier accuracy operating from a single +5V supply, driving a 300mV_{P-P} and a 600mV_{P-P} signal into a 150Ω load. Over the output DC voltage range of 0.5V to 3.25V, differential gain and phase are less than 0.05% and 0.05° respectively and defines the optimum output voltage range of the ISL4089. Figure 6 also shows that as the signal level increases, a corresponding decrease in the output DC level (min/max voltage swing) can be expected. The V_{REF} input enables the output DC voltage level to be optimally programmed within the min/max voltage range, according to Equation 2. The values in Figure 6 take into account the additional amplifier overhead (300mV_{P-P} and 600mV_{P-P}) needed by the video signal. Although the AC performance degrades below ~0.5V, the ISL4089 maintains DC accuracy down to 10mV.

Limiting the Output Current

No output short circuit current limit exists on these parts. All applications need to limit the output current to less than 60mA. Adequate thermal heat sinking of the parts is also required.

Application Information

A typical single supply application circuit using the EL1883 sync separator to generate the DC-restore hold command, is shown in Figure 13. The ISL4089 is configured for a gain of 2, and 75Ω input and output terminations are used for cable driving; providing an end to end gain of 1. DC-restore is performed during sync tip using the composite sync output of the EL1883, which clamps the -300mV input sync tip level to 0VDC at the ISL4089 output (Figure 15 - lower trace). Clamping sync tip to 0VDC forces the black level, color burst and active video to the +300mV level at the 75Ω load in the terminal equipment, and to +600mV at the ISL4089 output pin. The +600mV DC offset is safely within the lower linear range of the ISL4089 output (Figure 6 - Differential Gain - Phase) and the 2V maximum video amplitude at the output is safely within the upper limit. In applications where the sync tip level can't be guaranteed, positioning the active video within the linear range can be accomplished using the back porch clamp output of the EL1883 and supplying +1V to the V_{REF} input. This has the effect of clamping the back porch to the +1V V_{REF} level at the output while enabling the negative sync tip level to pass through to the output.

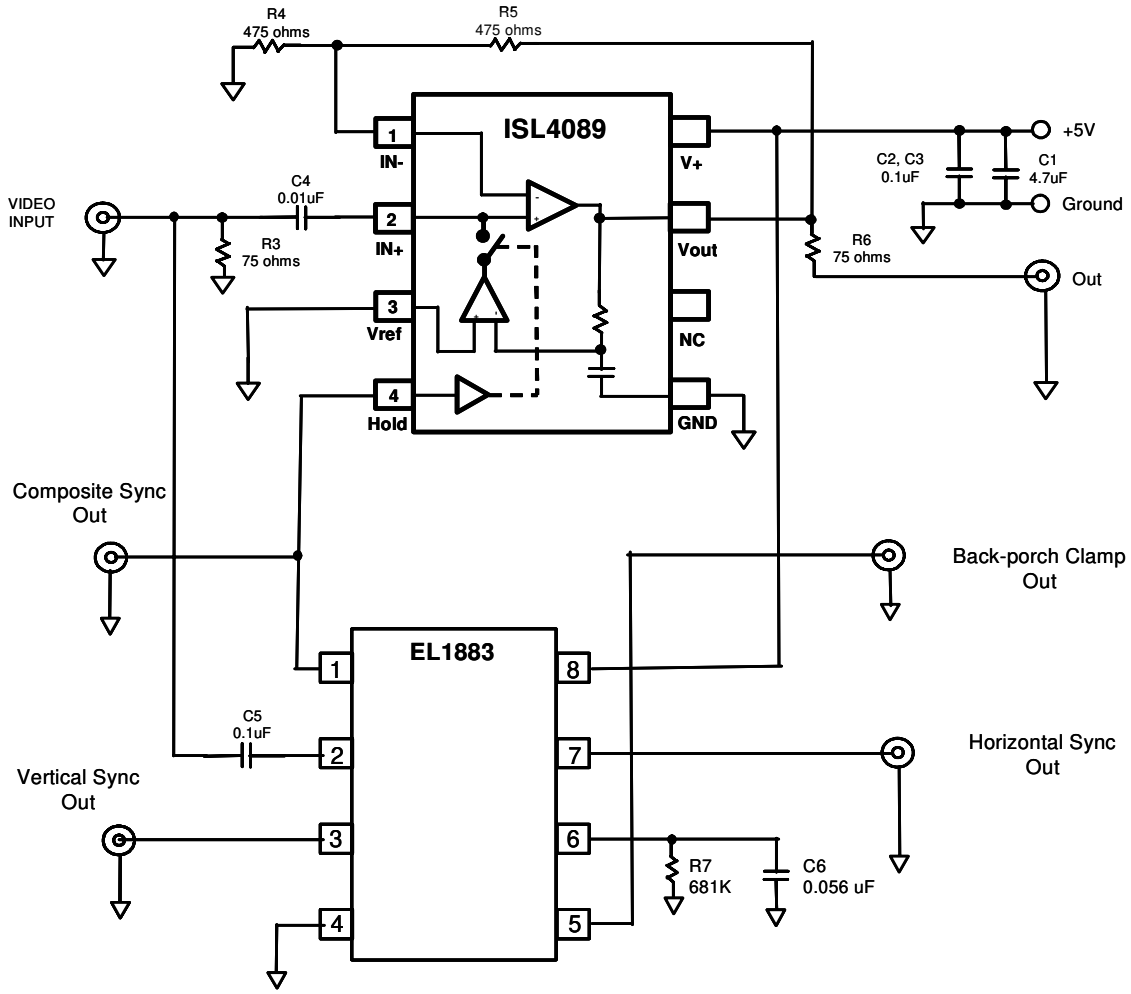
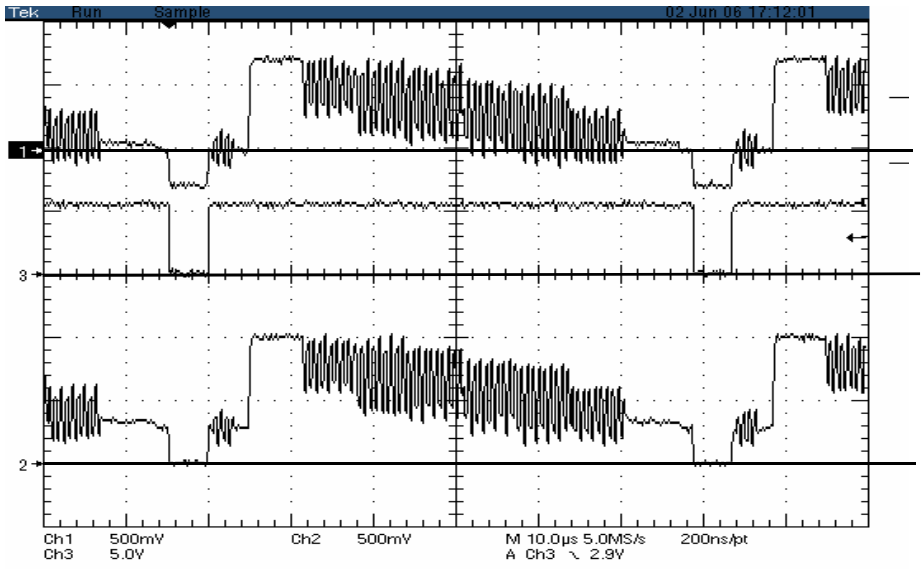


FIGURE 14. APPLICATION CIRCUIT USING THE EL1883 SYNC SEPARATOR TO GENERATE DC-RESTORE HOLD CONTROL



COMPOSITE VIDEO INPUT

0VDC

COMPOSITE SYNC INPUT

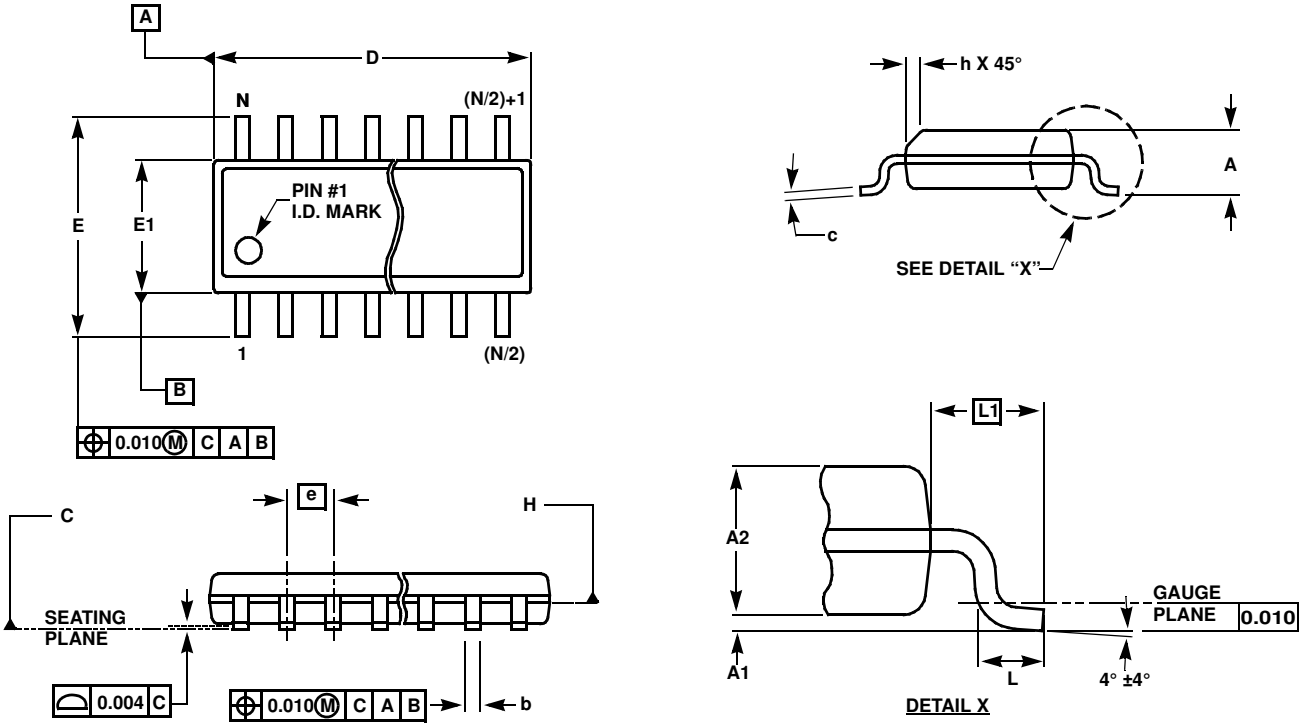
0VDC

DC-RESTORED VIDEO OUTPUT

0VDC

FIGURE 15. DC-RESTORE USING COMPOSITE SYNC AND V_{REF} = 0VDC

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

SYMBOL	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	TOLERANCE	NOTES
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. L 2/01

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality