



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



DDC Accelerator (DDCA)

The ISL54103 DDC Accelerator (DDCA) is a dual active pull-up bus terminator designed to improve data transmission speed on the DDC 2-wire serial bus interfaces.

The DDCA detects rising input transitions with two internal voltage references and two comparators per channel. After the voltage on a data line crosses the first threshold (V_{TRIPL}), the boost pull-up current source is activated to speed transition. After the voltage crosses the second threshold (V_{TRIPH}), the boost pull-up current source is de-activated, leaving an active pull-up current of 275 μ A on the line. When both channels are HIGH, the pull-up current for both lines is reduced to 100 μ A to save power. Internal logic ensures that the active and boost pull-up current sources are not activated during downward transitions.

The level for V_{TRIPH} is controlled by a bandgap voltage referred to V_{DD} . This feature makes the switching behavior invariant for all power supply voltages between 2.7V and 5.5V.

A noise filter on each channel prevents the circuit from responding to input transitions that do not exceed a voltage-time threshold. To activate the boost circuit, the input must exceed V_{TRIPL} by 100Vns (typical) (See Figure 10).

The DDCA permits operation of the bus at frequencies up to 100kHz, despite the capacitive loads of multiple devices and/or long PC board traces. Enhanced ESD protection on the accelerator pins are guaranteed to withstand 8kV ESD (HBM) events.

The DDC Accelerator provides an essential function in DDC applications because of distributed capacitance of the DDC wires in long video cables. By incorporating DDCA, systems using DDC can reliably increase their bus load, allowing longer cables, without the risk of data corruption.

Features

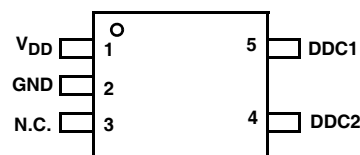
- Active Termination for DDC Lines
- Enhances System Bus Signal Rise Time
- More Reliable HDCP Performance In Video Multiplexers and Cable Extenders
- Increases Maximum Cable Length While Guaranteeing Data Integrity
- 2.2mA Current Boost on Low to High Transitions
- 8kV ESD Protection on SDA and SCL Pins
- Wide Operating Voltage Range: 2.7V to 5.5V
- Small Package - 5 Ld SOT-23
- Pb-free (RoHS Compliant)

Target Applications

- Video Multiplexers
- Video Cable Extenders
- Video Distribution Amplifiers
- Televisions
- Computer Monitors
- Projectors

Pinout

ISL54103
(5 LD SOT-23)
TOP VIEW



Pin Descriptions

SOT-23	SYMBOL	DESCRIPTION
1	V _{DD}	Supply Voltage
2	GND	Ground
3	N.C.	No Connect
4	DDC1	Active Pull-Up for DDC Signal
5	DDC2	Active Pull-Up for DDC Signal

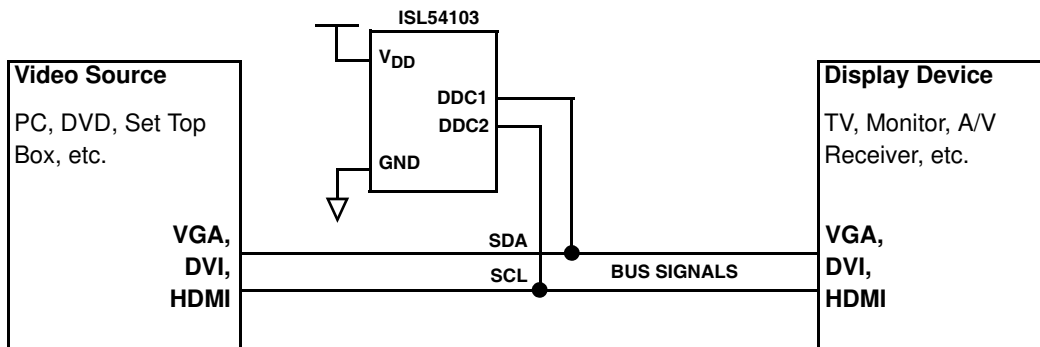
Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING (Note 4)	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL54103IHZ-T7	103Z	-40 to +85	5 Ld SOT-23	P5.064
ISL54103IHZ-T7A	103Z	-40 to +85	5 Ld SOT-23	P5.064

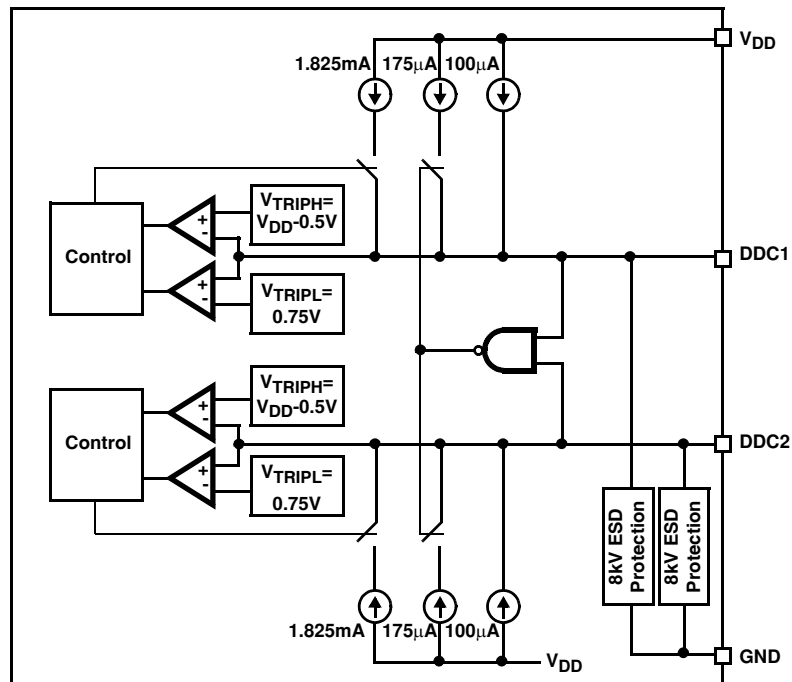
NOTES:

1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL54103](#). For more information on MSL please see techbrief [TB363](#).
4. The part marking is located on the bottom of the part.

System Diagram



IC Block Diagram



Absolute Maximum Ratings

Supply Voltage Range -1V to 6.5V
 Operating Junction Temperature +135°C
 Storage Temperature Range -65°C to +150°C
 Voltage on Pins -0.3V to $V_{DD}+0.3V$
 ESD Min Other Pins (HBM) >2kV
 ESD DDC1 and DDC2 Pins (HBM) >8kV

Thermal Information

Pb-Free Reflow Profile. see link below
<http://www.intersil.com/pbfree/Pb-FreeReflow.asp>

Recommended Operating Conditions

Temperature -40°C to +85°C
 Supply Voltage. 2.7V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Electrical Specifications Over all operating conditions unless otherwise specified, Typical values are measured at $V_{DD} = 3.3V$ and $T_A = +25^\circ C$

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
ANALOG PARAMETERS						
V_{DD}	Supply Voltage Range		2.7		5.5	V
$V_{DD\ RAMP}$	V_{DD} Ramp Rate		0.05		50	V/ms
I_{DD}	Supply Current	DDC1 = DDC2 = Open		80	100	μA
I_{OUT_SB}	Standby Pull-Up Current	DDC1 = DDC2 = $V_{DD} - 1.0V$		80	125	μA
I_{OUT_A1}	Active Pull-Up Current	DDC1 = GND; DDC2 = Open	125	275	350	μA
I_{OUT_A2}		DDC1 = Open; DDC2 = GND	125	275	350	μA
I_{OUT_B1}	Boost Pull-Up Current (Figure 2)	$V_{TRIPL} < DDC1 < V_{TRIPH}$, DDC2 = Open	1.6	2.2		mA
I_{OUT_B2}		$V_{TRIPL} < DDC2 < V_{TRIPH}$, DDC1 = Open	1.6	2.2		mA
V_{TRIPL}	Input Voltage Threshold Low		0.65	0.75	0.85	V
V_{TRIPH}	Input Voltage Threshold High		$V_{DD} - 0.60$	$V_{DD} - 0.50$	$V_{DD} - 0.40$	V
f_{MAX}	DDC Max Frequency				100	kHz
NSS	Noise Spike Suppression (Note 5) (Figure 10)			20		V-ns

NOTES:

5. Measured as area under triangular waveform above V_{TRIPL} , with time as base and V_{IN} as height (See Figure 10).
6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

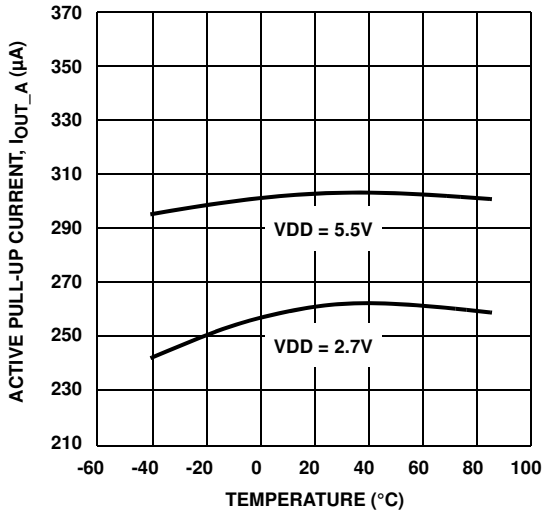


FIGURE 1. ACTIVE PULL-UP CURRENT, DDC PIN = 0V

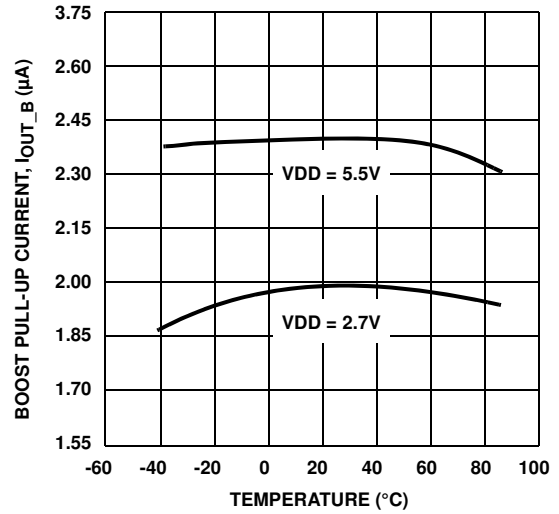


FIGURE 2. BOOST PULL-UP CURRENT, DDC PIN = VDD/2

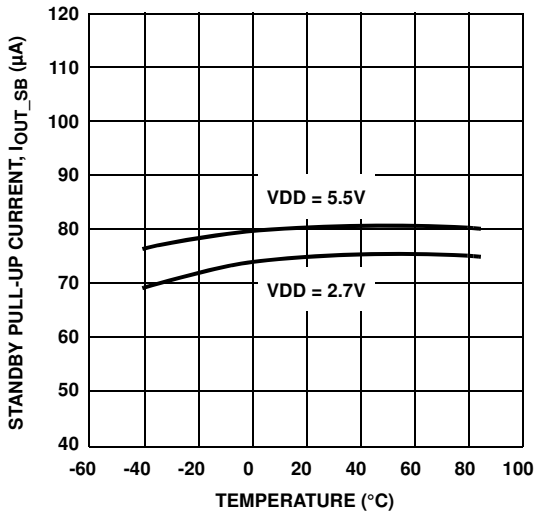


FIGURE 3. STANDBY PULL-UP CURRENT, DDC1, 2 = VDD - 0.5V

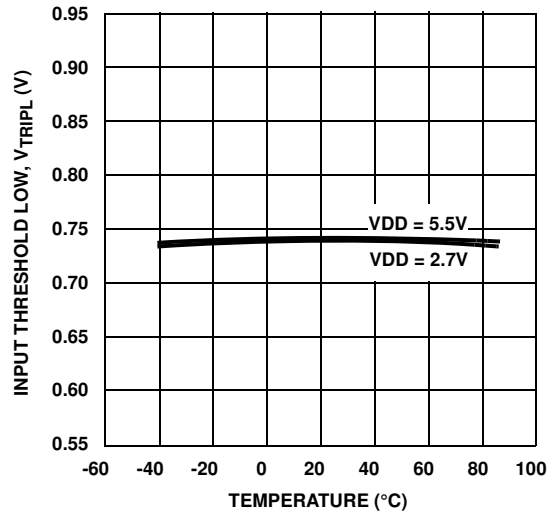


FIGURE 4. VTRIPL VOLTAGE

Typical Performance Curves (Continued)

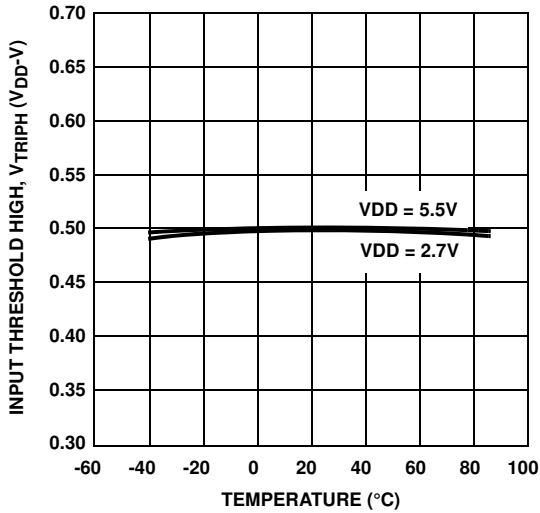
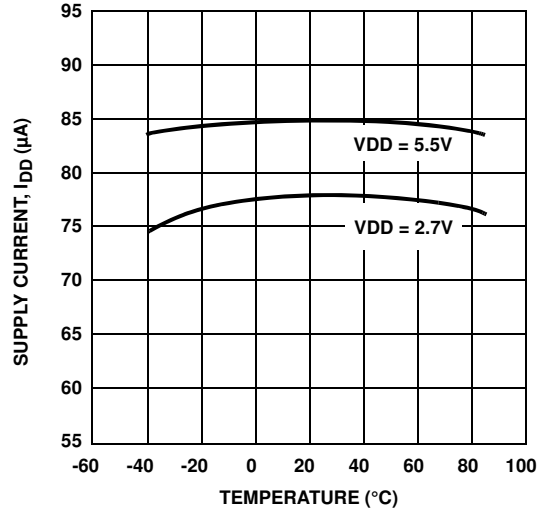
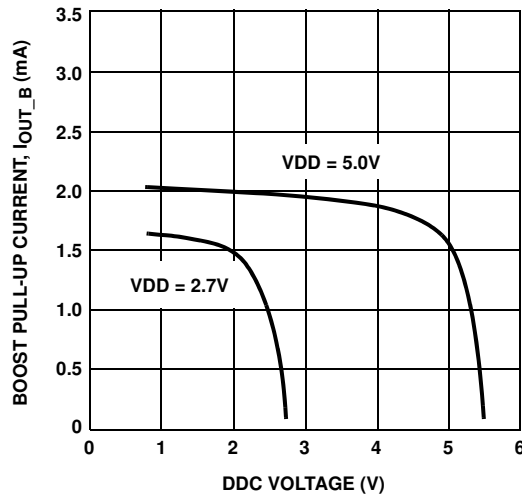
FIGURE 5. V_{TRIP_H} VOLTAGEFIGURE 6. I_{DD} CURRENT, DDC1 = DDC2 = OPEN

FIGURE 7. BOOST PULL-UP CURRENT vs DDC VOLTAGE

Functional Description

DDC Overview

DDC is a 2-wire serial communication standard based on the I²C standard. Devices communicate to each other using one clock (SCL) and one data (SDA) line. These are both bidirectional.

Each signal is connected to a positive supply voltage via a current-source or pull-up resistor (see “System Diagram” on page 3). When the bus is free, both lines are HIGH. The output stages of all devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function.

Simple pull-up resistors on the clock and data lines work well unless there are long signal lines. The combined

capacitance of long cables increases the rise time on the signal to such an extent that the communication becomes unreliable or fails to meet the bus timing specifications. Smaller value resistors can sometimes compensate for the extra capacitance, but this increases the current consumption when the signal lines are pulled LOW.

ISL54103 Operation

To improve the operation of the DDC where larger bus capacitance exists, the ISL54103 provides active pull-up using switched current sources. When the bus is idle and both lines are HIGH, a standby pull-up current of 100µA is used to maintain the signal level while minimizing power consumption. When either of the two signals is pulled LOW, an active pull-up current of 275µA maintains a good V_{OL} noise margin.

When the bus line is released, it is pulled high by the ISL54103 active current until the voltage exceeds the V_{TRIPH} level for a period of time. This voltage-time combination filters out noise on the signal line. Once the ISL54103 detects a valid rising edge, a 2.2mA boost current pulls the bus line high very quickly (see Figure 8). This boost current turns off when the input level reaches the V_{TRIPH} threshold and the pull-up current returns to the active level. If both inputs are HIGH, the pull-up current drops to the standby level of 100 μ A.

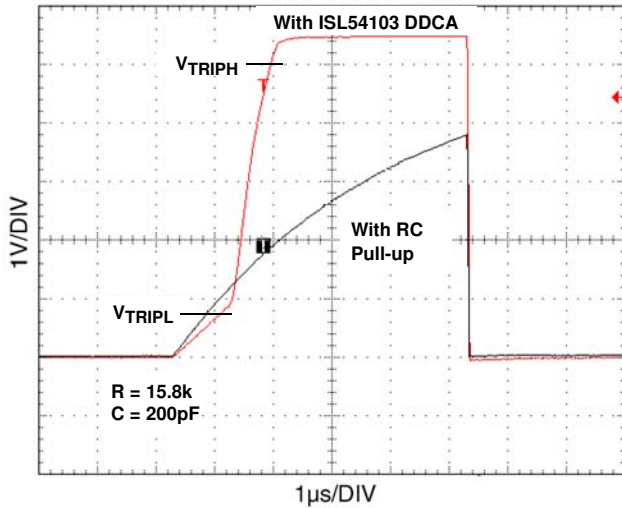


FIGURE 8. ISL54103 DDC SYSTEM BOOST PULL-UP COMPARED TO RESISTOR PULL-UP ($V_{DD} = 5.5V$)

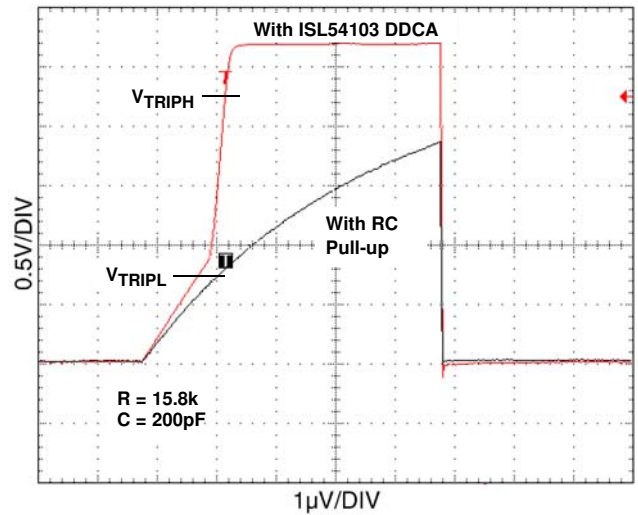


FIGURE 9. ISL54103 DDC SYSTEM BOOST PULL-UP COMPARED TO RESISTOR PULL-UP ($V_{DD} = 2.7V$)

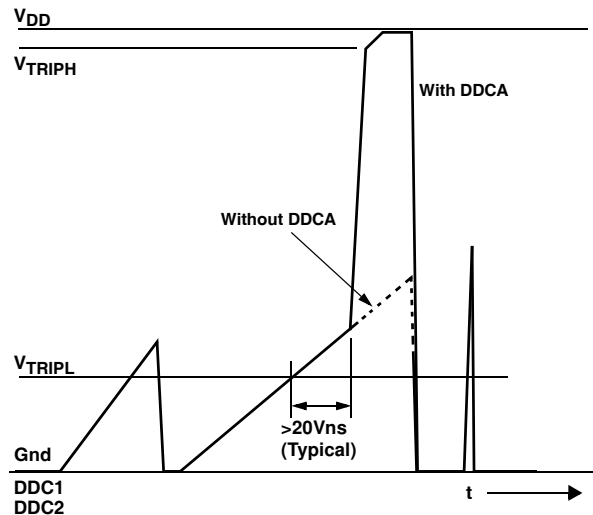


FIGURE 10. NOISE SUPPRESSION. BOOST CURRENT APPLIED WHEN INPUT SIGNAL EXCEEDS 20Vns (TYPICAL)

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

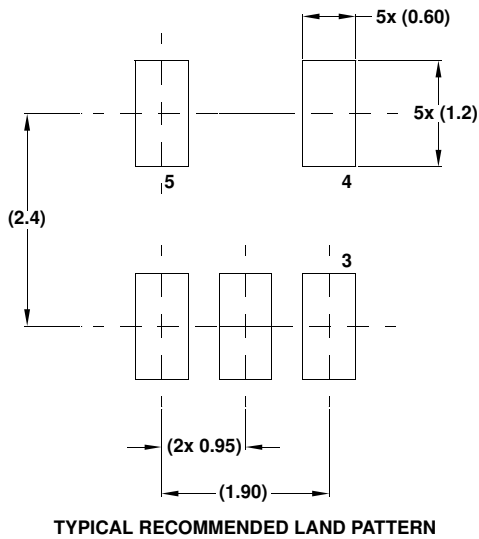
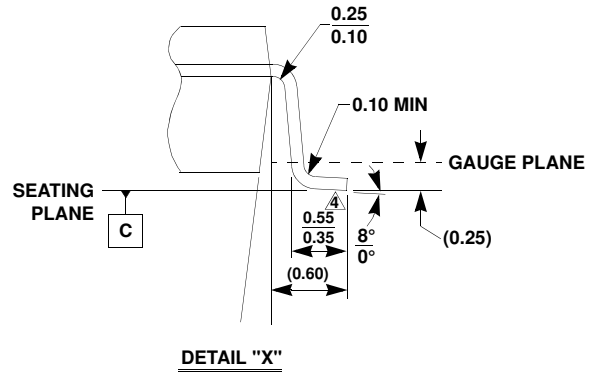
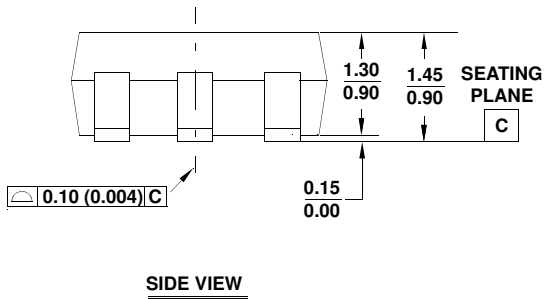
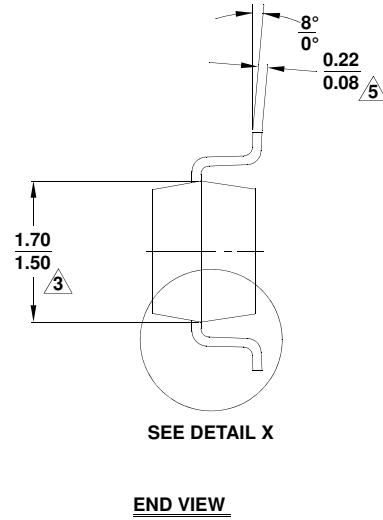
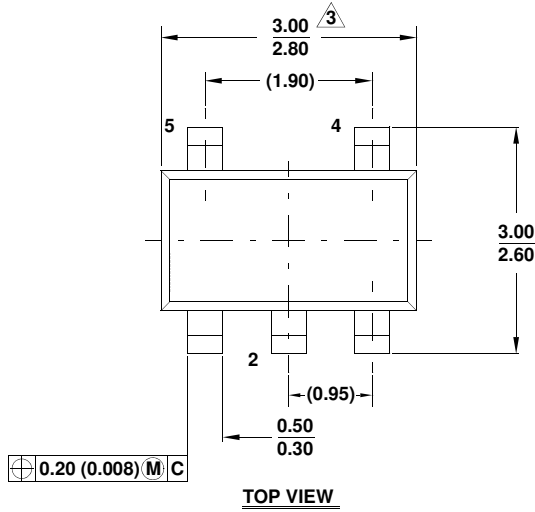
For information regarding Intersil Corporation and its products, see www.intersil.com

Package Outline Drawing

P5.064

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

Rev 3, 4/11



NOTES:

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 and JEDEC MO178AA.
3. Package length and width are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength measured at reference to gauge plane.
5. Lead thickness applies to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
6. Controlling dimension: MILLIMETER.
Dimensions in () for reference only.