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Triple 4:1 Single Supply Video Multiplexing Amplifier

The ISL59452 is a 4-input, single-supply, triple video multiplexer suited for component video applications. The device features single +5V supply operation, high bandwidth and TTL/CMOS logic compatible gain select (AV2) of x1 or x2. When HIZ is pulled high, the outputs are put into high-impedance states and the video inputs are disconnected putting the device in a low power state. This is an essential feature for power sensitive applications. The ISL59452 also features fast channel switching at pixel rates to allow for video overlays.

The ISL59452 will drive 150Ω loads making it suitable for 75Ω cable driving applications. The ISL59452 is ideal for RGB, YPbPr, as well as S-Video and composite applications.

The ISL59452 comes in a 32 Ld QFN package and is specified for operation over -40°C to +85°C temperature range.

Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL59452IRZ	ISL594 52IRZ	32 Ld 5x5 QFN	L32.5x5
ISL59452IRZ-T7*	ISL594 52IRZ	32 Ld 5x5 QFN	L32.5x5

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

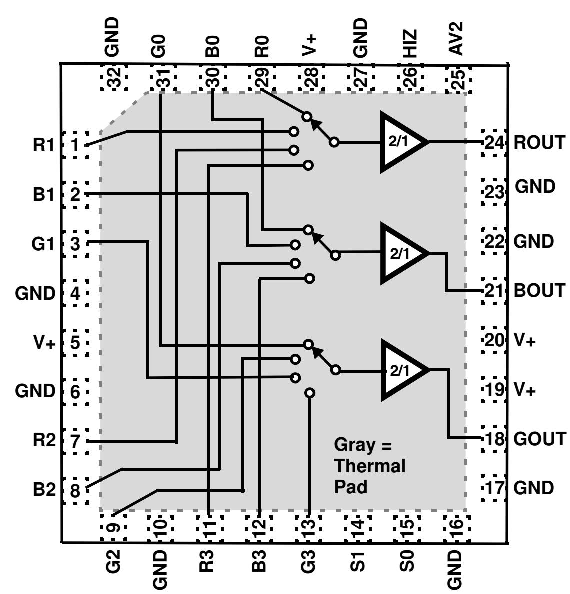
- 250MHz Small Signal Bandwidth (GAIN 1)
- Capable of Pixel Rate Channel Switching
- +5V Single Supply Operation
- TTL/CMOS Compatible Gain Select of x1 or x2
- High Impedance Output Setting
- Ideal for RGB/YPbPr/S-Video/Composite Video Signals
- 150Ω Output Load Capability for Video Cable Driving
- 0.0013% Differential Gain and 0.035° Differential Phase Accuracy
- Pb-Free (RoHS Compliant)

Applications

- SDTVs and HDTVs
- Set-Top Boxes
- Video Overlay
- Security Video
- Broadcast Video Equipment

Pinout

ISL59452
(32 LD QFN)
TOP VIEW



EXPOSED THERMAL PAD MUST BE CONNECTED TO GND.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V+ to GND) 5.5V
Input Voltage to GND . . . . GND - 0.5V to V+ + 0.5V
Voltage between HIZ, AV2 and GND . . . . GND -0.5;V+ +0.5V
Supply Turn-on Slew Rate 1V/µs
Digital and Analog Input Current (Note 1) 50mA
Output Current (Continuous) 50mA
ESD Rating
  Human Body Model (Per MIL-STD-883 Method 3015.7) 2500V
  Machine Model 300V

Thermal Information

Storage Temperature Range . . . . -65°C to +150°C
Ambient Operating Temperature . . . . -40°C to +85°C
Operating Junction Temperature . . . . -40°C to +125°C
Power Dissipation . . . . See Curves
Pb-free reflow profile . . . . .see link below
  http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.
2. Parts are 100% tested at +25°C. Over temperature limits established by characterization and are not production tested.

Electrical Specifications

V+ = +5V, GND = 0V, T_A = +25°C, R_L = 150Ω to GND, AV2 = HIZ = 0.8V, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
DC CHARACTERISTICS						
V+	Supply Voltage		4.5	5.0	5.5	V
$+I_S$ Enabled	Enabled Supply Current	No load, V_{IN} = 0V, HIZ = 0.8V		45	75	mA
$+I_S$ Disabled	Disabled Supply Current	No load, V_{IN} = 0V, HIZ = 2.0V		3	5	mA
V_{OS}	Output Offset Voltage	AV2 = 0.8V, GAIN = 1, V_{IN} = 0.1V	-35	0	35	mV
		AV2 = 2.0V, GAIN = 2, V_{IN} = 0.1V	-35	0	35	mV
I_B	Input Bias Current	V_{IN} = 2.2V, No Load	-6	-4	-2	µA
$R_{OUT-DIS}$	Disabled Output Resistance (DC)	HIZ = 2.0V	1.5	2	2.5	kΩ
A_V	Voltage Gain	AV2 = 0.8V, GAIN = 1	.98	1	1.02	V/V
		AV2 = 2.0V, GAIN = 2	1.95	1.99	2.05	V/V
$PSRR_{DC}$	Power Supply Rejection Ratio	V+ = 4.5V to 5.5V	50	55		dB
OUTPUT AMPLIFIERS						
V_{OUT+}	Output High Swing	R_L = 150Ω, V_{IN} = 4V, AV2 = 2.0V, GAIN = 2	3.5			V
V_{OUT-}	Output Low Swing	R_L = 150Ω,V_{IN} = 0V, AV2 = 2.0V, GAIN = 2			30	mV
I_{SC}	Short Circuit Current	Sourcing, V_{IN} = 3V, AV2 = 2.0V, R_L = 10Ω to GND, GAIN = 2		125		mA
		Sinking, V_{IN} = 0V, R_L = 10Ω to +3V		57		mA
LOGIC (AV2, HIZ, S1, S0)						
V_{IH}	Input High Voltage (HIGH)		2			V
V_{IL}	Input Low Voltage (LOW)				0.8	V
I_{IH}	Input High Current (Logic Inputs)	S1 = S0 = 5V (no pull-up or pull-down)	-2	0	2	µA
		AV2 = HIZ= 5V (300kΩ internal pull-downs)	8	17	34	µA
I_{IL}	Input Low Current (Logic Inputs)	S1 = S0 = 0V (no pull-up or pull-down)	-2	0	2	µA
		AV2 = HIZ = 5V (300kΩ internal pull-downs)	-2	0	2	µA
AC GENERAL						
PSRR	Power Supply Rejection Ratio	V_{IN} = 0V, f = 10kHz to 10MHz, V+ = $5V_{DC}$ +100mV_{P-P} sine wave		55		dB
X_{TALK}	Channel to Channel Crosstalk (ROUT/BOUT to Green Input)	f = 10MHz, V_{IN} = 0.7V_{P-P}; (GAIN = 1)		75		dB
		f = 10MHz, V_{IN} = 0.7V_{P-P}; (GAIN = 2)		70		dB

Electrical Specifications

$V+ = +5V$, $GND = 0V$, $T_A = +25°C$, $R_L = 150\Omega$ to GND, AV2 = HIZ = 0.8V, unless otherwise specified. **(Continued)**

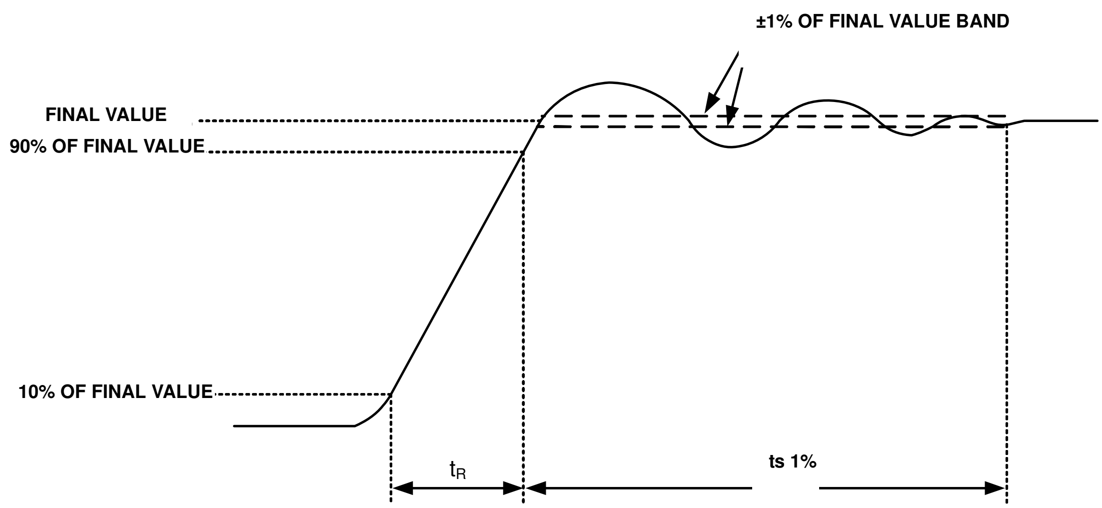
PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
Off - ISO	Off-State Isolation (any de-selected output to driven input)	f = 10MHz, Ch-Ch Off Isolation $V_{IN} = 0.7V_{P-P}$; (GAIN = 1)		90		dB
		f = 10MHz, Ch-Ch Off Isolation $V_{IN} = 0.7V_{P-P}$; (GAIN = 2)		90		dB
dG	Differential Gain Error	$R_L = 150$		0.0013		%
dP	Differential Phase Error	$R_L = 150$		0.035		°
BW	Small Signal -3dB Bandwidth	$V_{OUT} = 0.1V_{P-P}$; $R_L = 150\Omega$, $C_L = 0.6pF$ (GAIN = 1)		250		MHz
		$V_{OUT} = 0.2V_{P-P}$; $R_L = 150\Omega$, $C_L = 0.6pF$ (GAIN = 2)		210		MHz
	Large Signal -3dB Bandwidth	$V_{OUT} = 0.7V_{P-P}$; $R_L = 150\Omega$, $C_L = 0.6pF$ (GAIN = 1)		240		MHz
		$V_{OUT} = 1.4V_{P-P}$; $R_L = 150\Omega$, $C_L = 0.6pF$ (GAIN = 2)		200		MHz
BW_0.1	0.1dB Bandwidth	$V_{OUT} = 1.4V_{P-P}$; $R_L = 150\Omega$, $C_L = 0.6pF$ (GAIN = 1)		40		MHz
		$V_{OUT} = 1.4V_{P-P}$; $R_L = 150\Omega$, $C_L = 0.6pF$ (GAIN = 2)		33		MHz
SR+	Positive Slew Rate	V_{IN} = 0.5V to 2.5V, time = 20% to 80%, $R_L = 150\Omega$, AV2 = 0.8V, $C_L = 2.1pF$, GAIN = 1		480		V/µs
		V_{IN} = 0.5V to 1.5V, time = 20% to 80%, $R_L = 150\Omega$, AV2 = 2.0V, $C_L = 2.1pF$, GAIN = 2		980		V/µs
SR-	Negative Slew Rate	V_{IN} = 2.5V to 0.5V, time = 80% to 20%, $R_L = 150\Omega$, AV2 = 0.8V, $C_L = 2.1pF$, GAIN = 1		300		V/µs
		V_{IN} = 1.5V to 0.5V, time = 80% to 20%, $R_L = 150\Omega$, AV2 = 2.0V, $C_L = 2.1pF$, GAIN = 2		568		V/µs
TRANSIENT RESPONSE						
t_R	Rise Time 10% to 90%	$V_{OUT} = 1V_{P-P}$; $R_L = 150\Omega$, $C_L = 2.1pF$, AV2 = 0.8V, GAIN = 1		1.72		ns
		$V_{OUT} = 1V_{P-P}$; $R_L = 150\Omega$, $C_L = 2.1pF$, AV2 = 2.0V, GAIN = 2		1		ns
		$V_{OUT} = 2V_{P-P}$; $R_L = 150\Omega$, $C_L = 2.1pF$, AV2 = 2.0V, GAIN = 2		1.88		ns
t_F	Fall Time 90% to 10%	$V_{OUT} = 1V_{P-P}$; $R_L = 150\Omega$, $C_L = 2.1pF$, AV2 = 0.8V, GAIN = 1		2.7		ns
		$V_{OUT} = 1V_{P-P}$; $R_L = 150\Omega$, $C_L = 2.1pF$, AV2 = 2.0V, GAIN = 2		2.2		
		$V_{OUT} = 2V_{P-P}$; $R_L = 150\Omega$, $C_L = 2.1pF$, AV2 = 2.0V, GAIN = 2		2.7		ns
$t_{S\ 1\%}$	Settling Time to 1%	$V_{OUT} = 1V_{P-P}$; $R_L = 150\Omega$, $C_L = 2.1pF$, GAIN = 1, time from 90% crossing to 1% of final value		3		ns
		$V_{OUT} = 1V_{P-P}$; $R_L = 150\Omega$, $C_L = 2.1pF$, GAIN = 2, time from 90% crossing to 1% of final value		5		ns
SWITCHING CHARACTERISTICS						
V_{GLITCH}	HIZ High to Low Switching Glitch	$V_{IN} = 1V$, $R_L = 150\Omega$; $C_L = 2.1pF$, AV2 = 0.8V		400		mV_{P-P}
		$V_{IN} = 1V$, $R_L = 150\Omega$; $C_L = 2.1pF$, AV2 = 2.0V		300		mV_{P-P}

Electrical Specifications

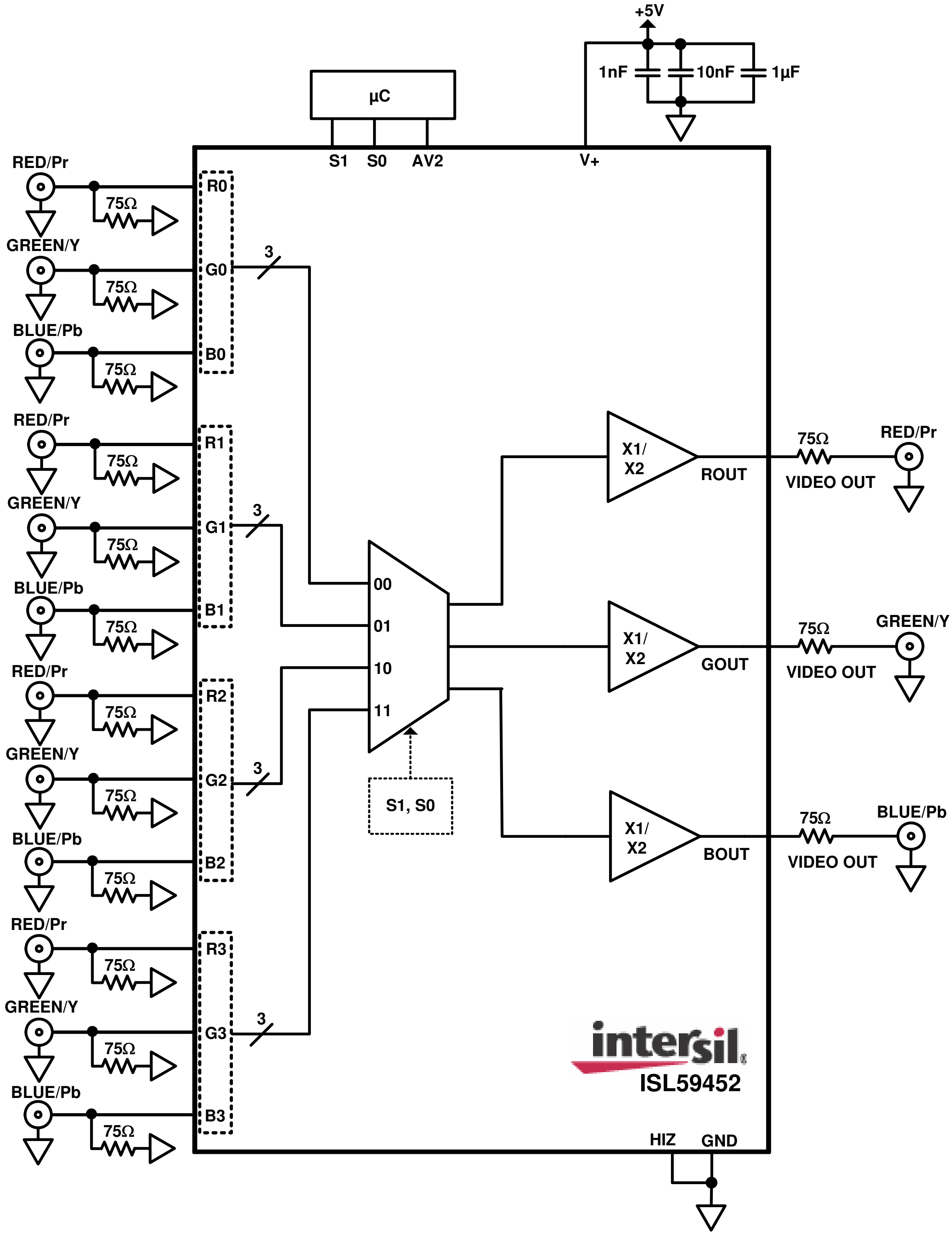
V+ = +5V, GND = 0V, T_A = +25°C, R_L = 150Ω to GND, AV2 = HIZ = 0.8V, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
t_{SW-L-H}	Channel Switching Delay Time Low to High	1.2V logic threshold to 10% movement of analog output		3		ns
t_{SW-H-L}	Channel Switching Delay Time High to Low	1.2V logic threshold to 10% movement of analog output		5		ns
$t_{HIZ-L-H}$	HIZ Switching Delay Time Low to High	1.2V logic threshold to 10% movement of analog output		30		ns
$t_{HIZ-H-L}$	HIZ Switching Delay Time High to Low	1.2V logic threshold to 10% movement of analog output		220		ns
tpd	Propagation Delay	10% input to 10% output, V_{IN} = 100mV_{P-P}		5		ns
		10% input to 10% output, V_{IN} = 700mV_{P-P}		2		ns

Settling Time Diagram



Typical Application Diagram



Typical Performance Curves

$V+ = +5V$, $R_L = 150\Omega$ to GND, $C_L = 0.6pF$, $T_A = +25°C$, unless otherwise specified.

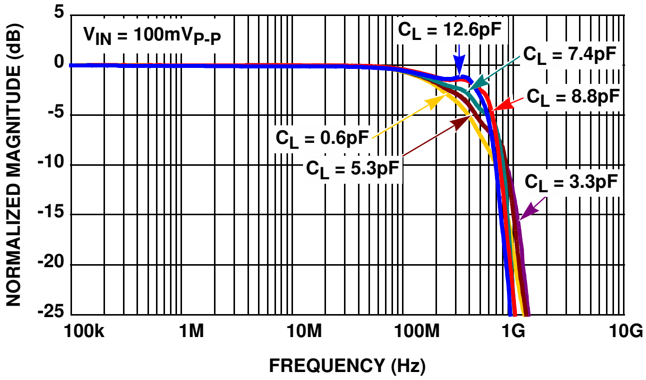


FIGURE 1. SMALL SIGNAL GAIN vs FREQUENCY vs C_L INTO 150Ω LOAD, GAIN = 1

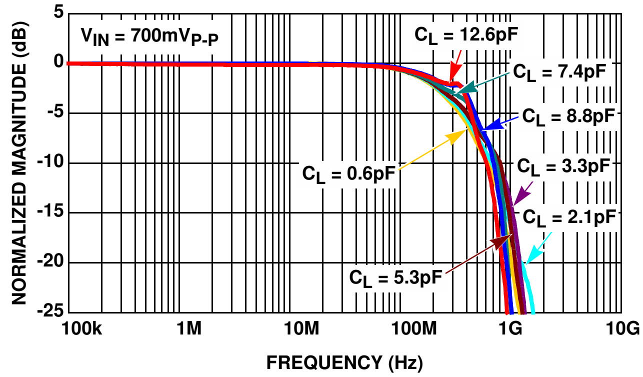


FIGURE 2. LARGE SIGNAL GAIN vs FREQUENCY vs C_L INTO 150Ω LOAD, GAIN = 1

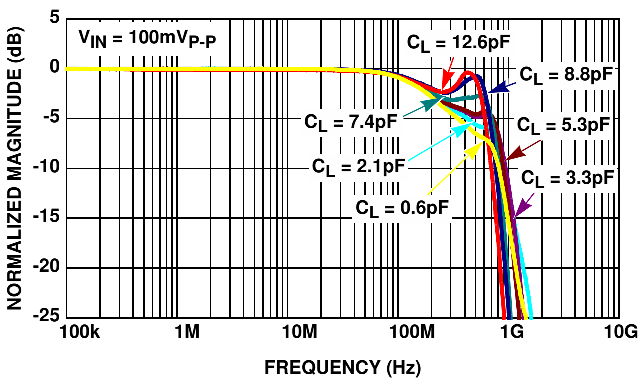


FIGURE 3. SMALL SIGNAL GAIN vs FREQUENCY vs C_L INTO 150Ω LOAD, GAIN = 2

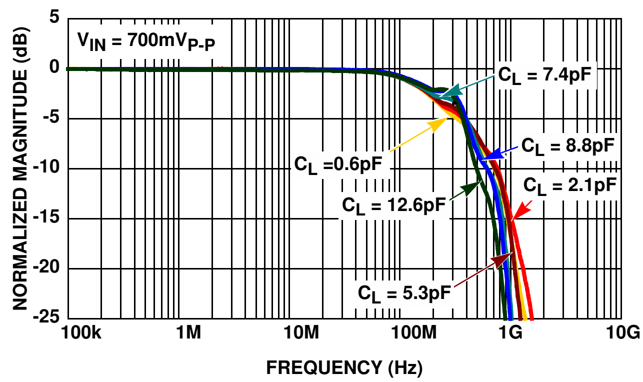


FIGURE 4. LARGE SIGNAL GAIN vs FREQUENCY vs C_L INTO 150Ω LOAD, GAIN = 2

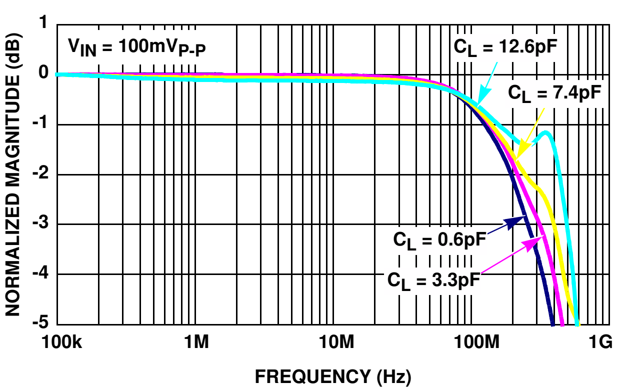


FIGURE 5. SMALL SIGNAL GAIN FLATNESS, GAIN = 1

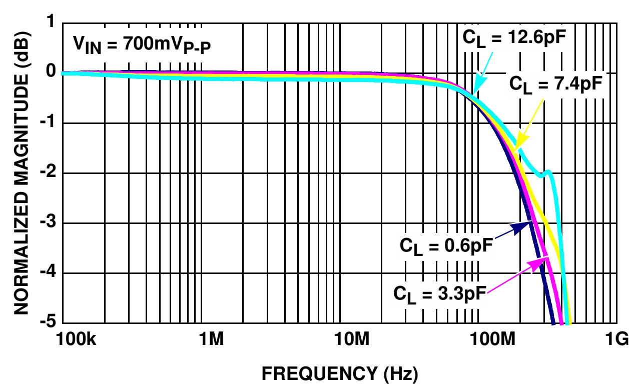


FIGURE 6. LARGE SIGNAL GAIN FLATNESS, GAIN = 1

Typical Performance Curves
V+ = +5V, R_L = 150Ω to GND, C_L = 0.6pF, T_A = +25°C, unless otherwise specified. **(Continued)**

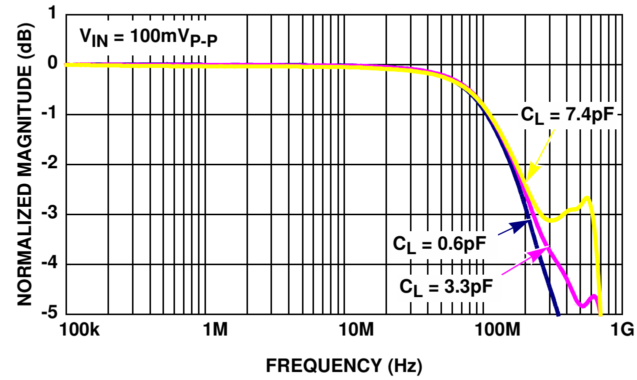


FIGURE 7. SMALL SIGNAL GAIN FLATNESS, GAIN = 2

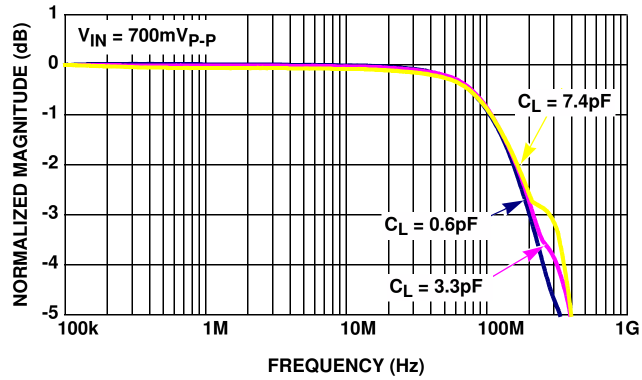


FIGURE 8. LARGE SIGNAL GAIN FLATNESS, GAIN = 2

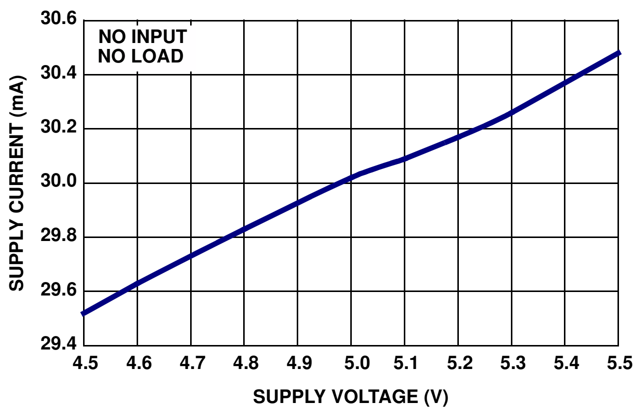


FIGURE 9. SUPPLY CURRENT vs SUPPLY VOLTAGE

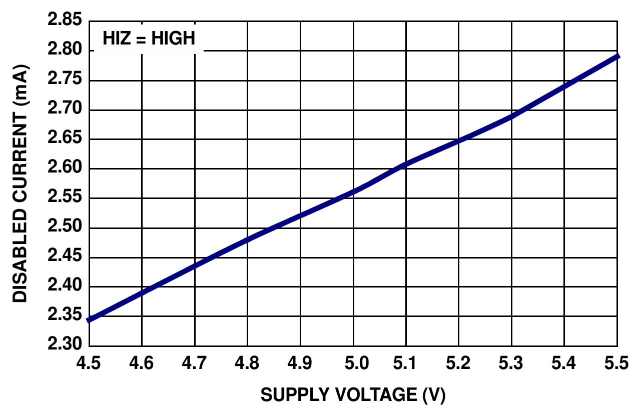


FIGURE 10. DISABLED SUPPLY CURRENT vs SUPPLY VOLTAGE

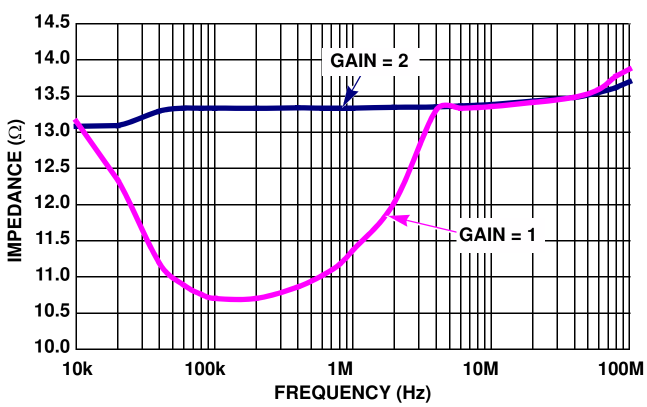


FIGURE 11. Z_{OUT} vs FREQUENCY - ENABLED

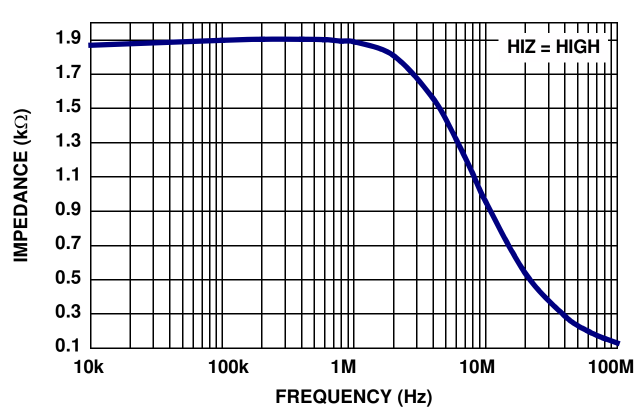


FIGURE 12. Z_{OUT} vs FREQUENCY - DISABLED

Typical Performance Curves
V+ = +5V, R_L = 150Ω to GND, C_L = 0.6pF, T_A = +25°C, unless otherwise specified. **(Continued)**

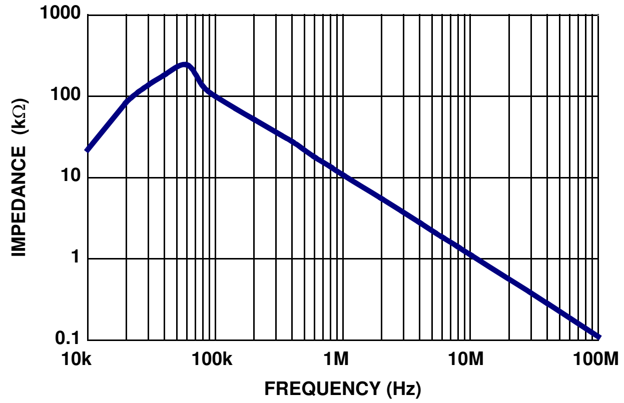


FIGURE 13. Z_{IN} vs FREQUENCY

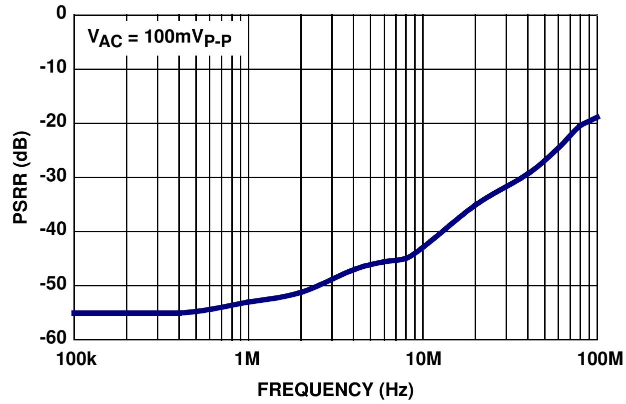


FIGURE 14. PSRR vs FREQUENCY

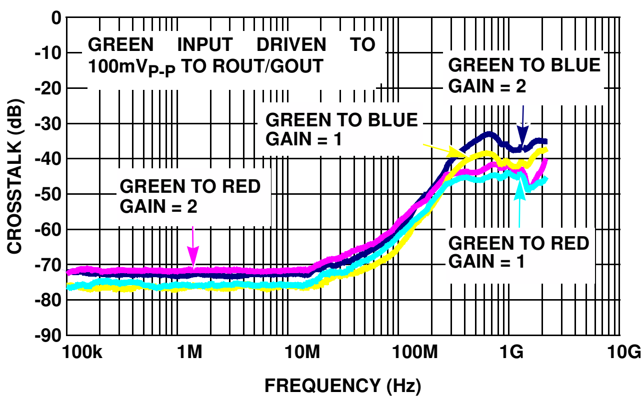


FIGURE 15. CROSSTALK

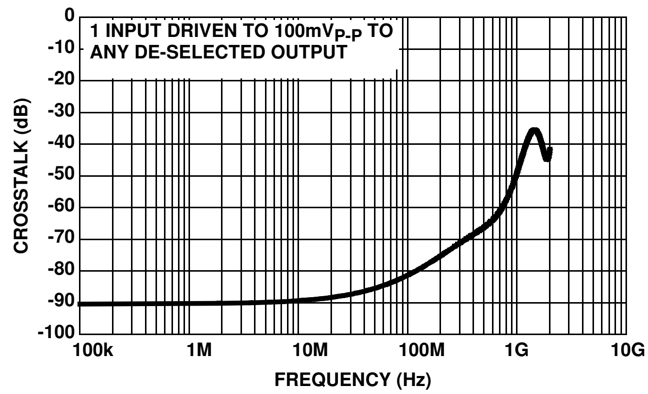


FIGURE 16. OFF ISOLATION

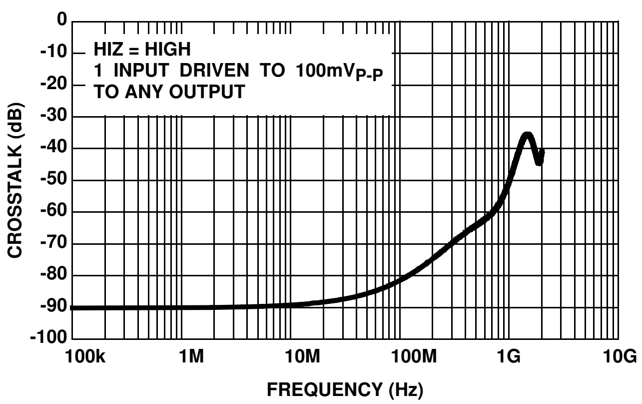


FIGURE 17. DISABLED ISOLATION

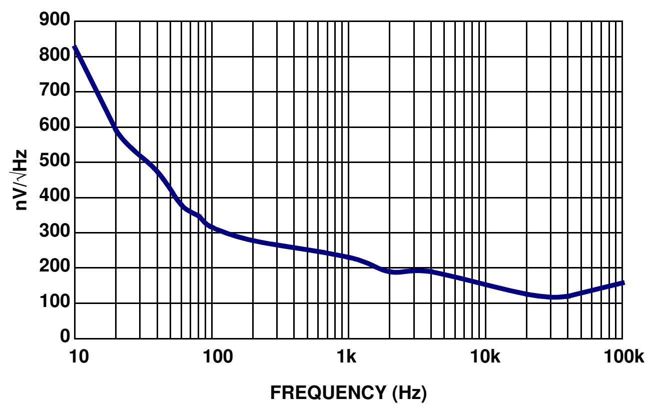


FIGURE 18. OUTPUT REFERRED NOISE vs FREQUENCY

Typical Performance Curves
$V+ = +5V$, $R_L = 150\Omega$ to GND, $C_L = 0.6pF$, $T_A = +25°C$, unless otherwise specified. **(Continued)**

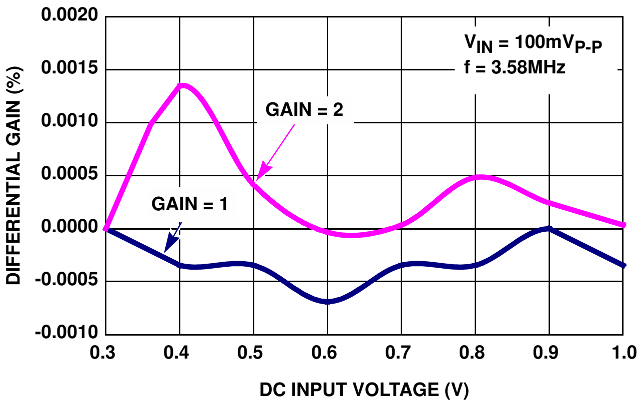


FIGURE 19. DIFFERENTIAL GAIN; $f_O = 3.58MHz$, $R_L = 150\Omega$

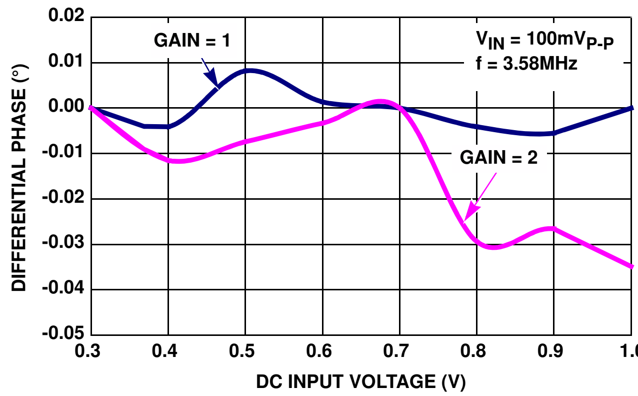


FIGURE 20. DIFFERENTIAL PHASE; $f_O = 3.58MHz$, $R_L = 150\Omega$

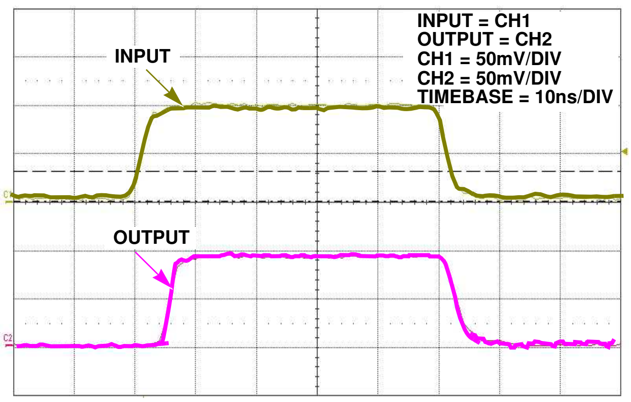


FIGURE 21. SMALL SIGNAL TRANSIENT RESPONSE; GAIN = 1

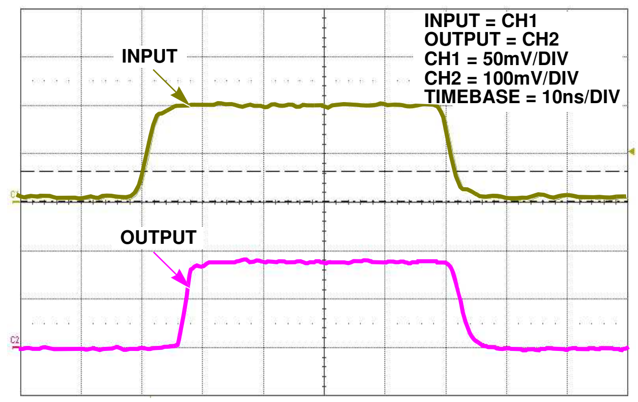


FIGURE 22. SMALL SIGNAL TRANSIENT RESPONSE; GAIN = 2

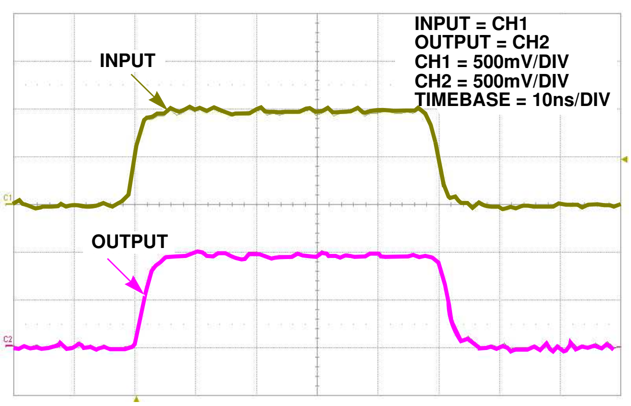


FIGURE 23. LARGE SIGNAL TRANSIENT RESPONSE; GAIN = 1

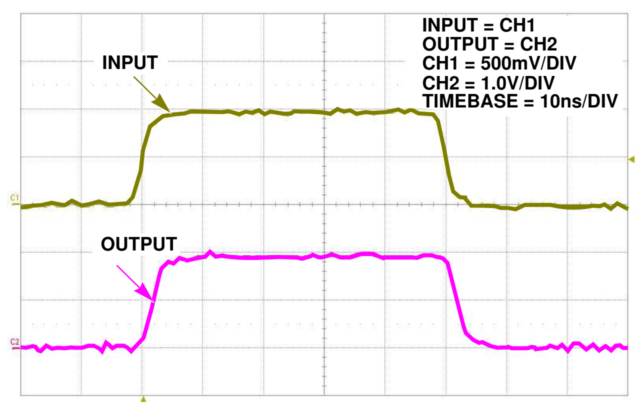


FIGURE 24. LARGE SIGNAL TRANSIENT RESPONSE; GAIN = 2

Typical Performance Curves
V+ = +5V, R_L = 150Ω to GND, C_L = 0.6pF, T_A = +25°C, unless otherwise specified. **(Continued)**

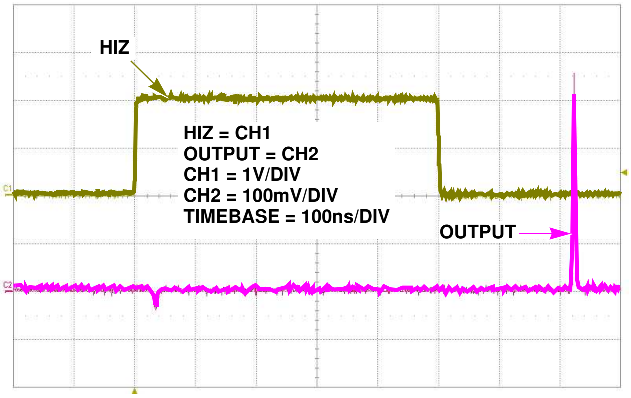


FIGURE 25. HIZ SWITCHING GLITCH, V_{IN} = 0, GAIN = 1

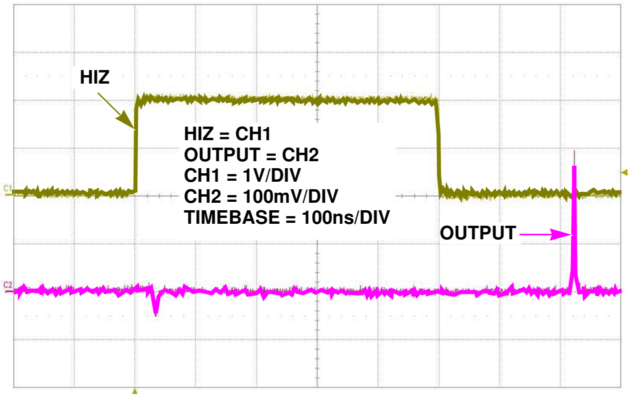


FIGURE 26. HIZ SWITCHING GLITCH, V_{IN} = 0, GAIN = 2

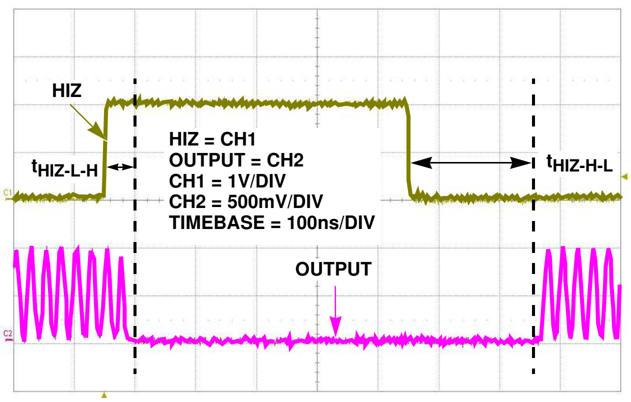


FIGURE 27. HIZ TIMING, GAIN = 1

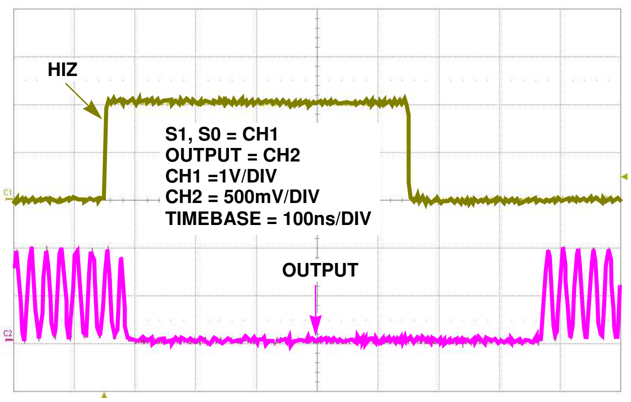


FIGURE 28. HIZ TIMING, GAIN = 2

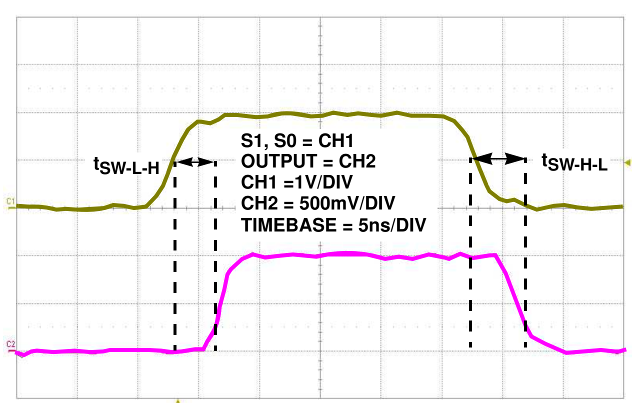


FIGURE 29. CHANNEL TO CHANNEL SWITCHING TIME

Typical Performance Curves
V+ = +5V, R_L = 150Ω to GND, C_L = 0.6pF, T_A = +25°C, unless otherwise specified. **(Continued)**

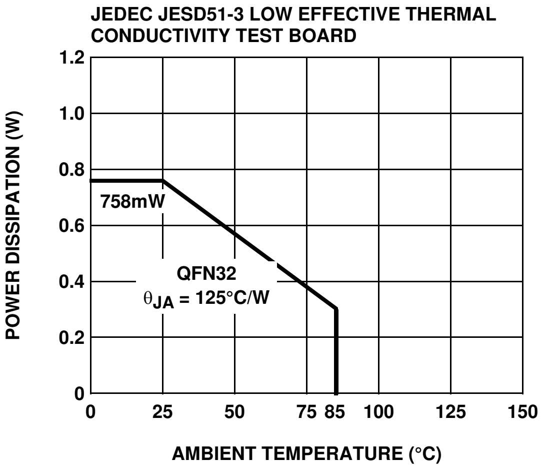


FIGURE 30. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

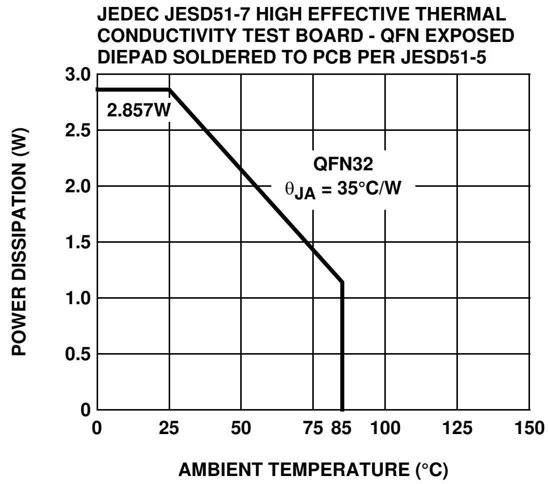


FIGURE 31. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Functional Block Diagram (Each Output Channel)

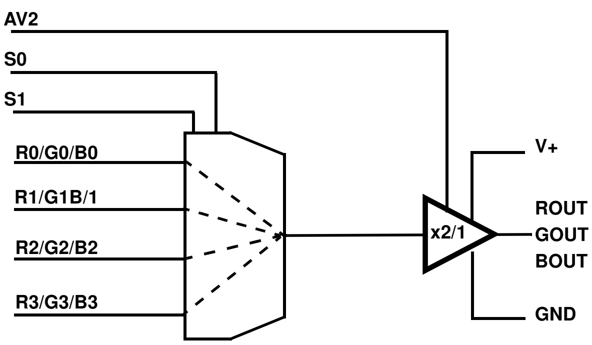
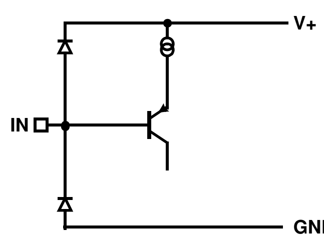


TABLE 1. CHANNEL SELECT LOGIC TABLE

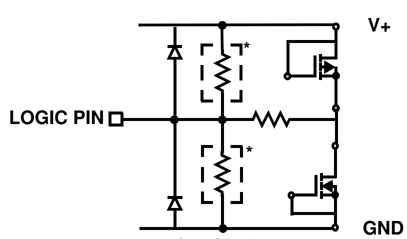
S1	S0	HIZ	OUTPUT
0	0	0	R0, G0, B0
0	1	0	R1, G1, B1
1	0	0	R2, G2, B2
1	1	0	R3, G3, B3
X	X	1	High Impedance, Inputs Disconnected

Pin Descriptions

ISL59452 (32 LD QFN)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	R1	Circuit 1	Channel 1 Red/Pr/Chroma Input
2	B1	Circuit 1	Channel 1 Blue/Pb/Chroma Input
3	G1	Circuit 1	Channel 1 Green/Luma Input
4, 6, 10, 16, 17, 22, 23, 27, 32	GND	Circuit 4	Ground
5, 19, 20, 28	V+	Circuit 4	Positive Supply. Bypass to GND with 0.01µF and 1nF capacitors.
7	R2	Circuit 1	Channel 2 Red/Pr/Chroma Input
8	B2	Circuit 1	Channel 2 Blue/Pb/Chroma Input
9	G2	Circuit 1	Channel 2 Green/Luma Input
11	R3	Circuit 1	Channel 3 Red/Pr/Chroma Input
12	B3	Circuit 1	Channel 3 Blue/Pb/Chroma Input
13	G3	Circuit 1	Channel 3 Green/Luma Input
14	S1	Circuit 2	Channel selection pin MSB (binary logic code). This pin does not have internal pull-up or pull-down resistors
15	S0	Circuit 2	Channel selection pin LSB (binary logic code). This pin does not have internal pull-up or pull-down resistors
18	GOUT	Circuit 3	Green/Luma Output
21	BOUT	Circuit 3	Blue/Pb/Chroma Output
24	ROUT	Circuit 3	Red/Pr/Chroma Output
25	AV2	Circuit 2	Gain Set. Set to logic high for gain of x2 (+6dB), or set to logic low for a gain of x1 (0dB). If left floating, an internal pull-down resitor pulls this pin low (300k pull-down).
26	HIZ	Circuit 2	Output disable (active high). Internal pull-down resistor ensures the device will be active with no connection to this pin. A logic high, puts the outputs in a high impedance state. Use this state to control logic when more than one MUX-amp share the same video output line. During high impedance state, there is a 2kΩ pull-down present at each output. If left floating, an internal pull-down resistor pulls this pin low (300k pull-down).
29	R0	Circuit 1	Channel 0 Red/Pr/Chroma Input
30	B0	Circuit 1	Channel 0 Blue/Pb/Chroma Input
31	G0	Circuit 1	Channel 0 Green/Luma Input
PAD	EP		Exposed Pad. Connect to GND

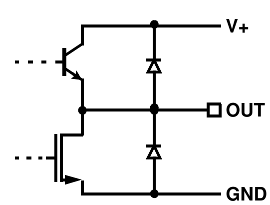


CIRCUIT 1

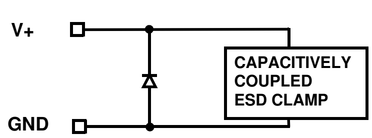


CIRCUIT 2

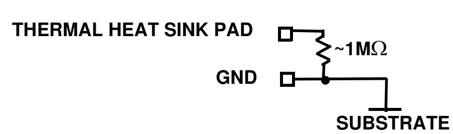
*NOT ALWAYS PRESENT.
REFER TO PIN DESCRIPTION



CIRCUIT 3



CIRCUIT 4



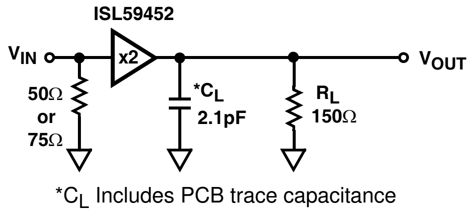


FIGURE 32A. TEST CIRCUIT WITH OPTIMAL OUTPUT LOAD

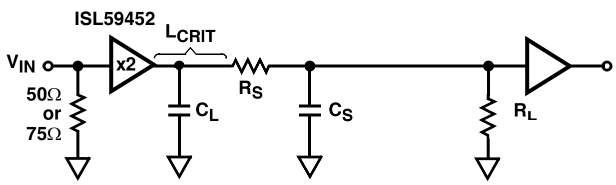


FIGURE 32B. INTER-STAGE APPLICATION CIRCUIT

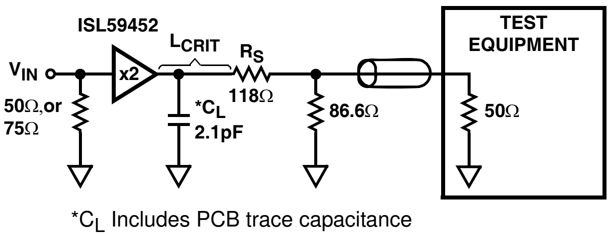


FIGURE 32C. 150Ω TEST CIRCUIT WITH 50Ω LOAD

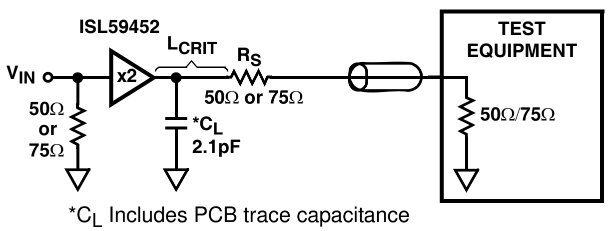


FIGURE 32D. BACKLOADED TEST CIRCUIT FOR 150Ω VIDEO CABLE APPLICATION

FIGURE 32. AC TEST CIRCUITS

AC Test Circuits

Figure 32A and 32B illustrate the optimum output load for testing AC performance at 150Ω loads. Figure 32C illustrates how to use the optimal 150Ω load for a 50Ω cable. Figure 32D illustrates the optimum output load for 50Ω and 75Ω cable-driving.

Application Information

General

The ISL59452 triple 4:1 video MUX features +5V single-supply operation, high bandwidth and TTL/CMOS logic compatible gain select (AV2) of x1 (0dB) or x2 (+6dB). The ISL59452 also features buffered high impedance analog inputs and excellent AC performance at output loads down to 150Ω for video cable-driving. The current feedback output amplifiers are stable operating into capacitive loads.

AC Design Considerations

High speed current-feed amplifiers are sensitive to capacitance at the inverting input and output terminals. Capacitance at the output terminal increases gain peaking and overshoot. The AC response of the ISL59452 is optimized for a total output capacitance of 2.1pF with a load of 150Ω (Figure 32A). When PCB trace capacitance and component capacitance exceed 2pF, overshoot becomes strongly dependent on the input pulse amplitude and slew rate. Increasing levels of output capacitance reduce stability, resulting in increased overshoot and settling time.

PC board trace length (L_{CRIT}) should be kept to a minimum in order to minimize output capacitance. At 500MHz, trace lengths approaching 1” begin exhibiting transmission line behavior and may cause excessive ringing if controlled impedance traces are not used. Figure 32B shows the optimum inter-stage circuit when the total output trace length is less than the critical length of the highest signal frequency.

As a general rule of thumb the trace lengths should be less than one-tenth of the wavelength of the highest frequency component in the signal. Equation 1 shows an approximate way to calculate L_{CRIT} in meters.

$$L_{CRIT} \le \frac{c}{10 \times f_{MAX} \times \sqrt{\varepsilon_R}} \quad \text{(EQ. 1)}$$

c = speed of light (3 x 10^8 m/s)

f_{MAX} = maximum frequency component

ε_R = relative dielectric of board material (e.g. FR4 = 4.2)

For applications where inter-stage distances are long but pulse response is not critical, capacitor C_S can be added to low values of R_S to form a low-pass filter to dampen pulse overshoot. This approach avoids the need for the large gain correction required by the -6dB attenuation of the back-loaded controlled impedance interconnect. Load resistor R_L is still required but can be 500Ω or greater, resulting in a much smaller attenuation factor.

For applications where pulse response is critical and where inter-stage distances exceed $L_{CRIT,}$ the circuit shown in Figure 32C is recommended. Resistor R_S constrains the capacitance seen by the amplifier output to the trace capacitance betweeen the output pin and the resistor. Therefore, R_S should be placed as close to the ISL59452 output pin as possible. For inter-stage distances much greater than $L_{CRIT,}$ the back-loaded circuit shown in Figure 32D should be used with controlled impedance PCB lines, with R_S and R_L equal to the controlled impedance.

Control Signals

S0, S1, AV2, and HIZ are binary coded, TTL/CMOS compatible control inputs. The S0, S1 pins select the inputs. All three output amplifiers are switched simultaneously from their respective inputs. When HIZ is pulled high, it puts the outputs in a high-impedance state. For control signal rise and fall times less than 10ns, the use of termination resistors on the control lines close to the part may be necessary to prevent reflections and to minimize transients coupled to the output. See Table 1 for the S1, S0 selection states.

HIZ State

An internal pull-down resistor ensures the device will be active with no connection to the HIZ pin. The HIZ state is established within approximately 30ns (Figure 26) by placing a logic high (>2V) on the HIZ pin. If the HIZ state is selected, the output impedance is ~2000Ω (Figure 12). The supply current during this state is reduced to ~3mA.

Limiting the Output Current

No output short circuit current limit exists on these parts. All applications need to limit the output current to less than 50mA. Adequate thermal heat sinking of the parts is also required.

PC Board Layout

The AC performance of this circuit depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum high frequency performance from your PC board.

- Use low inductance components, such as chip resistors and chip capacitors whenever possible.
- Minimize signal trace lengths. Trace inductance and capacitance can easily limit circuit performance. Avoid sharp corners; use rounded corners when possible. Vias in the signal lines add inductance at high frequency and should be avoided. PCB traces longer than 1" begin to exhibit transmission line characteristics with signal rise/fall times of 1ns or less. To maintain frequency performance with longer traces, use striplines.
- Match channel-to-channel analog I/O trace lengths and layout symmetry. This will minimize propagation delay mismatches.
- All signal I/O lines should be routed over continuous ground planes (i.e. no split planes or PCB gaps under these lines).
- Put the proper termination resistors in their optimum location as close to the device as possible.
- When testing, use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum.
- Decouple well, using aminimum of 2 power supply decoupling capacitors (1000pF, 0.01µF), placed as close to the devices as possible. Avoid vias between the capacitor and the device because vias adds unwanted inductance. Larger caps can be farther away. When vias are required in a layout, they should be routed as far away from the device as possible.

The QFN Package Requires Additional PCB Layout Rules for the Thermal Pad

The thermal pad is electrically connected to GND through the high resistance IC substrate. Its primary function is to provide heat sinking for the IC.

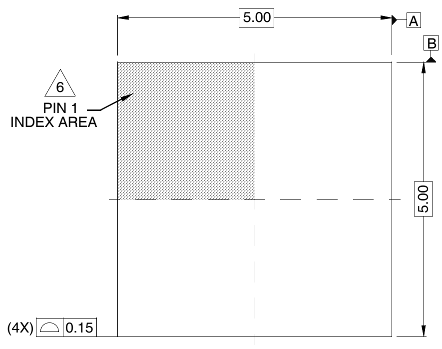
Maximum AC performance is achieved if the thermal pad is attached to a dedicated decoupled layer in a multi-layered PC board. In cases where a dedicated layer is not possible, AC performance may be reduced at upper frequencies.

- The thermal pad requirements are proportional to power dissipation and ambient temperature. A dedicated layer (oftern the ground plane) eliminates the need for individual thermal pad area. When a dedicated layer is not possible, a 1”x1” pad area is sufficient for an ISL59452 dissipating 0.5W at +50°C ambient. Pad area requirements should be evaluated according to the maximum ambient temperature, the maximum supply current (including worst case signals + loads), and the thermal characteristic of the PCB.

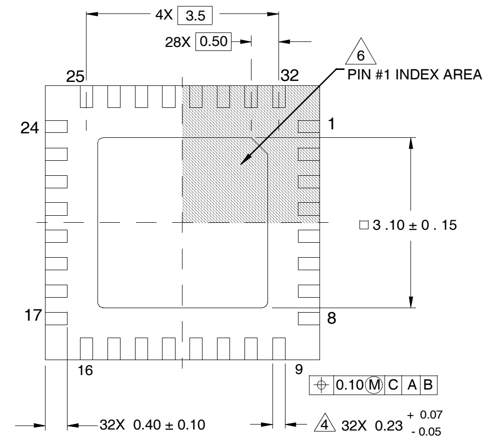
Package Outline Drawing

L32.5x5

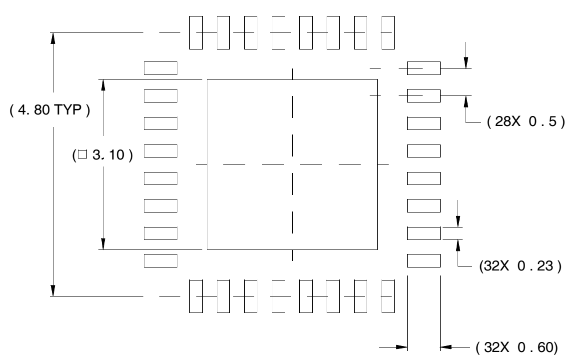
32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 02/07



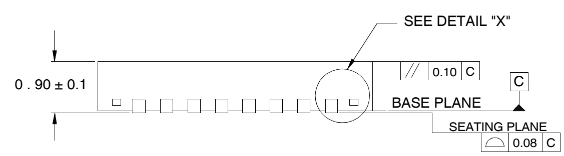
TOP VIEW



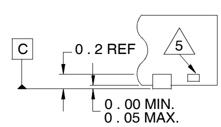
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.