



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



### 32x16 Video Crosspoint

The ISL59534 is a 300MHz 32x16 Video Crosspoint Switch. Each input has an integrated DC-restore clamp and an input buffer. Each output has a fast On-Screen Display (OSD) switch (for inserting graphics or other video) and an output buffer. The switch is non-blocking, so any combination of inputs to outputs can be chosen, including one channel driving multiple outputs. The Broadcast Mode directs one input to all 16 outputs. The output buffers can be individually controlled through the SPI interface, the gain can be programmed to +1 or +2, and each output can be placed into a high impedance mode.

The ISL59534 offers a typical -3dB signal bandwidth of 300MHz. Differential gain of 0.025% and differential gain of 0.05°, along with 0.1dB flatness out to 50MHz, make the ISL59534 suitable for many video applications.

The switch matrix configuration and output buffer gain are programmed through an SPI/QSPI™-compatible three-wire serial interface. The ISL59534 interface is designed to facilitate both fast updates and initialization. On power-up, all outputs are high impedance to avoid output conflicts.

The ISL59534 is available in a 356 ball HBGA package and specified over an extended -40°C to +85°C temperature range.

The single-supply ISL59534 can accommodate input signals from 0V to 3.5V and output voltages from 0V to 3.8V. Each input includes a clamp circuit that restores the input level to an externally applied reference in AC-coupled applications.

The ISL59535 is a fully differential input version of this device.

### Features

- 32x16 non-blocking switch with buffered inputs and outputs
- 300MHz typical bandwidth
- 0.025%/0.05° dG/dP
- Output gain switchable x1 or x2 for each channel
- Individual outputs can be put in a high impedance state
- -90dB Isolation at 6MHz
- SPI digital interface
- Single +5V supply operation
- Pb-free (RoHS compliant)

### Applications

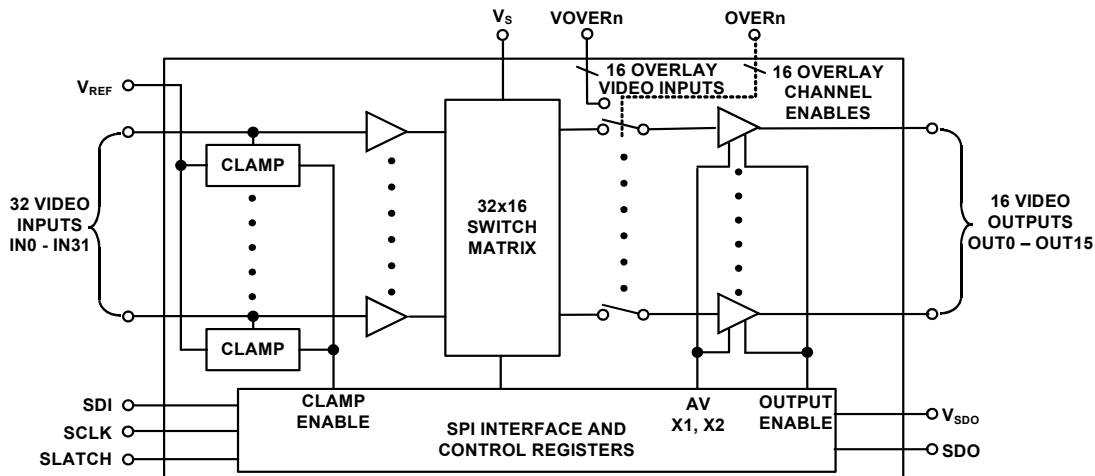
- Security camera switching
- RGB routing
- HDTV routing

### Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL59534IKEZ	ISL59534IKEZ	356 Ld HBGA	V356.27x27C

NOTE: These Intersil Pb-free WLCSP and BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

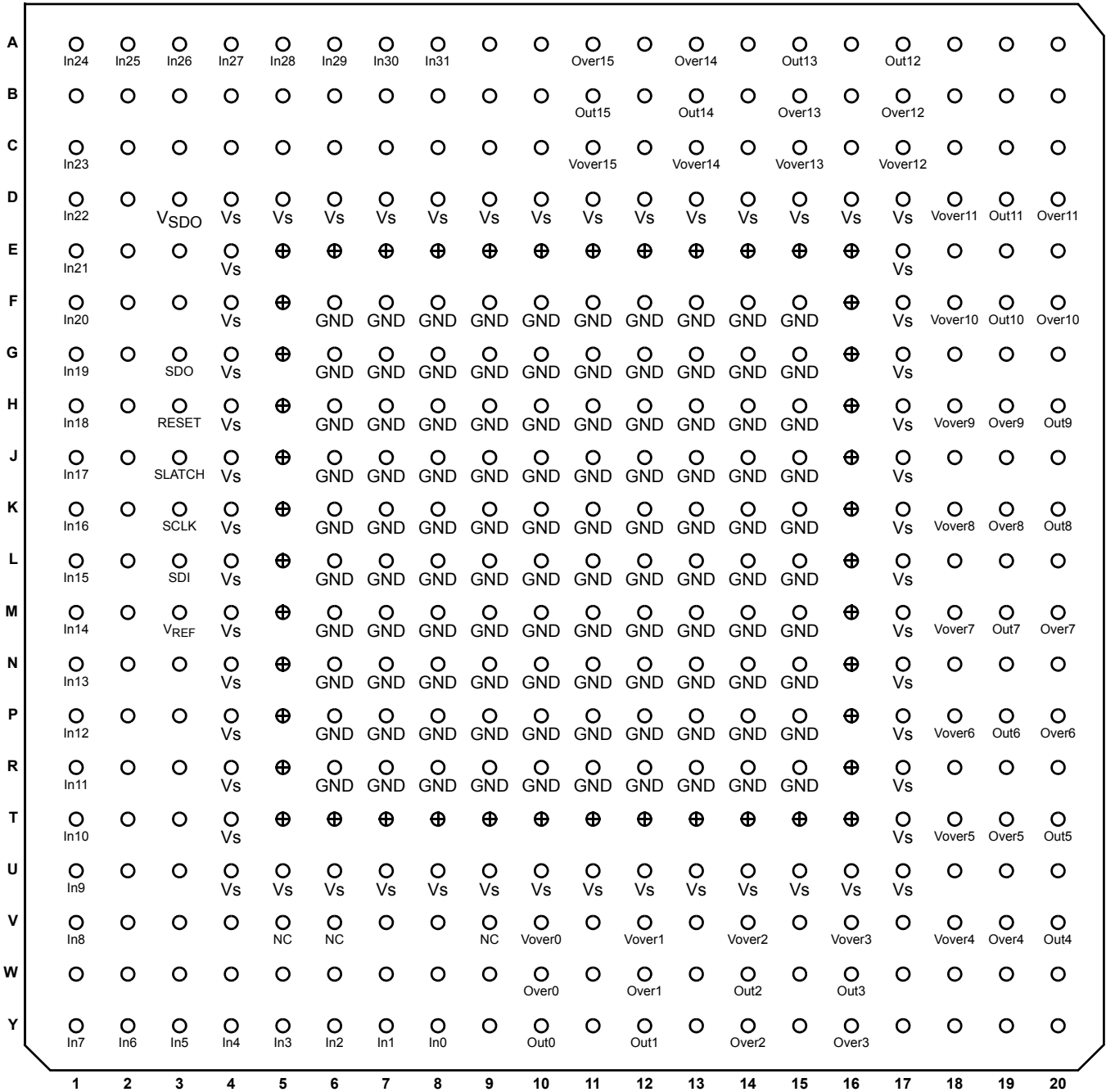
### Block Diagram



# ISL59534

## Pinout

### ISL59534 (356 LD HBGA) TOP VIEW



⊕ = NO BALLS

**BALLS LABELLED "NC" SHOULD BE LEFT UNCONNECTED - DO NOT TIE THEM TO GROUND!**  
**BALLS WITH NO LABELS MAY BE TIED TO GROUND TO SLIGHTLY REDUCE THERMAL IMPEDANCE.**



**Absolute Maximum Ratings** ( $T_A = +25^\circ\text{C}$ )

Supply Voltage between $V_S$ and GND	6.0V
Maximum Continuous Output Current	40mA
Maximum power supply ( $V_S$ ) slew rate	1V/ $\mu\text{s}$

**Thermal Information**

Thermal Resistance (Typical)	$\theta_{JA}$ ( $^\circ\text{C}/\text{W}$ )	$\theta_{JC}$ ( $^\circ\text{C}/\text{W}$ )
356 Ld HBGA (Notes 1, 2)	24	13.1
Maximum Die Temperature	+125 $^\circ\text{C}$	
Storage Temperature	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$	
Pb-free reflow profile	see link below	
<a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>		

**Operating Conditions**

ESD Classification	
Human Body Model	1500V
Machine Model	100V
Ambient Operating Temperature	-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

**NOTES:**

- $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- For  $\theta_{JC}$ , the "case temp" location is taken at the package top center.

**DC Electrical Specifications**  $V_S = 5\text{V}$ ,  $R_L = 150\Omega$  unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 3)	TYP	MAX (Note 3)	UNIT
$V_S$	Power Supply Voltage		4.5		5.5	V
$V_{SDO}$	Power Supply for SDO output pin	Establishes serial data output high level	1.2		5.5	V
$A_V$	Gain (between all primary inputs and all overlay inputs)	$A_V = 1$	0.98	1	1.02	V/V
		$A_V = 2$	1.96	2	2.04	V/V
GM	Gain Matching (to average of all other outputs)	$A_V = 1$	-1.5		+1.5	%
		$A_V = 2$	-1.5		+1.5	%
$V_{IN}$	Video Input Voltage Range	$A_V = 1$	0		3.5	V
$V_{OUT}$	Video Output Voltage Range	$A_V = 2$	0.1		3.8	V
$I_B$	Input Bias Current	Clamp function disabled (DC coupled inputs)	-10	-5	1	$\mu\text{A}$
		Clamp function enabled, $V_{IN} = V_{REF} + 0.5\text{V}$	0.5	2	10	$\mu\text{A}$
$I_{REF}$	$V_{REF}$ Input Current	Clamp function enabled		-110		$\mu\text{A}$
$V_{OS}$	Output Offset Voltage	$A_V = 1$	-20	8	35	mV
		$A_V = 2$	-100	-24	40	mV
$I_{OUT}$	Output Current	Sourcing, $R_L = 10\Omega$ to GND	60	108		mA
		Sinking, $R_L = 10\Omega$ to 2.5V	24	31		mA
PSRR	Power Supply Rejection Ratio	$A_V = 2$	50	70		dB
$I_S$	Supply Current	Enabled, all outputs enabled, no load current	385	445	505	mA
		Enabled, all outputs disabled, no load current	280	320	360	mA
		Disabled	1.2	1.8	2.4	mA

**AC Electrical Specifications**  $V_S = 5\text{V}$ ,  $R_L = 150\Omega$  unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 3)	TYP	MAX (Note 3)	UNIT
BW -3dB	3dB Bandwidth	$V_{OUT} = 200\text{mV}_{P-P}$ , $A_V = 2$		300		MHz
BW 0.1dB	0.1dB Bandwidth	$V_{OUT} = 200\text{mV}_{P-P}$ , $A_V = 2$		50		MHz
SR	Slew Rate	$V_{OUT} = 2V_{P-P}$ , $A_V = 2$	300	520	740	V/ $\mu\text{s}$
$T_S$	Settling Time to 0.1%	$V_{OUT} = 2V_{P-P}$ , $A_V = 2$		12		ns
Glitch	Switching Glitch, Peak	$A_V = 1$		40		mV
$T_{over}$	Overlay Delay Time	From OVER rising edge to output transition		6		ns
dG	Diff Gain	$A_V = 2$ , $R_L = 150\Omega$		0.025		%
dP	Diff Phase	$A_V = 2$ , $R_L = 150\Omega$		0.05		$^\circ$
$XT_{ADJACENT}$	Adjacent Channel Crosstalk	6MHz, $A_V = 1$		-90		dB
$XT_{HOSTILE}$	Hostile Crosstalk	6MHz, $A_V = 1$		-72		dB

**AC Electrical Specifications**  $V_S = 5V$ ,  $R_L = 150\Omega$  unless otherwise noted. (Continued)

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 3)	TYP	MAX (Note 3)	UNIT
$V_N$	Input Referred Noise Voltage			18		nV/ $\sqrt{\text{Hz}}$

NOTE:

3. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

**Pin Descriptions**

NAME	NUMBER	DESCRIPTION
IN0	Y8	Crosspoint Video Input
IN1	Y7	Crosspoint Video Input
IN2	Y6	Crosspoint Video Input
IN3	Y5	Crosspoint Video Input
IN4	Y4	Crosspoint Video Input
IN5	Y3	Crosspoint Video Input
IN6	Y2	Crosspoint Video Input
IN7	Y1	Crosspoint Video Input
IN8	V1	Crosspoint Video Input
IN9	U1	Crosspoint Video Input
IN10	T1	Crosspoint Video Input
IN11	R1	Crosspoint Video Input
IN12	P1	Crosspoint Video Input
IN13	N1	Crosspoint Video Input
IN14	M1	Crosspoint Video Input
IN15	L1	Crosspoint Video Input
IN16	K1	Crosspoint Video Input
IN17	J1	Crosspoint Video Input
IN18	H1	Crosspoint Video Input
IN19	G1	Crosspoint Video Input
IN20	F1	Crosspoint Video Input
IN21	E1	Crosspoint Video Input
IN22	D1	Crosspoint Video Input
IN23	C1	Crosspoint Video Input
IN24	A1	Crosspoint Video Input
IN25	A2	Crosspoint Video Input
IN26	A3	Crosspoint Video Input
IN27	A4	Crosspoint Video Input
IN28	A5	Crosspoint Video Input
IN29	A6	Crosspoint Video Input
IN30	A7	Crosspoint Video Input
IN31	A8	Crosspoint Video Input

**Pin Descriptions (Continued)**

NAME	NUMBER	DESCRIPTION
OUT0	Y10	Crosspoint Video Output
OUT1	Y12	Crosspoint Video Output
OUT2	W14	Crosspoint Video Output
OUT3	W16	Crosspoint Video Output
OUT4	V20	Crosspoint Video Output
OUT5	T20	Crosspoint Video Output
OUT6	P19	Crosspoint Video Output
OUT7	M19	Crosspoint Video Output
OUT8	K20	Crosspoint Video Output
OUT9	H20	Crosspoint Video Output
OUT10	F19	Crosspoint Video Output
OUT11	D19	Crosspoint Video Output
OUT12	A17	Crosspoint Video Output
OUT13	A15	Crosspoint Video Output
OUT14	B13	Crosspoint Video Output
OUT15	B11	Crosspoint Video Output
OVER0	W10	Overlay Logic Control (with pulldown)
OVER1	W12	Overlay Logic Control (with pulldown)
OVER2	Y14	Overlay Logic Control (with pulldown)
OVER3	Y16	Overlay Logic Control (with pulldown)
OVER4	V19	Overlay Logic Control (with pulldown)
OVER5	T19	Overlay Logic Control (with pulldown)
OVER6	P20	Overlay Logic Control (with pulldown)
OVER7	M20	Overlay Logic Control (with pulldown)
OVER8	K19	Overlay Logic Control (with pulldown)
OVER9	H19	Overlay Logic Control (with pulldown)
OVER10	F20	Overlay Logic Control (with pulldown)
OVER11	D20	Overlay Logic Control (with pulldown)
OVER12	B17	Overlay Logic Control (with pulldown)
OVER13	B15	Overlay Logic Control (with pulldown)
OVER14	A13	Overlay Logic Control (with pulldown)
OVER15	A11	Overlay Logic Control (with pulldown)

**Pin Descriptions** (Continued)

NAME	NUMBER	DESCRIPTION
VOVER0	V10	Overlay Video Input
VOVER1	V12	Overlay Video Input
VOVER2	V14	Overlay Video Input
VOVER3	V16	Overlay Video Input
VOVER4	V18	Overlay Video Input
VOVER5	T18	Overlay Video Input
VOVER6	P18	Overlay Video Input
VOVER7	M18	Overlay Video Input
VOVER8	K18	Overlay Video Input
VOVER9	H18	Overlay Video Input
VOVER10	F18	Overlay Video Input
VOVER11	D18	Overlay Video Input
VOVER12	C17	Overlay Video Input
VOVER13	C15	Overlay Video Input
VOVER14	C13	Overlay Video Input
VOVER15	C11	Overlay Video Input
V <sub>REF</sub>	M3	DC-restore clamp reference input. In an AC-coupled configuration (DC-Restore clamp enabled), the sync tip of composite video inputs will be restored to this level. Set to 0.3 to 0.7V for optimum performance. In an DC-coupled configuration (DC-Restore clamp disabled), this pin should be tied to ground. <b>Do not let the V<sub>REF</sub> pin float!</b> A floating V <sub>REF</sub> pin drifts high and, if the clamp function is enabled, will cause all of the outputs to simultaneously try to drive ~4V DC into their 150Ω loads.
SLATCH	J3	Serial Latch. Serial data is latched into ISL59534 on rising edge of SLATCH.
SCLK	K3	Serial data clock
SDI	L3	Serial data input
SDO	G3	Serial data output. Can be tied to SDI of another ISL59534 to enable daisy-chaining of multiple devices.
RESET	H3	Reset input. Pull high then low to reset device, but not needed in normal operation. Tie to ground in final application.
V <sub>SDO</sub>	D3	Power supply for SDO pin. Tie to +5V for a 0 to 5V SDO output signal swing.
V <sub>S</sub>		+5V power supply

**Pin Descriptions** (Continued)

NAME	NUMBER	DESCRIPTION
GND		Ground
NC		No Connect - <i>Do not electrically connect to anything, including ground.</i>

Typical Performance Curves

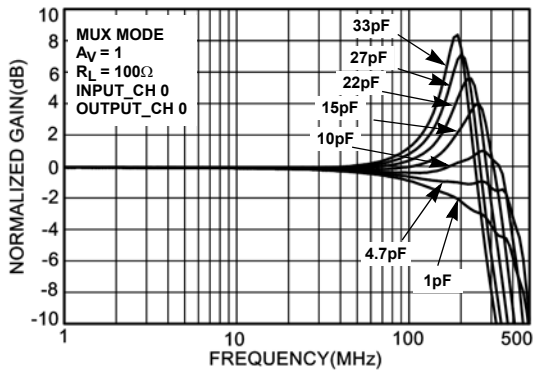


FIGURE 1. FREQUENCY RESPONSE - VARIOUS  $C_L$ ,  $A_V = 1$ , MUX MODE

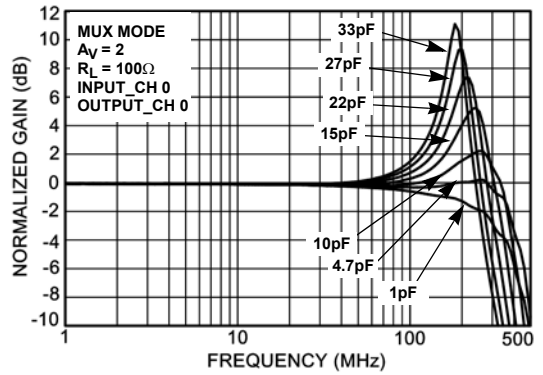


FIGURE 2. FREQUENCY RESPONSE - VARIOUS  $C_L$ ,  $A_V = 2$ , MUX MODE

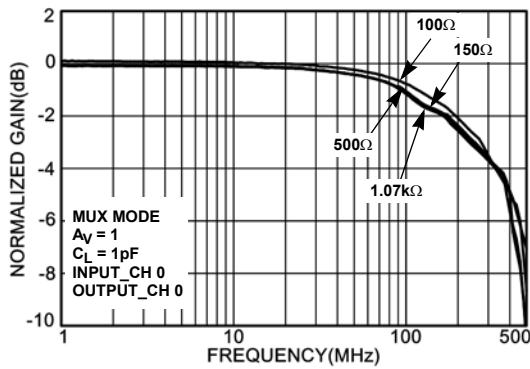


FIGURE 3. FREQUENCY RESPONSE - VARIOUS  $R_L$ ,  $A_V = 1$ , MUX MODE

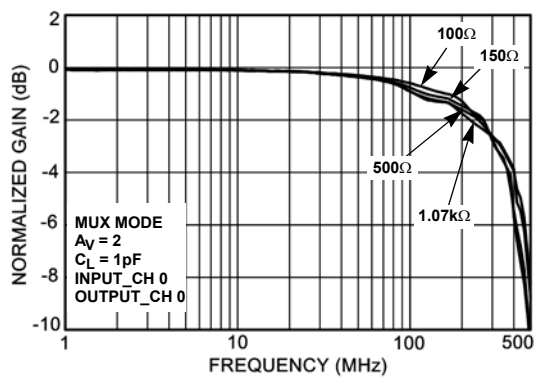


FIGURE 4. FREQUENCY RESPONSE - VARIOUS  $R_L$ ,  $A_V = 2$ , MUX MODE

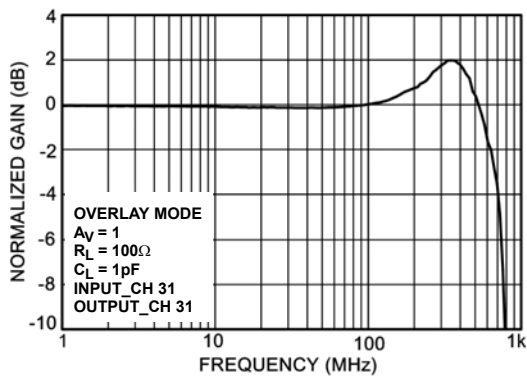


FIGURE 5. FREQUENCY RESPONSE - OVERLAY INPUT,  $A_V = 1$

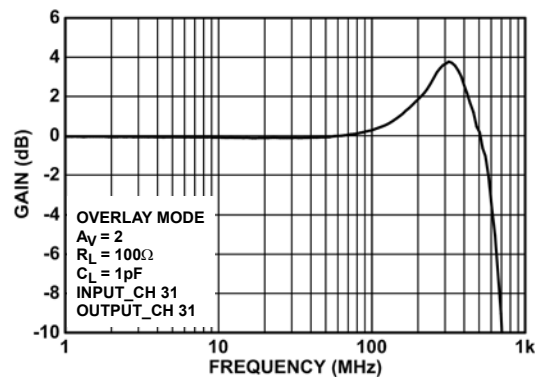


FIGURE 6. FREQUENCY RESPONSE - OVERLAY INPUT,  $A_V = 2$

Typical Performance Curves (Continued)

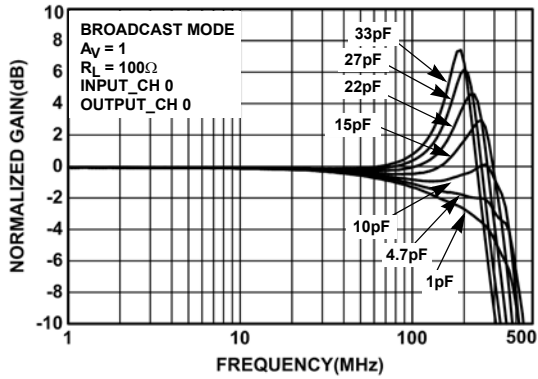


FIGURE 7. FREQUENCY RESPONSE - VARIOUS  $C_L$ ,  $A_V = 1$ , BROADCAST MODE

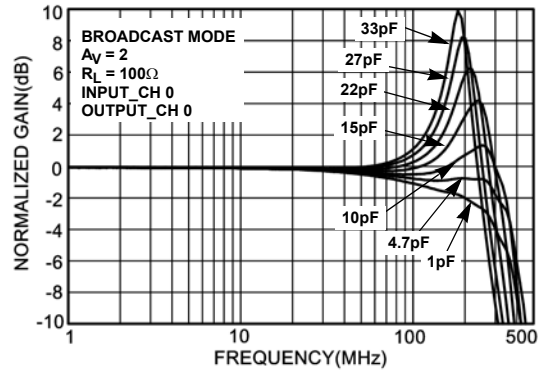


FIGURE 8. FREQUENCY RESPONSE - VARIOUS  $C_L$ ,  $A_V = 2$ , BROADCAST MODE

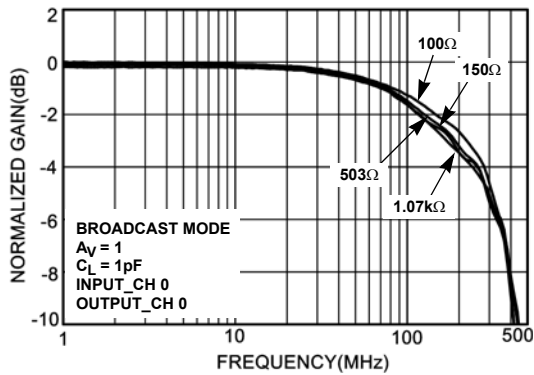


FIGURE 9A. FREQUENCY RESPONSE - VARIOUS  $R_L$ ,  $A_V = 1$ , BROADCAST MODE

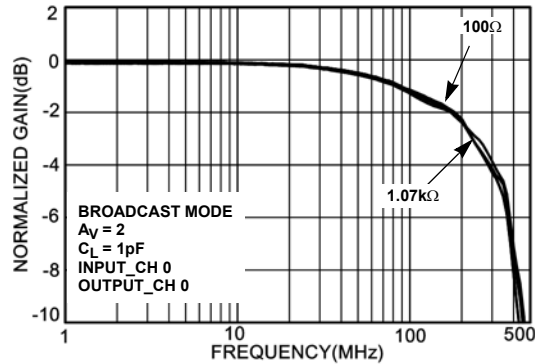


FIGURE 10. FREQUENCY RESPONSE - VARIOUS  $R_L$ ,  $A_V = 2$ , BROADCAST MODE

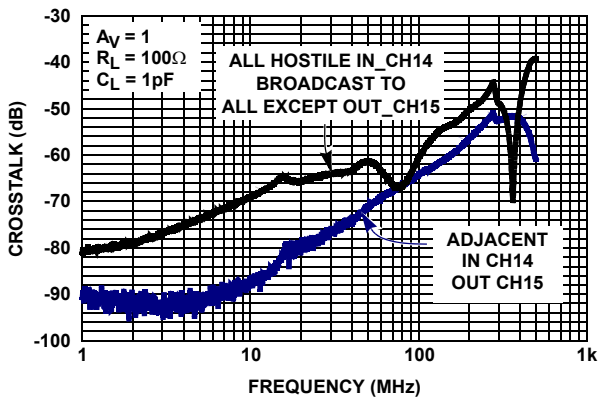


FIGURE 11. CROSSTALK -  $A_V = 1$

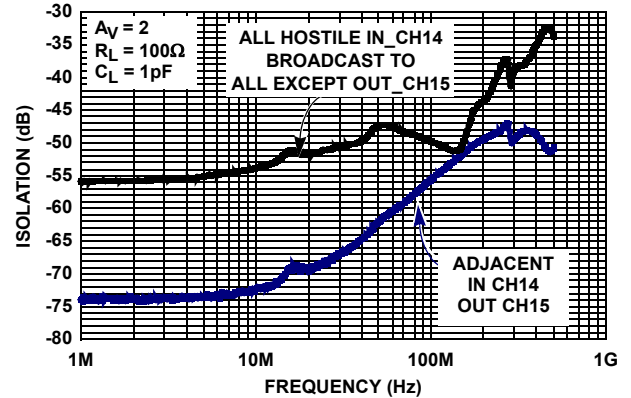


FIGURE 12. CROSSTALK -  $A_V = 2$



Typical Performance Curves (Continued)

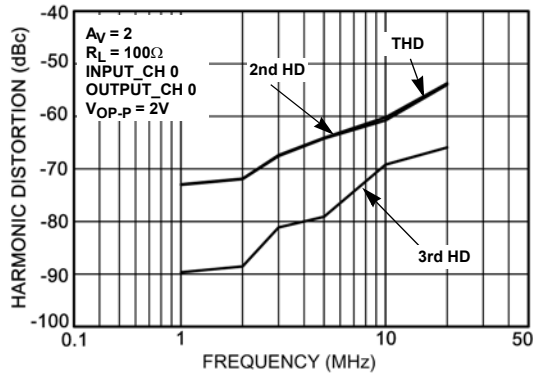


FIGURE 13. HARMONIC DISTORTION vs FREQUENCY

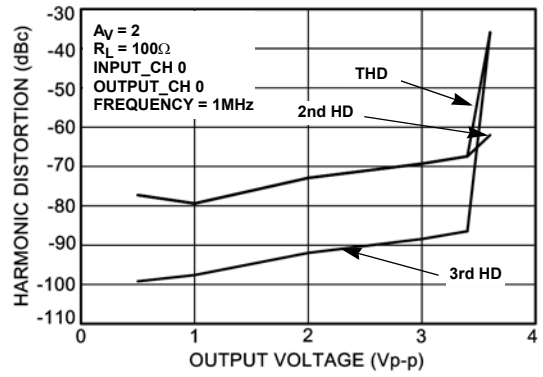


FIGURE 14. HARMONIC DISTORTION vs  $V_{OUT\_P-P}$

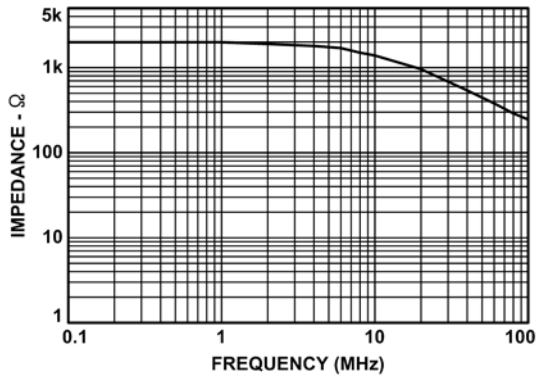


FIGURE 15. DISABLED OUTPUT IMPEDANCE

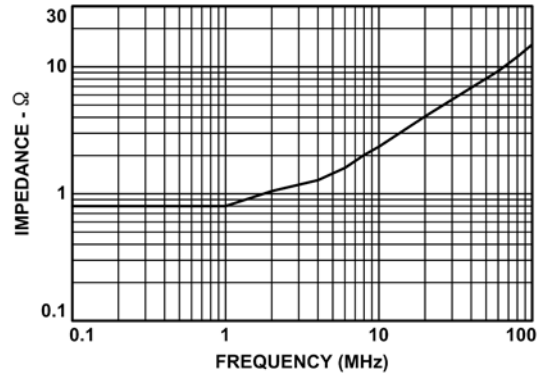


FIGURE 16. ENABLED OUTPUT IMPEDANCE

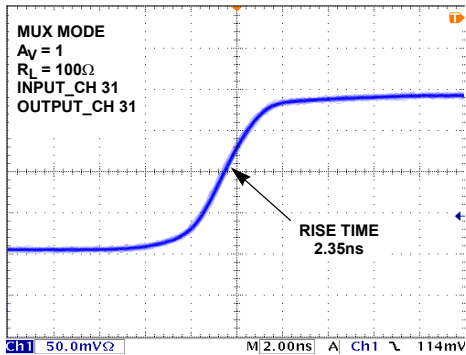


FIGURE 17. RISE TIME -  $A_V = 1$

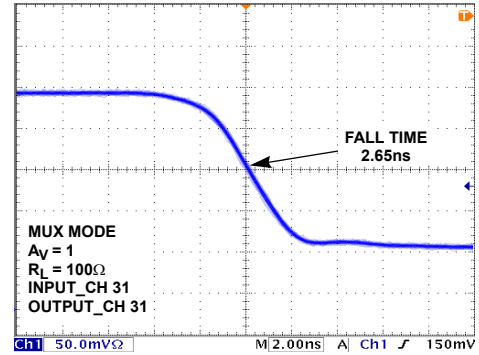


FIGURE 18. FALL TIME -  $A_V = 1$

Typical Performance Curves (Continued)

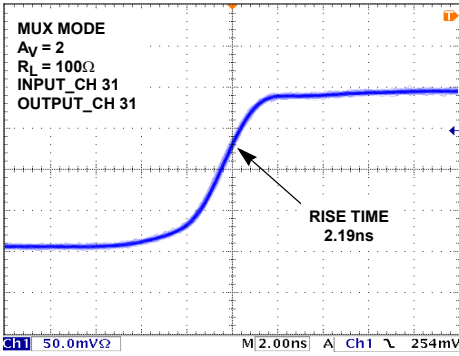


FIGURE 19. RISE TIME -  $A_V = 2$

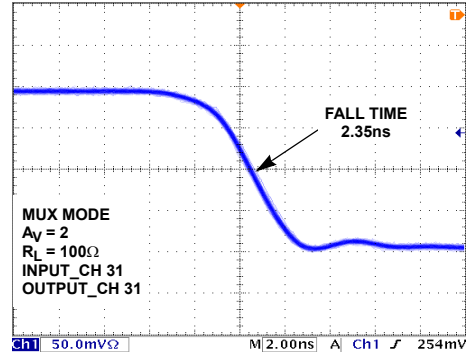


FIGURE 20. FALL TIME -  $A_V = 2$

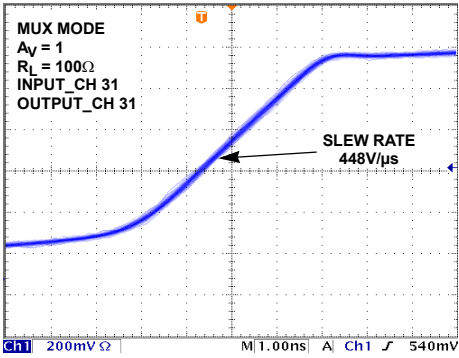


FIGURE 21. RISING SLEW RATE -  $A_V = 1$

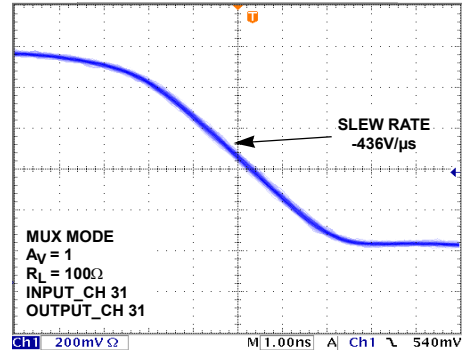


FIGURE 22. FALLING SLEW RATE -  $A_V = 1$

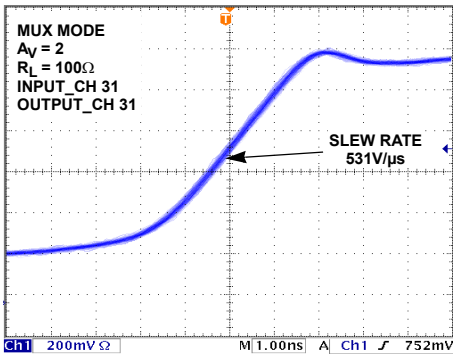


FIGURE 23. RISING SLEW RATE -  $A_V = 2$

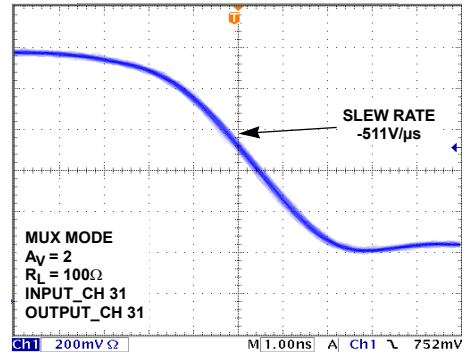


FIGURE 24. FALLING SLEW RATE -  $A_V = 2$

Typical Performance Curves (Continued)

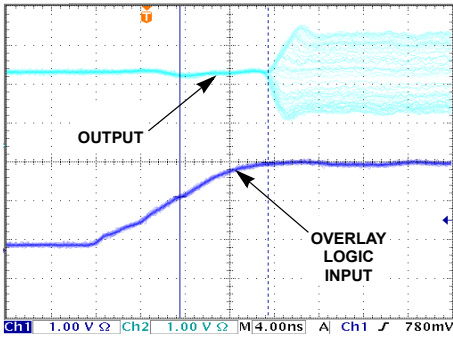


FIGURE 25. OVERLAY SWITCH TURN-ON DELAY TIME

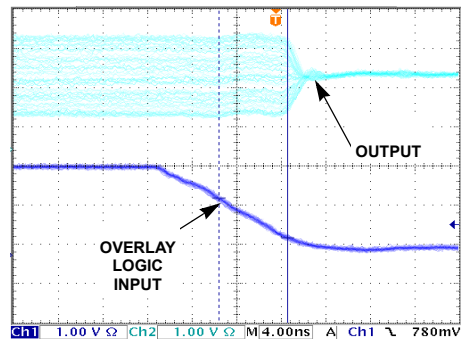


FIGURE 26. OVERLAY SWITCH TURN-OFF DELAY TIME

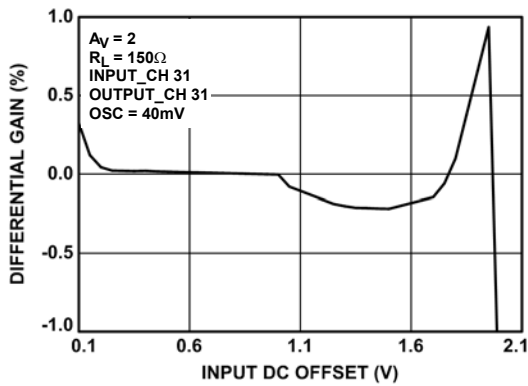


FIGURE 27. DIFFERENTIAL GAIN,  $A_V = 2$

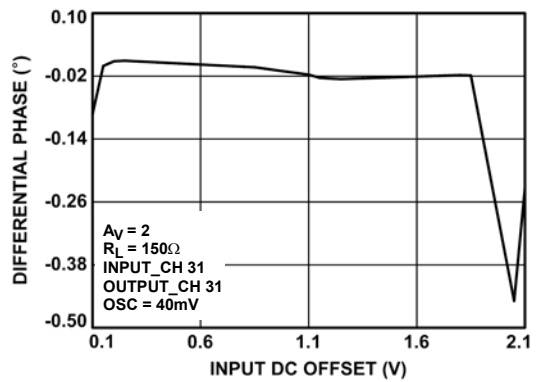


FIGURE 28. DIFFERENTIAL PHASE,  $A_V = 2$

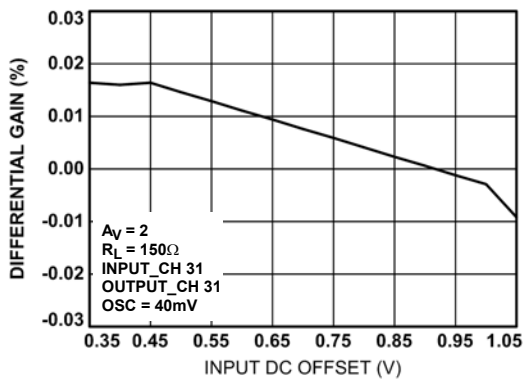


FIGURE 29. DIFFERENTIAL GAIN,  $A_V = 2$

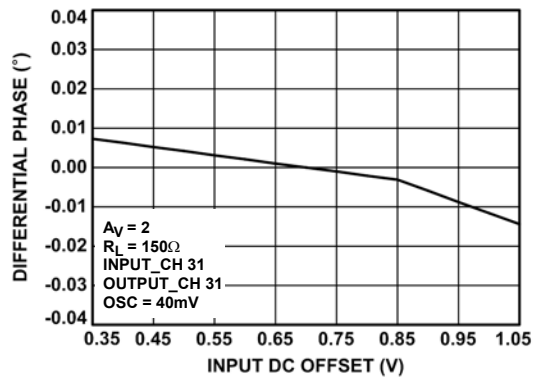


FIGURE 30. DIFFERENTIAL PHASE,  $A_V = 2$

Typical Performance Curves (Continued)

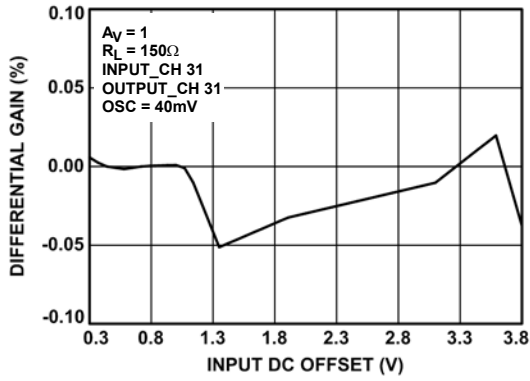


FIGURE 31. DIFFERENTIAL GAIN,  $A_V = 1$

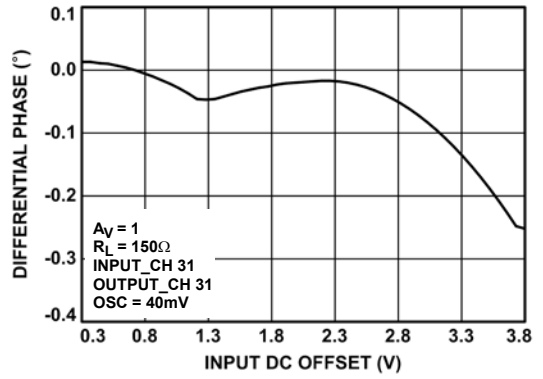


FIGURE 32. DIFFERENTIAL PHASE,  $A_V = 1$

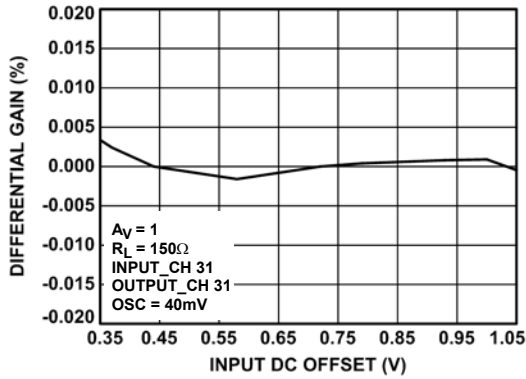


FIGURE 33. DIFFERENTIAL GAIN,  $A_V = 1$

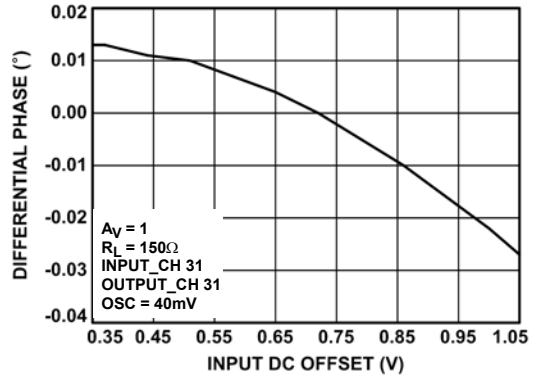


FIGURE 34. DIFFERENTIAL PHASE,  $A_V = 1$

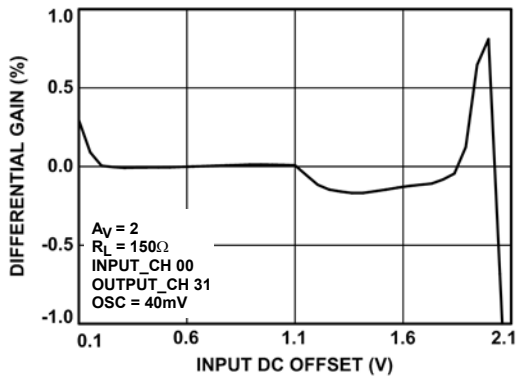


FIGURE 35. DIFFERENTIAL GAIN,  $A_V = 2$

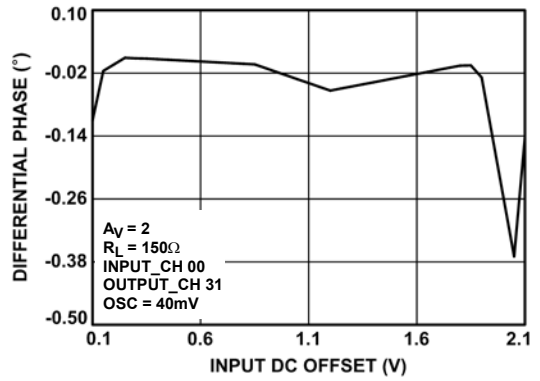


FIGURE 36. DIFFERENTIAL PHASE,  $A_V = 2$

Typical Performance Curves (Continued)

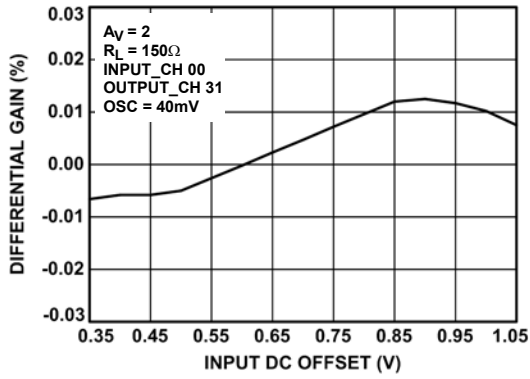


FIGURE 37. DIFFERENTIAL GAIN,  $A_V = 2$

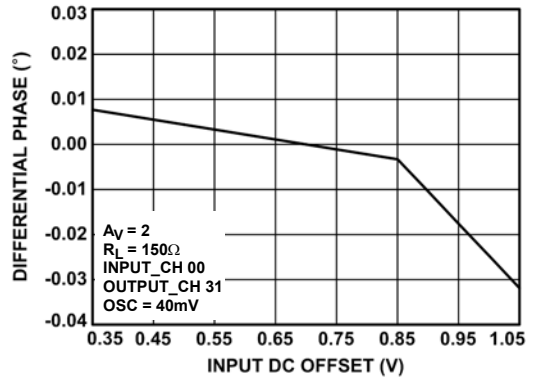


FIGURE 38. DIFFERENTIAL PHASE,  $A_V = 2$

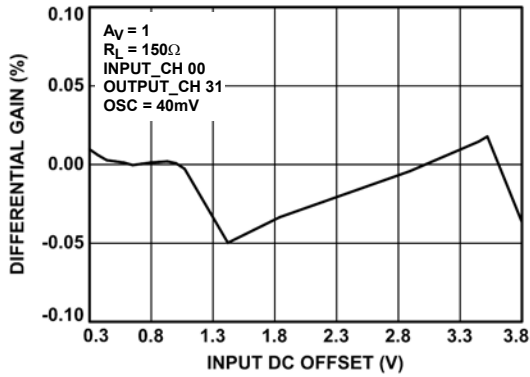


FIGURE 39. DIFFERENTIAL GAIN,  $A_V = 1$

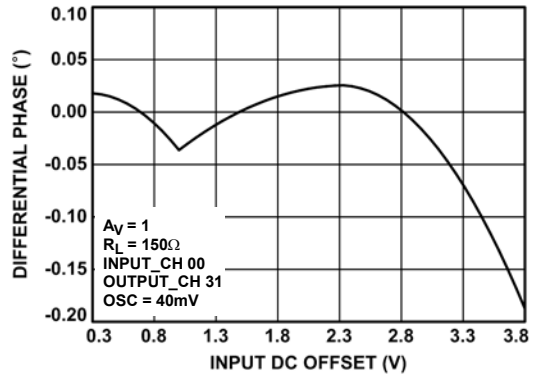


FIGURE 40. DIFFERENTIAL PHASE,  $A_V = 1$

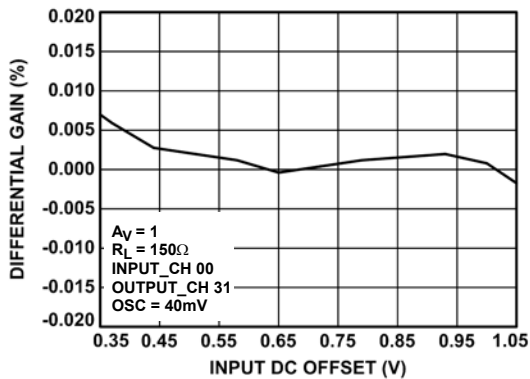


FIGURE 41. DIFFERENTIAL GAIN,  $A_V = 1$

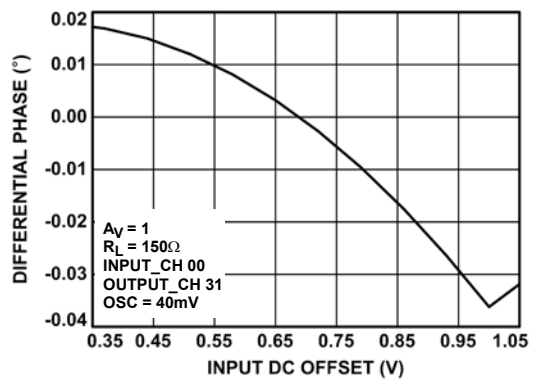


FIGURE 42. DIFFERENTIAL PHASE,  $A_V = 1$



Typical Performance Curves (Continued)

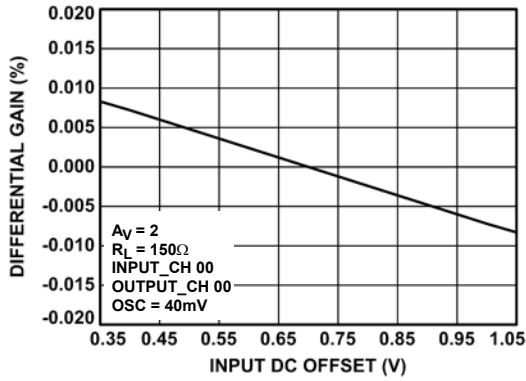


FIGURE 43. DIFFERENTIAL GAIN, OVERLAY,  $A_V = 2$

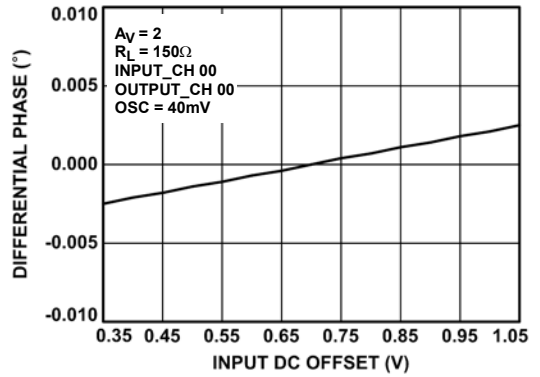


FIGURE 44. DIFFERENTIAL PHASE, OVERLAY,  $A_V = 2$

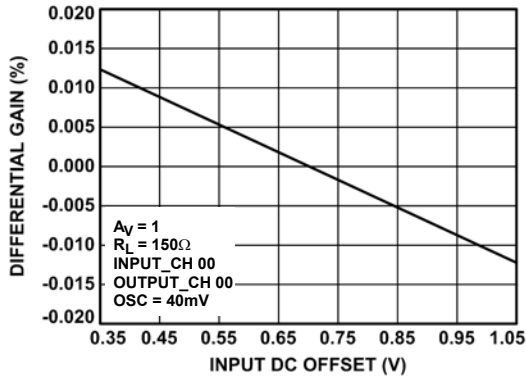


FIGURE 45. DIFFERENTIAL GAIN, OVERLAY,  $A_V = 1$

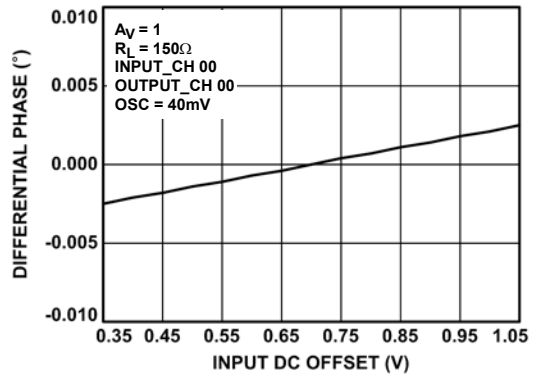


FIGURE 46. DIFFERENTIAL PHASE, OVERLAY,  $A_V = 1$

3dB Bandwidth, MUX Mode,  $A_V = 1$ ,  $R_L = 100\Omega$  [MHz]

		INPUT CHANNELS																																	
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		
OUTPUT CHANNELS	0	262					270					268					235						236					235							236
	1			217																												214			
	2					277																									272				
	3							288																				290							
	4										269															271									
	5	273										274					256								272										
	6													255									258												
	7															268				274															
	8																278	286																	
	9																265					277													
	10	281											282					265						288											283
	11												285												350										
	12									196																		216							
	13						269																							285					
	14				199																											281			
	15	238						230						238					220						280					287					

3dB Bandwidth, MUX Mode,  $A_V = 2$ ,  $R_L = 100\Omega$  [MHz]

		INPUT CHANNELS																																	
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		
OUTPUT CHANNELS	0	304					323					324					305						313					320						308	
	1			290																												294			
	2					353																									348				
	3							371																				370							
	4										360																366								
	5	351											350					317							350									340	
	6															348																			
	7																327				341														
	8																	325	338																
	9																	339																	
	10	351												350																					348
	11													371																					
	12																																		
	13																																		
	14																																		
	15	311																																	

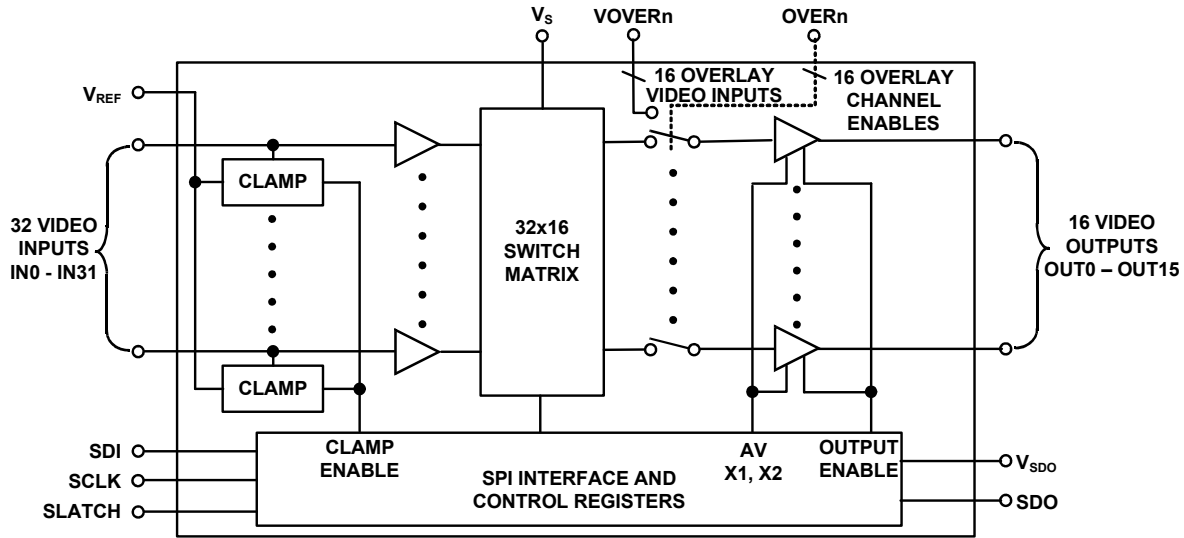
**3dB Bandwidth, Broadcast Mode,  $A_V = 1$ ,  $R_L = 100\Omega$  [MHz]**

		INPUT CHANNELS																																						
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31							
OUTPUT CHANNELS	0	196	204	193	175	154	154	158	161	169	157	155	146	125	121	115	109	81	81	79	80	85	85	86	86	83	82	82	77	80	82	85	86							
	1	172		163													104															85		87						
	2	165				128											99													79				89						
	3	152						123									95											81						89						
	4	133									113						86									82								89						
	5	132										113					91							88											92					
	6	125												94			87					81													92					
	7	127														90	88		85																	97				
	8	124															89	88																			100			
	9	116													88		84			87																	100			
	10	114											97				84							98														102		
	11	108									94						80									100												102		
	12	106								96							79											99											106	
	13	108					96										81												98											114
	14	104			98												78																105							115
15	107	110	108	103	98	98	98	99	101	99	97	95	87	86	84	81	113	112	112	114	126	126	128	129	124	118	114	111	120	122	129	131								

**3dB Bandwidth, Broadcast Mode,  $A_V = 2$ ,  $R_L = 100\Omega$  [MHz]**

		INPUT CHANNELS																																							
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31								
OUTPUT CHANNELS	0	270	277	268	247	213	216	227	244	258	223	208	196	147	142	132	123	85	85	85	86	91	91	92	93	90	88	86	85	89	90	92	94								
	1	240		223													112															88				92					
	2	233				158											108												83								95				
	3	204						146									105										88											95			
	4	172									128						92									85												94			
	5	170										126					97							94															98		
	6	152												103			93				89																		99		
	7	155														96	94		89																				105		
	8	146															93	94																					109		
	9	133														94	90			93																			109		
	10	129											106				89							106																113	
	11	119										102					84									107														112	
	12	116								103							83										107													117	
	13	120					103										84												108												135
	14	113			106												82																	113							133
15	117	121	118	112	105	105	106	108	110	107	104	101	93	91	88	85	130	127	127	130	153	150	158	163	149	140	133	126	140	146	161	164									

## Block Diagram



## General Description

The ISL59534 is a 32x16 integrated video crosspoint switch matrix with input and output buffers and On-Screen Display (OSD) insertion. This device operates from a single +5V supply. Any output can be generated from any of the 32 input video signal sources, and each output can have OSD information inserted through a dedicated, fast 2:1 mux located before the output buffer. There is also a Broadcast mode allowing any one input to be broadcast to all 16 outputs. A DC restore clamp function enables the ISL59534 to AC-couple incoming video.

The ISL59534 offers a -3dB signal bandwidth of 300MHz. Differential gain and differential phase of 0.025% and 0.05° respectively, along with 0.1dB flatness out to 50MHz make this ideal for multiplexing composite NTSC and PAL signals. The switch matrix configuration and output buffer gain are programmed through an SPI/QSPI™-compatible, three-wire serial interface. The ISL59534 interface is designed to facilitate both fast initialization and configuration changes. On power-up, all outputs are initialized to the disabled state to avoid output conflicts in the user's system.

## Digital Interface

The ISL59534 uses a serial interface to program the configuration registers. The serial interface uses three signals (SCLK, SDI, and SLATCH) for programming the ISL59534, while a fourth signal (SDO) enables optional daisy-chaining of multiple devices. The serial clock can run at up to 5MHz (5Mbits/s).

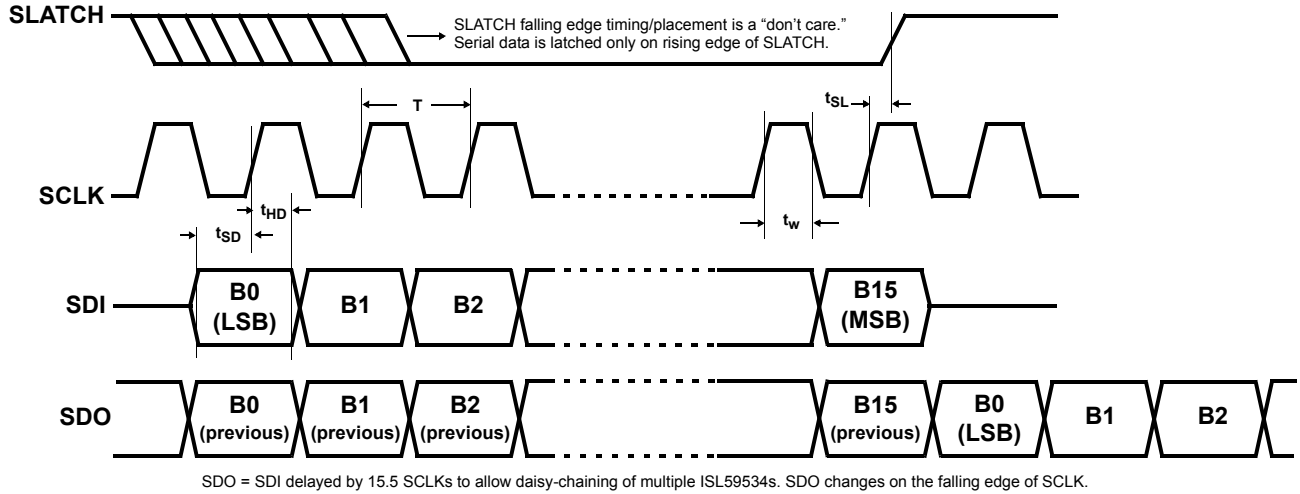
## Serial Interface

The ISL59534 is programmed through a simple serial interface. Data on the SDI (serial data input) pin is shifted into a 16-bit shift register on the rising edge of the SCLK (serial clock) signal. (This is continuously done regardless of the state of the SLATCH signal.) The LSB (bit 0) is loaded first and the MSB (bit 15) is loaded last (see the Serial Timing Diagram). After all 16 bits of data have been loaded into the shift register, the rising edge of SLATCH updates the internal registers.

While the ISL59534 has an SDO (Serial Data Out) pin, it does not have a register readback feature. The data on the SDO pin is an exact replica of the incoming data on the SDI pin, delayed by 15.5 SCLKs (an input bit is latched on the rising edge of SCLK, and is output on SDO on the falling edge of SCLK 15.5 SCLKs later). Multiple ISL59534's can be daisy-chained by connecting the SDO of one to the SDI of the other, with SCLK and SLATCH common to all the daisy-chained parts. After all the serial data is transmitted (16 bits \* n devices = 16\*n SCLKs), the rising edge of SLATCH will update the configuration registers of all n devices simultaneously.

The Serial Timing Diagram and Serial Timing Parameters table on page 17 show the timing requirements for the serial interface.

**Serial Timing Diagram**



**TABLE 1. SERIAL TIMING PARAMETERS**

PARAMETER	RECOMMENDED OPERATING RANGE	DESCRIPTION
T	≥200ns	SCLK period
t <sub>W</sub>	0.50 * T	Clock Pulse Width
t <sub>SD</sub>	≥20ns	Data Setup Time
t <sub>HD</sub>	≥20ns	Data Hold Time
t <sub>SL</sub>	≥20ns	Final SCLK rising edge (latching B15) to SLATCH rising edge

**Programming Model**

The ISL59534 is configured by a series of 16-bit serial control words. The three MSBs (B15-13) of each serial word determine the basic command:

**TABLE 2. COMMAND FORMAT**

B15	B14	B13	COMMAND	NUMBER OF WRITES
0	0	0	INPUT/OUTPUT: Maps input channels to output channels	32 (1 channel per write)
0	0	1	OUTPUT ENABLE: Output enable for individual channels	4 (4 channels per write)
0	1	0	GAIN SET: Gain (+1 or +2) for each channel	4 (4 channels per write)
0	1	1	BROADCAST: Enables broadcast mode and selects the input channel to be broadcast to all output channels	1
1	1	1	CONTROL: Clamp on/off, operational/standby mode, and global output enable/disable	1

**Mapping Inputs to Outputs**

Inputs are mapped to their desired outputs using the input/output control word. Its format is:

**TABLE 3. INPUT/OUTPUT WORD**

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	I <sub>4</sub>	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	-	-	-	O <sub>3</sub>	O <sub>2</sub>	O <sub>1</sub>	O <sub>0</sub>	

I<sub>4</sub>:I<sub>0</sub> form the 5-bit word indicating the input channel (0 to 31), and O<sub>3</sub>:O<sub>0</sub> determine the output channel which that input channel will map to. One input can be mapped to one or multiple outputs. To fully program the ISL59534, 32 INPUT/OUTPUT words must be transmitted - one for each input channel.

Note: Broadcast Mode must be disabled when configuring input/output mapping. INPUT/OUTPUT words transmitted while in Broadcast Mode will not be processed correctly and result in corrupt channel mapping when Broadcast Mode is disabled.



**Enabling Outputs**

The output enable control word is used to enable individual outputs. There are 16 channels to configure, so this is accomplished by writing 4 serial words, each controlling a bank of eight outputs at a time. The bank is selected by bits B9 and B8. The output enable control word format is:

**TABLE 4. OUTPUT ENABLE FORMAT**

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	1	0	0	0	0	0		O <sub>3</sub>		O <sub>2</sub>		O <sub>1</sub>		O <sub>0</sub>
0	0	1	0	0	0	0	1		O <sub>7</sub>		O <sub>6</sub>		O <sub>5</sub>		O <sub>4</sub>
0	0	1	0	0	0	1	0		O <sub>11</sub>		O <sub>10</sub>		O <sub>9</sub>		O <sub>8</sub>
0	0	1	0	0	0	1	1		O <sub>15</sub>		O <sub>14</sub>		O <sub>13</sub>		O <sub>12</sub>

Setting the O<sub>N</sub> bit = 0 tri-states the output. Setting the O<sub>N</sub> bit = 1 enables the output if the Global Output Enable bit is also set (the individual output enable bits are ANDed with the Global Output Enable bit before they are sent to the output stage).

**Setting the Gain**

The gain of each output may be set to +1 or +2 using the Gain Set word. It is in the same format as the output enable control word:

**TABLE 5. GAIN SET FORMAT**

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	1	0	0	0	0	0	0		G <sub>3</sub>		G <sub>2</sub>		G <sub>1</sub>		G <sub>0</sub>
0	1	0	0	0	0	0	1		G <sub>7</sub>		G <sub>6</sub>		G <sub>5</sub>		G <sub>4</sub>
0	1	0	0	0	0	1	0		G <sub>11</sub>		G <sub>10</sub>		G <sub>9</sub>		G <sub>8</sub>
0	1	0	0	0	0	1	1		G <sub>15</sub>		G <sub>14</sub>		G <sub>13</sub>		G <sub>12</sub>

Set G<sub>N</sub> = 0 for a gain of +1 or 1 for a gain of +2.

**Broadcast Mode**

The Broadcast Mode routes one input to all 16 outputs. The broadcast control word is:

**TABLE 6. BROADCAST FORMAT**

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	1	1	I <sub>4</sub>	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	0	0	0	0	0	0	0	Enable Broadcast 0: Broadcast Mode Disabled 1: Broadcast Mode Enabled

I<sub>4</sub>:I<sub>0</sub> form the 5 bit word indicating the input channel (0 to 31) to be sent to all 16 outputs. Set the Enable Broadcast bit (B0) = 1 to enable Broadcast Mode, or to 0 to disable Broadcast Mode. When Broadcast Mode is disabled, the previous channel assignments are restored.

**Control Word**

The ISL59534's power-on reset disables all outputs and places the part in a low-power standby mode. To enable the device, the following control word should be sent:

**TABLE 7. CONTROL WORD FORMAT**

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	0	0	Clamp 0: Clamp Disabled 1: Clamp Enabled	0	0	0	0	0	0	0	Power 0: Standby 1: Operational	Global Output Enable 0: All outputs tri-stated 1: Individual Output Enable bits control outputs

The Clamp bit enables the input clamp function, forcing the AC-coupled signal's most negative point to be equal to V<sub>REF</sub>.

**Note:** The Clamp bit turns the DC-Restore clamp function on or off for *all* channels - there is no DC-Restore on/off control for individual channels. The DC-Restore function only works with signals with sync tips (composite video). Signals that do

not have sync tips (the Chroma/C signal in s-video and the Pb, Pr signals in Component video), will be severely distorted if run through a DC-Restore/clamp function.

For this reason, the ISL59534 must be in DC-coupled mode (Clamp Disabled) to be compatible with s-video and component video signals.

### Bandwidth Considerations

Wide frequency response (high bandwidth) in a video system means better video resolution. Four sets of frequency response curves are shown in Figure 47. Depending on the switch configurations, and the routing (the path from the input to the output), bandwidth can vary between 100MHz and 350MHz. A short discussion of the trade-offs — including matrix configuration, output buffer gain selection, channel selection, and loading — follows.

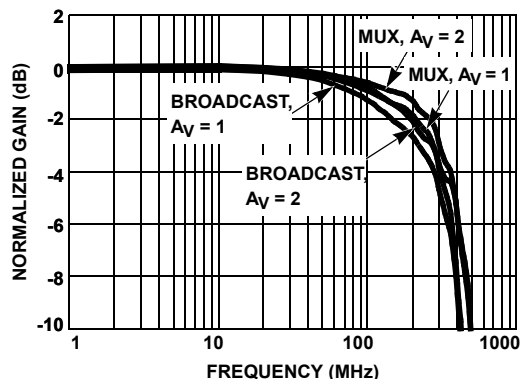


FIGURE 47. FREQUENCY RESPONSE FOR VARIOUS MODES

In multiplexer mode, one input typically drives one output channel, while in broadcast mode, one input drives all 16 outputs. As the number of outputs driven increases, the parasitic loading on that input increases. Broadcast Mode is the worst-case, where the capacitance of all 16 channels loads one input, reducing the overall bandwidth. In addition, due to internal device compensation, an output buffer gain of +2 has higher bandwidth than a gain of +1. Therefore, the highest bandwidth configuration is multiplexer mode (with each input mapped to only one output) and an output buffer gain of +2.

The relative locations of the input and output channels also have significant impact on the device bandwidth (due to the layout of the ISL59534 silicon). When the input and output channels are further away, there are additional parasitics as a result of the additional routing, resulting in lower bandwidth.

The bandwidth does not change significantly with resistive loading as shown in the typical performance curves. However several of the curves demonstrate that frequency response is sensitive to capacitance loading. This is most significant when laying out the PCB. If the PCB trace length between the output of the crosspoint switch and the back-termination resistor is not minimized, the additional parasitic capacitance will result in some peaking and eventually a reduction in overall bandwidth.

### Linear Operating Region

In addition to bandwidth optimization, to get the best linearity the ISL59534 should be configured to operate in its most linear operating region. Figure 48 shows the differential gain curve. The ISL59534 is a single supply 5V design with its most linear region between 0.1 and 2V. This range is fine for most video signals whose nominal signal amplitude is 1V. The most negative input level (the sync tip for composite video) should be maintained at 0.3V or above for best operation.

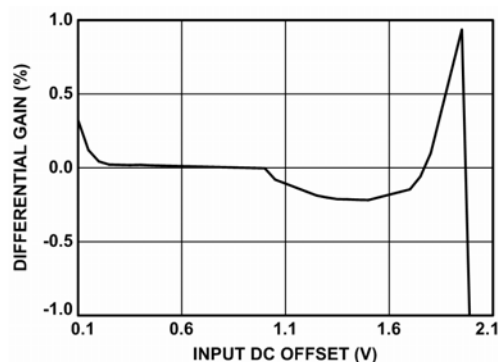


FIGURE 48. DIFFERENTIAL GAIN RESPONSE

In a DC-coupled application, it is the system designer's responsibility to ensure that the video signal is always in the optimum range.

When AC coupling, the ISL59534's Clamp (also called "DC restore") function automatically and continuously adjusts the DC level so that the most negative portion of the video is always equal to  $V_{REF}$ .

A discussion of the benefits of the DC restoration function begins by understanding the Clamp circuit shown in Figure 49. The incoming video signal is typically terminated into  $75\Omega$ , then AC coupled through  $C_1$ , at which point it is connected to the base of the buffer's diff pair. These components form the video path.

The Clamp function consists of  $Q_1$ ,  $D_1$ ,  $Q_2$ ,  $D_2$ , the two current sources, and the 3 switches controlled by the Clamp Enable signal. The  $V_{REF}$  voltage is level-shifted up two diode drops ( $Q_1$  and  $D_1$ ) to the base of  $Q_2$ . If the voltage at the cathode of  $D_2$  goes below  $V_{REF}$ ,  $Q_2$  and  $D_2$  will turn on, keeping the  $IN_x$  voltage at  $V_{REF}$ . If the voltage at  $IN_x$  is greater than  $V_{REF}$ ,  $Q_2$  and  $D_2$  are off and the  $IN_x$  node is high impedance. This is how the clamp function forces the lowest portion of the video signal (the sync tip) to always be equal to or greater than  $V_{REF}$ .

To make sure that the sync tip is always *equal to* (not equal to or greater than)  $V_{REF}$ ,  $i_1$  is constantly sinking  $\sim 2\mu A$  of current from  $C_1$ . This causes each sync tip to be slightly lower voltage than the previous sync tip, causing  $Q_2$  and  $D_2$  to turn on at each sync tip and raise the voltage to  $V_{REF}$ . The  $2\mu A$  pulldown with a  $0.1\mu F$  capacitor and a  $15kHz$  HSYNC frequency results in  $1.3mV$  of "droop" across every line, or

0.2% of the video signal. Because 1.3mV is only 0.2% of a 0.7V video signal, this droop is imperceptible to the human eye.

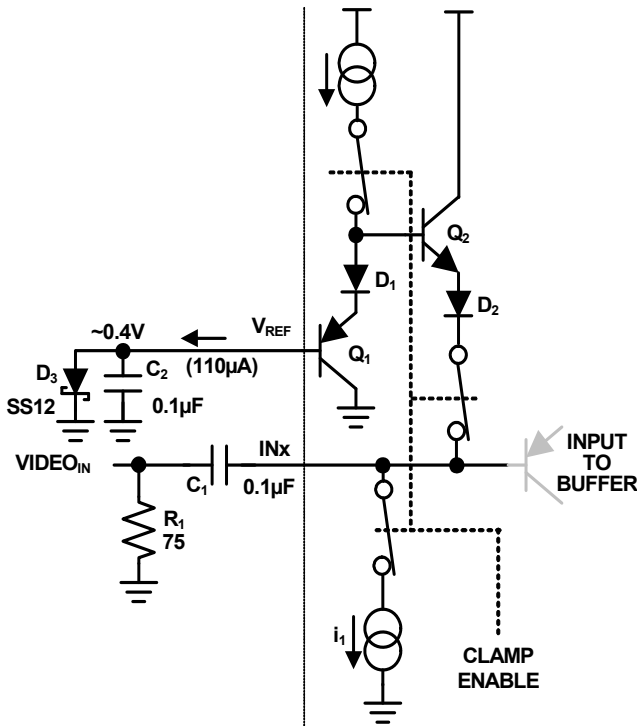


FIGURE 49. DC RESTORE BLOCK DIAGRAM

This is how the video is “DC-restored” after being AC coupled into the ISL59534. The sync tip voltage will be equal to  $V_{REF}$  on the right side of  $C_1$ , regardless of the DC level of the video on the left side of  $C_1$ . Due to various sources of offset in the actual clamp function, the actual sync tip level is typically about 75mV higher than  $V_{REF}$  (for  $V_{REF} = 0.4V$ ).

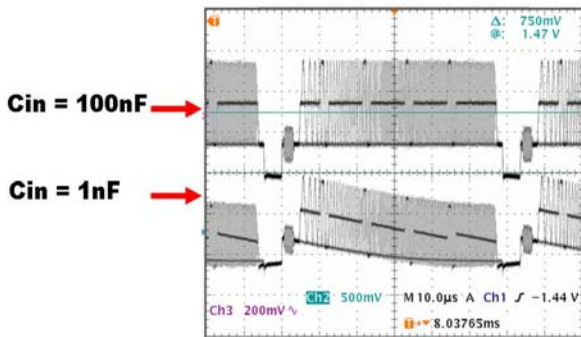


FIGURE 50. DC RESTORE VIDEO WAVEFORMS

It is important to choose the correct value for  $C_{IN}$ . Too small a value will generate too much droop, and the image will be visibly darker on the right than on the left. A  $C_{IN}$  value that is too large may cause the clamp to fail to converge. The droop rate ( $dV/dt$ ) is  $i_1/C_{IN}$  volts/second. In general, the droop voltage should be limited to  $<1$  IRE over a period of one line of video; so for 1 IRE = 7mV,  $I_B = 10\mu A$  maximum, and an NTSC waveform we will set  $C_{IN} > 10\mu A * 60\mu s / 7mV = 0.086\mu F$ . Figure 50 shows the result of  $C_{IN} = 0.1\mu F$

delivering acceptable droop and  $C_{IN} = 0.001\mu F$  producing excessive droop.

When the clamp function is disabled in the CONTROL register (Clamp = 0) to allow DC-coupled operation, the  $I_{CLAMP}$  current sinks/sources are disabled and the input passes through the DC Restore block unaffected. In this application  $V_{REF}$  may be tied to GND.

**Overlay Operation**

The ISL59534 features an overlay feature, that allows an external video signal or DC level to be inserted in place of that output channel’s video. When the  $OVER_N$  signal is taken high, the output signal on the  $OUT_N$  pin is replaced with the signal on the  $VOVER_N$  pin.

There are several ways the overlay feature can be used. Toggling the  $OVER_N$  signal at the frame rate or slower will replace the video frame(s) on the  $OUT_N$  pin with the video supplied on the  $VOVER_N$  pin.

Another option (for OSD displays, for example), is to put a DC level on the  $VOVER_N$  line and toggle the  $OVER_N$  signal at the pixel rate to create a monicolor image “overlaid” on channel N’s output signal.

Finally, by enabling the  $OVER_N$  signal for some portion of each line over a certain amount of lines, a picture-in-picture function can be constructed.

It’s important to note that the overlay inputs do not have the DC Restore function previously described - the overlay signal is DC coupled into the output. It is the system designer’s responsibility to ensure that the video levels are in the ISL59534’s linear region and matching the output channel’s offset and amplitude. One easy way to do this is to run the video to be overlaid through one of the ISL59534’s unused channels and then into the  $VOVER_N$  input.

The  $OVER_N$  pins all have weak pull-downs, so if they are unused, they can either be left unconnected or tied to GND.

**Power Dissipation and Thermal Resistance**

With a large number of switches, it is possible to exceed the  $+150^\circ C$  absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the crosspoint switch in a safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}} \tag{EQ. 1}$$

Where:

- $T_{JMAX}$  = Maximum junction temperature = +125°C
- $T_{AMAX}$  = Maximum ambient temperature = +85°C
- $\theta_{JA}$  = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^n (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}} \quad (\text{EQ. 2})$$

Where:

- $V_S$  = Supply voltage = 5V
- $I_{SMAX}$  = Maximum quiescent supply current = 505mA
- $V_{OUT}$  = Maximum output voltage of the application = 2V
- $R_{LOAD}$  = Load resistance tied to ground = 150
- $n = 1$  to 16 channels

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^n (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}} = 3.2W \quad (\text{EQ. 3})$$

The required  $\theta_{JA}$  to dissipate 3.2W is:

$$\theta_{JA} = \frac{T_{JMAX} - T_{AMAX}}{PD_{MAX}} = 12.5(^{\circ}C/W) \quad (\text{EQ. 4})$$

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9001 quality systems. Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

*Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

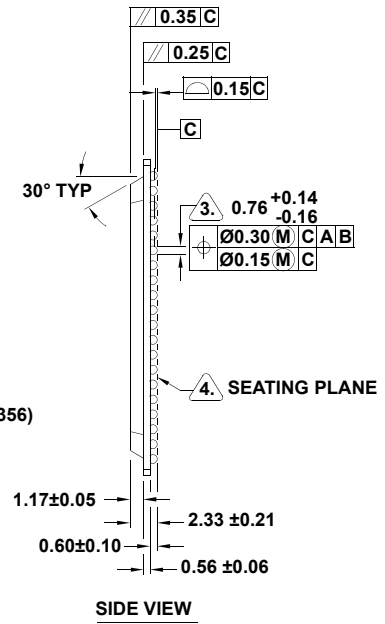
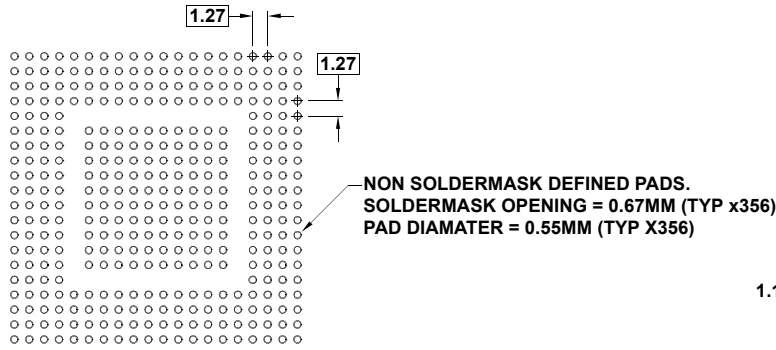
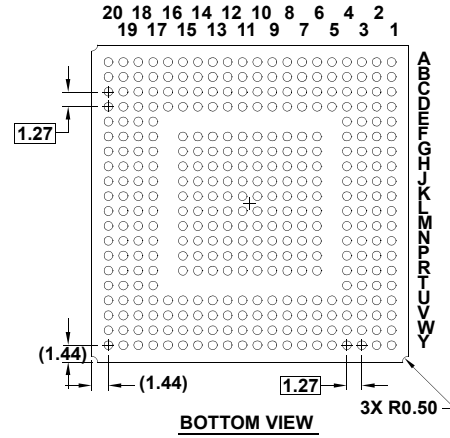
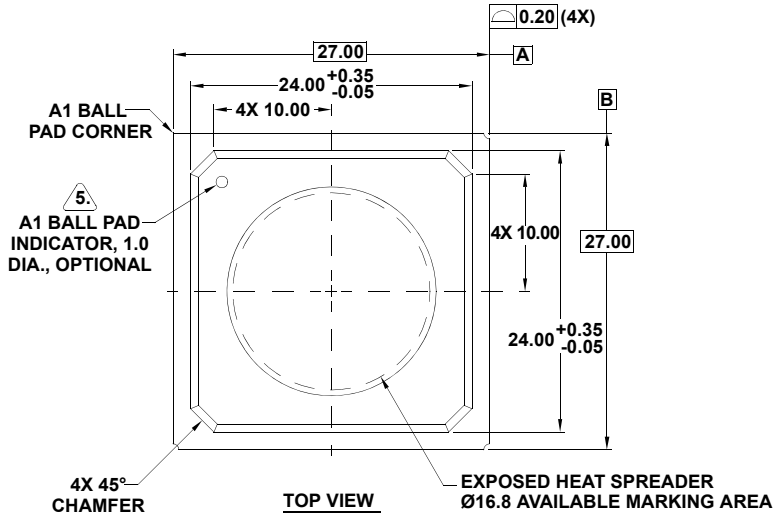
For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)

# Package Outline Drawing

## V356.27x27C

356 BALL HEATSINK PLASTIC BALL GRID ARRAY PACKAGE (HPBGA)

Rev 1, 6/10



**NOTES:**

1. All dimensions and tolerances conform to ASME Y14.5m-1994.
2. Dimensions are in millimeters.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. A1 ball pad corner I.D. for plate mold: To be marked by ink. Auto mold: Dimple to be formed by mold cap.
6. Reference specifications: This drawing conforms to JEDEC registered outline MS-034/A variation BAL-2.