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Multiphase PWM Regulator for AMD Fusion™ Mobile CPUs Using SVI 2.0

ISL62773A

The ISL62773A is fully compliant with AMD Fusion™ SVI 2.0 and provides a complete solution for microprocessor and graphics processor core power. The ISL62773A controller supports two Voltage Regulators (VRs) with three integrated gate drivers and two optional external drivers for maximum flexibility. The Core VR can be configured for 3-, 2-, or 1-phase operation while the Northbridge VR supports 2- or 1-phase configurations. The two VRs share a serial control bus to communicate with the AMD CPU and achieve lower cost and smaller board area compared with two-chip solutions.

The PWM modulator is based on Intersil's Robust Ripple Regulator R3™ Technology. Compared to traditional modulators, the R3™ modulator can automatically change switching frequency for faster transient settling time during load transients and improved light load efficiency.

The ISL62773A has several other key features. Both outputs support DCR current sensing with single NTC thermistor for DCR temperature compensation or accurate resistor current sensing. Both outputs utilize remote voltage sense, adjustable switching frequency, OC protection and power-good.

Applications

- AMD Fusion CPU/GPU core power
- Notebook computers

Features

- Supports AMD SVI 2.0 serial data bus interface
  - Serial VID clock frequency range 100kHz to 25MHz
- Dual output controller with integrated drivers
  - Two dedicated core drivers
  - One programmable driver for either Core or Northbridge
- Precision voltage regulation
  - 0.5% system accuracy over-temperature
  - 0.5V to 1.55V in 6.25mV steps
  - Enhanced load line accuracy
- Supports multiple current sensing methods
  - Lossless inductor DCR current sensing
  - Precision resistor current sensing
- Programmable 1-, 2- or 3-phase for the core output and 1- or 2-phase for the Northbridge output
- Adaptive body diode conduction time reduction
- Superior noise immunity and transient response
- Output current and voltage telemetry
- Differential remote voltage sensing
- High efficiency across entire load range
- Programmable slew rate
- Programmable VID offset and droop on both outputs
- Programmable switching frequency for both outputs
- Excellent dynamic current balance between phases
- Protection: OCP/WOC, OVP, PGOOD and thermal monitor
- Small footprint 48 Ld 6x6 QFN package
  - Pb-free (RoHS compliant)

Core Performance

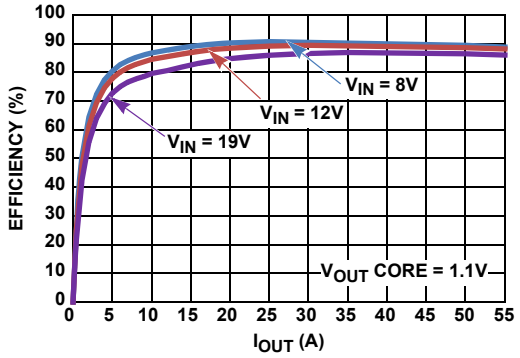


FIGURE 1. EFFICIENCY vs LOAD

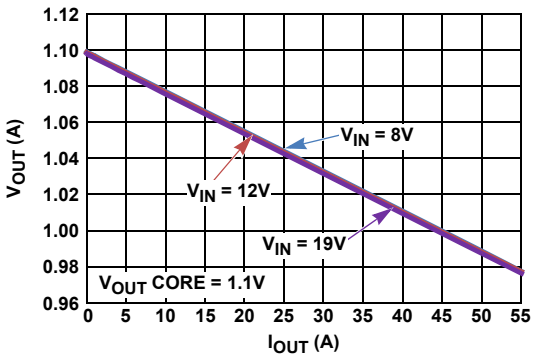


FIGURE 2. V_{OUT} vs LOAD

Table of Contents

Simplified Application Circuit for High Power CPU Core

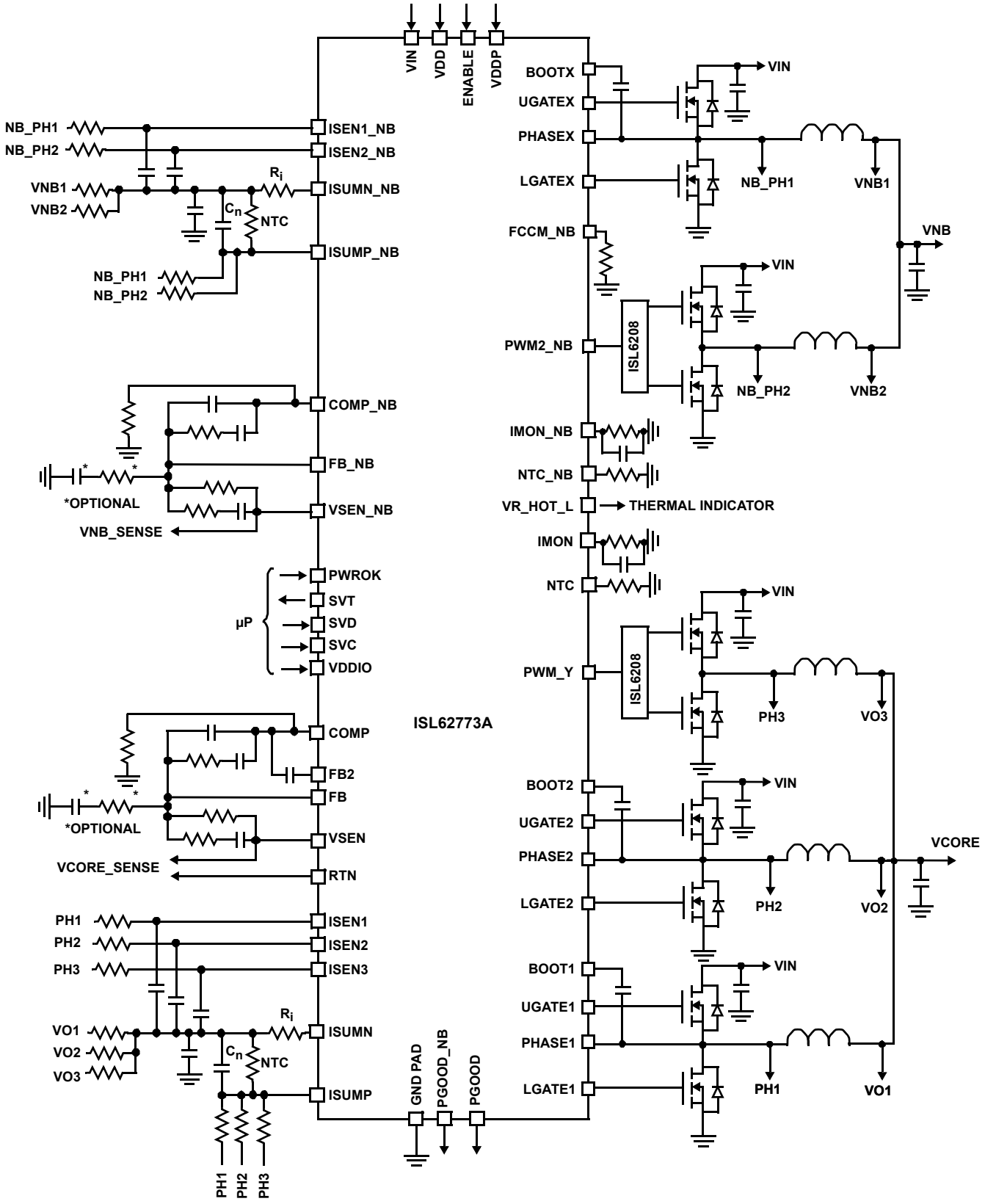


FIGURE 3. TYPICAL APPLICATION CIRCUIT USING INDUCTOR DCR SENSING

Simplified Application Circuit with 3 Internal Drivers Used for Core

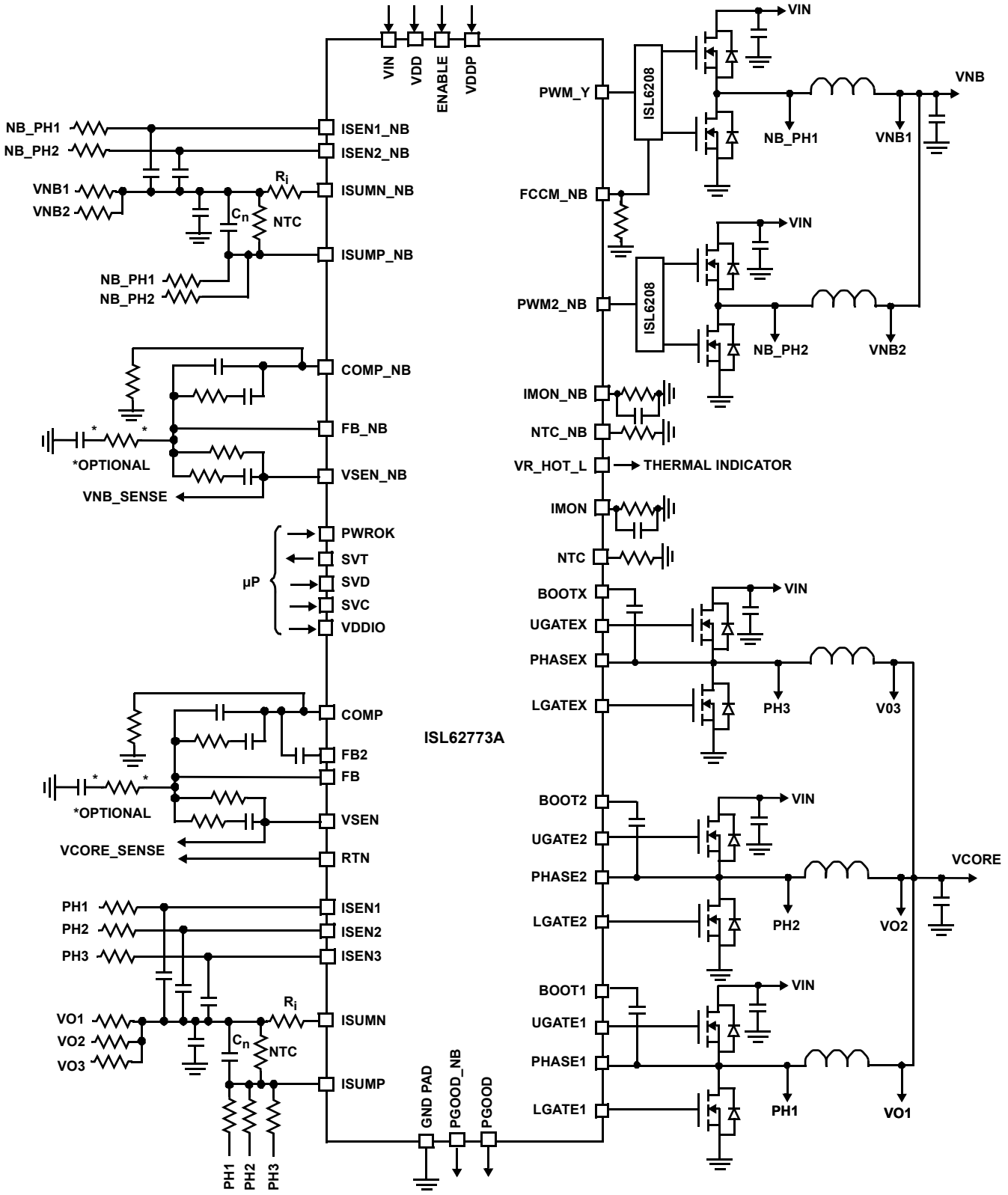


FIGURE 4. TYPICAL APPLICATION CIRCUIT USING INDUCTOR DCR SENSING

Simplified Application Circuit for Mid-Power CPUs [2+1 Configuration]

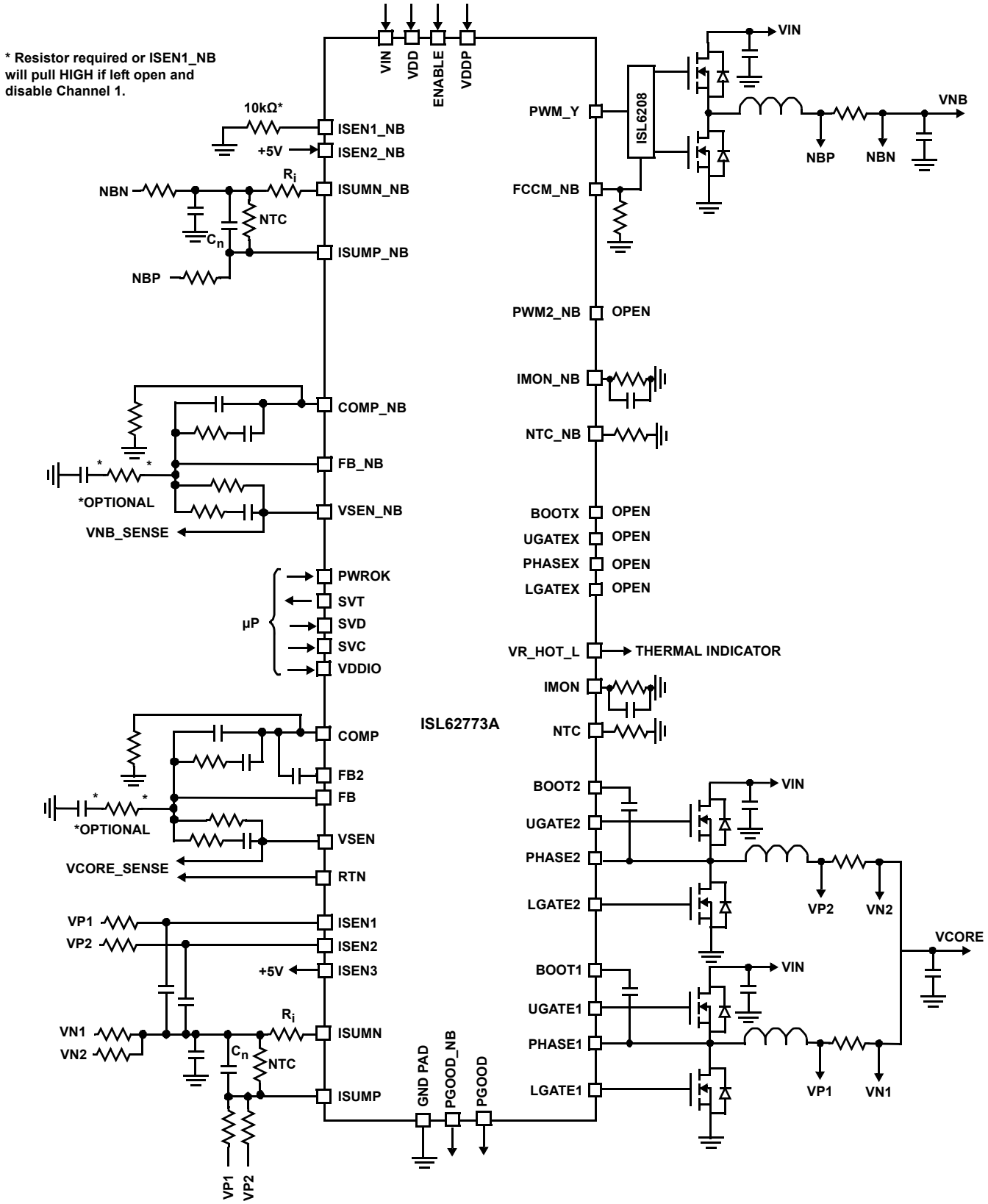


FIGURE 5. TYPICAL APPLICATION CIRCUIT USING RESISTOR SENSING

Simplified Application Circuit for Low Power CPUs [1+1 Configuration]

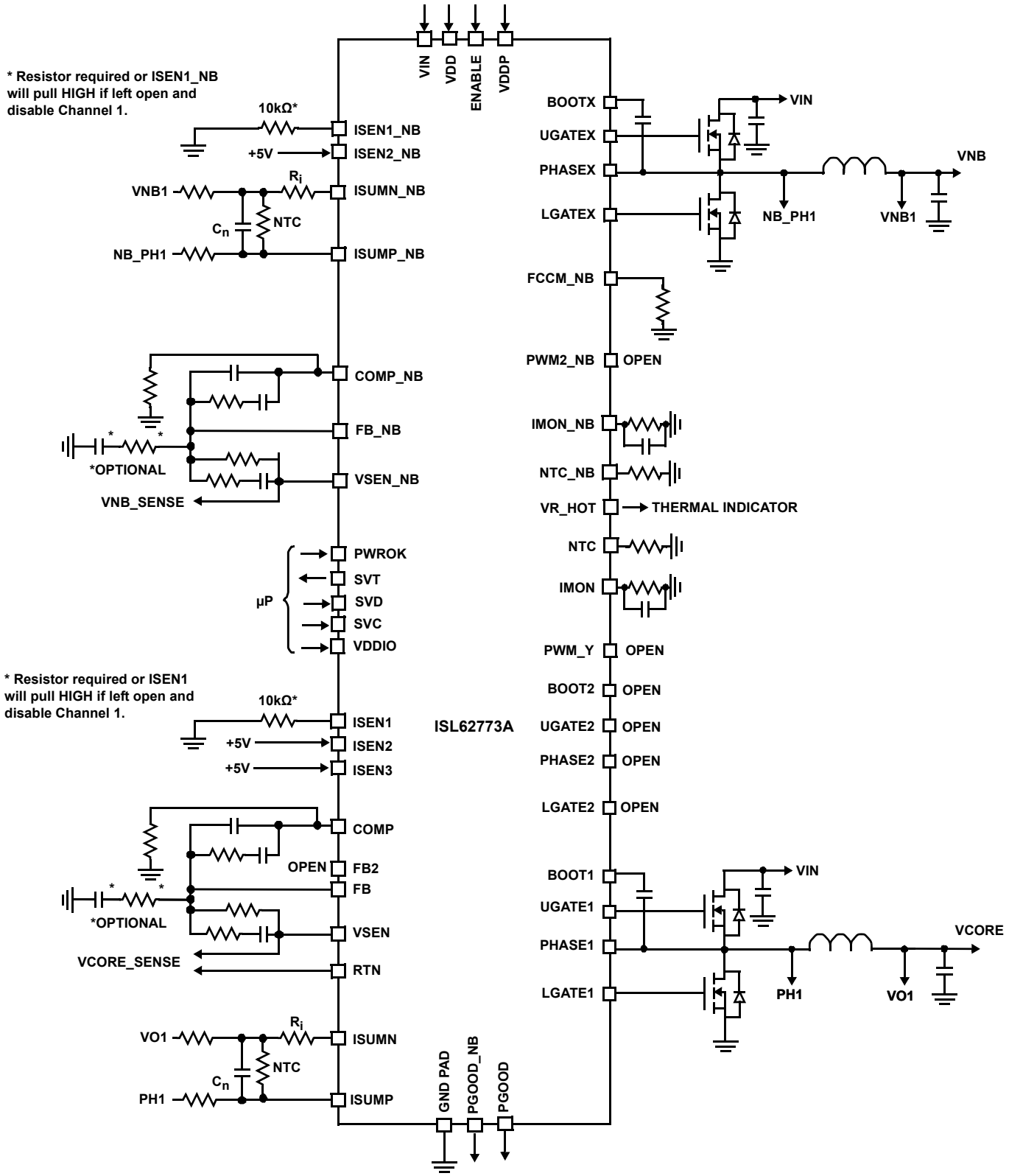


FIGURE 6. TYPICAL APPLICATION CIRCUIT USING INDUCTOR DCR SENSING

Block Diagram

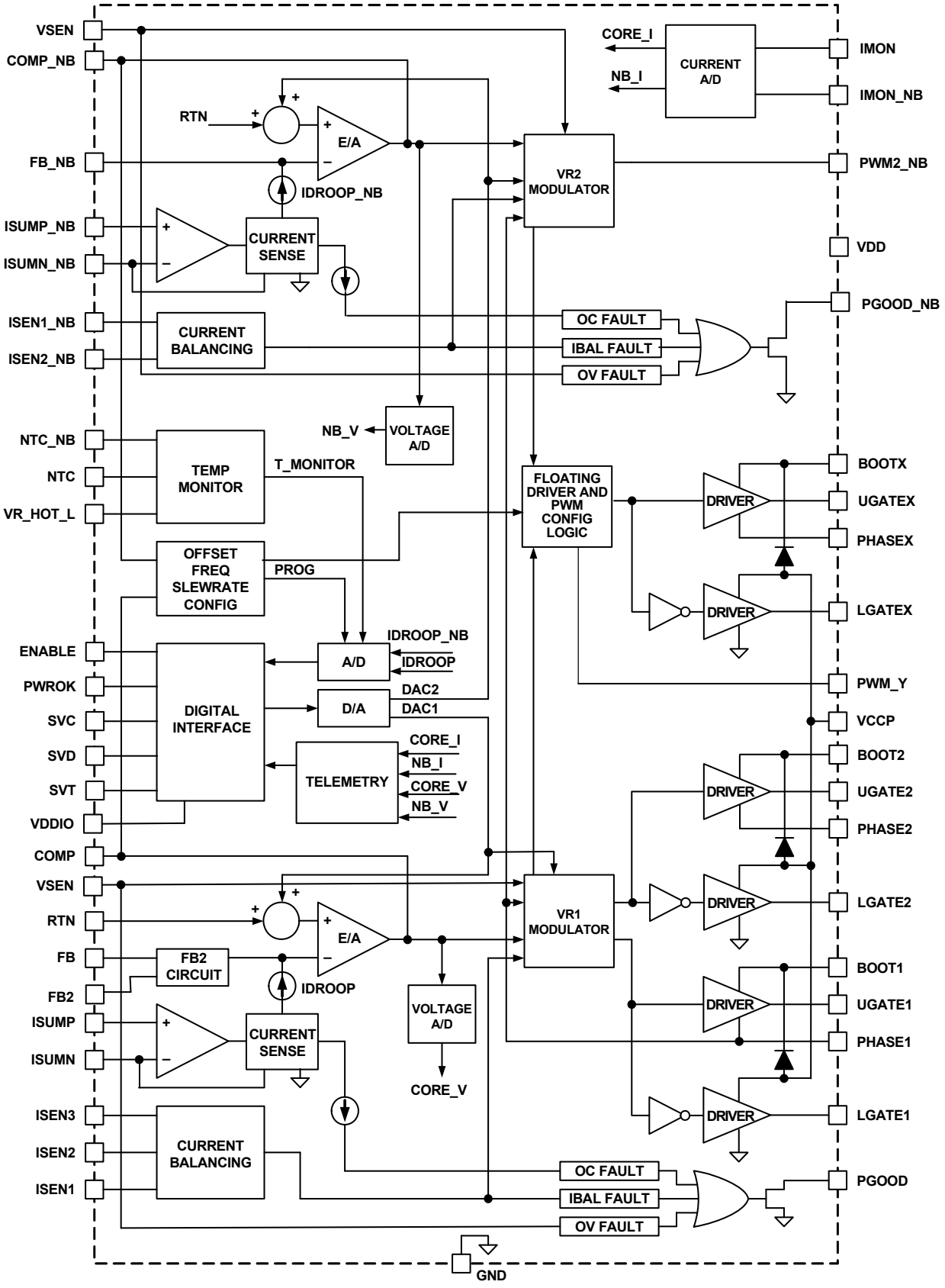
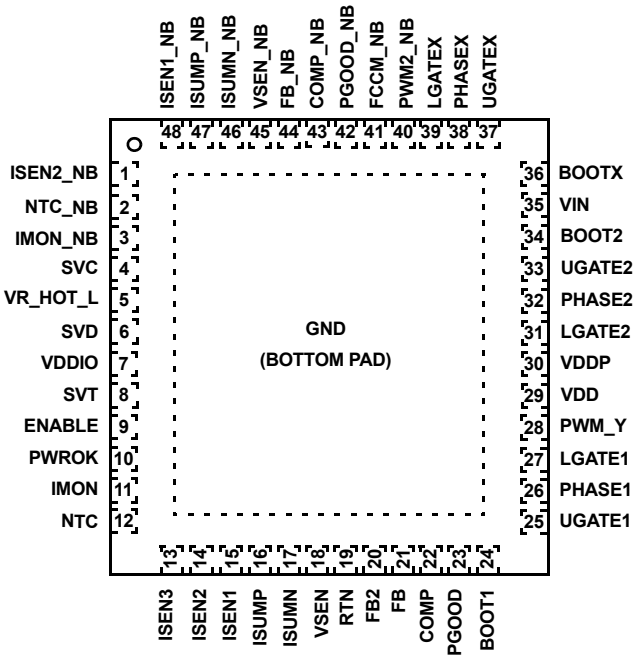


FIGURE 7. BLOCK DIAGRAM

Pin Configuration

ISL62773A
(48 LD QFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	ISEN2_NB	Individual current sensing for Channel 2 of the Northbridge VR. When ISEN2_NB is pulled to +5V, the controller will disable Channel 2 and the Northbridge VR will run single-phase.
2	NTC_NB	Thermistor input to VR_HOT_L circuit to monitor Northbridge VR temperature.
3	IMON_NB	Northbridge output current monitor. A current proportional to the Northbridge VR output current is sourced from this pin.
4	SVC	Serial VID clock input from the CPU processor master device.
5	VR_HOT_L	Thermal indicator signal to AMD CPU. Thermal overload open-drain output indicator active LOW.
6	SVD	Serial VID data bidirectional signal from the CPU processor master device to the VR.
7	VDDIO	VDDIO is the processor memory interface power rail and this pin serves as the reference to the controller IC for this processor I/O signal level.
8	SVT	Serial VID Telemetry (SVT) data line input to the CPU from the controller IC. Telemetry and VID-on-the-fly complete signal provided from this pin.
9	ENABLE	Enable input. A high level logic on this pin enables both VRs.
10	PWROK	System power-good input. When this pin is high, the SVI 2 interface is active and the I^2C protocol is running. While this pin is low, the SVC and SVD input states determine the pre-PWROK metal VID. This pin must be low prior to the ISL62773A PGOOD output going high per the AMD SVI 2.0 Controller Guidelines.
11	IMON	Core output current monitor. A current proportional to the Core VR output current is sourced from this pin.
12	NTC	Thermistor input to VR_HOT_L circuit to monitor Core VR temperature.
13	ISEN3	ISEN3 is the individual current sensing for Channel 3. When ISEN3 is pulled to +5V, the controller disables Channel 3, and the Core VR runs in two-phase mode.
14	ISEN2	Individual current sensing for Channel 2 of the Core VR. When ISEN2 is pulled to +5V, the controller disables Channel 2 and the Core VR runs in single-phase mode.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
15	ISEN1	Individual current sensing for Channel 1 of the Core VR. If ISEN2 is tied to +5V, this pin cannot be left open and must be tied to GND with a 10kΩ resistor. If ISEN1 is tied to +5V, the core portion of the IC is shut down.
16	ISUMP	Noninverting input of the transconductance amplifier for current monitor and load line of core output.
17	ISUMN	Inverting input of the transconductance amplifier for current monitor and load line of core output.
18	VSEN	Output voltage sense pin for the core controller. Connect to the +sense pin of the microprocessor die.
19	RTN	Output voltage sense return pin for both Core VR and Northbridge VR. Connect to the -sense pin of the microprocessor die.
20	FB2	There is a switch between the FB2 pin and the FB pin. The switch is on in 2-phase or 3-phase mode and is off in 1-phase mode. The components connecting to FB2 are used to adjust the compensation in 1-phase mode of the Core VR to achieve optimum performance.
21	FB	Output voltage feedback to the inverting input of the core controller error amplifier.
22	COMP	Core controller error amplifier output. A resistor from COMP to GND sets the Core VR offset voltage.
23	PGOOD	Open-drain output to indicate the core portion of the IC is ready to supply regulated voltage. Pull-up externally to VDD or 3.3V through a resistor.
24	BOOT1	Connect an MLCC capacitor across the BOOT1 and the PHASE1 pins. The boot capacitor is charged, through an internal boot diode connected from the VDDP pin to the BOOT1 pin, each time the PHASE1 pin drops below VDDP minus the voltage dropped across the internal boot diode.
25	UGATE1	Output of the Phase 1 high-side MOSFET gate driver of the Core VR. Connect the UGATE1 pin to the gate of the Phase 1 high-side MOSFET(s).
26	PHASE1	Current return path for the Phase 1 high-side MOSFET gate driver of VR1. Connect the PHASE1 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain and the output inductor of Phase 1.
27	LGATE1	Output of the Phase 1 low-side MOSFET gate driver of the Core VR. Connect the LGATE1 pin to the gate of the Phase 1 low-side MOSFET(s).
28	PWM_Y	Floating PWM output used for either Channel 3 of the Core VR or Channel 1 of the Northbridge VR depending on the FCCM_NB resistor connected between FCCM_NB and GND.
29	VDD	5V bias power. A resistor [2Ω] and a decoupling capacitor should be used from the +5V supply. A high quality, X7R dielectric MLCC capacitor is recommended.
30	VDDP	Input voltage bias for the internal gate drivers. Connect +5V to the VDDP pin. Decouple with at least 1µF of capacitance to GND. A high quality, X7R dielectric MLCC capacitor is recommended.
31	LGATE2	Output of the Phase 2 low-side MOSFET gate driver of the Core VR. Connect the LGATE2 pin to the gate of the Phase 2 low-side MOSFET(s).
32	PHASE2	Current return path for the Phase 2 high-side MOSFET gate driver of the Core VR. Connect the PHASE2 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain and the output inductor of Phase 2.
33	UGATE2	Output of the Phase 2 high-side MOSFET gate driver of the Core VR. Connect the UGATE2 pin to the gate of the Phase 2 high-side MOSFET(s).
34	BOOT2	Connect an MLCC capacitor across the BOOT2 and PHASE2 pins. The boot capacitor is charged, through an internal boot diode connected from the VDDP pin to the BOOT2 pin, each time the PHASE2 pin drops below VDDP minus the voltage dropped across the internal boot diode.
35	VIN	Battery supply voltage, used for feed-forward.
36	BOOTX	Boot connection of the programmable internal driver used for either Channel 3 of the Core VR or Channel 1 of the Northbridge VR based on the configuration state selected by the FCCM_NB resistor. Connect an MLCC capacitor across the BOOT1X and the PHASEX pins. The boot capacitor is charged, through an internal boot diode connected from the VDDP pin to the BOOTX pin, each time the PHASEX pin drops below VDDP minus the voltage dropped across the internal boot diode.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
37	UGATEX	High-side MOSFET gate driver portion of the programmable internal driver used for either Channel 3 of the Core VR or Channel 1 of the Northbridge VR based on the configuration state selected by the FCCM_NB resistor. Connect the UGATEX pin to the gate of the high-side MOSFET(s) for either Phase 3 of the Core VR or Phase 1 of the Northbridge VR based on the configuration state selected.
38	PHASEX	Phase connection of the programmable internal driver used for either Channel 3 of the Core VR or Channel 1 of the Northbridge VR based on the configuration state selected by the FCCM_NB resistor. Current return path for the high-side MOSFET gate driver of the floating internal driver. Connect the PHASEX pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain and the output inductor of either Phase 3 of the Core VR or Phase 1 of the Northbridge VR based on the configuration state selected.
39	LGATEX	Low-side MOSFET gate driver portion of floating internal driver used for either Channel 3 of the Core VR or Channel 1 of the Northbridge VR based on the configuration state selected by the FCCM_NB resistor. Connect the LGATEX pin to the gate of the low-side MOSFET(s) for either Phase 3 of the Core VR or Phase 1 of the Northbridge VR based on the configuration state selected.
40	PWM2_NB	PWM output for Channel 2 of the Northbridge VR. Disabled when ISEN2_NB is tied to +5V.
41	FCCM_NB	Diode emulation control signal for Intersil MOSFET Drivers. When FCCM_NB is LOW, diode emulation at the driver this pin connects to is allowed. A resistor from FCCM_NB pin to GND configures the PWM_Y and floating internal gate driver [BOOTX, UGATEX, PHASEX, LGATEX pins] to support Phase 3 of the Core VR and Phase 1 of the Northbridge VR. The FCCM_NB resistor value also is used to set the slew rate for the Core VR and Northbridge VR. A capacitor place holder from the FCCM_NB pin to GND is recommended for filtering noise on this pin due to layout.
42	PGOOD_NB	Open-drain output to indicate the Northbridge portion of the IC is ready to supply regulated voltage. Pull up externally to VDDP or 3.3V through a resistor.
43	COMP_NB	Northbridge VR error amplifier output. A resistor from COMP_NB to GND sets the Northbridge VR offset voltage and is used to set the switching frequency for the Core VR and Northbridge VR.
44	FB_NB	Output voltage feedback to the inverting input of the Northbridge controller error amplifier.
45	VSEN_NB	Output voltage sense pin for the Northbridge controller. Connect to the +sense pin of the microprocessor die.
46	ISUMN_NB	Inverting input of the transconductance amplifier for current monitor and load line of the Northbridge VR.
47	ISUMP_NB	Noninverting input of the transconductance amplifier for current monitor and load line of the Northbridge VR.
48	ISEN1_NB	Individual current sensing for Channel 1 of the Northbridge VR. If ISEN2_NB is tied to +5V, this pin cannot be left open and must be tied to GND with a 10kΩ resistor. If ISEN1_NB is tied to +5V, the Northbridge portion of the IC is shutdown.
	GND (Bottom Pad)	Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pin.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL62773AHRZ	62773A HRZ	-10 to +100	48 Ld 6x6 QFN	L48.6x6B
ISL62773AIRZ	62773A IRZ	-40 to +100	48 Ld 6x6 QFN	L48.6x6B

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL62773A. For more information on MSL please see tech brief TB363.

Absolute Maximum Ratings

Supply Voltage, V_{DD}, V_{DDP} . . . . . -0.3V to +7V
Battery Voltage, V_{IN} . . . . . +28V
Boot Voltage (BOOT) . . . . . -0.3V to +33V
Boot to Phase Voltage (BOOT-PHASE) . . . . . -0.3V to +7V (DC)
-0.3V to +9V (<10ns)
Phase Voltage (PHASE) . . . . . -7V (<20ns Pulse Width, 10µJ)
UGATE Voltage (UGATE) . . . . . PHASE - 0.3V (DC) to BOOTPHASE - 5V
(<20ns Pulse Width, 10µJ) to BOOT LGATE Voltage
-2.5V (<20ns Pulse Width, 5µJ) to VDD + 0.3V
All Other Pins . . . . . -0.3V to (VDD + 0.3V)
Open-Drain Outputs, PGOOD, PGOOD_NB, VR_HOT_L. . . . . -0.3V to +7V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
48 Ld QFN Package (Notes 4, 5)	29	3.5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Supply Voltage, V_{DD} . . . . . +5V ±5%
Battery Voltage, V_{IN} . . . . . 4.5V to 25V
Ambient Temperature . . . . . HRZ, -10°C to +100°C
IRZ, -40°C to +100°C
Junction Temperature . . . . . -10°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: V_{DD} = 5V, T_A = -10°C to +100°C (HRZ), T_A = -40°C to +100°C (IRZ), f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +100°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6))	UNIT
INPUT POWER SUPPLY						
+5V Supply Current	I_{VDD}	ENABLE = 1V		8	**11**	mA
		ENABLE = 0V			**1**	µA
Battery Supply Current	I_{VIN}	ENABLE = 0V			**1**	µA
V_{IN} Input Resistance	R_{VIN}	ENABLE = 1V		620		kΩ
POWER-ON-RESET THRESHOLDS						
VDD POR Threshold	VDD_POR_r	V_{DD} rising		4.35	**4.50**	V
	VDD_POR_f	V_{DD} falling	**4.00**	4.15		V
SYSTEM AND REFERENCES						
System Accuracy	HRZ %Error (V_{OUT})	No load; closed loop, active mode range, VID = 0.75V to 1.55V	-0.5		+0.5	%
		VID = 0.25V to 0.74375V	-10		+10	mV
	IRZ %Error (V_{OUT})	No load; closed loop, active mode range, VID = 0.75V to 1.55V	-0.8		+0.8	%
		VID = 0.25V to 0.74375V	-12		+12	mV
Maximum Output Voltage	$V_{OUT(max)}$	VID = [00000000]		1.55		V
Minimum Output Voltage	$V_{OUT(min)}$	VID = [11111111]		0		V
CHANNEL FREQUENCY						
Nominal Channel Frequency	$f_{SW(nom)}$		**280**	300	**320**	kHz
Adjustment Range			**300**		**450**	kHz
AMPLIFIERS						
Current-Sense Amplifier Input Offset	HRZ	I_{FB} = 0A	-0.15		+0.15	mV
	IRZ	I_{FB} = 0A	-0.20		+0.20	mV
Error Amp DC Gain	A_{V0}			119		dB
Error Amp Gain-Bandwidth Product	GBW	C_L = 20pF		17		MHz

Electrical Specifications

Operating Conditions: V_{DD} = 5V, T_A = -10°C to +100°C (HRZ), T_A = -40°C to +100°C (IRZ), f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6))	UNIT
ISEN						
Input Bias Current				20		nA
POWER-GOOD (PGOOD AND PGOOD_NB) AND PROTECTION MONITORS						
PGOOD Low Voltage	V_{OL}	I_{PGOOD} = 4mA			**0.4**	V
PGOOD Leakage Current	I_{OH}	PGOOD = 3.3V	**-1**		**1**	µA
PWROK High Threshold				750		mV
VR_HOT_L Pull-Down				11		Ω
PWROK Leakage Current					**1**	µA
VR_HOT_L Leakage Current					**1**	µA
GATE DRIVER						
UGATE Pull-Up Resistance	R_{UGPU}	200mA source current		1.0	**1.5**	Ω
UGATE Source Current	I_{UGSRC}	UGATE - PHASE = 2.5V		2		A
UGATE Sink Resistance	R_{UGPD}	250mA sink current		1.0	**1.5**	Ω
UGATE Sink Current	I_{UGSNK}	UGATE - PHASE = 2.5V		2		A
LGATE Pull-Up Resistance	R_{LGPU}	250mA source current		1.0	**1.5**	Ω
LGATE Source Current	I_{LGSRC}	LGATE - VSSP = 2.5V		2		A
LGATE Sink Resistance	R_{LGPD}	250mA sink current		0.5	**0.9**	Ω
LGATE Sink Current	I_{LGSNK}	LGATE - VSSP = 2.5V		4		A
UGATE to LGATE Dead Time	t_{UGFLGR}	UGATE falling to LGATE rising, no load		23		ns
LGATE to UGATE Dead Time	t_{LGFUGR}	LGATE falling to UGATE rising, no load		28		ns
PROTECTION						
Overvoltage Threshold	OV_H	VSEN rising above setpoint for >1µs	**275**	325	**375**	mV
Undervoltage Threshold	OV_H	VSEN falls below setpoint for >1µs	**275**	325	**375**	mV
Current Imbalance Threshold		One ISEN above another ISEN for >1.2ms		9		mV
Way Overcurrent Trip Threshold [IMONx Current Based Detection]	$IMONx_{WOC}$	All states, I_{DROOP} = 60µA, R_{IMON} = 135kΩ		15		µA
Overcurrent Trip Threshold [IMONx Voltage Based Detection]	V_{IMONx_OCP}	All states, I_{DROOP} = 45µA, I_{IMONx} = 11.25µA, R_{IMON} = 135kΩ	**1.485**	1.510	**1.535**	V
LOGIC THRESHOLDS						
ENABLE Input Low	V_{IL}				**1**	V
ENABLE Input High	V_{IH}	HRZ	1.6			V
	V_{IH}	IRZ	1.65			V
ENABLE Leakage Current	I_{ENABLE}	ENABLE = 0V	**-1**	0	**1**	µA
		ENABLE = 1V		18	**35**	µA
SVT Impedance				50		Ω
SVC, SVD Input Low	V_{IL}	% of VDDIO			**30**	%
SVC, SVD Input High	V_{IH}	% of VDDIO	70			%
SVC, SVD Leakage		ENABLE = 0V, SVC, SVD = 0V and 1V	**-1**		**1**	µA
		ENABLE = 1V, SVC, SVD = 1V	**-5**		**1**	µA
		ENABLE = 1V, SVC, SVD = 0V	**-35**	-20	**-5**	µA
PWM						
PWM Output Low	V_{0L}	Sinking 5mA			**1.0**	V
PWM Output High	V_{0H}	Sourcing 5mA	**3.5**			V
PWM Tri-State Leakage		PWM = 2.5V		1		µA

Electrical Specifications Operating Conditions: V_{DD} = 5V, T_A = -10°C to +100°C (HRZ), T_A = -40°C to +100°C (IRZ), f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6))	UNIT
THERMAL MONITOR						
NTC Source Current		NTC = 0.6V	**27**	30	**33**	µA
NTC Thermal Warning Voltage			**600**	640	**680**	mV
NTC Thermal Warning Voltage Hysteresis				20		mV
NTC Thermal Shutdown Voltage			**530**	580	**630**	mV
SLEW RATE						
VID-on-the-Fly Slew Rate		Maximum programmed	**16**	20	**24**	mV/µs
		Minimum programmed	**8**	10	**12**	mV/µs

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Gate Driver Timing Diagram

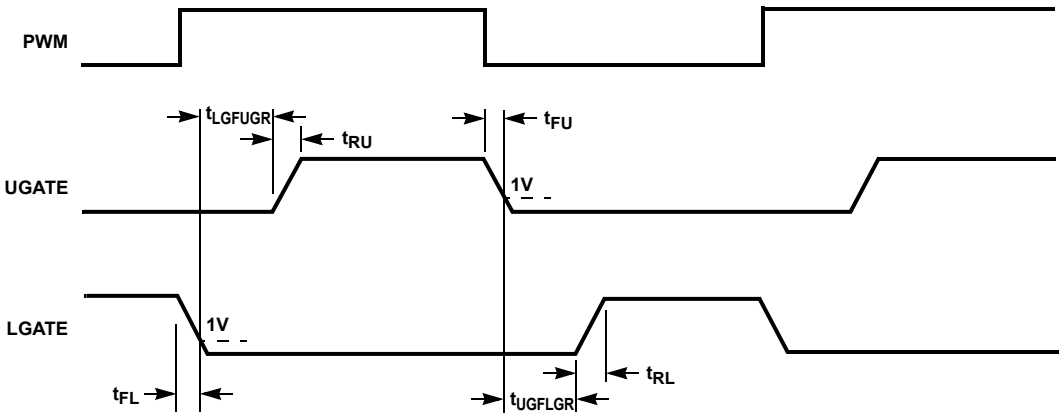


FIGURE 8. GATE DRIVER TIMING DIAGRAM

Theory of Operation

Multiphase R3™ Modulator

The ISL62773A is a multiphase regulator implementing two voltage regulators, CORE VR and Northbridge (NB) VR, on one chip controlled by AMD's™ SVI2™ protocol. The CORE VR can be programmed for 1-, 2- or 3-phase operation. The Northbridge VR can be configured for 1- or 2-phase operation. Both regulators use the Intersil patented R3™ (Robust Ripple Regulator) Modulator. The R3™ Modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. Figure 9 conceptually shows the multiphase R3™ Modulator circuit, and Figure 10 shows the operation principles.

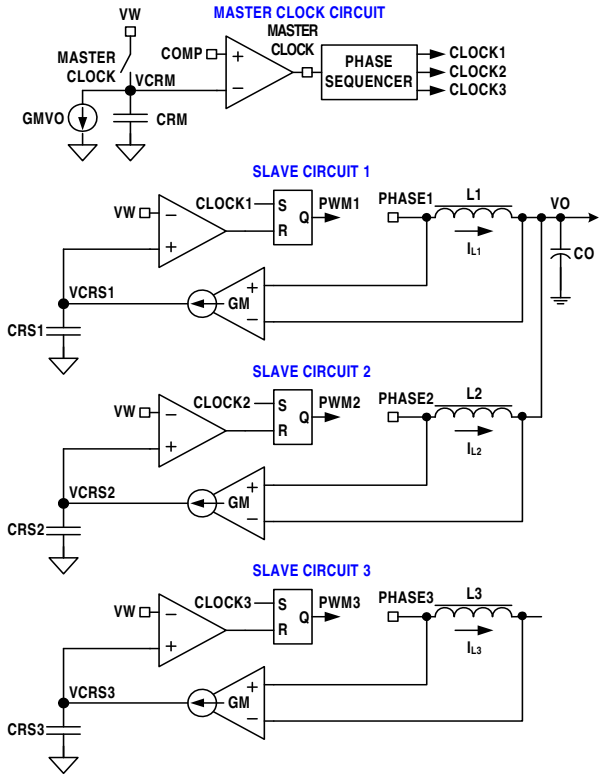


FIGURE 9. R3™ MODULATOR CIRCUIT

Inside the IC, the modulator uses the master clock circuit to generate the clocks for the slave circuits. The modulator discharges the ripple capacitor C_{rm} with a current source equal to $g_m V_o$, where g_m is a gain factor. C_{rm} voltage, V_{CRM}, is a sawtooth waveform traversing between the VW and COMP voltages. It resets to VW when it hits COMP and generates a one-shot master clock signal. A phase sequencer distributes the master clock signal to the slave circuits. If the CORE VR is in 3-phase mode, the master clock signal is distributed to the three phases, and the Clock 1~3 signals will be 120° out-of-phase. If the Core VR is in 2-phase mode, the master clock signal is distributed to Phases 1 and 2, and the Clock1 and Clock2 signals will be 180° out-of-phase. If the Core VR is in 1-phase mode, the master clock signal will be distributed to Phase 1 only and be the Clock1 signal.

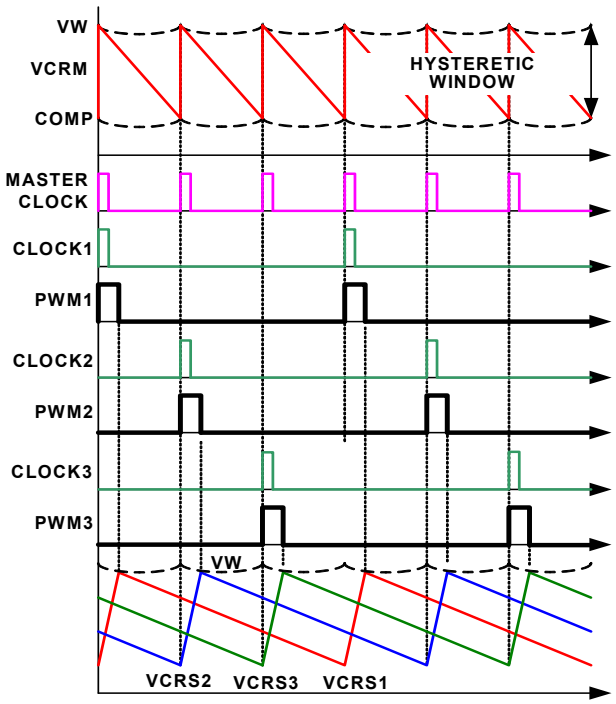


FIGURE 10. R3™ MODULATOR OPERATION PRINCIPLES IN STEADY STATE

Each slave circuit has its own ripple capacitor C_{rs}, whose voltage mimics the inductor ripple current. A g_m amplifier converts the inductor voltage into a current source to charge and discharge C_{rs}. The slave circuit turns on its PWM pulse upon receiving the clock signal, and the current source charges C_{rs}. When C_{rs} voltage V_{Crs} hits VW, the slave circuit turns off the PWM pulse, and the current source discharges C_{rs}.

Since the controller works with V_{crs}, which are large amplitude and noise-free synthesized signals, it achieves lower phase jitter than conventional hysteretic mode and fixed PWM mode controllers. Unlike conventional hysteretic mode converters, the error amplifier allows the ISL62773A to maintain a 0.5% output voltage accuracy.

Figure 11 shows the operation principles during load insertion response. The COMP voltage rises during load insertion, generating the master clock signal more quickly, so the PWM pulses turn on earlier, increasing the effective switching frequency. This allows for higher control loop bandwidth than conventional fixed frequency PWM controllers. The VW voltage rises as the COMP voltage rises, making the PWM pulses wider. During load release response, the COMP voltage falls. It takes the master clock circuit longer to generate the next master clock signal so the PWM pulse is held off until needed. The VW voltage falls as the COMP voltage falls, reducing the current PWM pulse width. This kind of behavior gives the ISL62773A excellent response speed.

The fact that all the phases share the same VW window voltage also ensures excellent dynamic current balance among phases.

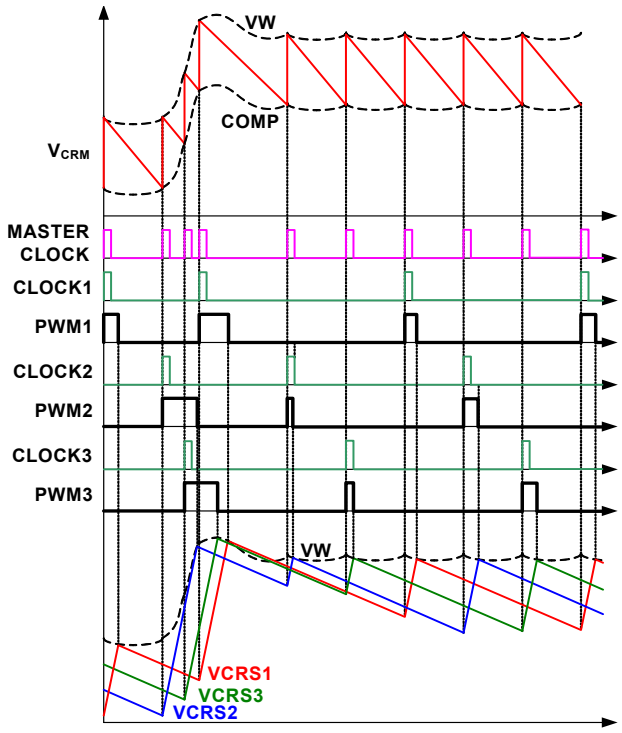


FIGURE 11. R3™ MODULATOR OPERATION PRINCIPLES IN LOAD INSERTION RESPONSE

Diode Emulation and Period Stretching

The ISL62773A can operate in Diode Emulation (DE) mode to improve light-load efficiency. In DE mode, the low-side MOSFET conducts when the current is flowing from source to drain and does not allow reverse current, thus emulating a diode. As Figure 12 shows, when LGATE is on, the low-side MOSFET carries current, creating negative voltage on the phase node due to the voltage drop across the on-resistance. The ISL62773A monitors the current by monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

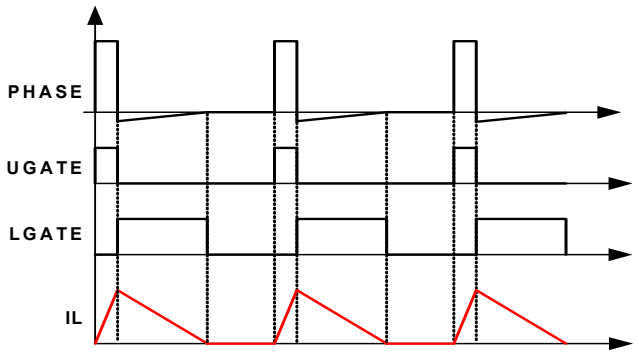


FIGURE 12. DIODE EMULATION

If the load current is light enough, as Figure 12 shows, the inductor current reaches and stays at zero before the next phase node pulse, and the regulator is in Discontinuous Conduction Mode (DCM). If the load current is heavy enough, the inductor current will never reach 0A, and the regulator is in CCM, although the controller is in DE mode.

Figure 13 shows the operation principle in diode emulation mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size and therefore is the same, making the inductor current triangle the same in the three cases. The ISL62773A clamps the ripple capacitor voltage V_{CRS} in DE mode to make it mimic the inductor current. It takes the COMP voltage longer to hit V_{CRS}, naturally stretching the switching period. The inductor current triangles move farther apart, such that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light-load efficiency.

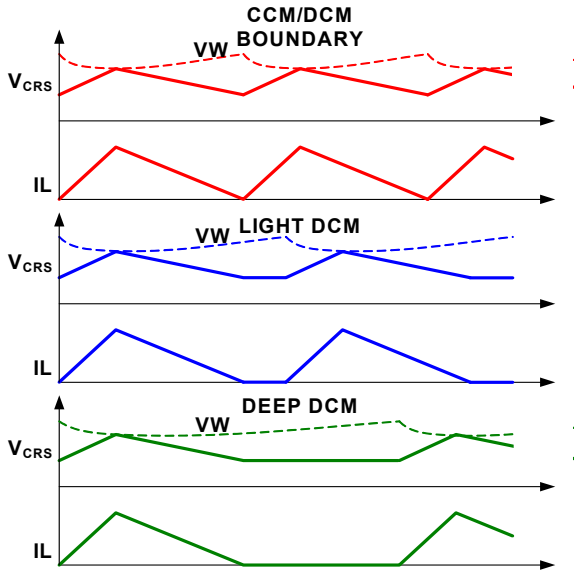


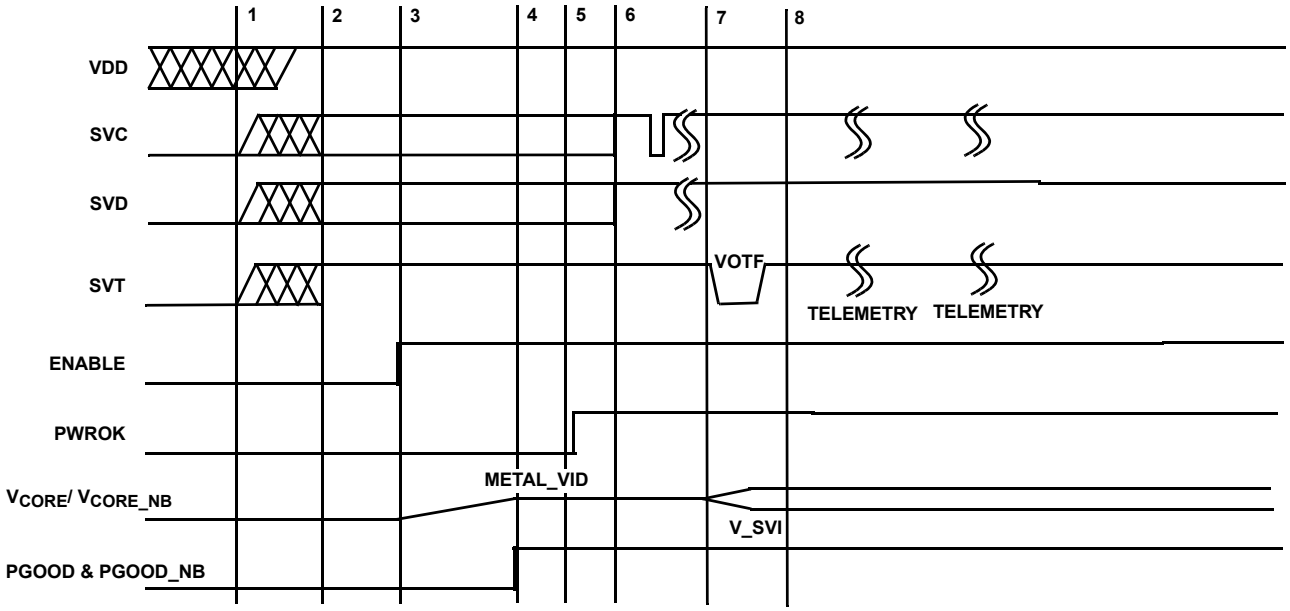
FIGURE 13. PERIOD STRETCHING

Channel Configuration

Individual PWM channels of either VR can be disabled by connecting the ISENx pin of the channel not required to +5V. For example, placing the controller in a 2+1 configuration, as shown in Figure 5 on page 5, requires ISEN3 of the Core VR and ISEN2 of the Northbridge VR to be tied to +5V. This disables Channel 3 of the Core VR and Channel 2 of the Northbridge VR. ISEN1_NB must be tied through a 10kΩ resistor to GND to prevent this pin from pulling high and disabling the channel. Connecting ISEN1 or ISEN1_NB to +5V will disable the corresponding VR output. This feature allows debug of individual VR outputs.

Power-On Reset

Before the controller has sufficient bias to guarantee proper operation, the ISL62773A requires a +5V input supply tied to VDD and VDDP to exceed the VDD rising Power-On Reset (POR) threshold. Once this threshold is reached or exceeded, the ISL62773A has enough bias to check the state of the SVI inputs once ENABLE is taken high. Hysteresis between the rising and the falling thresholds assure the ISL62773A does not inadvertently turn off unless the bias voltage drops substantially (see “Electrical Specifications” on page 11). Note that VIN must be present for the controller to drive the output voltage.



Interval 1 to 2: ISL62773A waits to POR.

Interval 2 to 3: SVC and SVD are externally set to pre-Metal VID code.

Interval 3 to 4: ENABLE locks pre-Metal VID code. Both outputs soft-start to this level.

Interval 4 to 5: PGOOD signal goes HIGH, indicating proper operation.

Interval 5 to 6: PGOOD and PGOOD_NB high is detected and PWROK is taken high. The ISL62773A is prepared for SVI commands.

Interval 6 to 7: SVC and SVD data lines communicate change in VID code.

Interval 7 to 8: ISL62773A responds to VID-ON-THE-FLY code change and issues a VOTF for positive VID changes.

Post 8: Telemetry is clocked out of the ISL62773A.

FIGURE 14. SVI INTERFACE TIMING DIAGRAM: TYPICAL PRE-PWROK METAL VID START-UP

Start-Up Timing

With VDD above the POR threshold, the controller start-up sequence begins when ENABLE exceeds the logic high threshold. Figure 15 shows the typical soft-start timing of the Core and Northbridge VRs. Once the controller registers ENABLE as a high, the controller checks that state of a few programming pins during the typical 8ms delay prior to beginning soft-starting the Core and Northbridge outputs. The pre-PWROK Metal VID is read from the state of the SVC and SVD pins and programs the DAC, the programming resistors on COMP, COMP_NB, and FCCM_NB are read to configure internal drivers, switching frequency, slew rate and output offsets. These programming resistors are discussed in subsequent sections. The ISL62773A uses a digital soft-start to ramp up the DAC to the Metal VID level programmed. The soft-start slew rate is programmed by the FCCM_NB resistor which is used to set the VID-on-the-fly slew rate as well. See "VID-on-the-Fly Slew Rate Selection" on page 21 for more details on selecting the FCCM_NB resistor. PGOOD is asserted high at the end of the soft-start ramp.

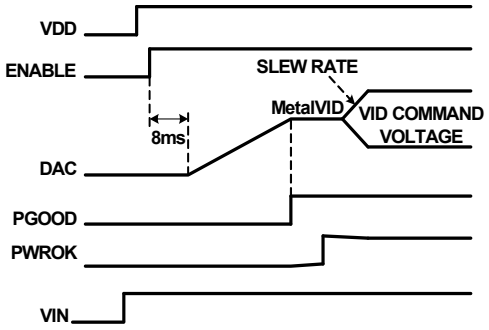


FIGURE 15. TYPICAL SOFT-START WAVEFORMS

Voltage Regulation and Load Line Implementation

After the soft-start sequence, the ISL62773A regulates the output voltages to the pre-PWROK metal VID programmed, see Table 6. The ISL62773A controls the no-load output voltage to an accuracy of ±0.5% over the range of 0.75V to 1.55V. A differential amplifier allows voltage sensing for precise voltage regulation at the microprocessor die.

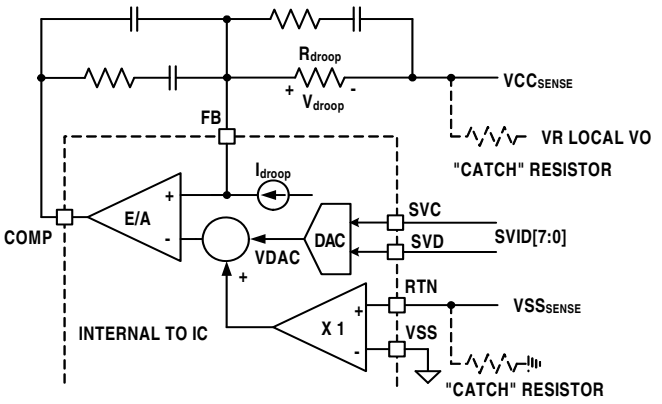


FIGURE 16. DIFFERENTIAL SENSING AND LOAD LINE IMPLEMENTATION

As the load current increases from zero, the output voltage droops from the VID programmed value by an amount proportional to the load current, to achieve the load line. The ISL62773A can sense the inductor current through the intrinsic DC Resistance (DCR) of the inductors, as shown in Figures 3 and 4, or through resistors in series with the inductors as shown in Figure 5. In both methods, capacitor C_n voltage represents the total inductor current. An internal amplifier converts C_n voltage into an internal current source, I_{sum}, with the gain set by resistor R_i, see Equation 1.

$$I_{sum} = \frac{V_{Cn}}{R_i} \quad \text{(EQ. 1)}$$

The I_{sum} current is used for load line implementation, current monitoring on the IMON pins and overcurrent protection.

Figure 16 shows the load line implementation. The ISL62773A drives a current source (I_{droop}) out of the FB pin which is a ratio of the I_{sum} current, as described by Equation 2.

$$I_{droop} = \frac{5}{4} \times I_{sum} = \frac{5}{4} \times \frac{V_{Cn}}{R_i} \quad \text{(EQ. 2)}$$

When using inductor DCR current sensing, a single NTC element is used to compensate the positive temperature coefficient of the copper winding, thus sustaining the load line accuracy with reduced cost.

I_{droop} flows through resistor R_{droop} and creates a voltage drop as shown in Equation 3.

$$V_{droop} = R_{droop} \times I_{droop} \quad \text{(EQ. 3)}$$

V_{droop} is the droop voltage required to implement load line. Changing R_{droop} or scaling I_{droop} can change the load line slope. Since I_{sum} sets the overcurrent protection level, it is recommended to first scale I_{sum} based on OCP requirement, then select an appropriate R_{droop} value to obtain the desired load line slope.

Differential Sensing

Figure 16 also shows the differential voltage sensing scheme. VCC_{SENSE} and VSS_{SENSE} are the remote voltage sensing signals from the processor die. A unity gain differential amplifier senses the VSS_{SENSE} voltage and adds it to the DAC output. The error amplifier regulates the inverting and noninverting input voltages to be equal as shown in Equation 4:

$$VCC_{SENSE} + V_{droop} = V_{DAC} + VSS_{SENSE} \quad \text{(EQ. 4)}$$

Rewriting Equation 4 and substituting Equation 3 gives Equation 5 the exact equation required for load line implementation.

$$VCC_{SENSE} - VSS_{SENSE} = V_{DAC} - R_{droop} \times I_{droop} \quad \text{(EQ. 5)}$$

The VCC_{SENSE} and VSS_{SENSE} signals come from the processor die. The feedback is open circuit in the absence of the processor. As Figure 16 shows, it is recommended to add a “catch” resistor to feed the VR local output voltage back to the compensator, and to add another “catch” resistor to connect the VR local output ground to the RTN pin. These resistors, typically 10Ω~100Ω, provide voltage feedback if the system is powered up without a processor installed.

Phase Current Balancing

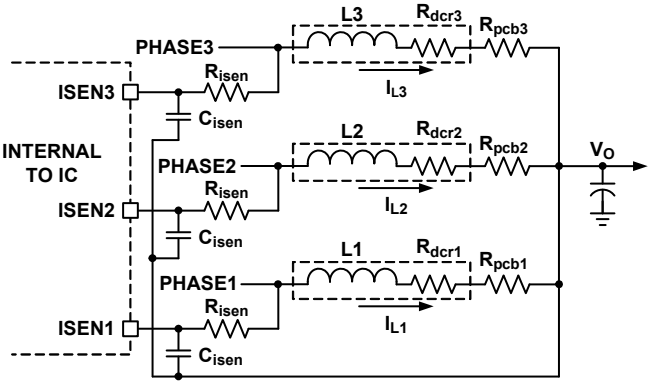


FIGURE 17. CURRENT BALANCING CIRCUIT

The ISL62773A monitors individual phase average current by monitoring the ISEN1, ISEN2 and ISEN3 voltages. Figure 17 shows the recommended current balancing circuit for DCR sensing. Each phase node voltage is averaged by a low-pass filter consisting of R_{isen} and C_{isen}, and is presented to the corresponding ISEN pin. R_{isen} should be routed to the inductor phase-node pad in order to eliminate the effect of phase node parasitic PCB DCR. Equations 6 through 8 give the ISEN pin voltages:

$$V_{ISEN1} = (R_{dcr1} + R_{pcb1}) \times I_{L1} \quad \text{(EQ. 6)}$$

$$V_{ISEN2} = (R_{dcr2} + R_{pcb2}) \times I_{L2} \quad \text{(EQ. 7)}$$

$$V_{ISEN3} = (R_{dcr3} + R_{pcb3}) \times I_{L3} \quad \text{(EQ. 8)}$$

Where R_{dcr1}, R_{dcr2} and R_{dcr3} are inductor DCR; R_{pcb1}, R_{pcb2} and R_{pcb3} are parasitic PCB DCR between the inductor output side pad and the output voltage rail; and I_{L1}, I_{L2} and I_{L3} are inductor average currents.

The ISL62773A will adjust the phase pulse-width relative to the other phases to make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$, thus to achieve $I_{L1} = I_{L2} = I_{L3}$, when $R_{dcr1} = R_{dcr2} = R_{dcr3}$ and $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

Using the same components for L1, L2 and L3 provides a good match of R_{dcr1}, R_{dcr2} and R_{dcr3}. Board layout determines R_{pcb1}, R_{pcb2} and R_{pcb3}. It is recommended to have a symmetrical layout for the power delivery path between each inductor and the output voltage rail, such that $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

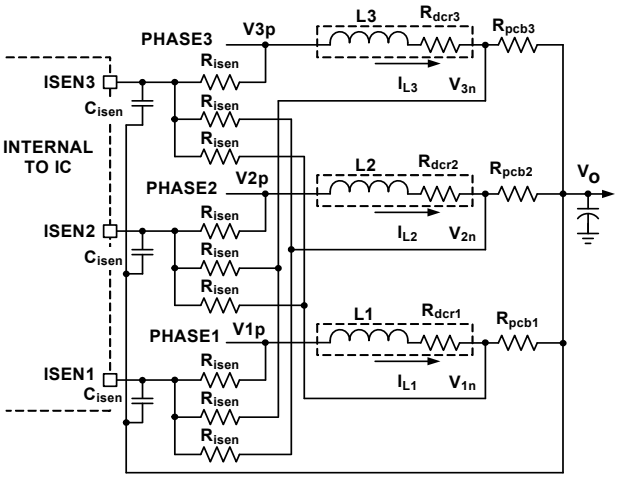


FIGURE 18. DIFFERENTIAL-SENSING CURRENT BALANCING CIRCUIT

Sometimes, it is difficult to implement symmetrical layout. For the circuit shown in Figure 17, asymmetric layout causes different R_{pcb1}, R_{pcb2} and R_{pcb3} values, thus creating a current imbalance. Figure 18 shows a differential sensing current balancing circuit recommended for ISL62773A. The current sensing traces should be routed to the inductor pads so they only pick up the inductor DCR voltage. Each ISEN pin sees the average voltage of three sources: its own, phase inductor phase-node pad, and the other two phase inductor output side pads. Equations 9 through 11 give the ISEN pin voltages:

$$V_{ISEN1} = V_{1p} + V_{2n} + V_{3n} \quad \text{(EQ. 9)}$$

$$V_{ISEN2} = V_{1n} + V_{2p} + V_{3n} \quad \text{(EQ. 10)}$$

$$V_{ISEN3} = V_{1n} + V_{2n} + V_{3p} \quad \text{(EQ. 11)}$$

The ISL62773A will make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$ as shown in Equations 12 and 13:

$$V_{1p} + V_{2n} + V_{3n} = V_{1n} + V_{2p} + V_{3n} \quad \text{(EQ. 12)}$$

$$V_{1n} + V_{2p} + V_{3n} = V_{1n} + V_{2n} + V_{3p} \quad \text{(EQ. 13)}$$

Rewriting Equation 12 gives Equation 14:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} \quad \text{(EQ. 14)}$$

Rewriting Equation 13 gives Equation 15:

$$V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad \text{(EQ. 15)}$$

Combining Equation 14 and 15 gives:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad \text{(EQ. 16)}$$

Therefore:

$$R_{dcr1} \times I_{L1} = R_{dcr2} \times I_{L2} = R_{dcr3} \times I_{L3} \quad \text{(EQ. 17)}$$

Current balancing ($I_{L1} = I_{L2} = I_{L3}$) is achieved when $R_{dcr1} = R_{dcr2} = R_{dcr3}$. R_{pcb1}, R_{pcb2} and R_{pcb3} do not have any effect.

Since the slave ripple capacitor voltages mimic the inductor currents, the R3™ modulator can naturally achieve excellent current balancing during steady state and dynamic operations. Figure 19 shows the current balancing performance of the evaluation board with load transient of 12A/51A at different rep rates. The inductor currents follow the load current dynamic change with the output capacitors supplying the difference. The inductor currents can track the load current well at a low repetition rate, but cannot keep up when the repetition rate gets into the hundred-kHz range, where it is out of the control loop bandwidth. The controller achieves excellent current balancing in all cases installed.

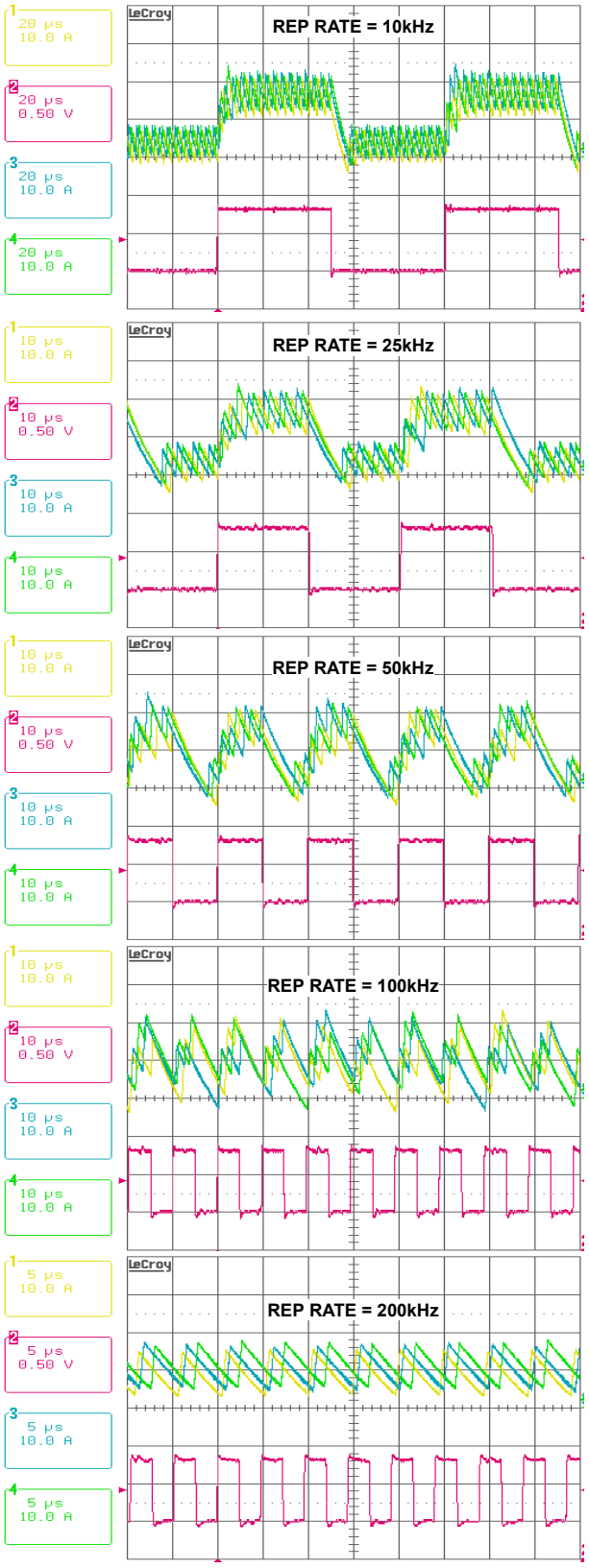


FIGURE 19. CURRENT BALANCING DURING DYNAMIC OPERATION. CH1: I_{L1}, CH2: I_{LOAD}, CH3: I_{L2}, CH4: I_{L3}

Modes of Operation

TABLE 1. CORE VR MODES OF OPERATION

CONFIG.	ISEN3	ISEN2	PSL0_L AND PSI1_L	MODE	IMON OCP THRESHOLD
3-phase Core VR	To Power Stage	To Power Stage	11	3-phase CCM	1.5V
			01	2-phase CCM	
			00	1-phase DE	
2-phase Core VR	Tied to 5V	To Power Stage	11	2-phase CCM	1.5V
			01	1-phase CCM	
			00	1-phase DE	
1-phase Core VR	Tied to 5V	Tied to 5V	11	1-phase CMM	1.5V
			01		
			00	1-phase DE	

The Core VR can be configured for 3, 2- or 1-phase operation. Table 1 shows Core VR configurations and operational modes, programmed by the ISEN3 and ISEN2 pin status and the PSL0_L and PSL1_L commands via the SVI 2 interface, see Table 9.

For a 2-phase configuration, tie the ISEN3 pin to 5V. In this configuration, phases 1 and 2 are active. To select a 1-phase configuration, tie the ISEN3 pin and the ISEN2 pin to 5V. In this configuration, only phase-1 is active.

In a 3-phase configuration, the Core VR operates in 3-phase CCM, with PSI0_L and PSI_L both high. If PSI0_L is taken low via the SVI 2 interface, the Core VR sheds Phase 3 and continues to operate in 2-phase CCM. When both PSI0_L and PSI1_L are taken low, the Core VR drops Phase2 and enters 1-phase DE mode.

For 2-phase configurations, the Core VR operates in 2-phase CCM with PSI0_L and PSI_L both high. If PSI0_L is taken low via the SVI 2 interface, the Core VR sheds Phase 2 and continues to operate in CCM. When both PSI0_L and PSI1_L are taken low, the Core VR enters 1-phase DE mode.

In a 1-phase configuration, the Core VR operates in 1-phase CCM when PSI0_L is high or low. When both PSI0_l and PSI1_L are taken low, the VR enters 1-phase DE mode.

The Core VR can be disabled completely by connecting ISEN1 to +5V.

ISL62773A Northbridge VR can be configured for 2- or 1-phase operation. Table 2 shows the Northbridge VR configurations and operational modes, which are programmed by the ISEN2_NB pin status and the PSI0_L and PSI1_L bits of the SVI 2 command.

TABLE 2. NORTHBRIDGE VR MODES OF OPERATION

ISEN2_NB	CONFIG.	PSL0_L AND PSI1_L	MODE	IMON OCP THRESHOLD
To Power Stage	2-phase NB VR	11	2-phase CCM	1.5V
		01	1-phase CCM	
		00	1-phase DE	
Tied to 5V	1-phase NB VR	11	1-phase CCM	1.5V
		01		
		00	1-phase DE	

In a 1-phase configuration, the ISEN2_NB pin is tied to +5V. The Northbridge VR operates in 1-phase CCM and enters 1-phase DE when both PSI0_L and PSI1_L are low.

The Northbridge VR can be disabled completely by tying ISEN1_NB to 5V.

The Core and Northbridge VRs have an overcurrent threshold of 1.5V on IMON and IMON_NB respectively, and this level does not vary based on channel configuration. See the "Overcurrent" subsection on page 26, of "Protection Features" for more details.

Dynamic Operation

Core VR and Northbridge VR behave the same during dynamic operation. The controller responds to VID-on-the-fly changes by slewing to the new voltage at the slew rate programmed, see Table 4. During negative VID transitions, the output voltage decays to the lower VID value at the slew rate determined by the load.

The R3™ modulator intrinsically has voltage feed-forward. The output voltage is insensitive to a fast slew rate input voltage change.

FB2 Function

The Core VR features an FB2 pin. The FB2 function is only available when the Core VR is in a 2-phase configuration.

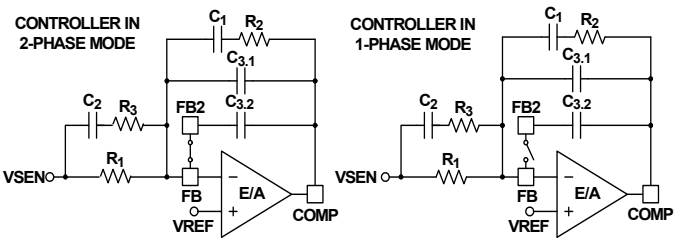


FIGURE 20. FB2 FUNCTION

Figure 20 shows the FB2 function. A switch (called FB2 switch) turns on to short the FB and the FB2 pins when the controller is in 2-phase mode. Capacitors $C_{3.1}$ and $C_{3.2}$ are in parallel, serving as part of the compensator. When the controller enters 1-phase mode, the FB2 switch turns off, removing $C_{3.2}$ and leaving only $C_{3.1}$ in the compensator. The compensator gain increases with the removal of $C_{3.2}$. By properly sizing $C_{3.1}$ and $C_{3.2}$, the compensator can be optimal for both 2-phase mode and 1-phase mode.

When the FB2 switch is off, $C_{3.2}$ is disconnected from the FB pin. However, the controller still actively drives the FB2 pin voltage to follow the FB pin voltage such that $C_{3.2}$ voltage always follows $C_{3.1}$ voltage. When the controller turns on the FB2 switch, $C_{3.2}$ is reconnected to the compensator smoothly.

The FB2 function ensures excellent transient response in both 2-phase and 1-phase mode. If the FB2 function is not used, populate $C_{3.1}$ only.

Adaptive Body Diode Conduction Time Reduction

In DCM, the controller turns off the low-side MOSFET when the inductor current approaches zero. During on-time of the low-side MOSFET, phase voltage is negative and the amount is the MOSFET $r_{DS(ON)}$ voltage drop, which is proportional to the inductor current. A phase comparator inside the controller monitors the phase voltage during on-time of the low-side MOSFET and compares it with a threshold to determine the zero crossing point of the inductor current. If the inductor current has not reached zero when the low-side MOSFET turns off, it will flow through the low-side MOSFET body diode, causing the phase node to have a larger voltage drop until it decays to zero. If the inductor current has crossed zero and reversed the direction when the low-side MOSFET turns off, it will flow through the high-side MOSFET body diode, causing the phase node to have a spike until it decays to zero. The controller continues monitoring the phase voltage after turning off the low-side MOSFET. To minimize the body diode-related loss, the controller also adjusts the phase comparator threshold voltage accordingly in iterative steps such that the low-side MOSFET body diode conducts for approximately 40ns.

Resistor Configuration Options

The ISL62773A uses the COMP, COMP_NB and FCCM_NB pins to configure some functionality within the IC. Resistors from these pins to GND are read during the first portion of the soft-start sequence. The following sections outline how to select the resistor values for each of these pins to correctly program the output voltage offset of each output, the configuration of the floating DriverX and PWM_Y output, VID-on-the-fly slew rate and switching frequency used for both VRs.

VR Offset Programming

A positive or negative offset is programmed for the Core VR using a resistor to ground from the COMP pin and the Northbridge in a similar manner from the COMP_NB pin. Table 3 provides the resistor value to select the desired output voltage offset. The 1% tolerance resistor value shown in the table must be used to program the corresponding Core or NB output voltage offset. The MIN and MAX tolerance values provide margin to insure the 1% tolerance resistor will be read correctly.

TABLE 3. COMP AND COMP_NB OUTPUT VOLTAGE OFFSET SELECTION

RESISTOR VALUE [kΩ]			COMP $V_{CORE\ OFFSET}$ [mV]	COMP_NB OFFSET [mV]
MIN TOLERANCE	1% TOLERANCE VALUE	MAX TOLERANCE		
5.54	5.62	5.70	-43.75	18.75
7.76	7.87	7.98	-37.5	31.25
11.33	11.5	11.67	-31.25	43.76
16.65	16.9	17.15	-25	50
19.3	19.6	19.89	-18.75	37.5
24.53	24.9	25.27	-12.5	25
33.49	34.0	34.51	-6.25	12.5
40.58	41.2	41.81	6.25	0
51.52	52.3	53.08	18.75	18.75
72.10	73.2	74.29	31.25	31.25
93.87	95.3	96.72	43.76	43.76
119.19	121	122.81	50	50
151.69	154	156.31	37.5	37.5
179.27	182	184.73	25	25
206.85	210	213.15	12.5	12.5
	OPEN		0	0

Floating DriverX AND PWM_Y Configuration

The ISL62773A allows for one internal driver and one PWM output to be configured to opposite VRs depending on the desired configuration of the Northbridge VR. Internal DriverX can be used as Channel 1 of the Northbridge VR with PWM_Y used for Channel 3 of the Core VR. Using this partitioning, a 2+1 or 1+1 configured ISL62773A would not require an external driver.

If routing of the driver signals would be a cause of concern due to having an internal driver on the Northbridge VR, then the ISL62773A can be configured to use PWM_Y as Channel 1 on the Northbridge VR. DriverX would then be used as Channel 3 of the Core VR. This allows the placement of the external drivers for the Northbridge VR to be closer to the output stage(s) depending on the number of active Phases, providing placement and layout flexibility to the Northbridge VR.

The floating internal driver and PWM output are configured based on the programming resistor from FCCM_NB to GND. The FCCM_NB programming resistor value also sets the slew rate and switching frequency of the Core and Northbridge VRs. These features are outlined in the following sections. Table 4 shows which resistor values sets the configuration and slew rate for the ISL63773A. The resistor value shown in the table must be used and the resistor tolerance must be 1%. The MIN and MAX tolerance around each resistor value is the same as Table 3 and provides margin to insure the 1% tolerance resistor will be read correctly.

TABLE 4. FCCM_NB RESISTOR SELECTION

RESISTOR VALUE [kΩ]	SLEW RATE FOR CORE AND NORTHBRIDGE [mV/µs]	DriverX	PWM_Y
5.62	20	Core VR Channel 3	NB VR Channel 1
7.87	15		
11.5	12.5		
16.9	10		
19.6	20		
24.9	15		
34.0	12.5		
41.2	10		
52.3	20	NB VR Channel 1	Core VR Channel 3
73.2	15		
95.3	12.5		
121	10		
154	20		
182	15		
210	12.5		
OPEN	10		

VID-on-the-Fly Slew Rate Selection

The FCCM_NB resistor is also used to select the slew rate for VID changes commanded by the processor. Once selected, the slew rate is locked in during soft-start and is not adjustable during operation. The lowest slew rate which can be selected is 10mV/µs which is above the minimum of 7.5mV/µs required by the SVI 2 specification. The slew rate selected sets the slew rate for both Core and Northbridge VRs; they cannot be independently selected.

CCM Switching Frequency

The Core and Northbridge VR switching frequency is set by the programming resistors on COMP_NB and FCCM_NC. When the ISL62773A is in Continuous Conduction Mode (CCM), the switching frequency is not absolutely constant due to the nature of the R3™ Modulator. As explained in "Multiphase R3™ Modulator" on page 14, the effective switching frequency increases during load insertion and decreases during load release to achieve fast response. Thus, the switching frequency is relatively constant at steady state. Variation is expected when the power stage condition, such as input voltage, output voltage, load, etc. changes. The variation is usually less than 10% and does not have any significant effect on output voltage ripple magnitude. Table 5 defines the switching frequency based on the resistor values used to program the COMP_NB and FCCM_NB pins. Use the previous tables related to COMP_NB and FCCM_NB to determine the correct resistor value in these ranges to program the desired output offset, slew rate and DriverX/PWM_Y configuration.

TABLE 5. SWITCHING FREQUENCY SELECTION

FREQUENCY [kHz]	COMP_NB RANGE [kΩ]	FCCM_NB RANGE [kΩ]
300	57.6 to OPEN	19.1 to 41.2 or 154 to OPEN
350	5.62 to 41.2	19.1 to 41.2 or 154 to OPEN
400	57.6 to OPEN	5.62 to 16.9 or 57.6 to 121
450	5.62 to 41.2	5.62 to 16.9 or 57.6 to 121

The controller monitors SVI commands to determine when to enter power-saving mode, implement dynamic VID changes and shut down individual outputs.

AMD Serial VID Interface 2.0

The on-board Serial VID Interface 2.0 (SVI 2) circuitry allows the AMD processor to directly control the Core and Northbridge voltage reference levels within the ISL62773A. Once the PWROK signal goes high, the IC begins monitoring the SVC and SVD pins for instructions. The ISL62773A uses a Digital-to-Analog Converter (DAC) to generate a reference voltage based on the decoded SVI value. See Figure 14 on page 16 for a simple SVI interface timing diagram.

Pre-PWROK Metal VID

Typical motherboard start-up begins with the controller decoding the SVC and SVD inputs to determine the pre-PWROK Metal VID setting (see Table 6). Once the ENABLE input exceeds the rising threshold, the ISL62773A decodes and locks the decoded value into an on-board hold register.

TABLE 6. PRE-PWROK METAL VID CODES

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Once the programming pins are read, the internal DAC circuitry begins to ramp Core and Northbridge VRs to the decoded pre-PWROK Metal VID output level. The digital soft-start circuitry ramps the internal reference to the target gradually at a fixed rate of approximately 5mV/µs until the output voltage reaches ~250mV and then at the programmed slew rate. The controlled ramp of all output voltage planes reduces inrush current during the soft-start interval. At the end of the soft-start interval, the PGOOD and PGOOD_NB outputs transition high, indicating both output planes are within regulation limits.

If the ENABLE input falls below the enable falling threshold, the ISL62773A tri-states both outputs. PGOOD and PGOOD_NB are pulled low with the loss of ENABLE. The Core and Northbridge VR output voltages decay, based on output capacitance and load leakage resistance. If bias to VDD falls below the POR level, the ISL62773A responds in the manner previously described. Once VDD and ENABLE rise above their respective rising thresholds, the internal DAC circuitry reacquires a pre-PWROK metal VID code and the controller soft-starts.

SVI Interface Active

Once the Core and Northbridge VRs have successfully soft-started and PGOOD and PGOOD_NB signals transition high, PWROK can be asserted externally to the ISL62773A. Once PWROK is asserted to the IC, SVI instructions can begin as the controller actively monitors the SVI interface. Details of the SVI Bus protocol are provided in the “AMD Serial VID Interface 2.0 (SVI 2) Specification”. See AMD publication #48022.

Once a VID change command is received, the ISL62773A decodes the information to determine which VR is affected and the VID target is determined by the byte combinations in Table 7. The internal DAC circuitry steps the output voltage of the VR commanded to the new VID level. During this time, one or more of the VR outputs could be targeted. In the event either VR is commanded to power-off by serial VID commands, the PGOOD signal remains asserted.

If the PWROK input is deasserted, then the controller steps both the Core and the Northbridge VRs back to the stored pre-PWROK metal VID level in the holding register from initial soft-start. No attempt is made to read the SVC and SVD inputs during this time. If PWROK is reasserted, then the ISL62773A SVI interface waits for instructions.

If ENABLE goes low during normal operation, all external MOSFETs are tri-stated and both PGOOD and PGOOD_NB are pulled low. This event clears the pre-PWROK metal VID code and forces the controller to check SVC and SVD upon restart, storing the pre-PWROK metal VID code found on restart.

A POR event on either VCC or VIN during normal operation shuts down both regulators and both PGOOD outputs are pulled low. The pre-PWROK metal VID code is not retained. Loss of VIN during operation will typically cause the controller to enter a fault condition on one or both outputs. The controller will shut down both Core and Northbridge VRs and latch off. The pre-PWROK metal VID code is not retained during the process of cycling ENABLE to reset the fault latch and restart the controller.

VID-on-the-Fly Transition

Once PWROK is high, the ISL62773A detects this flag and begins monitoring the SVC and SVD pins for SVI instructions. The microprocessor follows the protocol outlined in the following sections to send instructions for VID-on-the-fly transitions. The ISL62773A decodes the instruction and acknowledges the new VID code. For VID codes higher than the current VID level, the ISL62773A begins stepping the commanded VR outputs to the new VID target at the fixed slew rate of 10mV/µs. Once the DAC ramps to the new VID code, a VID-on-the-Fly Complete (VOTFC) request is sent on the SVI lines.

When the VID codes are lower than the current VID level, the ISL62773A checks the state of power state bits in the SVI command. If power state bits are not active, the controller begins stepping the regulator output to the new VID target. If the power

state bits are active, the controller allows the output voltage to decay and slowly steps the DAC down with the natural decay of the output. This allows the controller to quickly recover and move to a high VID code if commanded. The controller issues a VOTFC request on the SVI lines once the SVI command is decoded and prior to reaching the final output voltage.

VOTFC requests do not take priority over telemetry per the AMD SVI 2 specification.

SVI Data Communication Protocol

The SVI WIRE protocol is based on the I^2C bus concept. Two wires [Serial Clock (SVC) and Serial Data (SVD)], carry information between the AMD processor (master) and VR controller (slave) on the bus. The master initiates and terminates SVI transactions and drives the clock, SVC, during a transaction. The AMD processor is always the master, and the voltage regulators are the slaves. The slave receives the SVI transactions and acts accordingly. Mobile SVI WIRE protocol timing is based on high-speed mode I^2C. See AMD publication #48022 for additional details.

TABLE 7. SERIAL VID CODES

SVID[7:0]	VOLTAGE (V)	SVID[7:0]	VOLTAGE (V)	SVID[7:0]	VOLTAGE (V)	SVID[7:0]	VOLTAGE (V)
0000_0000	1.55000	0010_0000	1.35000	0100_0000	1.15000	0110_0000	0.95000
0000_0001	1.54375	0010_0001	1.34375	0100_0001	1.14375	0110_0001	0.94375
0000_0010	1.53750	0010_0010	1.33750	0100_0010	1.13750	0110_0010	0.93750
0000_0011	1.53125	0010_0011	1.33125	0100_0011	1.13125	0110_0011	0.93125
0000_0100	1.52500	0010_0100	1.32500	0100_0100	1.12500	0110_0100	0.92500
0000_0101	1.51875	0010_0101	1.31875	0100_0101	1.11875	0110_0101	0.91875
0000_0110	1.51250	0010_0110	1.31250	0100_0110	1.11250	0110_0110	0.91250
0000_0111	1.50625	0010_0111	1.30625	0100_0111	1.10625	0110_0111	0.90625
0000_1000	1.50000	0010_1000	1.30000	0100_1000	1.10000	0110_1000	0.90000
0000_1001	1.49375	0010_1001	1.29375	0100_1001	1.09375	0110_1001	0.89375
0000_1010	1.48750	0010_1010	1.28750	0100_1010	1.08750	0110_1010	0.88750
0000_1011	1.48125	0010_1011	1.28125	0100_1011	1.08125	0110_1011	0.88125
0000_1100	1.47500	0010_1100	1.27500	0100_1100	1.07500	0110_1100	0.87500
0000_1101	1.46875	0010_1101	1.26875	0100_1101	1.06875	0110_1101	0.86875
0000_1110	1.46250	0010_1110	1.26250	0100_1110	1.06250	0110_1110	0.86250
0000_1111	1.45625	0010_1111	1.25625	0100_1111	1.05625	0110_1111	0.85625
0001_0000	1.45000	0011_0000	1.25000	0101_0000	1.05000	0111_0000	0.85000
0001_0001	1.44375	0011_0001	1.24375	0101_0001	1.04375	0111_0001	0.84375
0001_0010	1.43750	0011_0010	1.23750	0101_0010	1.03750	0111_0010	0.83750
0001_0011	1.43125	0011_0011	1.23125	0101_0011	1.03125	0111_0011	0.83125
0001_0100	1.42500	0011_0100	1.22500	0101_0100	1.02500	0111_0100	0.82500
0001_0101	1.41875	0011_0101	1.21875	0101_0101	1.01875	0111_0101	0.81875
0001_0110	1.41250	0011_0110	1.21250	0101_0110	1.01250	0111_0110	0.81250
0001_0111	1.40625	0011_0111	1.20625	0101_0111	1.00625	0111_0111	0.80625
0001_1000	1.40000	0011_1000	1.20000	0101_1000	1.00000	0111_1000	0.80000
0001_1001	1.39375	0011_1001	1.19375	0101_1001	0.99375	0111_1001	0.79375
0001_1010	1.38750	0011_1010	1.18750	0101_1010	0.98750	0111_1010	0.78750
0001_1011	1.38125	0011_1011	1.18125	0101_1011	0.98125	0111_1011	0.78125
0001_1100	1.37500	0011_1100	1.17500	0101_1100	0.97500	0111_1100	0.77500
0001_1101	1.36875	0011_1101	1.16875	0101_1101	0.96875	0111_1101	0.76875
0001_1110	1.36250	0011_1110	1.16250	0101_1110	0.96250	0111_1110	0.76250

TABLE 7. SERIAL VID CODES (Continued)

SVID[7:0]	VOLTAGE (V)	SVID[7:0]	VOLTAGE (V)	SVID[7:0]	VOLTAGE (V)	SVID[7:0]	VOLTAGE (V)
0001_1111	1.35625	0011_1111	1.15625	0101_1111	0.95625	0111_1111	0.75625
1000_0000	0.75000	1010_0000	0.55000*	1100_0000	0.35000*	1110_0000	0.15000*
1000_0001	0.74375	1010_0001	0.54375*	1100_0001	0.34375*	1110_0001	0.14375*
1000_0010	0.73750	1010_0010	0.53750*	1100_0010	0.33750*	1110_0010	0.13750*
1000_0011	0.73125	1010_0011	0.53125*	1100_0011	0.33125*	1110_0011	0.13125*
1000_0100	0.72500	1010_0100	0.52500*	1100_0100	0.32500*	1110_0100	0.12500*
1000_0101	0.71875	1010_0101	0.51875*	1100_0101	0.31875*	1110_0101	0.11875*
1000_0110	0.71250	1010_0110	0.51250*	1100_0110	0.31250*	1110_0110	0.11250*
1000_0111	0.70625	1010_0111	0.50625*	1100_0111	0.30625*	1110_0111	0.10625*
1000_1000	0.70000	1010_1000	0.50000*	1100_1000	0.30000*	1110_1000	0.10000*
1000_1001	0.69375	1010_1001	0.49375*	1100_1001	0.29375*	1110_1001	0.09375*
1000_1010	0.68750	1010_1010	0.48750*	1100_1010	0.28750*	1110_1010	0.08750*
1000_1011	0.68125	1010_1011	0.48125*	1100_1011	0.28125*	1110_1011	0.08125*
1000_1100	0.67500	1010_1100	0.47500*	1100_1100	0.27500*	1110_1100	0.07500*
1000_1101	0.66875	1010_1101	0.46875*	1100_1101	0.26875*	1110_1101	0.06875*
1000_1110	0.66250	1010_1110	0.46250*	1100_1110	0.26250*	1110_1110	0.06250*
1000_1111	0.65625	1010_1111	0.45625*	1100_1111	0.25625*	1110_1111	0.05625*
1001_0000	0.65000	1011_0000	0.45000*	1101_0000	0.25000*	1111_0000	0.05000*
1001_0001	0.64375	1011_0001	0.44375*	1101_0001	0.24375*	1111_0001	0.04375*
1001_0010	0.63750	1011_0010	0.43750*	1101_0010	0.23750*	1111_0010	0.03750*
1001_0011	0.63125	1011_0011	0.43125*	1101_0011	0.23125*	1111_0011	0.03125*
1001_0100	0.62500	1011_0100	0.42500*	1101_0100	0.22500*	1111_0100	0.02500*
1001_0101	0.61875	1011_0101	0.41875*	1101_0101	0.21875*	1111_0101	0.01875*
1001_0110	0.61250	1011_0110	0.41250*	1101_0110	0.21250*	1111_0110	0.01250*
1001_0111	0.60625	1011_0111	0.40625*	1101_0111*	0.20625*	1111_0111	0.00625*
1001_1000	0.60000*	1011_1000	0.40000*	1101_1000	0.20000*	1111_1000	OFF*
1001_1001	0.59375*	1011_1001	0.39375*	1101_1001	0.19375*	1111_1001	OFF*
1001_1010	0.58750*	1011_1010	0.38750*	1101_1010	0.18750*	1111_1010	OFF*
1001_1011	0.58125*	1011_1011	0.38125*	1101_1011	0.18125*	1111_1011	OFF*
1001_1100	0.57500*	1011_1100	0.37500*	1101_1100	0.17500*	1111_1100	OFF*
1001_1101	0.56875*	1011_1101	0.36875*	1101_1101	0.16875*	1111_1101	OFF*
1001_1110	0.56250*	1011_1110	0.36250*	1101_1110	0.16250*	1111_1110	OFF*
1001_1111	0.55625*	1011_1111	0.35625*	1101_1111	0.15625*	1111_1111	OFF*

NOTE: *Indicates a VID not required for AMD Family 10h processors. Loosened AMD requirements at these levels.

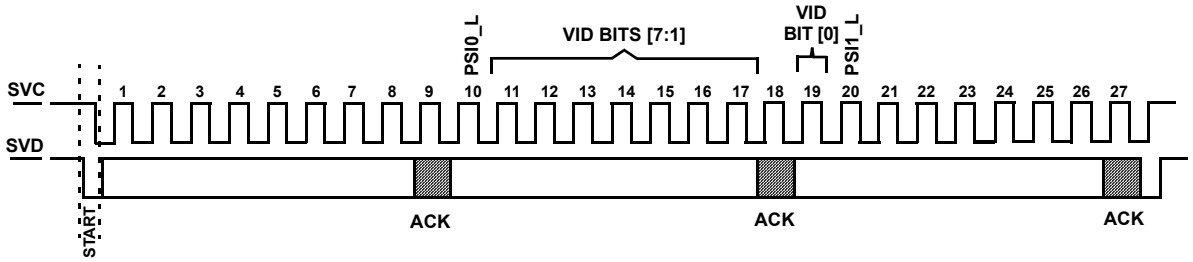


FIGURE 21. SVD PACKET STRUCTURE

SVI Bus Protocol

The AMD processor bus protocol is compliant with SMBus send byte protocol for VID transactions. The AMD SVD packet structure is shown in Figure 21. The description of each bit of the three bytes that make up the SVI command are shown in Table 8. During a transaction, the processor sends the start sequence followed by each of the three bytes which end with an optional acknowledge bit. The ISL62773A does not drive the SVD line during the ACK bit. Finally, the processor sends the stop sequence. After the ISL62773A has detected the stop, it can then proceed with the commanded action from the transaction.

TABLE 8. SVD DATA PACKET

BITS	DESCRIPTION
1:5	Always 11000b
6	Core domain selector bit, if set then the following data byte contains VID, power state, telemetry control, load line trim and offset trim apply to the Core VR.
7	Northbridge domain selector bit, if set then the following data byte contains VID, power state, telemetry control, load line trim and offset trim apply to the Northbridge VR.
8	Always 0b
9	Acknowledge bit
10	PSI0_L
11:17	VID Code bits [7:1]
18	Acknowledge bit
19	VID code bit [0]
20	PSI1_L
21	TFN (Telemetry Functionality)
22:24	Load line slope trim
25:26	Offset trim [1:0]
27	Acknowledge bit

Power States

SVI 2 defines two power state indicator levels (see Table 9). As processor current consumption reduces, the power state indicator level changes to improve VR efficiency under low power conditions.

For the Core VR operating in 3-phase mode, when PSI0_L is asserted Channels 2 and 3 are tri-stated and Channel 1 enters diode emulation mode to boost efficiency. When PSI1_L is asserted, the Core VR continues to operate in this mode.

For the Northbridge VR operating in 2-phase mode, when PSI0_L is asserted, Channel 2 is tri-stated and Channel 1 enters diode emulation mode to boost efficiency. When PSI1_L is asserted, the Core VR continues to operate in this fashion.

It is possible for the processor to assert or deassert PSI0_L and PSI1_L out of order. PSI0_L takes priority over PSI1_L. If PSI0_L is deasserted while PSI1_L is still asserted, the ISL62773A will return the selected VR back full channel CCM operation.

TABLE 9. PSI0_L, PSI1_L AND TFN DEFINITION

FUNCTION	BIT	DESCRIPTION
PSI0_L	10	Power state indicate level 0. When this signal is asserted (active Low) the processor is in a low enough power state for the ISL62773A to take action to boost efficiency by dropping phases and entering 1-Phase DE.
PSI1_L	20	Power state indicate level 1. When this signal is asserted (active Low) the processor is in a low enough power state for the ISL62773A to take action to boost efficiency by dropping phases and entering 1-Phase DE.

Dynamic Load Line Slope Trim

The ISL62773A supports the SVI 2 ability for the processor to manipulate the load line slope of the Core and Northbridge VRs independently using the serial VID interface. The slope manipulation applies to the initial load line slope. A load line slope trim will typically coincide with a VOTF change. See Table 10 for more information about the load line slope trim feature of the ISL62773A.

TABLE 10. LOAD LINE SLOPE TRIM DEFINITION

LOAD LINE SLOPE TRIM [2:0]	DESCRIPTION
000	Disable LL
001	-40% mΩ change
010	-20% mΩ change
011	No change
100	+20% mΩ change
101	+40% mΩ change
110	+60% mΩ change
111	+80% mΩ change