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Data Sheet | July 22, 2005 | FN9133.2

Li-ion/Li Polymer Battery Charger

The ISL6292C is an integrated single-cell Li-ion or Li-polymer battery charger capable of operating with an input voltage as low as 2.4V. This charger is designed to work with various types of ac adapters.

The ISL6292C operates as a linear charger when the ac adapter is a voltage source. The battery is charged in a CC/CV (constant current/constant voltage) profile. The charge current is programmable with an external resistor up to 1.5A. The ISL6292C can also work with a current-limited adapter to minimize the thermal dissipation, in which case the ISL6292C combines the benefits of both a linear charger and a pulse charger.

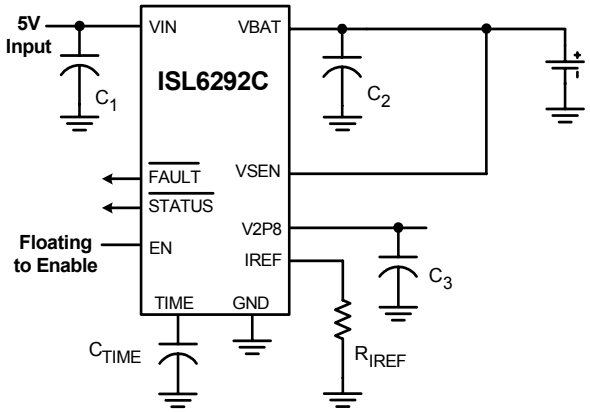
The ISL6292C features charge current thermal foldback to guarantee safe operation when the printed circuit board is space limited for thermal dissipation. Additional features include preconditioning of an over-discharged battery, automatic recharge, and thermally enhanced DFN package.

Ordering Information

PART # (NOTE)	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6292CCR3Z	-20 to 70	10 Ld 3x3 DFN (Pb-free)	L10.3x3
ISL6292CCR3Z-T	10 Ld 3x3 DFN Tape and Reel (Pb-free)		

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Typical Application Circuit



Features

- Complete Charger for Single-Cell Li-ion Batteries
- **Very Low Thermal Dissipation**
- Integrated Pass Element and Current Sensor
- No External Blocking Diode Required
- 1% Voltage Accuracy
- Programmable Current Limit up to 1.5A
- **Charge Current Thermal Foldback**
- **Accepts Multiple Types of Adapters**
- **Guaranteed to Operate at 2.65V After Start Up**
- Ambient Temperature Range: -20°C to 70°C
- Thermally-Enhanced DFN Packages
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

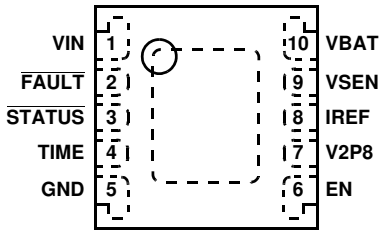
- Handheld Devices including Medical Handhelds
- PDAs, Cell Phones and Smart Phones
- Portable Instruments, MP3 Players
- Self-Charging Battery Packs
- Stand-Alone Chargers
- USB Bus-Powered Chargers

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Technical Brief TB379 “Thermal Characterization of Packaged Semiconductor Devices”
- Technical Brief TB389 “PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages”

Pinout

ISL6292C (3x3 DFN)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage (VIN) . . . . . -0.3 to 7V
Output Pin Voltage (BAT, VSEN, V2P8) . . . . . -0.3 to 5.5V
Signal Input Voltage (TIME, IREF) . . . . . -0.3 to 3.2V
Output Pin Voltage (STATUS, FAULT) . . . . . -0.3 to 7V
Charge Current 1.6A
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . 2500V
Machine Model (Per EIAJ ED-4701 Method C-111) 200V

Recommended Operating Conditions

Ambient Temperature Range . . . . . -20°C to 70°C
Supply Voltage, VIN . . . . . 4.3V to 6.5V

Thermal Information

Thermal Resistance (Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
3x3 DFN Package	46	4

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. θ_{JC}, "case temperature" location is at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

Electrical Specifications

Typical values are tested at VIN = 5V and 25°C Ambient Temperature, maximum and minimum values are guaranteed over 0°C to 70°C Ambient Temperature with a supply voltage in the range of 4.3V to 6.5V, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER-ON RESET						
Rising VIN Threshold			3.0	3.4	3.95	V
Falling VIN Threshold			2.25	2.4	2.65	V
STANDBY CURRENT						
VBAT Pin Sink Current	$I_{STANDBY}$	VIN floating or EN = LOW	-	-	3.0	µA
VIN Pin Supply Current	I_{VIN}	VBAT floating and EN pulled low	-	30	-	µA
VIN Pin Supply Current	I_{VIN}	VBAT floating and EN floating	-	1	-	mA
VOLTAGE REGULATION						
Output Voltage	V_{CH}		4.20	4.256	4.30	V
Dropout Voltage		VBAT = 3.7V, 0.5A	-	175	-	mV
CHARGE CURRENT						
Constant Charge Current (Note 3)	I_{CHARGE}	R_{IREF} = 80kΩ, V_{BAT} = 3.7V	0.9	1.0	1.1	A
Trickle Charge Current	$I_{TRICKLE}$	R_{IREF} = 80kΩ, V_{BAT} = 2.0V	-	110	-	mA
End-of-Charge Threshold	I_{MIN}	R_{IREF} = 80kΩ	85	110	135	mA
RECHARGE THRESHOLD						
Recharge Voltage Threshold	V_{RECHRG}		3.90	4.053	4.155	V
TRICKLE CHARGE THRESHOLD						
Trickle Charge Threshold Voltage	V_{MIN}		2.73	2.84	3.04	V
TEMPERATURE MONITORING						
Charge Current Foldback Threshold (Note 4)	T_{FOLD}		85	100	115	°C
Current Foldback Gain (Note 4)	G_{FOLD}		-	100	-	mA/°C

Electrical Specifications Typical values are tested at VIN = 5V and 25°C Ambient Temperature, maximum and minimum values are guaranteed over 0°C to 70°C Ambient Temperature with a supply voltage in the range of 4.3V to 6.5V, unless otherwise noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR						
Oscillation Period	T_{OSC}	C_{TIME} = 15nF	2.4	3.0	3.6	ms
LOGIC OUTPUTS						
STATUS/FAULT Sink Current		Pin Voltage = 0.8V	5	-	-	mA

NOTES:

3. The actual charge current may be affected by the thermal foldback function if the thermal dissipation capability is not enough or by the on resistance of the power MOSFET if the charger input voltage is too close to the output voltage.
4. Guaranteed by design, not a tested parameter.

Pin Descriptions

VIN (Pin 1)

VIN is the input power source. Connect to a wall adapter.

FAULT (Pin 2)

FAULT is an open-drain output indicating fault status. This pin is pulled to LOW under any fault conditions. Any time a FAULT condition happens, it will reset the counter of the charger.

STATUS (Pin 3)

STATUS is an open-drain output indicating charging and inhibit states. The STATUS pin is pulled LOW when the charger is charging a battery. It will be forced to high impedance when the charge current drops to I_{MIN}. This high impedance mode will be latched until a recharge cycle or a new charge cycle starts.

TIME (Pin 4)

The TIME pin determines the oscillation period by connecting a timing capacitor between this pin and GND. The oscillator also provides a time reference for the charger.

GND (Pin 5)

GND is the connection to system ground.

EN (Pin 6)

EN is the enable logic input. Connect the EN pin to LOW to disable the charger or leave it floating to enable the charger.

V2P8 (Pin 7)

This is a 2.8V reference voltage output. This pin outputs a 2.8V voltage source when the input voltage is above POR threshold, otherwise it outputs zero. The V2P8 pin can be used as an indication for adapter presence.

IREF (Pin 8)

This is the programming input for the constant charging current. It maintains at 0.8V when the charger is in normal operation.

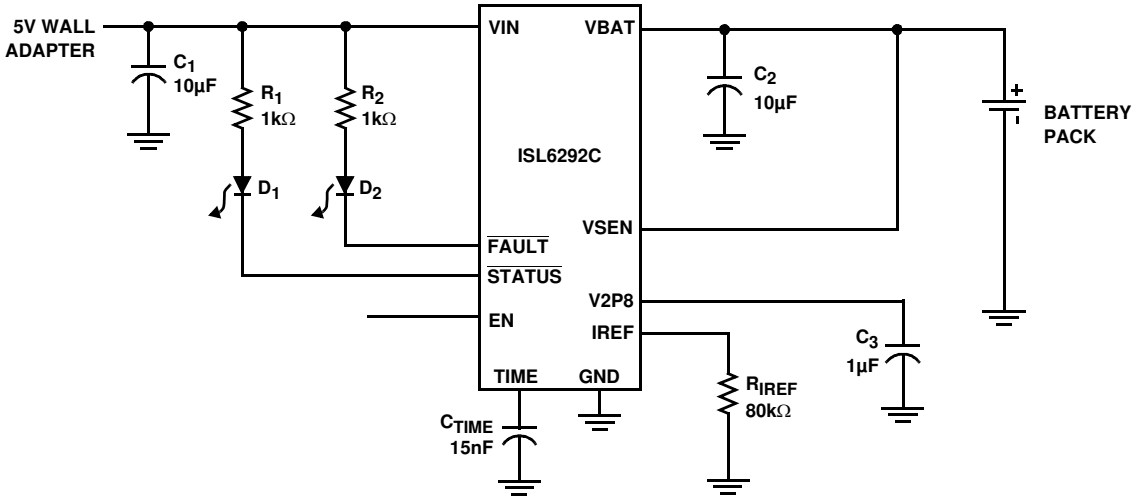
VSEN (Pin 9)

VSEN is the remote voltage sense pin. Connect this pin as close as possible to the battery pack positive connection. If the VSEN pin is floating, its voltage drops to zero volt and the charger operates in the Trickle mode.

VBAT (Pin 10)

VBAT is the connection to the battery. Typically a 10μF Tantalum capacitor is needed for stability when there is no battery attached. When a battery is attached, only a 0.1μF ceramic capacitor is required.

Typical Applications



Block Diagram

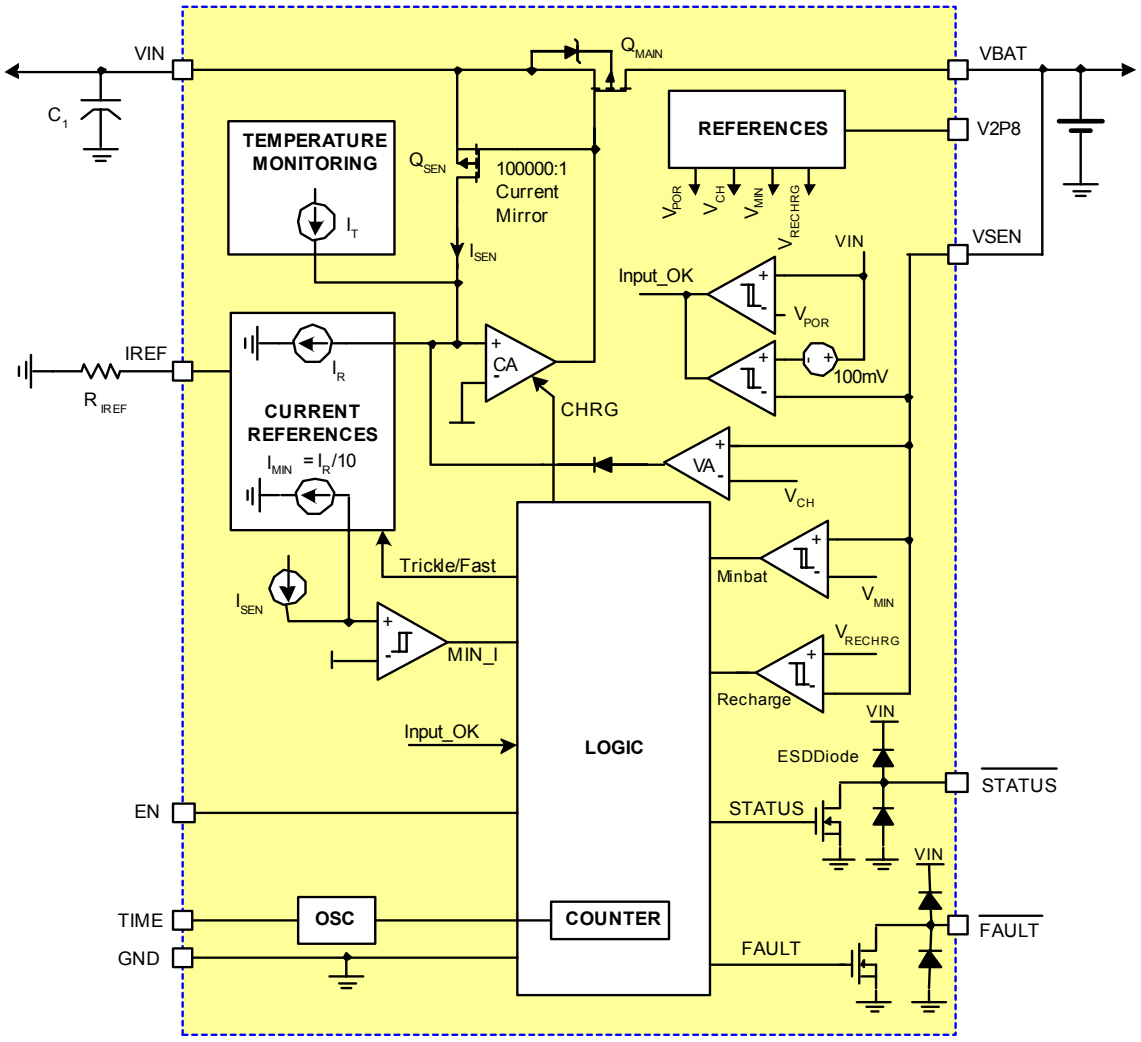


FIGURE 1. BLOCK DIAGRAM

Charging Flow Chart

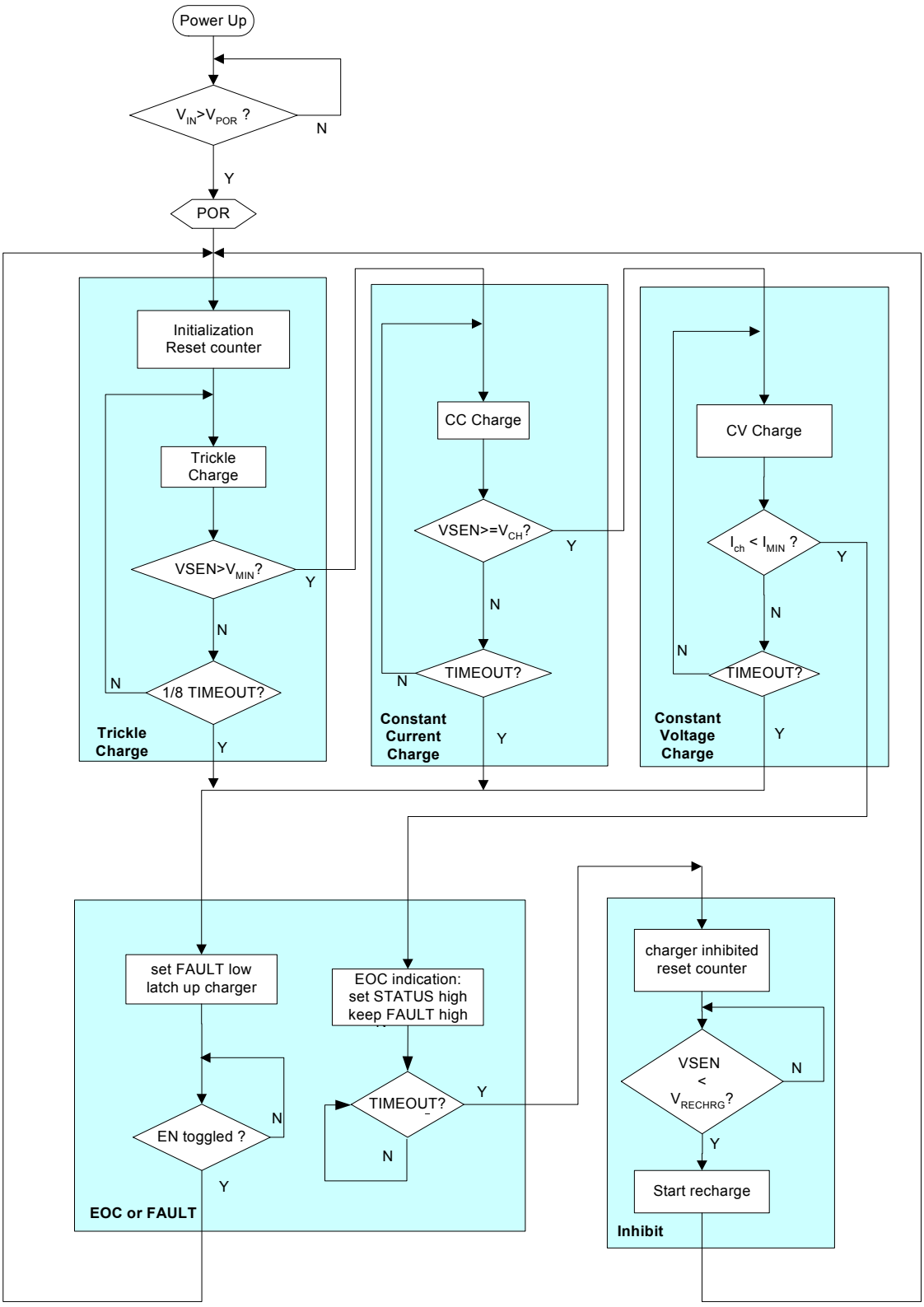


FIGURE 2. CHARGING FLOW CHART

Theory of Operation

The ISL6292C is an integrated charger for single-cell Li-ion or Li-polymer batteries. The ISL6292C functions as a traditional linear charger when powered with a voltage-source adapter. When powered with a current-limited adapter, the charger minimizes the thermal dissipation commonly seen in traditional linear chargers.

As a linear charger, the ISL6292C charges a battery in the popular constant current (CC) and constant voltage (CV) profile. The constant charge current I_{REF} is programmable up to 1.5A with an external resistor. The charge voltage V_{CH} has 1% accuracy over the entire recommended operating condition range. The charger always preconditions the battery with 10% of the programmed current at the beginning of a charge cycle, until the battery voltage is verified to be above the minimum fast charge voltage, V_{MIN}. This low-current preconditioning charge mode is named trickle mode. The verification takes 15 cycles of an internal oscillator whose period is programmable with the timing capacitor. A thermal-foldback feature removes the thermal concern typically seen in linear chargers. The charger reduces the charge current automatically as the IC internal temperature rises above 100°C to prevent further temperature rise. The thermal-foldback feature guarantees safe operation when the printed circuit board (PCB) is space limited for thermal dissipation.

The charger offers a safety timer for setting the fast charge time (TIMEOUT) limit to prevent charging a dead battery for an extensively long time. The trickle mode is limited to 1/8 of TIMEOUT.

The charger automatically re-charges the battery when the battery voltage drops below a recharge threshold. When the wall adapter is not present, the ISL6292C draws less than 1µA current from the battery.

Three indication pins are available from the charger to indicate the charge status. The V2P8 outputs a 2.8V dc voltage when the input voltage is above the power-on reset (POR) level and can be used as the power-present indication. This pin is capable of sourcing a 2mA current, so it can also be used to bias external circuits.

The STATUS pin is an open-drain logic output that turns LOW at the beginning of a charge cycle until the end-of-charge (EOC) condition is qualified. The EOC condition is: the battery voltage rises above the recharge threshold and the charge current falls below a user-programmable EOC current threshold. Once the EOC condition is qualified, the STATUS output rises to HIGH and is latched. The latch is released at the beginning of a charge or re-charge cycle. The open-drain FAULT pin turns low when a charge time fault occurs or when the IREF pin is pulled below 0.35V or above 1.4V.

Figure 3 shows the typical charge curves in a traditional linear charger powered with a constant-voltage adapter. From the top to bottom, the curves represent the constant input voltage, the battery voltage, the charge current and the power dissipation in the charger. The power dissipation P_{CH} is given by the following equation:

$$P_{CH} = (V_{IN} - V_{BAT}) \cdot I_{CHARGE} \quad \text{(EQ. 1)}$$

where I_{CHARGE} is the charge current. The maximum power dissipation occurs during the beginning of the CC mode. The maximum power the IC is capable of dissipating is dependent on the thermal impedance of the printed-circuit board (PCB). Figure 3 shows, with dotted lines, two cases that the charge currents are limited by the maximum power dissipation capability due to the thermal foldback.

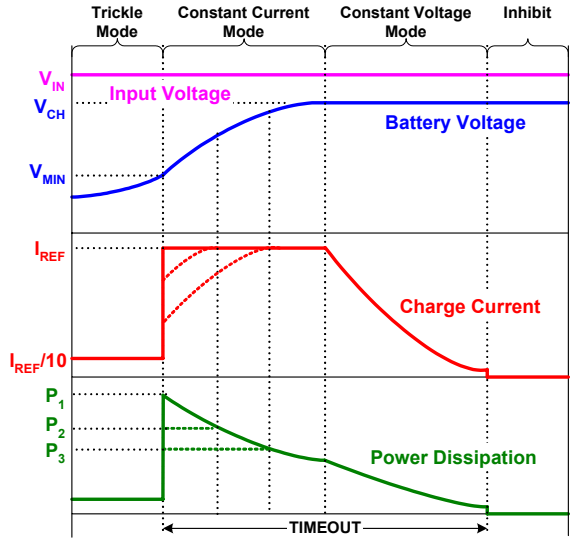


FIGURE 3. TYPICAL CHARGE CURVES USING A CONSTANT-VOLTAGE ADAPTER

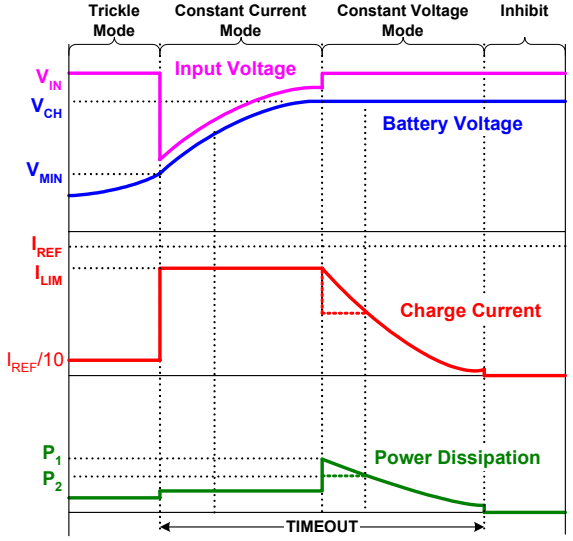


FIGURE 4. TYPICAL CHARGE CURVES USING A CURRENT-LIMITED ADAPTER

When using a current-limited adapter, the thermal situation in the ISL6292C is totally different. Figure 4 shows the typical charge curves when a current-limited adapter is employed. The operation requires the I_{REF} to be programmed higher than the limited current I_{LIM} of the adapter, as shown in Figure 4. The key difference of the charger operating under such conditions occurs during the CC mode.

The Block Diagram, Figure 1, aids in understanding the operation. The current loop consists of the current amplifier CA and the sense MOSFET Q_{SEN}. The current reference I_R is programmed by the IREF pin. The current amplifier CA regulates the gate of the sense MOSFET Q_{SEN} so that the sensed current I_{SEN} matches the reference current I_R. The main MOSFET Q_{MAIN} and the sense MOSFET Q_{SEN} form a current mirror with a ratio of 100,000:1, that is, the output charge current is 100,000 times I_R. In the CC mode, the current loop tries to increase the charge current by enhancing the sense MOSFET Q_{SEN}, so that the sensed current matches the reference current. On the other hand, the adapter current is limited, the actual output current will never meet what is required by the current reference. As a result, the current error amplifier CA keeps enhancing the Q_{SEN} as well as the main MOSFET Q_{MAIN}, until they are fully turned on. Therefore, the main MOSFET becomes a power switch instead of a linear regulation device. The power dissipation in the CC mode becomes:

$$P_{CH} = R_{DS(ON)} \cdot I_{CHARGE}^2 \quad \text{(EQ. 2)}$$

where $R_{DS(ON)}$ is the resistance when the main MOSFET is fully turned on. This power is typically much less than the peak power in the traditional linear mode.

The worst power dissipation when using a current-limited adapter typically occurs at the beginning of the CV mode, as shown in Figure 4. The equation 1 applies during the CV mode. When using a very small PCB whose thermal impedance is relatively large, it is possible that the internal temperature can still reach the thermal foldback threshold. In that case, the IC is thermally protected by lowering the charge current, as shown by the dotted lines in the charge current and power curves. Appropriate design of the adapter can further reduce the peak power dissipation of the ISL6292C. See the Application Information section of the ISL6292 data sheet (www.intersil.com) for more information.

Figure 5 illustrates the typical signal waveforms for the linear charger from the power-up to a recharge cycle. More detailed Applications Information is given below.

Applications Information

Power on Reset (POR)

The ISL6292C resets itself as the input voltage rises above the POR rising threshold. The V2P8 pin outputs a 2.8V voltage, the internal oscillator starts to oscillate, the internal timer is reset, and the charger begins to charge the battery. The two indication pins, STATUS and FAULT, indicate a LOW and a HIGH logic signal respectively. Figure 5 illustrates the start up of the charger between t_0 to t_2.

The ISL6292C has a typical rising POR threshold of 3.4V and a falling POR threshold of 2.4V. The 2.4V falling threshold guarantees charger operation with a current-limited adapter to minimize the thermal dissipation.

Charge Cycle

A charge cycle consists of three charge modes: trickle mode, constant current (CC) mode, and constant voltage (CV) mode. The charge cycle always starts with the trickle mode until the battery voltage stays above V_{MIN} (2.84V typical) for 15 consecutive cycles of the internal oscillator. If the battery voltage drops below V_{MIN} during the 15 cycles, the 15-cycle counter is reset and the charger stays in the trickle mode. The charger moves to the CC mode after verifying the battery voltage. As the battery-pack terminal voltage rises to the final charge voltage V_{CH}, the CV mode begins. The terminal voltage is regulated at the constant V_{CH} in the CV mode and the charge current is expected to decline. After the charge current drops below I_{MIN} (1/10 of I_{REF}, see End-of-Charge Current for more detail), the ISL6292C indicates the end-of-charge (EOC) with the STATUS pin. The charging actually does not terminate until the internal timer completes its length of TIMEOUT in order to bring the battery to its full capacity. Signals in a charge cycle are illustrated in Figure 5 between points t_2 to t_5.

The following events initiate a new charge cycle:

- POR,
- the battery voltage drops below a recharge threshold after completing a charge cycle,
- or, the EN pin is toggled from GND to floating.

Further description of these events are given later in this data sheet.

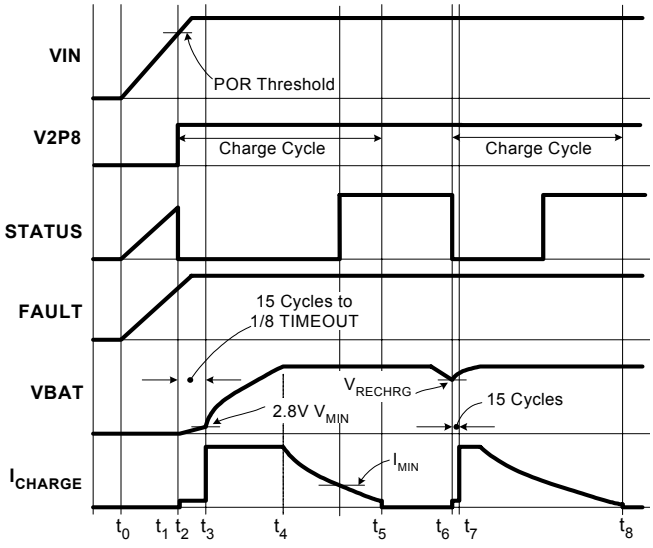


FIGURE 5. OPERATION WAVEFORMS

Recharge

After a charge cycle completes, charging is prohibited until the battery voltage drops to a recharge threshold, V_{RECHRG} (see Electrical Specifications). Then a new charge cycle starts at point t_6 and ends at point t_8, as shown in Figure 5. The safety timer is reset at t_6.

Internal Oscillator

The internal oscillator establishes a timing reference. The oscillation period is programmable with an external timing capacitor, C_{TIME}, as shown in Typical Applications. The oscillator charges the timing capacitor to 1.5V and then discharges it to 0.5V in one period, both with 10µA current. The period T_{OSC} is:

$$T_{OSC} = 0.2 \cdot 10^6 \cdot C_{TIME} \quad (\text{seconds}) \qquad \text{(EQ. 3)}$$

A 1nF capacitor results in a 0.2ms oscillation period. The accuracy of the period is mainly dependent on the accuracy of the capacitance and the internal current source.

Total Charge Time

The total charge time for the CC mode and CV mode is limited to a length of TIMEOUT. A 22-stage binary counter increments each oscillation period of the internal oscillator to set the TIMEOUT. The TIMEOUT can be calculated as:

$$TIMEOUT = 2^{22} \cdot T_{OSC} = 14 \cdot \frac{C_{TIME}}{1nF} \quad (\text{minutes}) \qquad \text{(EQ. 4)}$$

A 1nF capacitor leads to 14 minutes of TIMEOUT. For example, a 15nF capacitor sets the TIMEOUT to be 3.5 hours. The charger has to reach the end-of-charge condition before the TIMEOUT, otherwise, a TIMEOUT fault is issued. The TIMEOUT fault latches up the charger. There are two ways to release such a latch-up: either to recycle the input power, or toggle the EN pin to disable the charger and then enable it again.

The trickle mode charge has a time limit of 1/8 TIMEOUT. If the battery voltage does not reach V_{MIN} within this limit, a TIMEOUT fault is issued and the charger latches up. The charger stays in trickle mode for at least 15 cycles of the internal oscillator and, at most, 1/8 of TIMEOUT, as shown in Figure 5.

Charge Current Programming

The charge current in the CC mode is programmed by the IREF pin. The voltage of IREF is regulated to a 0.8V reference voltage. The charging current during the constant current mode is 100,000 times that of the current in the R_{IREF} resistor. Hence, the charge current is,

$$I_{REF} = \frac{0.8V}{R_{IREF}} \times 10^5 (A) \qquad \text{(EQ. 5)}$$

TABLE 1. CHARGE CURRENT vs R_{IREF} VALUES (Note)

R_{IREF} (kΩ)	CHARGE CURRENT (mA)		
	MIN	TYP	MAX
267	250	300	350
160	450	500	550
100	720	800	880
88.9	810	900	990
80	900	1000	1100

NOTE: The limits are still preliminary. Additional samples will be tested for the final results.

Table 1 shows the charge current vs. selected R_{IREF} values.

The ISL6292C is designed to be safe when the IREF pin is accidentally short-circuited to an external source or to ground. If the IREF pin is driven by an external source to below 0.38V or above 1.5V for any reason, the charger is disabled and the FAULT pin turns to LOW to indicate a fault condition. The charger will resume charging after the fault condition is removed. When the IREF is driven by a voltage between 0.38V to 0.5V (typical value), the charge current is limited to 100mA; or when driven to a voltage between 1.2V to 1.5V, the charge current is limited to 500mA. For any voltage between 0.5V to 1.2V, the charge current will drop to a very low value. This feature can protect the charger from a large charging current when IREF is accidentally shorted to ground or to a high voltage. Figure 6 shows the charge current when the IREF pin voltage is driven from 0V to 3V.

End-of-Charge (EOC) Current

The EOC current I_{MIN} sets the level at which the charger starts to indicate the end of the charge with the STATUS pin, as shown in Figure 5. The charger actually does not terminate charging until the end of the TIMEOUT, as described in the Total Charge Time section. In the

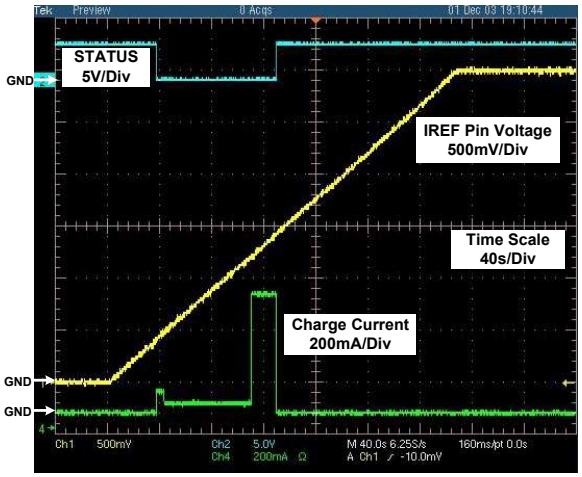


FIGURE 6. CHARGE CURRENT WHEN IREF PIN IS DRIVEN BY AN EXTERNAL VOLTAGE SOURCE

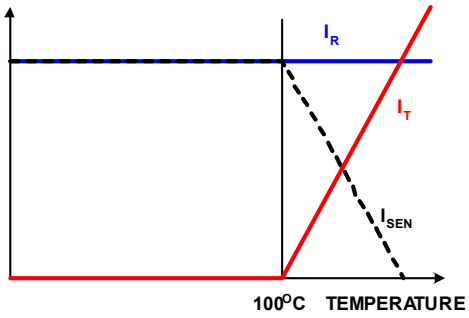


FIGURE 7. CURRENT SIGNALS AT THE AMPLIFIER CA INPUT.

ISL6292C, the EOC current is internally set to 1/10 of the CC charge current, that is,

$$I_{MIN} = \frac{1}{10} \cdot I_{REF} \quad \text{(EQ. 6)}$$

At the EOC, the STATUS signal rises to HIGH and is latched. The latch is not reset until a recharge cycle or a new charge cycle starts.

Charge Current Thermal Foldback

Over-heating is always a concern in a linear charger. The maximum power dissipation usually occurs at the beginning of a charge cycle when the battery voltage is at its minimum but the charge current is at its maximum. The charge current thermal foldback function in the ISL6292C frees users from the over-heating concern.

Figure 7 shows the current signals at the summing node of the current error amplifier CA in the Block Diagram. I_R is the reference. I_T is the current from the Temperature Monitoring block. The I_T has no impact on the charge current until the internal temperature reaches approximately 100°C; then I_T rises at a rate of 1µA/°C. When I_T rises, the current control loop forces the sensed current I_{SEN} to reduce at the same rate. As a mirrored current, the charge current is 100,000 times that of the sensed current and reduces at a rate of 100mA/°C. For a charger with the constant charge current set at 1A, the charge current is reduced to zero when the internal temperature rises to 110°C. The actual charge current settles between 100°C to 110°C.

Usually the charge current should not drop below I_{MIN} because of the thermal foldback. For some extreme cases if that does happen, the charger does not indicate end-of-charge unless the battery voltage is already above the recharge threshold.

2.8V Bias Voltage

The ISL6292C provides a 2.8V voltage for biasing the internal control and logic circuit. This voltage is also available for external circuits such as the NTC thermistor circuit. The maximum allowed external load is 2mA.

Indications

The ISL6292C has three indications: the input presence, the charge status, and the fault indication. The input presence is indicated by the V2P8 pin while the other two indications are presented by the STATUS pin and FAULT pin respectively. Figure 8 shows the V2P8 pin voltage vs. the input voltage. Table 2 summarizes the other two pins.

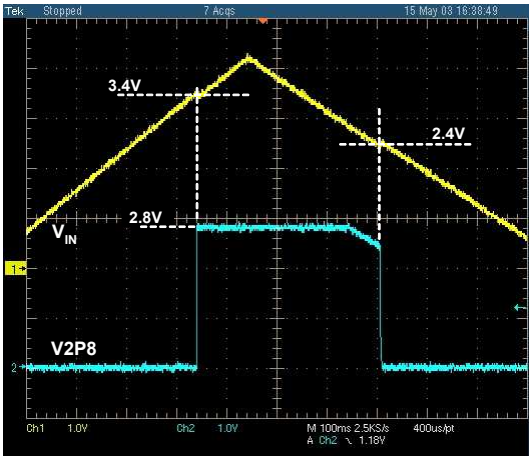


FIGURE 8. THE V2P8 PIN OUTPUT vs THE INPUT VOLTAGE AT THE VIN PIN. VERTICAL: 1V/DIV, HORIZONTAL: 100ms/DIV

TABLE 2. STATUS INDICATIONS

FAULT	STATUS	INDICATION
High	High	Charge completed with no fault (Inhibit) or Standby
High	Low	Charging in one of the three modes
Low	High	Fault

NOTE: Both outputs are pulled up with external resistors.

Shutdown

The ISL6292C can be shutdown by pulling the EN pin to ground. When shut down, the charger draws typically less than 30µA current from the input power and the 2.8V output at the V2P8 pin is also turned off. The EN pin needs be driven with an open-drain or open-collector logic output, so that the EN pin is floating when the charger is enabled. If the EN pin is driven by an external source, the POR threshold voltage will be affected.

Input and Output Capacitor Selection

Typically any type of capacitors can be used for the input and the output. Use of a 0.47µF or higher value ceramic capacitor for the input is recommended. When the battery is attached to the charger, the output capacitor can be any ceramic type with the value higher than 0.1µF. However, if there is a chance the charger will be used as an LDO linear regulator, a 10µF tantalum capacitor is recommended.

Stability With Large Ceramic Output Capacitors

The ISL6292C partially relies on the ESR (equivalent series resistance) of the output capacitor for the loop stability. When the system has a large ceramic capacitor or a number of ceramic capacitors in parallel, the ESR value can be too low for a stable operation. A low-value resistor should be inserted between the sensed feedback (VSEN pin) and the external large-value ceramic capacitor to improve the stability, as shown in Figure 9.

In applications that have a sense resistor between the VBAT pin and the VSEN pin, such as the R_1 shown in Figure 10, two small resistors can be used to create an equivalent low value resistor between the VSEN pin and the large capacitor, to avoid another more expensive low-value sense resistor. R_2 and R_3 in Figure 10 show how the two resistors are connected. The equivalent low-value resistance is,

$$R_{eq} = \frac{R_3}{R_2 + R_3} \cdot R_1 \qquad \text{(EQ. 7)}$$

The value of (R_2 + R_3) should be significantly larger than that of the sense resistor R_1 to minimize the accuracy of the current sensing. The parallel value of R_2 and R_3 should be significantly smaller than 72kΩ (internal resistive divider value for setting the charger output voltage) to minimize the impact on the output voltage. Figure 10 shows two 20Ω resistor. The sum is 40Ω, much higher than the 150mΩ R_1. The parallel value is 10Ω, negligible compared to the 72kΩ resistive divider. Such a selection is a good trade-off to result in 75mΩ equivalent low-value resistance between the VSEN pin and the large capacitor.

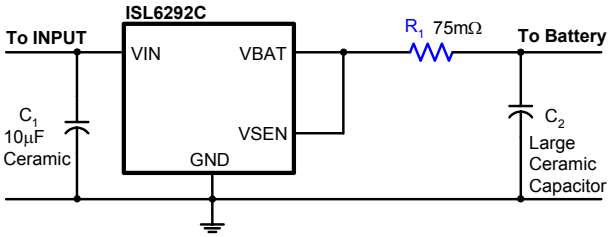


FIGURE 9. INSERTING R_1 TO IMPROVE THE STABILITY OF APPLICATIONS WITH LARGE CERAMIC CAPACITOR IS USED AT THE OUTPUT

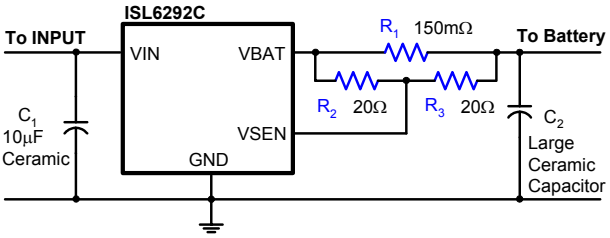


FIGURE 10. THE CIRCUIT TO GENERATE THE EQUIVALENT LOW-VALUE RESISTOR

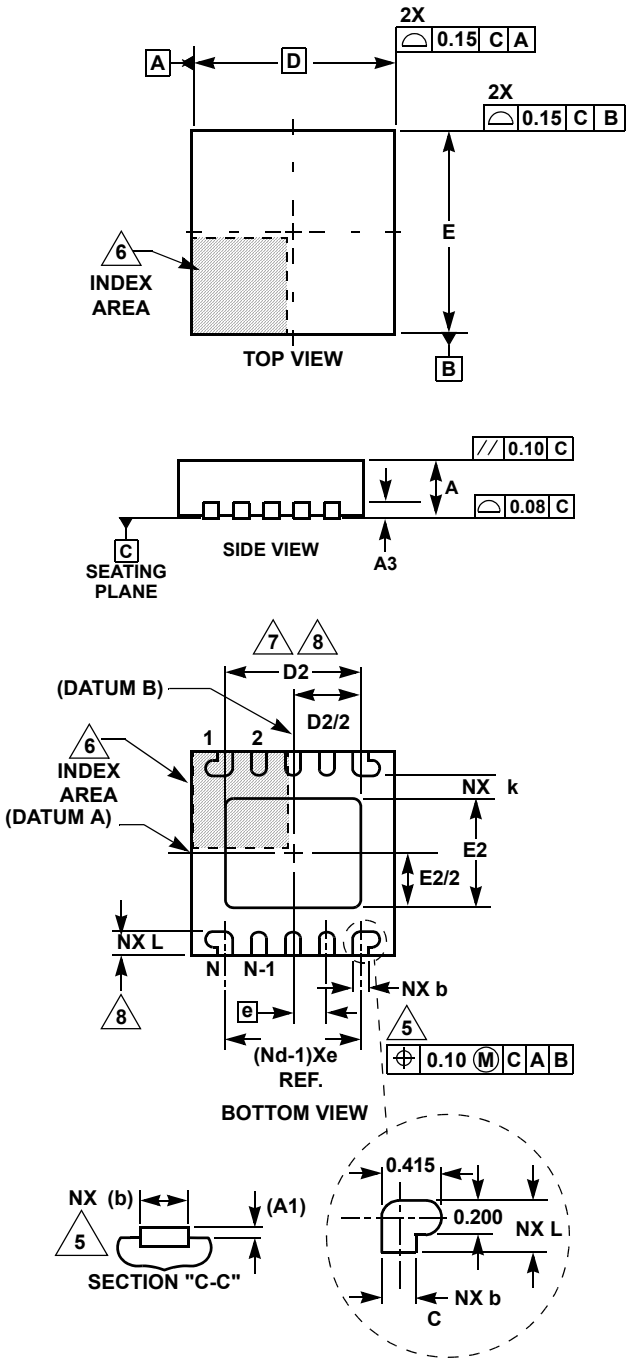
Working with Current-Limited Adapter

The ISL6292C can work with a current-limited adapter to significantly reduce the thermal dissipation during charging. Refer to the ISL6292 data sheet, which can be found at http://www.intersil.com, for more details.

Board Layout Recommendations

The ISL6292C internal thermal foldback function limits the charge current when the internal temperature reaches approximately 100°C. In order to maximize the current capability, it is very important that the exposed pad under the package is properly soldered to the board and is connected to other layers through thermal vias. More thermal vias and more copper attached to the exposed pad usually result in better thermal performance. On the other hand, the number of vias is limited by the size of the pad. The 3x3 DFN package allows 8 vias be placed in two rows. Since the pins on the 3x3 DFN package are on only two sides, as much top layer copper as possible should be connected to the exposed pad to minimize the thermal impedance. Refer to the ISL6292 evaluation boards for layout examples.

Dual Flat No-Lead Plastic Package (DFN)



L10.3x3

10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.18	0.23	0.28	5,8
D		3.00 BSC		-
D2	1.95	2.00	2.05	7,8
E		3.00 BSC		-
E2	1.55	1.60	1.65	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.35	0.40	8
N		10		2
Nd		5		3

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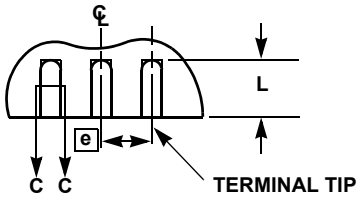
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.



FOR ODD TERMINAL/SIDE