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Four-Phase Buck PWM Controller with Integrated MOSFET Drivers and I²C Interface for Intel VR10, VR11, and AMD Applications

The ISL6322 four-phase PWM control IC provides a precision voltage regulation system for advanced microprocessors. The integration of power MOSFET drivers into the controller IC marks a departure from the separate PWM controller and driver configuration of previous multiphase product families. By reducing the number of external parts, this integration is optimized for a cost and space saving power management solution.

One outstanding feature of this controller IC is its multi-processor compatibility, allowing it to work with both Intel and AMD microprocessors. Included are programmable VID codes for Intel VR10, VR11, as well as AMD DAC tables. A unity gain, differential amplifier is provided for remote voltage sensing, compensating for any potential difference between remote and local grounds. The output voltage can also be positively or negatively offset through the use of a single external resistor.

The ISL6322 includes an I²C interface, allowing the controller to communicate with other devices over an I²C bus. Signals sent over this bus can command the ISL6322 to adjust voltage margining offset, converter switching frequency, and overvoltage protection levels, and can select the integrated driver adaptive dead time scheme.

The ISL6322 also includes advanced control loop features for optimal transient response to load apply and removal. One of these features is highly accurate, fully differential, continuous DCR current sensing for load line programming and channel current balance. Active Pulse Positioning (APP) modulation is another unique feature, allowing for quicker initial response to high di/dt load transients.

This controller also allows the user the flexibility to choose between PHASE detect or LGATE detect adaptive dead time schemes. This ability allows the ISL6322 to be used in a multitude of applications where either scheme is required.

Protection features of this controller IC include a set of sophisticated overvoltage, undervoltage, and overcurrent protection. Furthermore, the ISL6322 includes protection against an open circuit on the remote sensing inputs. Combined, these features provide advanced protection for the microprocessor and power system.

Features

- Integrated Multiphase Power Conversion
 - 2-Phase or 3-Phase Operation with Internal Drivers
 - 4-Phase Operation with External PWM Driver Signal
- Precision Core Voltage Regulation
 - Differential Remote Voltage Sensing
 - ±0.5% System Accuracy Over-Temperature
 - Adjustable Reference-Voltage Offset
- Optimal Transient Response
 - Active Pulse Positioning (APP) Modulation
 - Adaptive Phase Alignment (APA)
- Fully Differential, Continuous DCR Current Sensing
 - Accurate Load Line Programming
 - Precision Channel Current Balancing
- I²C Interface
 - Voltage Margining Offset
 - Switching Frequency Adjustment
 - Overvoltage Protection Level Adjustment
 - Selects Adaptive Dead Time Scheme
- User Selectable I²C “Slave Only” Device Address: 1000_110x or 1000_111x
- User Selectable Adaptive Dead Time Scheme
 - PHASE Detect or LGATE Detect for Application Flexibility
- Variable Gate Drive Bias: 5V to 12V
- Multi-Processor Compatible
 - Intel VR10 and VR11 Modes of Operation
 - AMD Mode of Operation
- Microprocessor Voltage Identification Inputs
 - 8-bit DAC
 - Selectable between Intel’s Extended VR10, VR11, AMD 5-bit, and AMD 6-bit DAC Tables
 - Dynamic VID Technology
- Overcurrent Protection
- Multi-Tiered Overvoltage Protection
- Digital Soft-Start
- Selectable Operation Frequency up to 1.5MHz Per Phase
- Pb-Free Plus Anneal Available (RoHS Compliant)

ISL6322

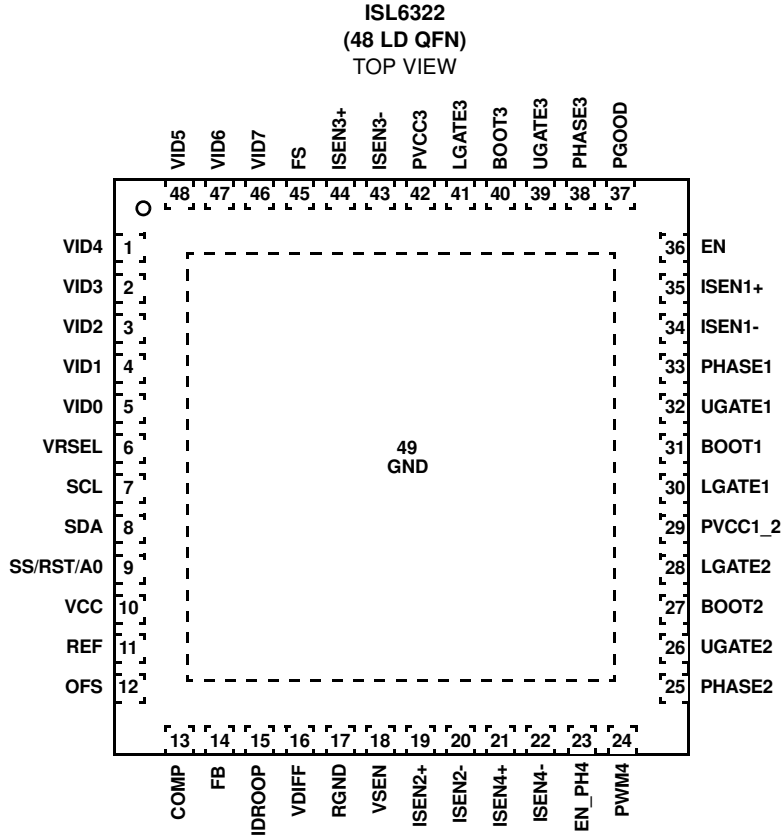
Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6322CRZ*	ISL6322 CRZ	0 to +70	48 Ld 7x7 QFN	L48.7x7
ISL6322IRZ*	ISL6322 IRZ	-40 to +85	48 Ld 7x7 QFN	L48.7x7

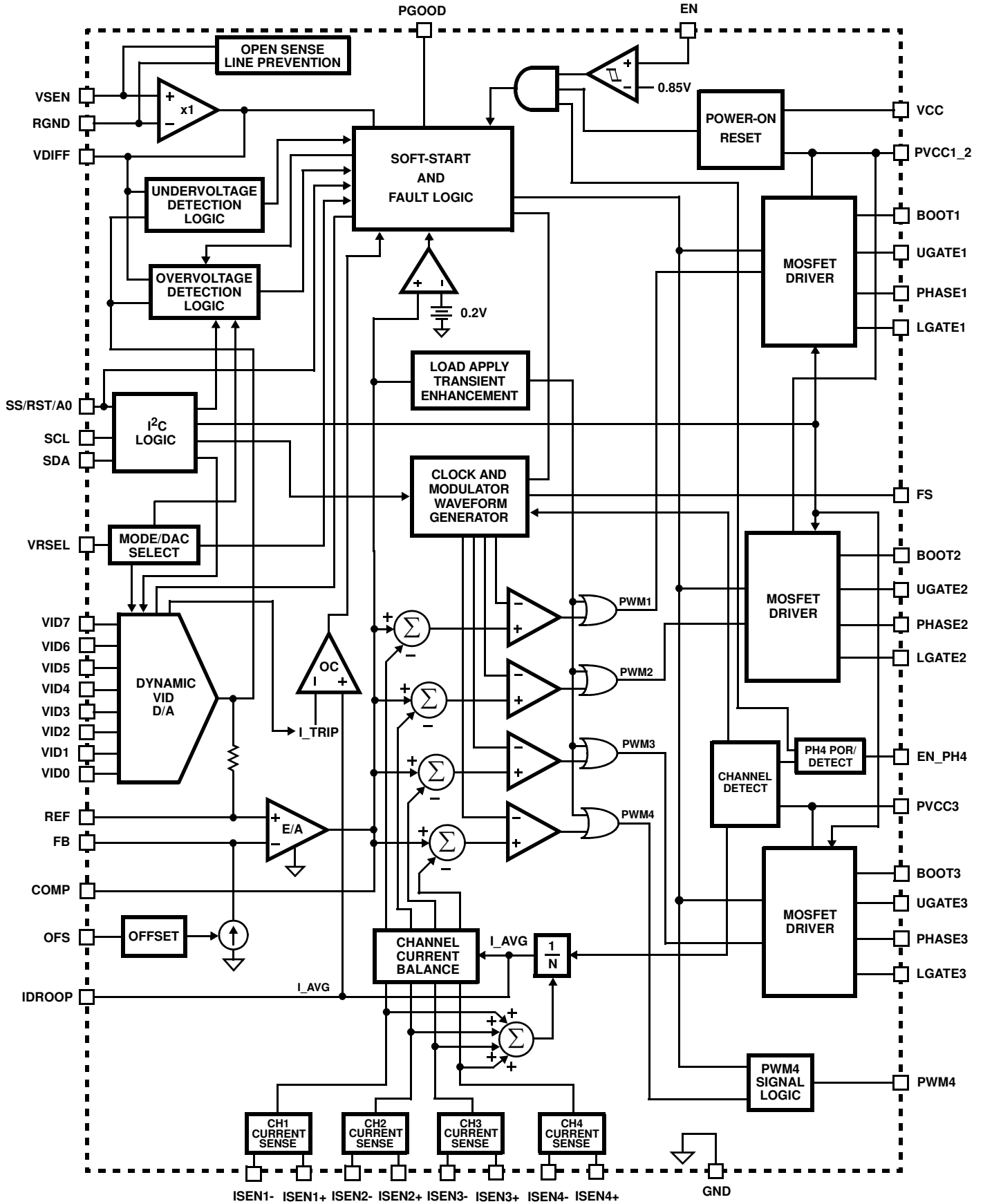
*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

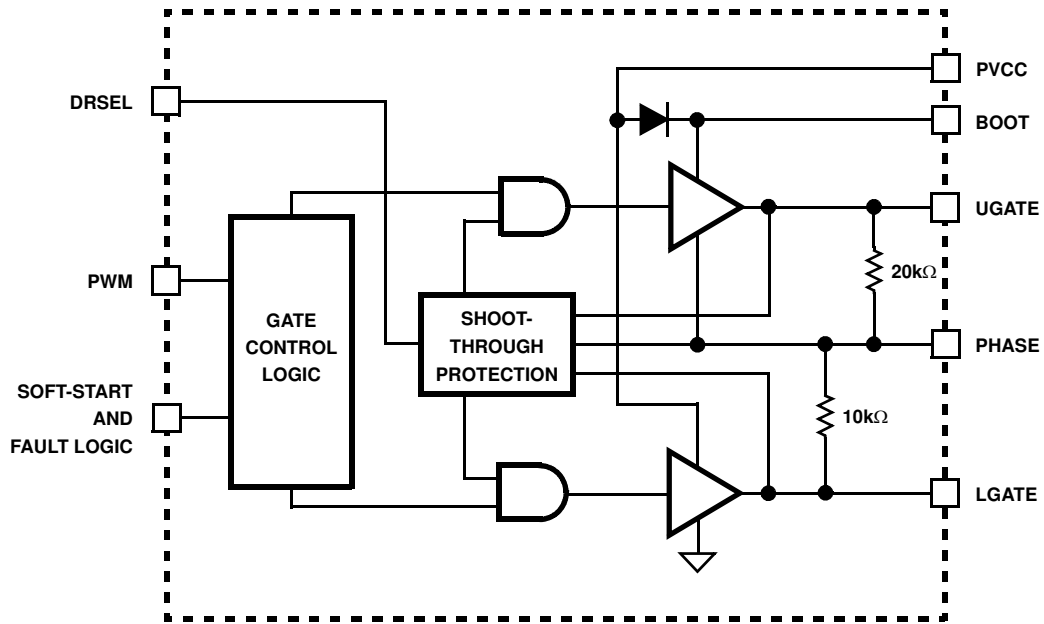
Pinout



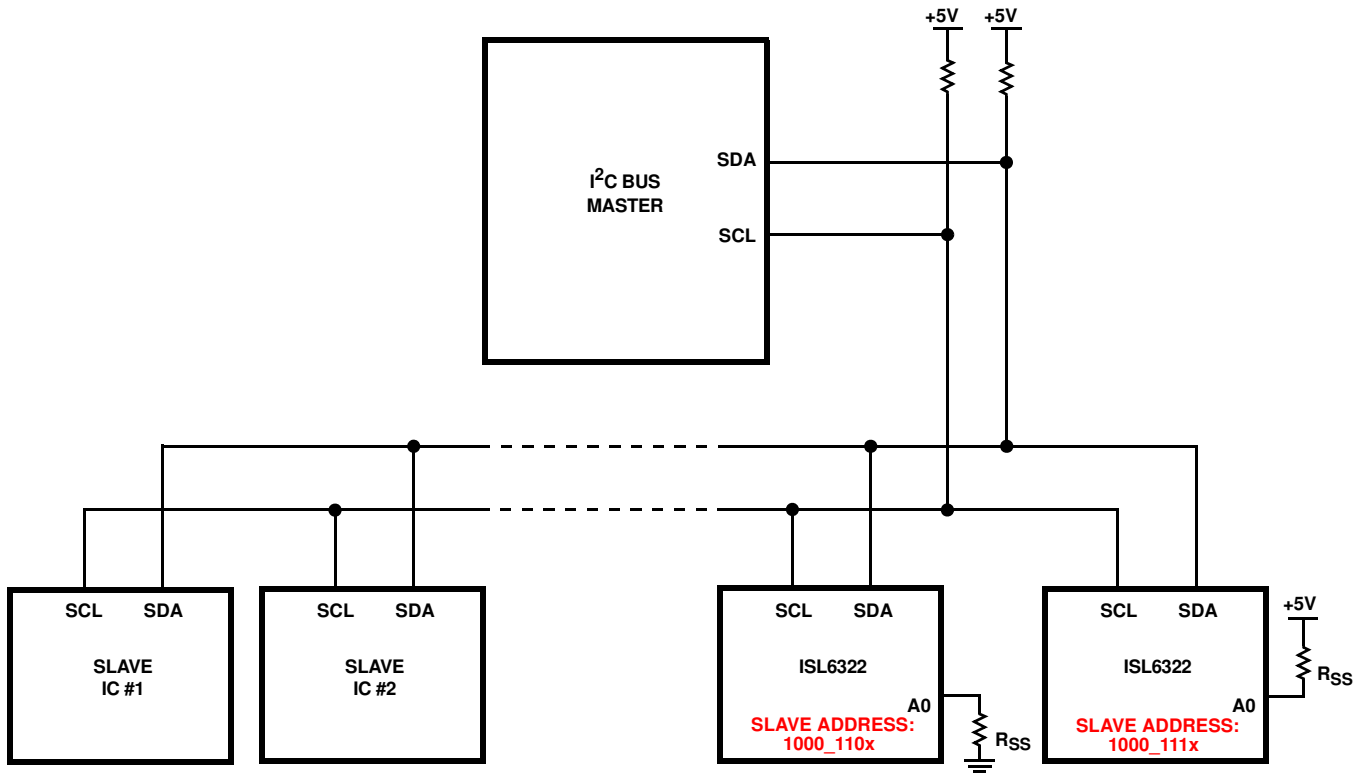
Block Diagram



ISL6322 Integrated Driver Block Diagram

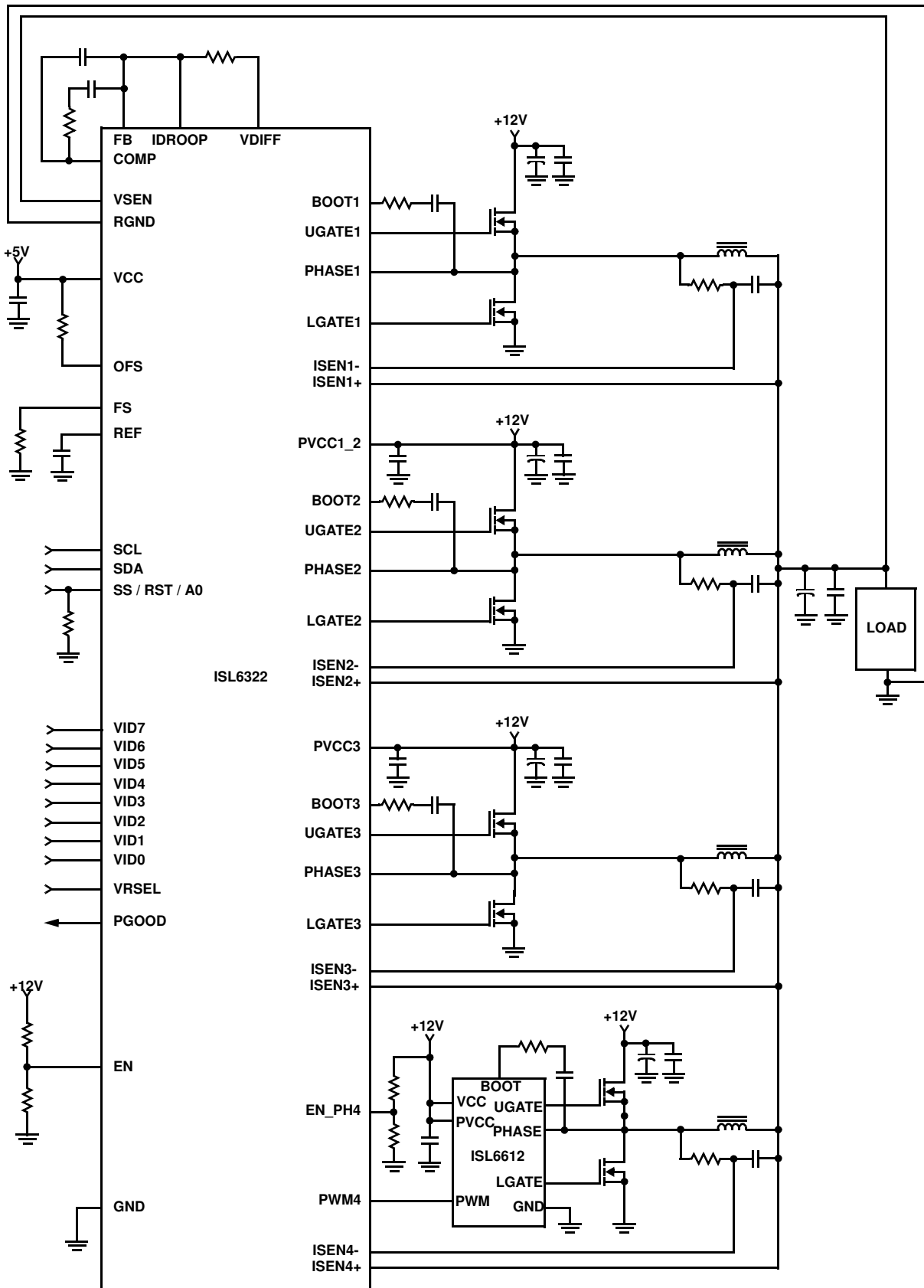


Simplified I²C Bus Architecture



NOTE: PIN A0 SELECTS THE SLAVE ADDRESS FOR THE ISL6322

Typical Application - ISL6322 (4-Phase)



Absolute Maximum Ratings

Supply Voltage, VCC	-0.3V to +6V
Supply Voltage, PVCC	-0.3V to +15V
BOOT Voltage, V _{BOOT}	GND - 0.3V to GND + 36V
BOOT to PHASE Voltage, V _{BOOT} - PHASE	-0.3V to 15V (DC) -0.3V to 16V (<10ns, 10μJ)
PHASE Voltage, V _{PHASE}	GND - 0.3V to 15V (PVCC = 12) GND - 8V (<400ns, 20μJ) to 24V (<200ns, V _{BOOT} - PHASE = 12V)
UGATE Voltage, V _{UGATE}	V _{PHASE} - 0.3V to V _{BOOT} + 0.3V V _{PHASE} - 3.5V (<100ns Pulse Width, 2μJ) to V _{BOOT} + 0.3V
LGATE Voltage, V _{LGATE}	GND - 0.3V to PVCC + 0.3V GND - 5V (<100ns Pulse Width, 2μJ) to PVCC + 0.3V
Input, Output, or I/O Voltage	GND - 0.3V to VCC + 0.3V
ESD Classification	Class I JEDEC STD

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 1, 2)	27	2.5
Maximum Junction Temperature	+150°C	
Maximum Storage Temperature Range	-65°C to +150°C	
Pb-free reflow profile	see link below http://www.intersil.com/pbfree/Pb-FreeReflow.asp	

Recommended Operating Conditions

VCC Supply Voltage	+5V ±5%
PVCC Supply Voltage	+5V to 12V ±5%
Ambient Temperature (ISL6322CRZ)	0°C to +70°C
Ambient Temperature (ISL6322IRZ)	-40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.
- Limits established by characterization and are not production tested.

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
BIAS SUPPLIES					
Input Bias Supply Current	I _{VCC} ; EN = high	15	20	25	mA
Gate Drive Bias Current - PVCC1_2 Pin	I _{PVCC1_2} ; EN = high	2	4.3	6	mA
Gate Drive Bias Current - PVCC3 Pin	I _{PVCC3} ; EN = high	1	2.1	3	mA
VCC POR (Power-On Reset) Threshold	VCC rising	4.25	4.38	4.50	V
	VCC falling	3.75	3.88	4.00	V
PVCC POR (Power-On Reset) Threshold	PVCC rising	4.25	4.38	4.50	V
	PVCC falling	3.60	3.88	4.00	V
PWM MODULATOR					
Oscillator Frequency Accuracy, f _{SW}	R _T = 100kΩ (±0.1%)	225	250	275	kHz
Adjustment Range of Switching Frequency	(Note 3)	0.08		1.0	MHz
Oscillator Ramp Amplitude, V _{PP}	(Note 3)		1.50		V
CONTROL THRESHOLDS					
EN Rising Threshold			0.85		V
EN Hysteresis			110		mV
EN_PH4 Rising Threshold		1.160	1.210	1.250	V
EN_PH4 Falling Threshold		1.00	1.06	1.10	V
COMP Shutdown Threshold	COMP falling	0.1	0.2	0.3	V
REFERENCE AND DAC					
System Accuracy (1.000V to 1.600V)		-0.5		0.5	%
System Accuracy (0.600V to 1.000V)		-1.0		1.0	%
System Accuracy (0.375V - 0.600V)		-2.0		2.0	%
DAC Input Low Voltage (VR10, VR11)				0.4	V
DAC Input High Voltage (VR10, VR11)		0.8			V

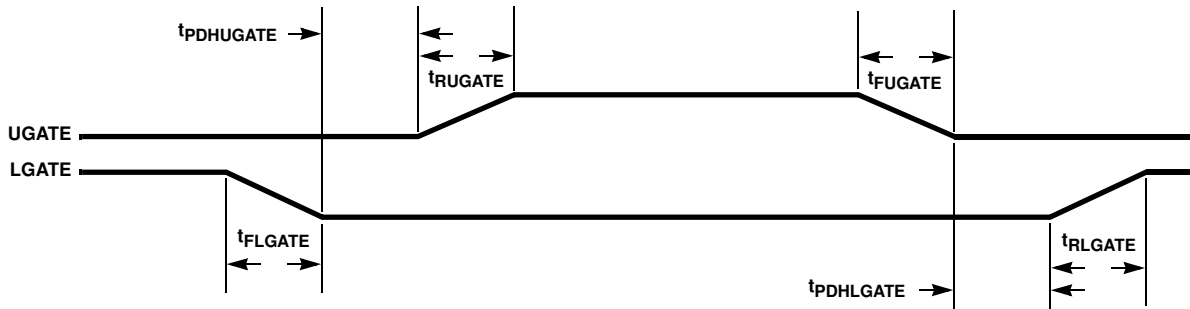
Electrical Specifications Recommended Operating Conditions, Unless Otherwise Specified. (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DAC Input Low Voltage (AMD)				0.6	V
DAC Input High Voltage (AMD)		1.0			V
PIN-ADJUSTABLE OFFSET					
OFS Sink Current Accuracy (Negative Offset)	R _{OFS} = 10kΩ from OFS to GND	37.0	40.0	43.0	μA
OFS Source Current Accuracy (Positive Offset)	R _{OFS} = 30kΩ from OFS to VCC	50.5	53.5	56.5	μA
ERROR AMPLIFIER					
DC Gain	R _L = 10k to ground, (Note 3)		96		dB
Gain-Bandwidth Product	C _L = 100pF, R _L = 10k to ground, (Note 3)		20		MHz
Slew Rate	C _L = 100pF, Load = ±400μA, (Note 3)		8		V/μs
Maximum Output Voltage	Load = 1mA	3.90	4.20		V
Minimum Output Voltage	Load = -1mA		1.30	1.5	V
SOFT-START RAMP					
Soft-Start Ramp Rate	VR10/VR11, R _S = 100kΩ		1.563		mV/μs
	AMD		2.063		mV/μs
Adjustment Range of Soft-Start Ramp Rate (Note 3)		0.625		6.25	mV/μs
PWM OUTPUT					
PWM Output Voltage LOW Threshold	I _{load} = ±500μA			0.5	V
PWM Output Voltage HIGH Threshold	I _{load} = ±500μA	4.5			V
CURRENT SENSING					
Current Sense Resistance, R _{ISEN}	T = +25°C	297	300	303	Ω
Sensed Current Tolerance	I _{SEN1+} = I _{SEN2+} = I _{SEN3+} = I _{SEN4+} = 80μA	76	80	84	μA
OVERCURRENT PROTECTION					
Overcurrent Trip Level - Average Channel	Normal operation	110	125	140	μA
	Dynamic VID change	143	163	183	μA
Overcurrent Trip Level - Individual Channel	Normal operation	150	177	204	μA
	Dynamic VID change (Note 3)	209.4	238	266.6	μA
PROTECTION					
Undervoltage Threshold	V _{SEN} falling	55	60	65	%VID
Undervoltage Hysteresis	V _{SEN} rising		10		%VID
Overvoltage Threshold During Soft-Start	VR10/VR11	1.24	1.28	1.32	V
	AMD	2.13	2.20	2.27	V
Overvoltage Threshold (Default)	V _{SEN} rising	VDAC + 225mV	VDAC + 250mV	VDAC + 275mV	V
Overvoltage Threshold (Alternate)	V _{SEN} rising	VDAC + 150mV	VDAC + 175mV	VDAC + 200mV	V
Overvoltage Hysteresis	V _{SEN} falling		100		mV
SWITCHING TIME (Note 3)					
UGATE Rise Time	t _{RUGATE} ; V _{PVCC} = 12V, 3nF load, 10% to 90%		26		ns
LGATE Rise Time	t _{RLGATE} ; V _{PVCC} = 12V, 3nF load, 10% to 90%		18		ns
UGATE Fall Time	t _{FUGATE} ; V _{PVCC} = 12V, 3nF load, 90% to 10%		18		ns
LGATE Fall Time	t _{FLGATE} ; V _{PVCC} = 12V, 3nF load, 90% to 10%		12		ns

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Specified. (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UGATE Turn-On Non-Overlap	$t_{PDHUGATE}$: $V_{PVCC} = 12V$, 3nF load, adaptive		10		ns
LGATE Turn-On Non-Overlap	$t_{PDHLGATE}$: $V_{PVCC} = 12V$, 3nF load, adaptive		10		ns
GATE DRIVE RESISTANCE (Note 3)					
Upper Drive Source Resistance	$V_{PVCC} = 12V$, 15mA source current	1.25	2.0	3.0	Ω
Upper Drive Sink Resistance	$V_{PVCC} = 12V$, 15mA sink current	0.9	1.65	3.0	Ω
Lower Drive Source Resistance	$V_{PVCC} = 12V$, 15mA source current	0.85	1.25	2.2	Ω
Lower Drive Sink Resistance	$V_{PVCC} = 12V$, 15mA sink current	0.60	0.80	1.35	Ω
OVER TEMPERATURE SHUTDOWN (Note 3)					
Thermal Shutdown Setpoint		-	160	-	$^{\circ}C$
Thermal Recovery Setpoint		-	100	-	$^{\circ}C$

Timing Diagram



Functional Pin Description

VCC

VCC is the bias supply for the IC's small-signal circuitry. Connect this pin to a +5V supply and decouple using a quality 0.1µF ceramic capacitor.

PVCC1_2 and PVCC3

These pins are the power supply pins for the corresponding channel MOSFET drive, and can be connected to any voltage from +5V to +12V depending on the desired MOSFET gate-drive level. Decouple these pins with a quality 1.0µF ceramic capacitor.

Leaving PVCC3 unconnected or grounded programs the controller for 2-phase operation.

GND

GND is the bias and reference ground for the IC.

EN

This pin is a threshold-sensitive (approximately 0.85V) enable input for the controller. Held low, this pin disables controller operation. Pulled high, the pin enables the controller for operation.

FS

A resistor, placed from FS to ground, sets the switching frequency of the controller.

VID0, VID1, VID2, VID3, VID4, VID5, VID6, and VID7

These are the inputs for the internal DAC that provides the reference voltage for output regulation. These pins respond to TTL logic thresholds. These pins are internally pulled high, to approximately 1.2V, by 40µA internal current sources for Intel modes of operation, and pulled low by 20µA internal current sources for AMD modes of operation. The internal pull-up current decreases to 0 as the VID voltage approaches the internal pull-up voltage. All VID pins are compatible with external pull-up voltages not exceeding the IC's bias voltage (VCC).

VRSEL

The state of this pin selects which of the available DAC tables will be used to decode the VID inputs and puts the controller into the corresponding mode of operation. For VR10 mode of operation VRSEL should be less than 0.6V. The VR11 mode of operation can be selected by setting VRSEL between 0.6V and 3.0V, and AMD compliance is selected if this pin is between 3.0V and VCC.

VSEN and RGND

VSEN and RGND are inputs to the precision differential remote-sense amplifier and should be connected to the sense pins of the remote load.

PHASE1, PHASE2, and PHASE3

Connect these pins to the sources of the corresponding

VDIFF

VDIFF is the output of the differential remote-sense amplifier. The voltage on this pin is equal to the difference between VSEN and RGND.

FB and COMP

These pins are the internal error amplifier inverting input and output respectively. FB, VDIFF, and COMP are tied together through external R-C networks to compensate the regulator.

IDROOP

The IDROOP pin is the average channel-current sense output. Connecting this pin through a tuned parallel R-C network to FB allows the converter to incorporate output voltage droop proportional to the output current. If voltage droop is not desired leave this pin unconnected.

REF

The REF input pin is the positive input of the error amplifier. It is internally connected to the DAC output through a 1kΩ resistor. A capacitor is used between the REF pin and ground to smooth the voltage transition during Dynamic VID operations.

OFS

The OFS pin provides a means to program a DC current for generating an offset voltage across the resistor between FB and VDIFF. The offset current is generated via an external resistor and precision internal voltage references. The polarity of the offset is selected by connecting the resistor to GND or VCC. For no offset, the OFS pin should be left unconnected.

ISEN1-, ISEN1+, ISEN2-, ISEN2+, ISEN3-, ISEN3+, ISEN4-, and ISEN4+

These pins are used for differentially sensing the corresponding channel output currents. The sensed currents are used for channel balancing, protection, and load line regulation.

Connect ISEN1-, ISEN2-, ISEN3-, and ISEN4- to the node between the RC sense elements surrounding the inductor of their respective channel. Tie the ISEN+ pins to the VCORE side of their corresponding channel's sense capacitor.

UGATE1, UGATE2, and UGATE3

Connect these pins to the corresponding upper MOSFET gates. These pins are used to control the upper MOSFETs and are monitored for shoot-through prevention purposes.

BOOT1, BOOT2, and BOOT3

These pins provide the bias voltage for the corresponding upper MOSFET drives. Connect these pins to appropriately-chosen external bootstrap capacitors. Internal bootstrap diodes connected to the PVCC pins provide the necessary bootstrap charge.

upper MOSFETs. These pins are the return path for the upper MOSFET drives.

LGATE1, LGATE2, and LGATE3

These pins are used to control the lower MOSFETs. Connect these pins to the corresponding lower MOSFETs' gates.

PWM4

Pulse-width modulation output. Connect this pin to the PWM input pin of an Intersil driver IC if 4-phase operation is desired.

EN_PH4

This pin has two functions. First, a resistor divider connected to this pin will provide a POR power-up synch between the on-chip and external driver. The resistor divider should be designed so that when the POR-trip point of the external driver is reached the voltage on this pin should be 1.21V.

The second function of this pin is disabling PWM4 for 3-phase operation. This can be accomplished by connecting this pin to a +5V supply.

SS/RST/A0

This pin has three different functions associated with it. The first is that a resistor (R_{SS}), placed from this pin to ground, or VCC, will set the soft-start ramp slope for the Intel DAC modes of operation. Refer to Equations 18 and 19 for proper resistor calculation.

The second function of this pin is that it selects which of the two 8-bit Slave I²C addresses the controller will use. Connecting the R_{SS} resistor on this pin to ground will choose slave address one(1000_110x), while connecting this resistor to VCC will select slave address two(1000_111x).

The third function of this pin is a reset to the I²C registers. During normal operation of the part, if this pin is ever grounded, all of the I²C registers are reset to 0000_0000. An open drain device is recommended as the means of grounding this pin for resetting the I²C registers.

SCL

Connect this pin to the clock signal for the I²C bus, which is a logic level input signal. The clock signal tells the controller when data is available on the I²C bus.

SDA

Connect this pin to the bidirectional data line of the I²C bus, which is a logic level input/output signal. All I²C data is sent over this line, including the address of the device the bus is trying to communicate with, and what functions the device should perform.

PGOOD

During normal operation PGOOD indicates whether the output voltage is within specified overvoltage and undervoltage limits. If the output voltage exceeds these limits or a reset event occurs (such as an overcurrent event), PGOOD is pulled low. PGOOD is always low prior to the end of soft-start.

Operation

Multiphase Power Conversion

Microprocessor load current profiles have changed to the point that using single-phase regulators is no longer a viable solution. Designing a regulator that is cost-effective, thermally sound, and efficient has become a challenge that only multiphase converters can accomplish. The ISL6322 controller helps simplify implementation by integrating vital functions and requiring minimal external components. The "Block Diagram" on page 3 provides a top level view of multiphase power conversion using the ISL6322 controller.

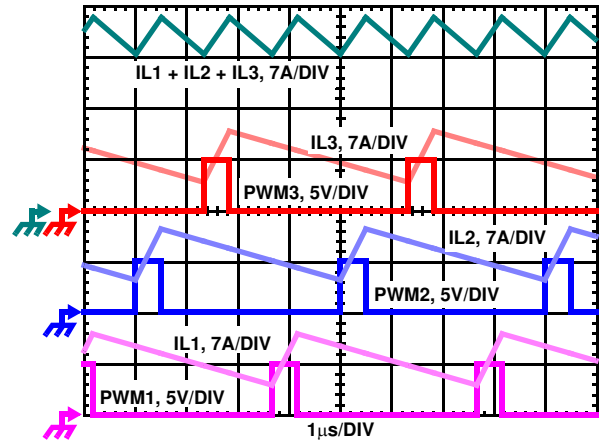


FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

Interleaving

The switching of each channel in a multiphase converter is timed to be symmetrically out of phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the three-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of phases (Equations 1 and 2). Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and lower total output capacitance for any performance specification.

Figure 1 illustrates the multiplicative effect on output ripple frequency. The three channel currents (IL1, IL2, and IL3) combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM pulse is terminated 1/3 of a cycle after the PWM pulse of the previous phase. The peak-to-peak current for each phase is about 7A, and the DC components of the inductor currents combine to feed the load.

To understand the reduction of ripple current amplitude in the multiphase circuit, examine the equation representing an individual channel peak-to-peak inductor current.

$$I_{PP} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{L \cdot f_S \cdot V_{IN}} \quad (\text{EQ. 1})$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and f_S is the switching frequency.

The output capacitors conduct the ripple component of the inductor current. In the case of multiphase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2. Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors.

$$I_{C(P-P)} = \frac{(V_{IN} - N \cdot V_{OUT}) \cdot V_{OUT}}{L \cdot f_S \cdot V_{IN}} \quad (\text{EQ. 2})$$

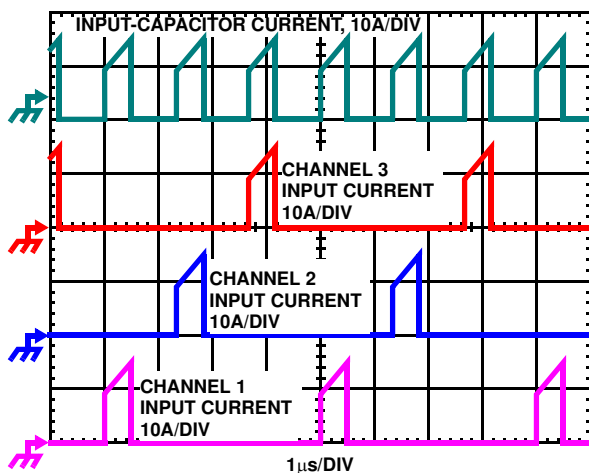


FIGURE 2. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multiphase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 2 illustrates input currents from a three-phase converter combining to reduce the total input ripple current.

The converter depicted in Figure 2 delivers 1.5V to a 36A load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has 11.9A RMS input capacitor current. The single-phase converter

must use an input capacitor bank with twice the RMS current capacity as the equivalent three-phase converter.

Active Pulse Positioning (APP) Modulated PWM Operation

The ISL6322 uses a proprietary Active Pulse Positioning (APP) modulation scheme to control the internal PWM signals that command each channel's driver to turn their upper and lower MOSFETs on and off. The time interval in which a PWM signal can occur is generated by an internal clock, whose cycle time is the inverse of the switching frequency set by the resistor between the FS pin and ground. The advantage of Intersil's proprietary Active Pulse Positioning (APP) modulator is that the PWM signal has the ability to turn on at any point during this PWM time interval, and turn off immediately after the PWM signal has transitioned high. This is important because it allows the controller to quickly respond to output voltage drops associated with current load spikes, while avoiding the ring back affects associated with other modulation schemes.

The PWM output state is driven by the position of the error amplifier output signal, V_{COMP} , minus the current correction signal relative to the proprietary modulator ramp waveform as illustrated in Figure 3. At the beginning of each PWM time interval, this modified V_{COMP} signal is compared to the internal modulator waveform. As long as the modified V_{COMP} voltage is lower than the modulator waveform voltage, the PWM signal is commanded low. The internal MOSFET driver detects the low state of the PWM signal and turns off the upper MOSFET and turns on the lower synchronous MOSFET. When the modified V_{COMP} voltage crosses the modulator ramp, the PWM output transitions high, turning off the synchronous MOSFET and turning on the upper MOSFET. The PWM signal will remain high until the modified V_{COMP} voltage crosses the modulator ramp again. When this occurs the PWM signal will transition low again.

During each PWM time interval the PWM signal can only transition high once. Once PWM transitions high it can not transition high again until the beginning of the next PWM time interval. This prevents the occurrence of double PWM pulses occurring during a single period.

To further improve the transient response, ISL6322 also implements Intersil's proprietary Adaptive Phase Alignment (APA) technique, which turns on all phases together under transient events with large step current. With both APP and APA control, ISL6322 can achieve excellent transient performance and reduce the demand on the output capacitors.

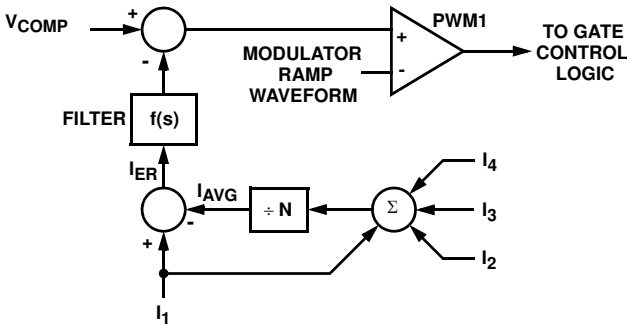
Channel-Current Balance

One important benefit of multiphase operation is the thermal advantage gained by distributing the dissipated heat over multiple devices and greater area. By doing this the designer avoids the complexity of driving parallel MOSFETs and the

expense of using expensive heat sinks and exotic magnetic materials.

In order to realize the thermal advantage, it is important that each channel in a multiphase converter be controlled to carry equal amounts of current at any load level. To achieve this, the currents through each channel must be sampled every switching cycle. The sampled currents, I_n , from each active channel are summed together and divided by the number of active channels. The resulting cycle average current, I_{AVG} , provides a measure of the total load-current demand on the converter during each switching cycle. Channel-current balance is achieved by comparing the sampled current of each channel to the cycle average current, and making the proper adjustment to each channel pulse width based on the error. Intersil's patented current-balance method is illustrated in Figure 3, with error correction for Channel 1 represented. In the figure, the cycle average current, I_{AVG} , is compared with the Channel 1 sample, I_1 , to create an error signal I_{ER} .

The filtered error signal modifies the pulse width commanded by V_{COMP} to correct any unbalance and force I_{ER} toward zero. The same method for error signal correction is applied to each active channel.



Note: Channel 3 and 4 are optional

FIGURE 3. CHANNEL-1 PWM FUNCTION AND CURRENT-BALANCE ADJUSTMENT

Continuous Current Sampling

In order to realize proper current-balance, the currents in each channel are sensed continuously every switching cycle. During this time the current-sense amplifier uses the ISEN inputs to reproduce a signal proportional to the inductor current, I_L . This sensed current, I_{SEN} , is simply a scaled version of the inductor current.

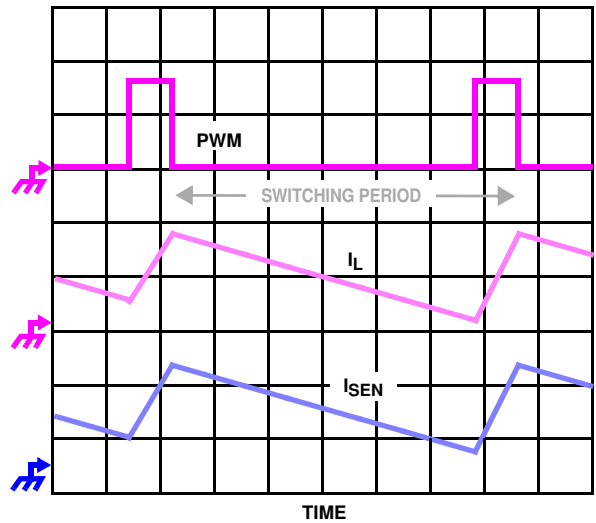


FIGURE 4. CONTINUOUS CURRENT SAMPLING

The ISL6322 supports inductor DCR current sensing to continuously sense each channel's current for channel-current balance. The internal circuitry, shown in Figure 5 represents Channel N of an N-Channel converter. This circuitry is repeated for each channel in the converter, but may not be active depending on how many channels are operating.

Inductor windings have a characteristic distributed resistance or DCR (Direct Current Resistance). For simplicity, the inductor DCR is considered as a separate lumped quantity, as shown in Figure 5. The channel current I_L , flowing through the inductor, passes through the DCR. Equation 3 shows the s-domain equivalent voltage, V_L , across the inductor.

$$V_L(s) = I_L \cdot (s \cdot L + DCR) \tag{EQ. 3}$$

A simple R-C network across the inductor (R_1 and C) extracts the DCR voltage, as shown in Figure 5. The voltage across the sense capacitor, V_C , can be shown to be proportional to the channel current I_L , shown in Equation 4.

$$V_C(s) = \frac{\left(\frac{s \cdot L}{DCR} + 1\right)}{(s \cdot R_1 \cdot C + 1)} \cdot DCR \cdot I_L \tag{EQ. 4}$$

In some cases it may be necessary to use a resistor divider R-C network to sense the current through the inductor. This can be accomplished by placing a second resistor, R_2 , across the sense capacitor. In these cases the voltage across the sense capacitor, V_C , becomes proportional to the channel current I_L , and the resistor divider ratio, K .

$$V_C(s) = \frac{\left(\frac{s \cdot L}{DCR} + 1\right)}{\left(s \cdot \frac{(R_1 \cdot R_2)}{R_1 + R_2} \cdot C + 1\right)} \cdot K \cdot DCR \cdot I_L \quad (\text{EQ. 5})$$

$$K = \frac{R_2}{R_2 + R_1} \quad (\text{EQ. 6})$$

If the R-C network components are selected such that the RC time constant matches the inductor L/DCR time constant, then V_C is equal to the voltage drop across the DCR multiplied by the ratio of the resistor divider, K. **If a resistor divider is not being used, the value for K is 1.**

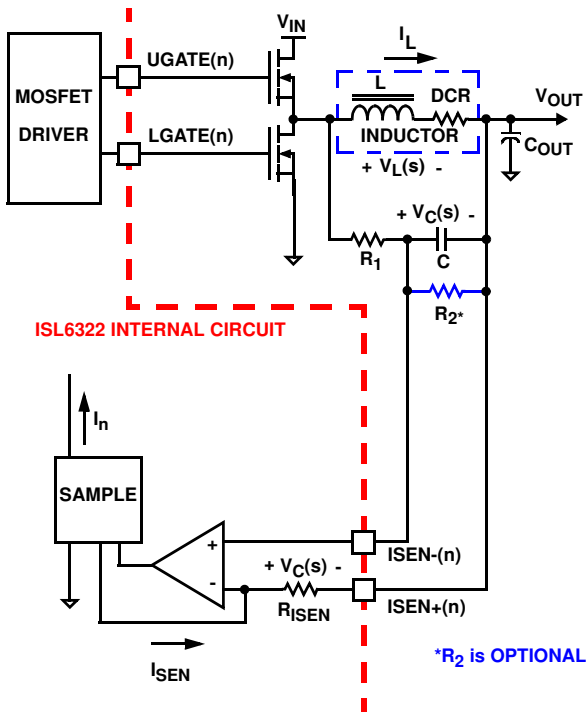


FIGURE 5. INDUCTOR DCR CURRENT SENSING CONFIGURATION

The capacitor voltage V_C , is then replicated across the sense resistor R_{ISEN} . The current through R_{ISEN} is proportional to the inductor current. Equation 7 shows that the proportion between the channel current and the sensed current (I_{SEN}) is driven by the value of the sense resistor, the resistor divider ratio, and the DCR of the inductor.

$$I_{SEN} = K \cdot I_L \cdot \frac{DCR}{R_{ISEN}} \quad (\text{EQ. 7})$$

Output Voltage Setting

The ISL6322 uses a digital to analog converter (DAC) to generate a reference voltage based on the logic signals at the VID pins. The DAC decodes the logic signals into one of the discrete voltages shown in Tables 2, 3, 4 and 5. In Intel modes of operation, each VID pin is pulled up to an internal 1.2V voltage by a weak current source (40µA), which

decreases to 0A as the voltage at the VID pin varies from 0 to the internal 1.2V pull-up voltage. In AMD modes of operation the VID pins are pulled low by a weak 20µA current source. External pull-up resistors or active-high output stages can augment the pull-up current sources, up to a voltage of 5V.

The ISL6322 accommodates four different DAC ranges: Intel VR10 (Extended), Intel VR11, AMD K8/K9 5-bit, and AMD 6-bit. The state of the VRSEL and VID7 pins decide which DAC version is active. Refer to Table 1 for a description of how to select the desired DAC version.

TABLE 1. ISL6322 DAC SELECT TABLE

DAC VERSION	VRSEL PIN	VID7 PIN
VR10(Extended)	VRSEL < 0.6V	-
VR11	0.8V < VRSEL < 3.0V	-
AMD 5-Bit	3.0V < VRSEL < VCC	low
AMD 6-Bit	3.0V < VRSEL < VCC	high

TABLE 2. VR10 (EXTENDED) VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VID5	VID6	VDAC
0	1	0	1	0	1	1	1.60000
0	1	0	1	0	1	0	1.59375
0	1	0	1	1	0	1	1.58750
0	1	0	1	1	0	0	1.58125
0	1	0	1	1	1	1	1.57500
0	1	0	1	1	1	0	1.56875
0	1	1	0	0	0	1	1.56250
0	1	1	0	0	0	0	1.55625
0	1	1	0	0	1	1	1.55000
0	1	1	0	0	1	0	1.54375
0	1	1	0	1	0	1	1.53750
0	1	1	0	1	0	0	1.53125
0	1	1	0	1	1	1	1.52500
0	1	1	0	1	1	0	1.51875
0	1	1	1	0	0	1	1.51250
0	1	1	1	0	0	0	1.50625
0	1	1	1	0	1	1	1.50000
0	1	1	1	0	1	0	1.49375
0	1	1	1	1	0	1	1.48750
0	1	1	1	1	0	0	1.48125
0	1	1	1	1	1	1	1.47500
0	1	1	1	1	1	0	1.46875
1	0	0	0	0	0	1	1.46250
1	0	0	0	0	0	0	1.45625

TABLE 2. VR10 (EXTENDED) VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VID5	VID6	VDAC
1	0	0	0	0	1	1	1.45000
1	0	0	0	0	1	0	1.44375
1	0	0	0	1	0	1	1.43750
1	0	0	0	1	0	0	1.43125
1	0	0	0	1	1	1	1.42500
1	0	0	0	1	1	0	1.41875
1	0	0	1	0	0	1	1.41250
1	0	0	1	0	0	0	1.40625
1	0	0	1	0	1	1	1.40000
1	0	0	1	0	1	0	1.39375
1	0	0	1	1	0	1	1.38750
1	0	0	1	1	0	0	1.38125
1	0	0	1	1	1	1	1.37500
1	0	0	1	1	1	0	1.36875
1	0	1	0	0	0	1	1.36250
1	0	1	0	0	0	0	1.35625
1	0	1	0	0	1	1	1.35000
1	0	1	0	0	1	0	1.34375
1	0	1	0	1	0	1	1.33750
1	0	1	0	1	0	0	1.33125
1	0	1	0	1	1	1	1.32500
1	0	1	0	1	1	0	1.31875
1	0	1	1	0	0	1	1.31250
1	0	1	1	0	0	0	1.30625
1	0	1	1	0	1	1	1.30000
1	0	1	1	0	1	0	1.29375
1	0	1	1	1	0	1	1.28750
1	0	1	1	1	0	0	1.28125
1	0	1	1	1	1	1	1.27500
1	0	1	1	1	1	0	1.26875
1	1	0	0	0	0	1	1.26250
1	1	0	0	0	0	0	1.25625
1	1	0	0	0	1	1	1.25000
1	1	0	0	0	1	0	1.24375
1	1	0	0	1	0	1	1.23750
1	1	0	0	1	0	0	1.23125
1	1	0	0	1	1	1	1.22500
1	1	0	0	1	1	0	1.21875
1	1	0	1	0	0	1	1.21250

TABLE 2. VR10 (EXTENDED) VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VID5	VID6	VDAC
1	1	0	1	0	0	0	1.20625
1	1	0	1	0	1	1	1.20000
1	1	0	1	0	1	0	1.19375
1	1	0	1	1	0	1	1.18750
1	1	0	1	1	0	0	1.18125
1	1	0	1	1	1	1	1.17500
1	1	0	1	1	1	0	1.16875
1	1	1	0	0	0	1	1.16250
1	1	1	0	0	0	0	1.15625
1	1	1	0	0	1	1	1.15000
1	1	1	0	0	1	0	1.14375
1	1	1	0	1	0	1	1.13750
1	1	1	0	1	0	0	1.13125
1	1	1	0	1	1	1	1.12500
1	1	1	0	1	1	0	1.11875
1	1	1	1	0	0	1	1.11250
1	1	1	1	0	0	0	1.10625
1	1	1	1	0	1	1	1.10000
1	1	1	1	0	1	0	1.09375
1	1	1	1	1	0	1	OFF
1	1	1	1	1	0	0	OFF
1	1	1	1	1	1	1	OFF
1	1	1	1	1	1	0	OFF
0	0	0	0	0	0	1	1.08750
0	0	0	0	0	0	0	1.08125
0	0	0	0	0	1	1	1.07500
0	0	0	0	0	1	0	1.06875
0	0	0	0	1	0	1	1.06250
0	0	0	0	1	0	0	1.05625
0	0	0	0	1	1	1	1.05000
0	0	0	0	1	1	0	1.04375
0	0	0	1	0	0	1	1.03750
0	0	0	1	0	0	0	1.03125
0	0	0	1	0	1	1	1.02500
0	0	0	1	0	1	0	1.01875
0	0	0	1	1	0	1	1.01250
0	0	0	1	1	0	0	1.00625
0	0	0	1	1	1	1	1.00000
0	0	0	1	1	1	0	0.99375

TABLE 2. VR10 (EXTENDED) VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VID5	VID6	VDAC
0	0	1	0	0	0	1	0.98750
0	0	1	0	0	0	0	0.98125
0	0	1	0	0	1	1	0.97500
0	0	1	0	0	1	0	0.96875
0	0	1	0	1	0	1	0.96250
0	0	1	0	1	0	0	0.95625
0	0	1	0	1	1	1	0.95000
0	0	1	0	1	1	0	0.94375
0	0	1	1	0	0	1	0.93750
0	0	1	1	0	0	0	0.93125
0	0	1	1	0	1	1	0.92500
0	0	1	1	0	1	0	0.91875
0	0	1	1	1	0	1	0.91250
0	0	1	1	1	0	0	0.90625
0	0	1	1	1	1	1	0.90000
0	0	1	1	1	1	0	0.89375
0	1	0	0	0	0	1	0.88750
0	1	0	0	0	0	0	0.88125
0	1	0	0	0	1	1	0.87500
0	1	0	0	0	1	0	0.86875
0	1	0	0	1	0	1	0.86250
0	1	0	0	1	0	0	0.85625
0	1	0	0	1	1	1	0.85000
0	1	0	0	1	1	0	0.84375
0	1	0	1	0	0	1	0.83750
0	1	0	1	0	0	0	0.83125

TABLE 3. VR11 VOLTAGE IDENTIFICATION CODES (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	0	0	0	1	0	1	0	1.55000
0	0	0	0	1	0	1	1	1.54375
0	0	0	0	1	1	0	0	1.53750
0	0	0	0	1	1	0	1	1.53125
0	0	0	0	1	1	1	0	1.52500
0	0	0	0	1	1	1	1	1.51875
0	0	0	1	0	0	0	0	1.51250
0	0	0	1	0	0	0	1	1.50625
0	0	0	1	0	0	1	0	1.50000
0	0	0	1	0	0	1	1	1.49375
0	0	0	1	0	1	0	0	1.48750
0	0	0	1	0	1	0	1	1.48125
0	0	0	1	0	1	1	0	1.47500
0	0	0	1	0	1	1	1	1.46875
0	0	0	1	1	0	0	0	1.46250
0	0	0	1	1	0	0	1	1.45625
0	0	0	1	1	0	1	0	1.45000
0	0	0	1	1	0	1	1	1.44375
0	0	0	1	1	1	0	0	1.43750
0	0	0	1	1	1	0	1	1.43125
0	0	0	1	1	1	1	0	1.42500
0	0	0	1	1	1	1	1	1.41875
0	0	1	0	0	0	0	0	1.41250
0	0	1	0	0	0	0	1	1.40625
0	0	1	0	0	0	1	0	1.40000
0	0	1	0	0	0	1	1	1.39375
0	0	1	0	0	1	0	0	1.38750
0	0	1	0	0	1	0	1	1.38125
0	0	1	0	0	1	1	0	1.37500
0	0	1	0	0	1	1	1	1.36875
0	0	1	0	1	0	0	0	1.36250
0	0	1	0	1	0	0	1	1.35625
0	0	1	0	1	0	1	0	1.35000
0	0	1	0	1	0	1	1	1.34375
0	0	1	0	1	1	0	0	1.33750
0	0	1	0	1	1	0	1	1.33125
0	0	1	0	1	1	1	0	1.32500
0	0	1	0	1	1	1	1	1.31875
0	0	1	1	0	0	0	0	1.31250

TABLE 3. VR11 VOLTAGE IDENTIFICATION CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	OFF
0	0	0	0	0	0	1	0	1.60000
0	0	0	0	0	0	1	1	1.59375
0	0	0	0	0	1	0	0	1.58750
0	0	0	0	0	1	0	1	1.58125
0	0	0	0	0	1	1	0	1.57500
0	0	0	0	0	1	1	1	1.56875
0	0	0	0	1	0	0	0	1.56250
0	0	0	0	1	0	0	1	1.55625

TABLE 3. VR11 VOLTAGE IDENTIFICATION CODES
(Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	0	1	1	0	0	0	1	1.30625
0	0	1	1	0	0	1	0	1.30000
0	0	1	1	0	0	1	1	1.29375
0	0	1	1	0	1	0	0	1.28750
0	0	1	1	0	1	0	1	1.28125
0	0	1	1	0	1	1	0	1.27500
0	0	1	1	0	1	1	1	1.26875
0	0	1	1	1	0	0	0	1.26250
0	0	1	1	1	0	0	1	1.25625
0	0	1	1	1	0	1	0	1.25000
0	0	1	1	1	0	1	1	1.24375
0	0	1	1	1	1	0	0	1.23750
0	0	1	1	1	1	0	1	1.23125
0	0	1	1	1	1	1	0	1.22500
0	0	1	1	1	1	1	1	1.21875
0	1	0	0	0	0	0	0	1.21250
0	1	0	0	0	0	0	1	1.20625
0	1	0	0	0	0	1	0	1.20000
0	1	0	0	0	0	1	1	1.19375
0	1	0	0	0	1	0	0	1.18750
0	1	0	0	0	1	0	1	1.18125
0	1	0	0	0	1	1	0	1.17500
0	1	0	0	0	1	1	1	1.16875
0	1	0	0	1	0	0	0	1.16250
0	1	0	0	1	0	0	1	1.15625
0	1	0	0	1	0	1	0	1.15000
0	1	0	0	1	0	1	1	1.14375
0	1	0	0	1	1	0	0	1.13750
0	1	0	0	1	1	0	1	1.13125
0	1	0	0	1	1	1	0	1.12500
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	0	0	1	1	1.09375
0	1	0	1	0	1	0	0	1.08750
0	1	0	1	0	1	0	1	1.08125
0	1	0	1	0	1	1	0	1.07500
0	1	0	1	0	1	1	1	1.06875

TABLE 3. VR11 VOLTAGE IDENTIFICATION CODES
(Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	1	0	1	1	0	0	0	1.06250
0	1	0	1	1	0	0	1	1.05625
0	1	0	1	1	0	1	0	1.05000
0	1	0	1	1	0	1	1	1.04375
0	1	0	1	1	1	0	0	1.03750
0	1	0	1	1	1	0	1	1.03125
0	1	0	1	1	1	1	0	1.02500
0	1	0	1	1	1	1	1	1.01875
0	1	1	0	0	0	0	0	1.01250
0	1	1	0	0	0	0	1	1.00625
0	1	1	0	0	0	1	0	1.00000
0	1	1	0	0	0	1	1	0.99375
0	1	1	0	0	1	0	0	0.98750
0	1	1	0	0	1	0	1	0.98125
0	1	1	0	0	1	1	0	0.97500
0	1	1	0	0	1	1	1	0.96875
0	1	1	0	1	0	0	0	0.96250
0	1	1	0	1	0	0	1	0.95625
0	1	1	0	1	0	1	0	0.95000
0	1	1	0	1	0	1	1	0.94375
0	1	1	0	1	1	0	0	0.93750
0	1	1	0	1	1	0	1	0.93125
0	1	1	0	1	1	1	0	0.92500
0	1	1	0	1	1	1	1	0.91875
0	1	1	1	0	0	0	0	0.91250
0	1	1	1	0	0	0	1	0.90625
0	1	1	1	0	0	1	0	0.90000
0	1	1	1	0	0	1	1	0.89375
0	1	1	1	0	1	0	0	0.88750
0	1	1	1	0	1	0	1	0.88125
0	1	1	1	0	1	1	0	0.87500
0	1	1	1	0	1	1	1	0.86875
0	1	1	1	1	0	0	0	0.86250
0	1	1	1	1	0	0	1	0.85625
0	1	1	1	1	0	1	0	0.85000
0	1	1	1	1	0	1	1	0.84375
0	1	1	1	1	1	0	0	0.83750
0	1	1	1	1	1	0	1	0.83125
0	1	1	1	1	1	1	0	0.82500

TABLE 3. VR11 VOLTAGE IDENTIFICATION CODES
(Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	1	1	1	1	1	1	1	0.81875
1	0	0	0	0	0	0	0	0.81250
1	0	0	0	0	0	0	1	0.80625
1	0	0	0	0	0	1	0	0.80000
1	0	0	0	0	0	1	1	0.79375
1	0	0	0	0	1	0	0	0.78750
1	0	0	0	0	1	0	1	0.78125
1	0	0	0	0	1	1	0	0.77500
1	0	0	0	0	1	1	1	0.76875
1	0	0	0	1	0	0	0	0.76250
1	0	0	0	1	0	0	1	0.75625
1	0	0	0	1	0	1	0	0.75000
1	0	0	0	1	0	1	1	0.74375
1	0	0	0	1	1	0	0	0.73750
1	0	0	0	1	1	0	1	0.73125
1	0	0	0	1	1	1	0	0.72500
1	0	0	0	1	1	1	1	0.71875
1	0	0	1	0	0	0	0	0.71250
1	0	0	1	0	0	0	1	0.70625
1	0	0	1	0	0	1	0	0.70000
1	0	0	1	0	0	1	1	0.69375
1	0	0	1	0	1	0	0	0.68750
1	0	0	1	0	1	0	1	0.68125
1	0	0	1	0	1	1	0	0.67500
1	0	0	1	0	1	1	1	0.66875
1	0	0	1	1	0	0	0	0.66250
1	0	0	1	1	0	0	1	0.65625
1	0	0	1	1	0	1	0	0.65000
1	0	0	1	1	0	1	1	0.64375
1	0	0	1	1	1	0	0	0.63750
1	0	0	1	1	1	0	1	0.63125
1	0	0	1	1	1	1	0	0.62500
1	0	0	1	1	1	1	1	0.61875
1	0	1	0	0	0	0	0	0.61250
1	0	1	0	0	0	0	1	0.60625
1	0	1	0	0	0	1	0	0.60000
1	0	1	0	0	0	1	1	0.59375
1	0	1	0	0	1	0	0	0.58750
1	0	1	0	0	1	0	1	0.58125

TABLE 3. VR11 VOLTAGE IDENTIFICATION CODES
(Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VDAC
1	0	1	0	0	1	1	0	0.57500
1	0	1	0	0	1	1	1	0.56875
1	0	1	0	1	0	0	0	0.56250
1	0	1	0	1	0	0	1	0.55625
1	0	1	0	1	0	1	0	0.55000
1	0	1	0	1	0	1	1	0.54375
1	0	1	0	1	1	0	0	0.53750
1	0	1	0	1	1	0	1	0.53125
1	0	1	0	1	1	1	0	0.52500
1	0	1	0	1	1	1	1	0.51875
1	0	1	1	0	0	0	0	0.51250
1	0	1	1	0	0	0	1	0.50625
1	0	1	1	0	0	1	0	0.50000
1	1	1	1	1	1	1	0	OFF
1	1	1	1	1	1	1	1	OFF

TABLE 4. AMD 5-BIT VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VDAC
1	1	1	1	1	Off
1	1	1	1	0	0.800
1	1	1	0	1	0.825
1	1	1	0	0	0.850
1	1	0	1	1	0.875
1	1	0	1	0	0.900
1	1	0	0	1	0.925
1	1	0	0	0	0.950
1	0	1	1	1	0.975
1	0	1	1	0	1.000
1	0	1	0	1	1.025
1	0	1	0	0	1.050
1	0	0	1	1	1.075
1	0	0	1	0	1.100
1	0	0	0	1	1.125
1	0	0	0	0	1.150
0	1	1	1	1	1.175
0	1	1	1	0	1.200
0	1	1	0	1	1.225
0	1	1	0	0	1.250
0	1	0	1	1	1.275

TABLE 4. AMD 5-BIT VOLTAGE IDENTIFICATION CODES
 (Continued)

VID4	VID3	VID2	VID1	VID0	VDAC
0	1	0	1	0	1.300
0	1	0	0	1	1.325
0	1	0	0	0	1.350
0	0	1	1	1	1.375
0	0	1	1	0	1.400
0	0	1	0	1	1.425
0	0	1	0	0	1.450
0	0	0	1	1	1.475
0	0	0	1	0	1.500
0	0	0	0	1	1.525
0	0	0	0	0	1.550

TABLE 5. AMD 6-BIT VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	0	0	0	0	0	1.5500
0	0	0	0	0	1	1.5250
0	0	0	0	1	0	1.5000
0	0	0	0	1	1	1.4750
0	0	0	1	0	0	1.4500
0	0	0	1	0	1	1.4250
0	0	0	1	1	0	1.4000
0	0	0	1	1	1	1.3750
0	0	1	0	0	0	1.3500
0	0	1	0	0	1	1.3250
0	0	1	0	1	0	1.3000
0	0	1	0	1	1	1.2750
0	0	1	1	0	0	1.2500
0	0	1	1	0	1	1.2250
0	0	1	1	1	0	1.2000
0	0	1	1	1	1	1.1750
0	1	0	0	0	0	1.1500
0	1	0	0	0	1	1.1250
0	1	0	0	1	0	1.1000
0	1	0	0	1	1	1.0750
0	1	0	1	0	0	1.0500
0	1	0	1	0	1	1.0250
0	1	0	1	1	0	1.0000
0	1	0	1	1	1	0.9750
0	1	1	0	0	0	0.9500

TABLE 5. AMD 6-BIT VOLTAGE IDENTIFICATION CODES
 (Continued)

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	1	1	0	0	1	0.9250
0	1	1	0	1	0	0.9000
0	1	1	0	1	1	0.8750
0	1	1	1	0	0	0.8500
0	1	1	1	0	1	0.8250
0	1	1	1	1	0	0.8000
0	1	1	1	1	1	0.7750
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.7500
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.7250
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7000
1	0	0	1	1	0	0.6875
1	0	0	1	1	1	0.6750
1	0	1	0	0	0	0.6625
1	0	1	0	0	1	0.6500
1	0	1	0	1	0	0.6375
1	0	1	0	1	1	0.6250
1	0	1	1	0	0	0.6125
1	0	1	1	0	1	0.6000
1	0	1	1	1	0	0.5875
1	0	1	1	1	1	0.5750
1	1	0	0	0	0	0.5625
1	1	0	0	0	1	0.5500
1	1	0	0	1	0	0.5375
1	1	0	0	1	1	0.5250
1	1	0	1	0	0	0.5125
1	1	0	1	0	1	0.5000
1	1	0	1	1	0	0.4875
1	1	0	1	1	1	0.4750
1	1	1	0	0	0	0.4625
1	1	1	0	0	1	0.4500
1	1	1	0	1	0	0.4375
1	1	1	0	1	1	0.4250
1	1	1	1	0	0	0.4125
1	1	1	1	0	1	0.4000
1	1	1	1	1	0	0.3875
1	1	1	1	1	1	0.3750

Voltage Regulation

The integrating compensation network shown in Figure 6 insures that the steady-state error in the output voltage is limited only to the error in the reference voltage (output of the DAC) and offset errors in the OFS current source, remote-sense and error amplifiers. Intersil specifies the guaranteed tolerance of the ISL6322 to include the combined tolerances of each of these elements.

The output of the error amplifier, V_{COMP} , is compared to the triangle waveform to generate the PWM signals. The PWM signals control the timing of the Internal MOSFET drivers and regulate the converter output so that the voltage at FB is equal to the voltage at REF. This will regulate the output voltage to be equal to Equation 8. The internal and external circuitry that controls voltage regulation is illustrated in Figure 6.

$$V_{OUT} = V_{REF} - V_{OFS} - V_{DROOP} \tag{EQ. 8}$$

The ISL6322 incorporates an internal differential remote-sense amplifier in the feedback path. The amplifier removes the voltage error encountered when measuring the output voltage relative to the controller ground reference point resulting in a more accurate means of sensing output voltage. Connect the microprocessor sense pins to the non-inverting input, VSEN, and inverting input, RGND, of the remote-sense amplifier. The remote-sense output, V_{DIFF} , is connected to the inverting input of the error amplifier through an external resistor.

Load-Line (Droop) Regulation

Some microprocessor manufacturers require a precisely controlled output resistance. This dependence of output voltage on load current is often termed “droop” or “load line” regulation. By adding a well controlled output impedance, the output voltage can effectively be level shifted in a direction which works to achieve the load-line regulation required by these manufacturers.

In other cases, the designer may determine that a more cost-effective solution can be achieved by adding droop. Droop can help to reduce the output-voltage spike that results from fast load-current demand changes.

The magnitude of the spike is dictated by the ESR and ESL of the output capacitors selected. By positioning the no-load voltage level near the upper specification limit, a larger negative spike can be sustained without crossing the lower limit. By adding a well controlled output impedance, the output voltage under load can effectively be level shifted down so that a larger positive spike can be sustained without crossing the upper specification limit.

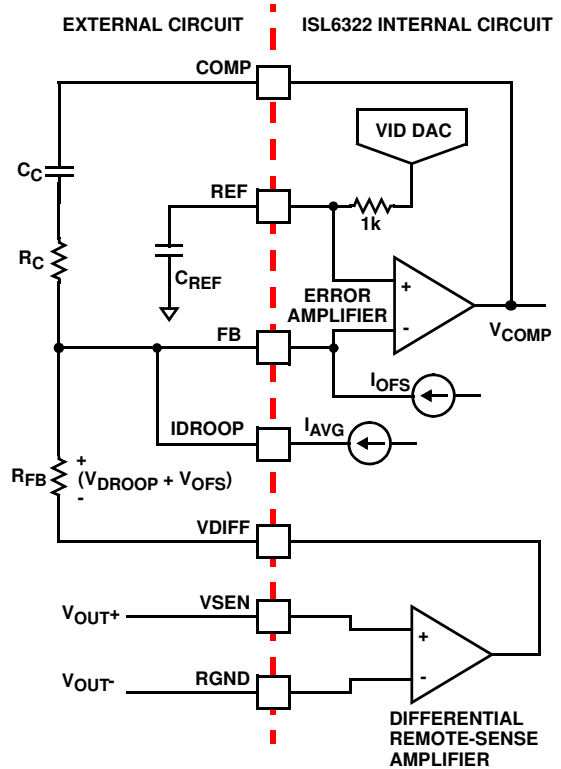


FIGURE 6. OUTPUT VOLTAGE AND LOAD-LINE REGULATION WITH OFFSET ADJUSTMENT

As shown in Figure 6, a current proportional to the average current of all active channels, I_{AVG} , flows from FB through a load-line regulation resistor R_{FB} . The resulting voltage drop across R_{FB} is proportional to the output current, effectively creating an output voltage droop with a steady-state value defined in Equation 9:

$$V_{DROOP} = I_{AVG} \cdot R_{FB} \tag{EQ. 9}$$

The regulated output voltage is reduced by the droop voltage V_{DROOP} . The output voltage as a function of load current is derived by combining Equation 9 with Equation 10.

$$V_{OUT} = V_{REF} - V_{OFS} - \left(\frac{I_{OUT}}{N} \cdot \frac{DCR}{R_{ISEN}} \cdot R_{FB} \right) \tag{EQ. 10}$$

In Equation 10, V_{REF} is the reference voltage, V_{OFS} is the programmed offset voltage, I_{OUT} is the total output current of the converter, R_{ISEN} is the internal sense resistor connected to the ISEN+ pin, and R_{FB} is the feedback resistor, N is the active channel number, and DCR is the Inductor DCR value.

Therefore the equivalent load-line impedance, i.e. droop impedance, is equal to Equation 11:

$$R_{LL} = \frac{R_{FB}}{N} \cdot \frac{DCR}{R_{ISEN}} \tag{EQ. 11}$$

Output-Voltage Offset Programming

The ISL6322 allows the designer to accurately adjust the offset voltage by connecting a resistor, R_{OFS} , from the OFS pin to VCC or GND. When R_{OFS} is connected between OFS and VCC, the voltage across it is regulated to 1.6V. This causes a proportional current (I_{OFS}) to flow into the FB pin. If R_{OFS} is connected to ground, the voltage across it is regulated to 0.4V, and I_{OFS} flows out of the FB pin. The offset current flowing through the resistor between VDIFF and FB will generate the desired offset voltage which is equal to the product ($I_{OFS} \times R_{FB}$). These functions are shown in Figures 7 and 8.

Once the desired output offset voltage has been determined, use the following formulas to set R_{OFS} :

For Negative Offset (connect R_{OFS} to GND):

$$R_{OFS} = \frac{0.4 \cdot R_{FB}}{V_{OFFSET}} \quad (EQ. 12)$$

For Positive Offset (connect R_{OFS} to VCC):

$$R_{OFS} = \frac{1.6 \cdot R_{FB}}{V_{OFFSET}} \quad (EQ. 13)$$

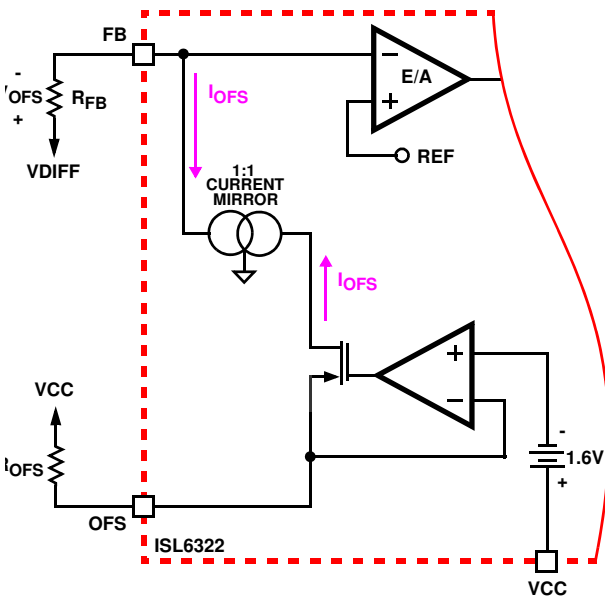


FIGURE 7. POSITIVE OFFSET OUTPUT VOLTAGE PROGRAMMING

Dynamic VID

Modern microprocessors need to make changes to their core voltage as part of normal operation. They direct the ISL6322 to do this by making changes to the VID inputs. The ISL6322 is required to monitor the DAC inputs and respond to on-the-fly VID changes in a controlled manner, supervising a safe output voltage transition without discontinuity or disruption. The DAC mode the ISL6322 is operating in determines how the controller responds to a dynamic VID change.

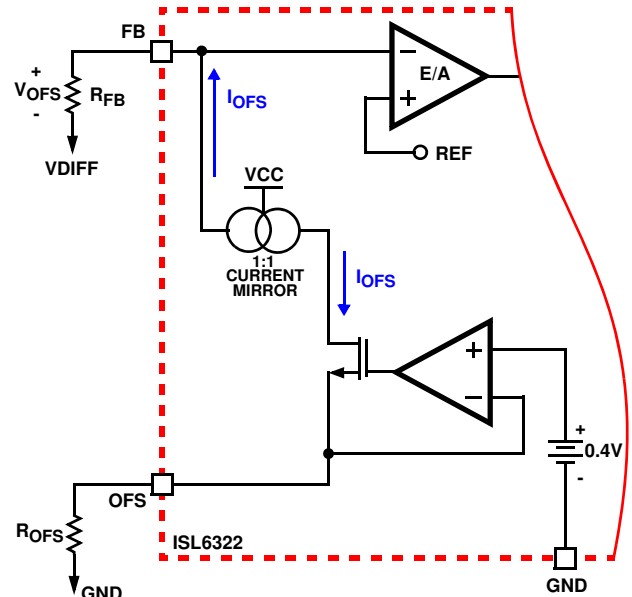


FIGURE 8. NEGATIVE OFFSET OUTPUT VOLTAGE PROGRAMMING

INTEL DYNAMIC VID TRANSITIONS

When in Intel VR10 or VR11 mode, the ISL6322 checks the VID inputs on the positive edge of an internal 3MHz clock. If a new code is established and it remains stable for 3 consecutive readings ($1\mu s$ to $1.33\mu s$), the ISL6322 recognizes the new code and changes the internal DAC reference directly to the new level. The Intel processor controls the VID transitions and is responsible for incrementing or decrementing one VID step at a time. In VR10 and VR11 settings, the ISL6322 will immediately change the internal DAC reference to the new requested value as soon as the request is validated, which means the fastest recommended rate at which a bit change can occur is once every $2\mu s$. In cases where the reference step is too large, the sudden change can trigger overcurrent or overvoltage events.

In order to ensure the smooth transition of output voltage during a VR10 or VR11 VID change, a VID step change smoothing network is required. This network is composed of an internal $1k\Omega$ resistor between the DAC and the REF pin, and the external capacitor C_{REF} between the REF pin and ground. The selection of C_{REF} is based on the time duration for 1-bit VID change and the allowable delay time.

Assuming the microprocessor controls the VID change at 1 bit every T_{VID} , the relationship between C_{REF} and T_{VID} is given by Equation 14.

$$C_{REF} = 0.001(S) \cdot T_{VID} \quad (EQ. 14)$$

As an example, for a VID step change rate of $5\mu s$ per bit, the value of C_{REF} is $5600pF$ based on Equation 14.

AMD Dynamic VID Transitions

When running in AMD 5-bit or 6-bit modes of operation, the ISL6322 responds differently to a dynamic VID change than when in Intel VR10 or VR11 mode. In the AMD modes, the ISL6322 still checks the VID inputs on the positive edge of an internal 3MHz clock. In these modes the VID code can be changed by more than a 1-bit step at a time. If a new code is established and it remains stable for 3 consecutive readings (1 μ s to 1.33 μ s), the ISL6322 recognizes the change and begins slewing the DAC in 6.25mV steps at a stepping frequency of 330kHz until the VID and DAC are equal. Thus, the total time required for a VID change, t_{DVID} , is dependent only on the size of the VID change (ΔV_{VID}).

The time required for a ISL6322-based converter in AMD 5-bit DAC configuration to make a 1.1V to 1.5V reference voltage change is about 194 μ s, as calculated using the following equation.

$$t_{DVID} = \frac{1}{330 \times 10^3} \cdot \left(\frac{\Delta V_{VID}}{0.00625} \right) \quad (\text{EQ. 15})$$

In order to ensure the smooth transition of output voltage during an AMD VID change, a VID step change smoothing network is required. This network is composed of an internal 1k Ω resistor between the DAC and the REF pin, and the external capacitor C_{REF} , between the REF pin and ground. For AMD VID transitions C_{REF} should be a 1000pF capacitor.

User Selectable Adaptive Deadtime Control Techniques

The ISL6322 integrated drivers incorporate two different adaptive deadtime control techniques, which the user can choose between. Both of these control techniques help to minimize deadtime, resulting in high efficiency from the reduced freewheeling time of the lower MOSFET body-diode conduction, and both help to prevent the upper and lower MOSFETs from conducting simultaneously. This is accomplished by ensuring either rising gate turns on its MOSFET with minimum and sufficient delay after the other has turned off.

The difference between the two adaptive deadtime control techniques is the method in which they detect that the lower MOSFET has transitioned off in order to turn on the upper MOSFET. The state of the internal I²C registers determines which of the two control techniques is active (see pages 27 through 31 for details of controlling deadtime control with I²C). The default setting is PHASE Detect. If the PHASE Detect Scheme is chosen, the voltage on the PHASE pin is monitored to determine if the lower MOSFET has transitioned off or not. Choosing the LGATE Detect Scheme instructs the controller to monitor the voltage on the LGATE pin to determine if the lower MOSFET has turned off or not. For both schemes, the method for determining whether the upper MOSFET has transitioned off in order to signal to turn on the lower MOSFET is the same.

PHASE DETECT

For the PHASE detect scheme, during turn-off of the lower MOSFET, the PHASE voltage is monitored until it reaches a -0.3V/+0.8V (forward/reverse inductor current). At this time the UGATE is released to rise. An auto-zero comparator is used to correct the $r_{DS(ON)}$ drop in the phase voltage preventing false detection of the -0.3V phase level during $r_{DS(ON)}$ conduction period. In the case of zero current, the UGATE is released after 35ns delay of the LGATE dropping below 0.5V. When LGATE first begins to transition low, this quick transition can disturb the PHASE node and cause a false trip, so there is 20ns of blanking time once LGATE falls until PHASE is monitored.

Once the PHASE is high, the advanced adaptive shoot-through circuitry monitors the PHASE and UGATE voltages during a PWM falling edge and the subsequent UGATE turn-off. If either the UGATE falls to less than 1.75V above the PHASE or the PHASE falls to less than +0.8V, the LGATE is released to turn-on.

LGATE DETECT

For the LGATE detect scheme, during turn-off of the lower MOSFET, the LGATE voltage is monitored until it reaches 1.75V. At this time the UGATE is released to rise.

Once the PHASE is high, the advanced adaptive shoot-through circuitry monitors the PHASE and UGATE voltages during a PWM falling edge and the subsequent UGATE turn-off. If either the UGATE falls to less than 1.75V above the PHASE or the PHASE falls to less than +0.8V, the LGATE is released to turn-on.

Internal Bootstrap Device

All three integrated drivers feature an internal bootstrap schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is also designed to prevent the bootstrap capacitor from overcharging due to the large negative swing at the PHASE node. This reduces voltage stress on the boot to phase pins.

The bootstrap capacitor must have a maximum voltage rating above $PVCC + 4V$ and its capacitance value can be chosen from Equation 22:

$$C_{BOOT_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT_CAP}} \quad (\text{EQ. 16})$$

$$Q_{GATE} = \frac{Q_{G1} \cdot PVCC}{V_{GS1}} \cdot N_{Q1}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs. The ΔV_{BOOT_CAP} term is defined as the allowable droop in the rail of the upper gate drive.

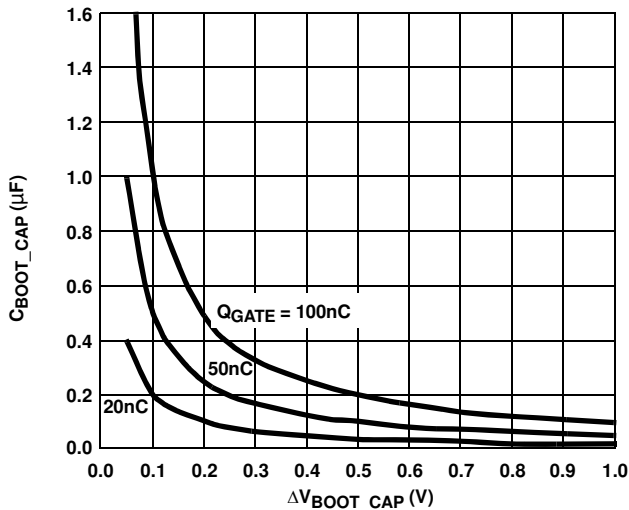


FIGURE 9. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

Gate Drive Voltage Versatility

The ISL6322 provides the user flexibility in choosing the gate drive voltage for efficiency optimization. The controller ties the upper and lower drive rails together. Simply applying a voltage from 5V up to 12V on PVCC sets both gate drive rail voltages simultaneously.

Initialization

Prior to initialization, proper conditions must exist on the EN, VCC, PVCC and the VID pins. When the conditions are met, the controller begins soft-start. Once the output voltage is within the proper window of operation, the controller asserts PGOOD.

Enable and Disable

While in shutdown mode, the PWM outputs are held in a high-impedance state to assure the drivers remain off. The following input conditions must be met, for both Intel and AMD modes of operation, before the ISL6322 is released from shutdown mode to begin the soft-start startup sequence:

1. The bias voltage applied at VCC must reach the internal power-on reset (POR) rising threshold. Once this threshold is reached, proper operation of all aspects of the ISL6322 is guaranteed. Hysteresis between the rising and falling thresholds assure that once enabled, the ISL6322 will not inadvertently turn off unless the bias voltage drops substantially (see "Electrical Specifications" on page 7).
2. The voltage on EN must be above 0.85V. The EN input allows for power sequencing between the controller bias voltage and another voltage rail. The enable comparator holds the ISL6322 in shutdown until the voltage at EN rises above 0.85V. The enable comparator has 110mV of hysteresis to prevent bounce.

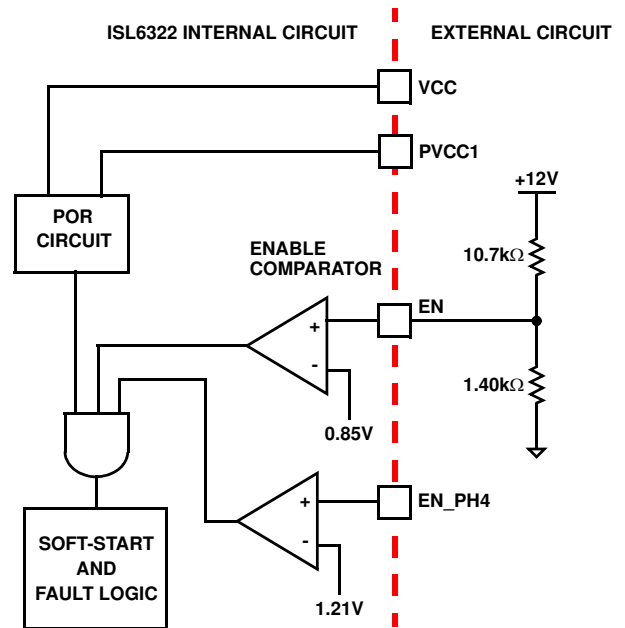


FIGURE 10. POWER SEQUENCING USING THRESHOLD-SENSITIVE ENABLE (EN) FUNCTION

3. The voltage on the EN_PH4 pin must be above 1.21V. The EN_PH4 input allows for power sequencing between the controller and the external driver.
4. The driver bias voltage applied at the PVCC pins must reach the internal power-on reset (POR) rising threshold. In order for the ISL6322 to begin operation, PVCC1 is the only pin that is required to have a voltage applied that exceeds POR. However, for 2 or 3-phase operation PVCC2 and PVCC3 must also exceed the POR threshold. Hysteresis between the rising and falling thresholds assure that once enabled, the ISL6322 will not inadvertently turn off unless the PVCC bias voltage drops substantially (see "Electrical Specifications" on page 7).

For Intel VR10, VR11 and AMD 6-bit modes of operation these are the only conditions that must be met for the controller to immediately begin the soft-start sequence. If running in AMD 5-bit mode of operation there is one more condition that must be met:

5. The VID code must not be 11111 in AMD 5-bit mode. This code signals the controller that no load is present. The controller will not allow soft-start to begin if this VID code is present on the VID pins.

Once all of these conditions are met the controller will begin the soft-start sequence and will ramp the output voltage up to the user designated level.

Intel Soft-Start

The soft-start function allows the converter to bring up the output voltage in a controlled fashion, resulting in a linear ramp-up. The soft-start sequence for the Intel modes of operation is slightly different than the AMD soft-start sequence.

For the Intel VR10 and VR11 modes of operation, the soft-start sequence is composed of four periods, as shown in Figure 11. Once the ISL6322 is released from shutdown and soft-start begins (as described in the “Enable and Disable” on page 23), the controller will have fixed delay period TD1. After this delay period, the VR will begin first soft-start ramp until the output voltage reaches 1.1V VBOOT voltage. Then, the controller will regulate the VR voltage at 1.1V for another fixed period TD3. At the end of TD3 period, ISL6322 will read the VID signals. If the VID code is valid, ISL6322 will initiate the second soft-start ramp until the output voltage reaches the VID voltage plus/minus any offset or droop voltage.

The soft-start time is the sum of the four periods as shown in Equation 17.

$$T_{SS} = TD1 + TD2 + TD3 + TD4 \quad (\text{EQ. 17})$$

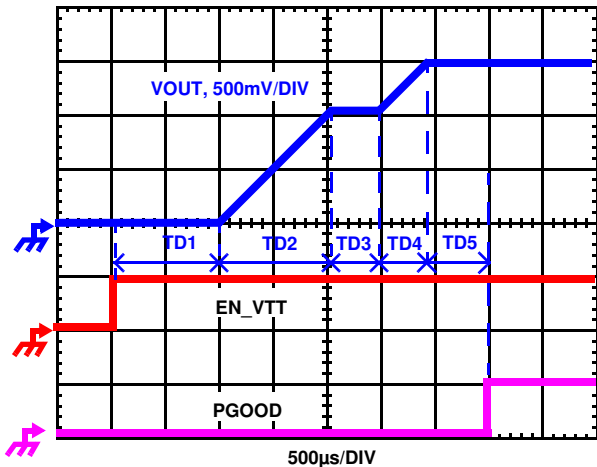


FIGURE 11. INTEL SOFT-START WAVEFORMS

TD1 is a fixed delay with the typical value as 1.40ms. TD3 is determined by the fixed 85µs plus the time to obtain valid VID voltage. If the VID is valid before the output reaches the 1.1V, the minimum time to validate the VID input is 500ns. Therefore the minimum TD3 is about 86µs.

During TD2 and TD4, ISL6322 digitally controls the DAC voltage change at 6.25mV per step. The time for each step is determined by the frequency of the soft-start oscillator which is defined by the resistor R_{SS} from SS pin to GND. The second soft-start ramp time TD2 and TD4 can be calculated based on the following equations:

$$TD2 = \frac{1.1 \cdot R_{SS}}{6.25 \cdot 25} (\mu\text{s}) \quad (\text{EQ. 18})$$

$$TD4 = \frac{|(V_{VID} - 1.1)| \cdot R_{SS}}{6.25 \cdot 25} (\mu\text{s}) \quad (\text{EQ. 19})$$

For example, when VID is set to 1.5V and the R_{SS} is set at 100kΩ, the first soft-start ramp time TD2 will be 704µs and the second soft-start ramp time TD4 will be 256µs.

NOTE: If the SS pin is grounded, the soft-start ramp in TD2 and TD4 will be defaulted to a 6.25mV step frequency of 330kHz.

After the DAC voltage reaches the final VID setting, PGOOD will be set to high with the fixed delay TD5. The typical value for TD5 is 440µs.

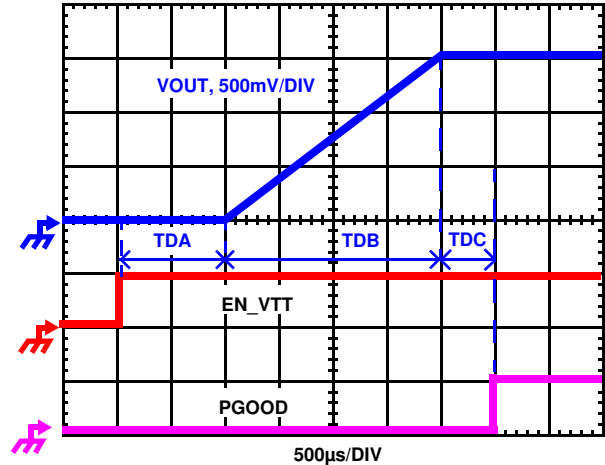


FIGURE 12. AMD SOFT-START WAVEFORMS

AMD Soft-Start

For the AMD 5-bit and 6-bit modes of operation, the soft-start sequence is composed of three periods, as shown in Figure 12. At the beginning of soft-start, the VID code is immediately obtained from the VID pins, followed by a fixed delay period TDA. After this delay period the ISL6322 will begin ramping the output voltage to the desired DAC level at a fixed rate of 6.25mV per step, with a stepping frequency of 330kHz. The amount of time required to ramp the output voltage to the final DAC voltage is referred to as TDB, and can be calculated as shown in Equation 20.

$$TDB = \frac{1}{330 \times 10^3} \cdot \left(\frac{V_{VID}}{0.00625} \right) \quad (\text{EQ. 20})$$

After the DAC voltage reaches the final VID setting, PGOOD will be set to high with the fixed delay TDC. The typical value for TDC can range between 1.5ms and 3.0ms.

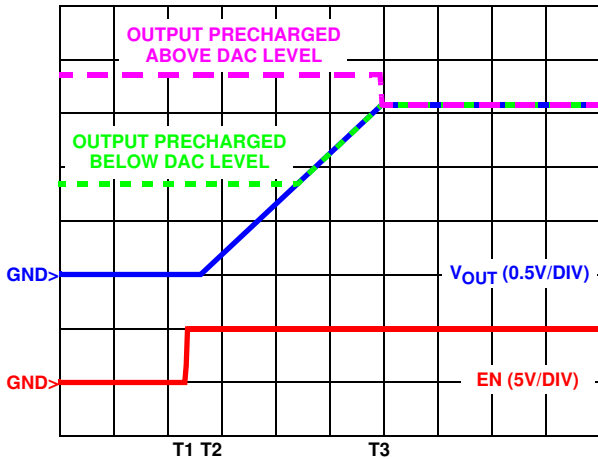


FIGURE 13. SOFT-START WAVEFORMS FOR ISL6322-BASED MULTIPHASE CONVERTER

Pre-Biased Soft-Start

The ISL6322 also has the ability to start up into a pre-charged output, without causing any unnecessary disturbance. The FB pin is monitored during soft-start, and should it be higher than the equivalent internal ramping reference voltage, the output drives hold both MOSFETs off. Once the internal ramping reference exceeds the FB pin potential, the output drives are enabled, allowing the output to ramp from the pre-charged level to the final level dictated by the DAC setting. Should the output be pre-charged to a level exceeding the DAC setting, the output drives are enabled at the end of the soft-start period, leading to an abrupt correction in the output voltage down to the DAC-set level.

Fault Monitoring and Protection

The ISL6322 actively monitors output voltage and current to detect fault conditions. Fault monitors trigger protective measures to prevent damage to a microprocessor load. One common power good indicator is provided for linking to external system monitors. The schematic in Figure 14 outlines the interaction between the fault monitors and the power good signal.

Power Good Signal

The power good pin (PGOOD) is an open-drain logic output that signals whether or not the ISL6322 is regulating the output voltage within the proper levels, and whether any fault conditions exist. This pin should be tied to a +5V source through a resistor.

During shutdown and soft-start PGOOD pulls low and releases high after a successful soft-start and the output voltage is operating between the undervoltage and overvoltage limits. PGOOD transitions low when an undervoltage, overvoltage, or overcurrent condition is detected or when the controller is disabled by a reset from EN, EN_PH4, POR, or one of the no-CPU VID codes. In the event of an overvoltage or overcurrent condition, the

controller latches off and PGOOD will not return high until after a successful soft-start. In the case of an undervoltage event, PGOOD will return high when the output voltage returns to within the undervoltage.

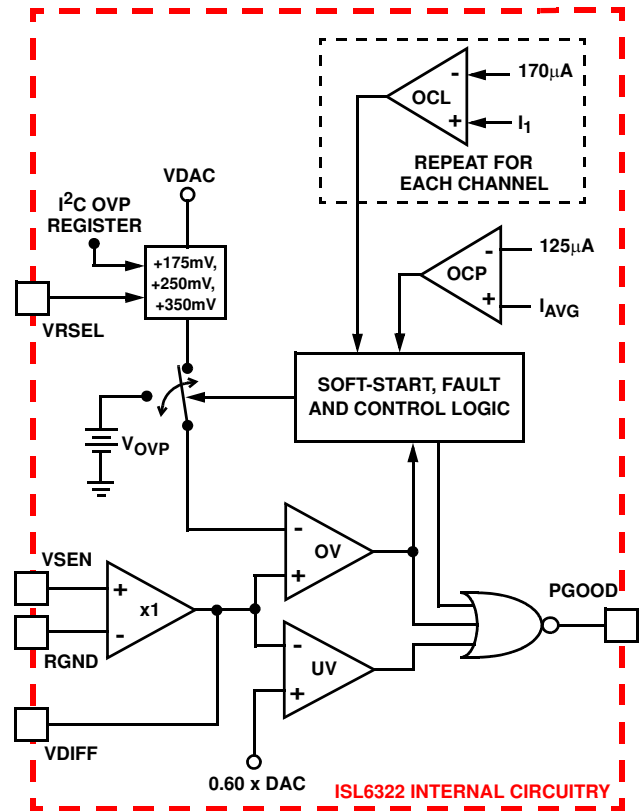


FIGURE 14. POWER GOOD AND PROTECTION CIRCUITRY

Undervoltage Detection

The undervoltage threshold is set at 60% of the VID code. When the output voltage (VSEN-RGND) is below the undervoltage threshold, PGOOD gets pulled low. No other action is taken by the controller. PGOOD will return high if the output voltage rises above 70% of the VID code.

Overvoltage Protection

The ISL6322 constantly monitors the sensed output voltage on the VDIF pin to detect if an overvoltage event occurs. When the output voltage rises above the OVP trip level actions are taken by the ISL6322 to protect the microprocessor load. The overvoltage protection trip level changes depending on what mode of operation the controller is in and what state the I²C registers and the VRSEL pin are in. Table 6 and 7 below list what the OVP trip levels are under all conditions (see pages 27 through 31 for details of controlling OVP thresholds with I²C).

At the inception of an overvoltage event, LGATE1, LGATE2 and LGATE3 are commanded high, PWM4 is commanded low, and the PGOOD signal is driven low. This turns on the all of the lower MOSFETs and pulls the output voltage below