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Advanced Linear EAPP Digital 6-Phase Green PWM Controller for Digital Power Management with NVM and AUTO Phase Shedding

ISL6398

The ISL6398 is a **smart** and **smallest** 6-Phase **Green** PWM controller, designed for networking, datacenter, and POL applications. It includes programmable functions and telemetries for easy use and system flexibility using SMBus, PMBus, or I^2C interface, which is designed to program NVM banks up to 8 different compensations and system parameters. This **minimizes** external components and significantly reduces design complexity and PCB area, and **simplifies** the manufacturing process.

The ISL6398 utilizes Intersil's proprietary **Advanced Linear EAPP** (Enhanced Active Pulse Positioning) **Digital** control scheme to achieve the extremely fast linear transient response with fewer output capacitors and overcomes many hurdles of traditional digital approach, which uses non-linear, discrete control method for both voltage loop and current balance loop and runs into beat frequency oscillation and non-linear response. The ISL6398 accurately monitors the load current via the IMON pin and reports this information via the READ_IOUT register for power management. The ISL6398 features auto-phase shedding. In low power operation, the magnetic core and switching losses are significantly reduced with lower phase count operation, yielding high efficiency at light load. When APA is triggered, the dropped phase(s) are added back to sustain heavy load transient response and efficiency. It optimizes the efficiency from light to full load for **Greener Environment** without sacrificing the transient performance.

The ISL6398 senses the output current continuously by a dedicated current sense resistor or the DCR of the output inductor. The sensed current flows through a digitally programmable 1% droop resistor for precision load line control. Current sensing circuits also provide the needed signals for channel-current balancing, average overcurrent protection and individual phase current limiting. The TM pin senses an NTC thermistor's temperature, which is internally digitized for thermal monitoring and for integrated thermal compensation of the current sense elements of the regulator.

The ISL6398 features remote voltage sensing and completely eliminates any potential difference between remote and local grounds. This improves regulation and protection accuracy. The threshold-sensitive enable input is available to accurately coordinate the start-up of the ISL6398 with other voltage rails.

Features

- SMBus/PMBus/I^2C Compatible
  - Programmable IMAX, TMAX, BOOT, and address
  - Programmable soft-start rate and DVID rate
  - Up to 1.5MHz
  - NVM to store up to 8 Configurations with programmable frequency, droop, auto, faults (OCP, UVP, CFP), etc.
  - No firmware requirement and hassle
- **Advanced Linear EAPP Digital** control scheme (patented)
  - Digitally programmable compensation
  - Auto phase shedding option for greener environment
  - Variable frequency control during load transients to reduce beat frequency oscillation
  - Linear control with evenly distributed PWM pulses for better phase current balance during load transients
  - Voltage feed-forward and ramp adjustable options
  - High frequency compensation option
  - Active phase adding and dropping for enhanced light load efficiency
- Phase doubler and coupled-inductor compatibility
- Differential remote voltage sensing with ±0.5% accuracy
- Programmable minimum phase count operation
- Programmable slew rate of dynamic VID with dynamic VID compensation (DVC)
- Support 3-state 5V or 3.3V PWM DrMOS and driver
- Zero current shutdown with ISL6627
- Precision resistor or DCR differential current sensing
  - Accurate load-line (Droop) programming and control
  - Accurate current monitoring and channel-current balancing with calibration capability
- True input current sensing for catastrophic failure protection
- Average overcurrent protection and channel current limiting
- High common mode current sense input (VCC-1.5V)
- Open sensing and single point of loop failure protection
- Thermal monitoring and integrated compensation
- 1- to 6-Phase option and up to 2MHz per phase
- Start-up into precharged load
- Pb-free (RoHS Compliant)
- 40 Ld 5x5 Plastic Package

Applications

- High efficiency and high density digital power
- High performance multi-phase POL and network
- Cloud Computing, Router, Data Center and Storage
- General processor power

Table of Contents

Ordering Information

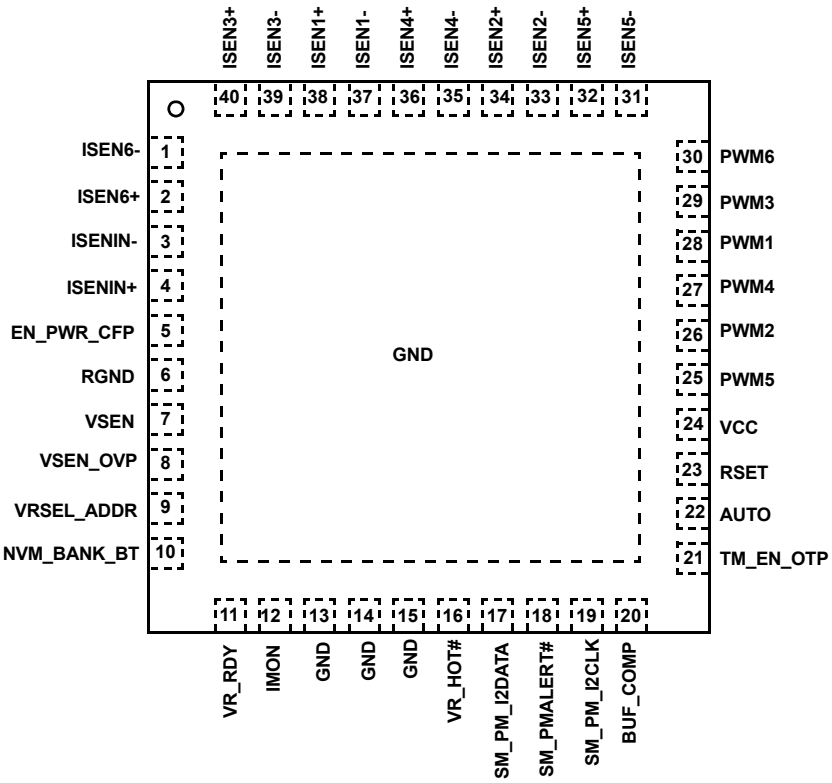
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6398HRTZ	ISL6398 HRTZ	-10 to +100	40 Ld 5x5 TQFN	L40.5x5
ISL6398IRTZ	ISL6398 IRTZ	-40 to +85	40 Ld 5x5 TQFN	L40.5x5
ISL6398EVAL1Z	120A 3-Phase Evaluation Board with On Board Transient			

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for ISL6398. For more information on MSL please see techbrief TB363.

Pin Configuration

ISL6398
(40 LD 5X5 TQFN)
TOP VIEW

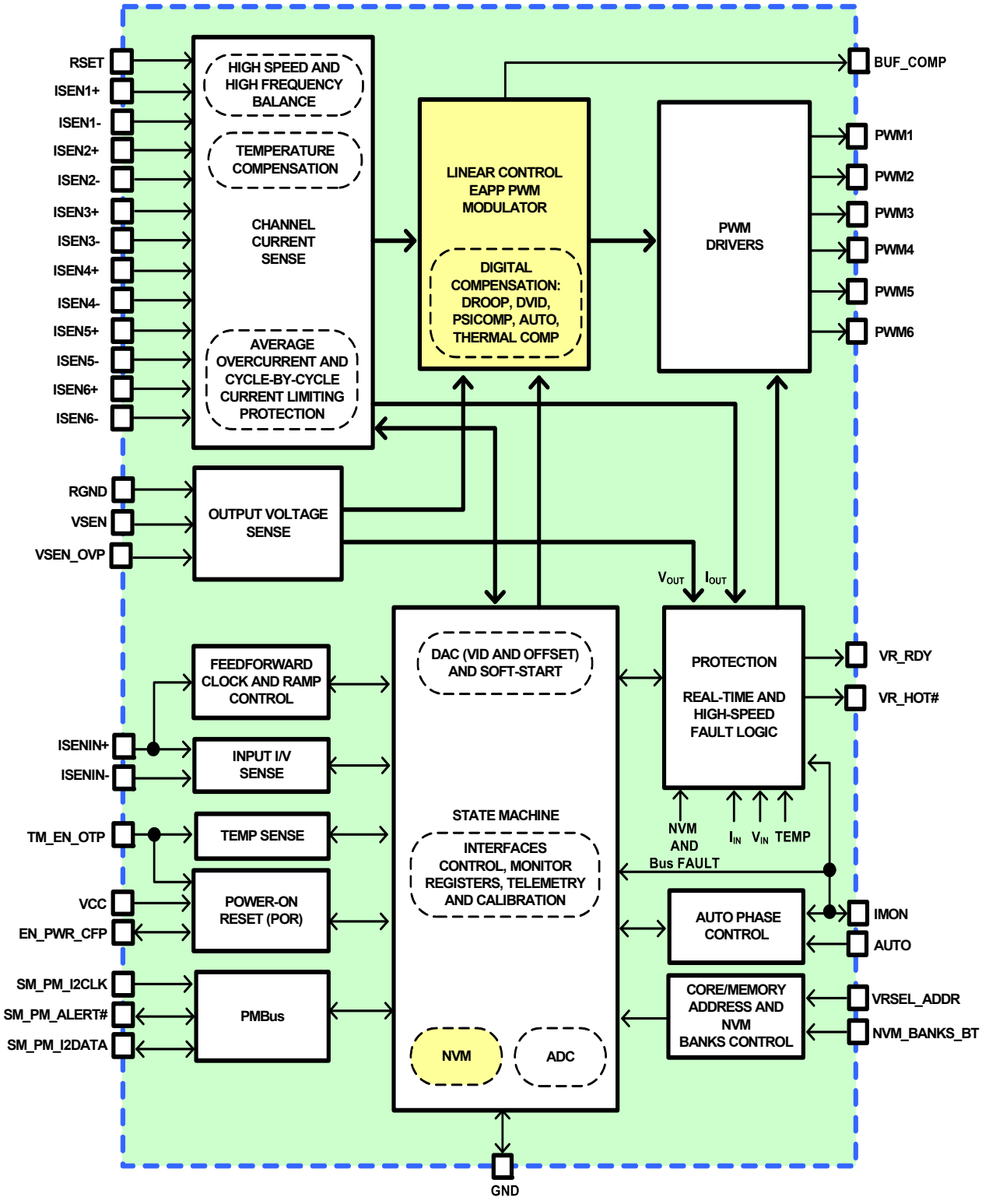


Driver Recommendation

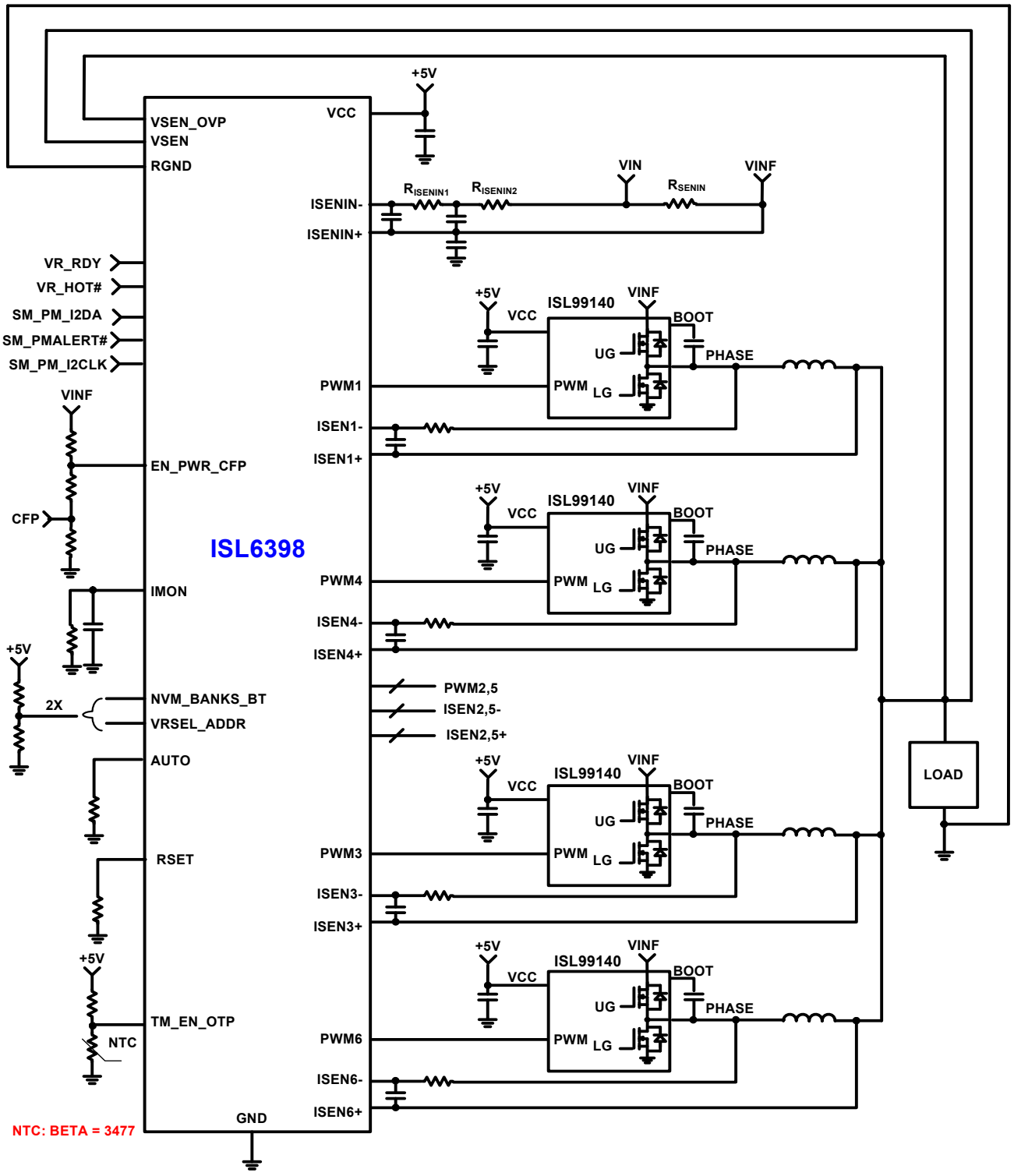
DRIVER	QUIESCENT CURRENT (mA)	GATE DRIVE (V)	# OF DRIVERS	DIODE EMULATION (DE)	COMMENTS
ISL6627	1.0	5V	Single	Yes	For dropped phases or all channels with Diode Emulation (DE) for low stress shutdown or phase dropping.
ISL6596	0.19	5V	Single	No	For dropped phases or all channels without DE.
ISL6610 ISL6610A	0.24	5V	Dual	No	For dropped phases or all channels without DE.
ISL6611A	1.25	5V	Dual	No	Phase Doubler with Integrated Drivers, up to 12-Phase. For all channels with DE Disabled.
ISL6617	5.0	N/A	N/A	No	PWM Doubler for DrMOS, up to 12- or 24-Phase. For all channels with DE Disabled.
ISL99140	0.47	5V	Single	Yes	DrMOS with 40A current capability. ISL99140's diode emulation is not compatible with ISL6398. Both DrMOS and ISL6398 should disable their diode emulation operation.

NOTE: Intersil 5V and 12V drivers are mostly pin-to-pin compatible and allow for dual footprint layout implementation to optimize MOSFET selection and efficiency. The 5V Drivers are more suitable for high frequency and high power density applications.

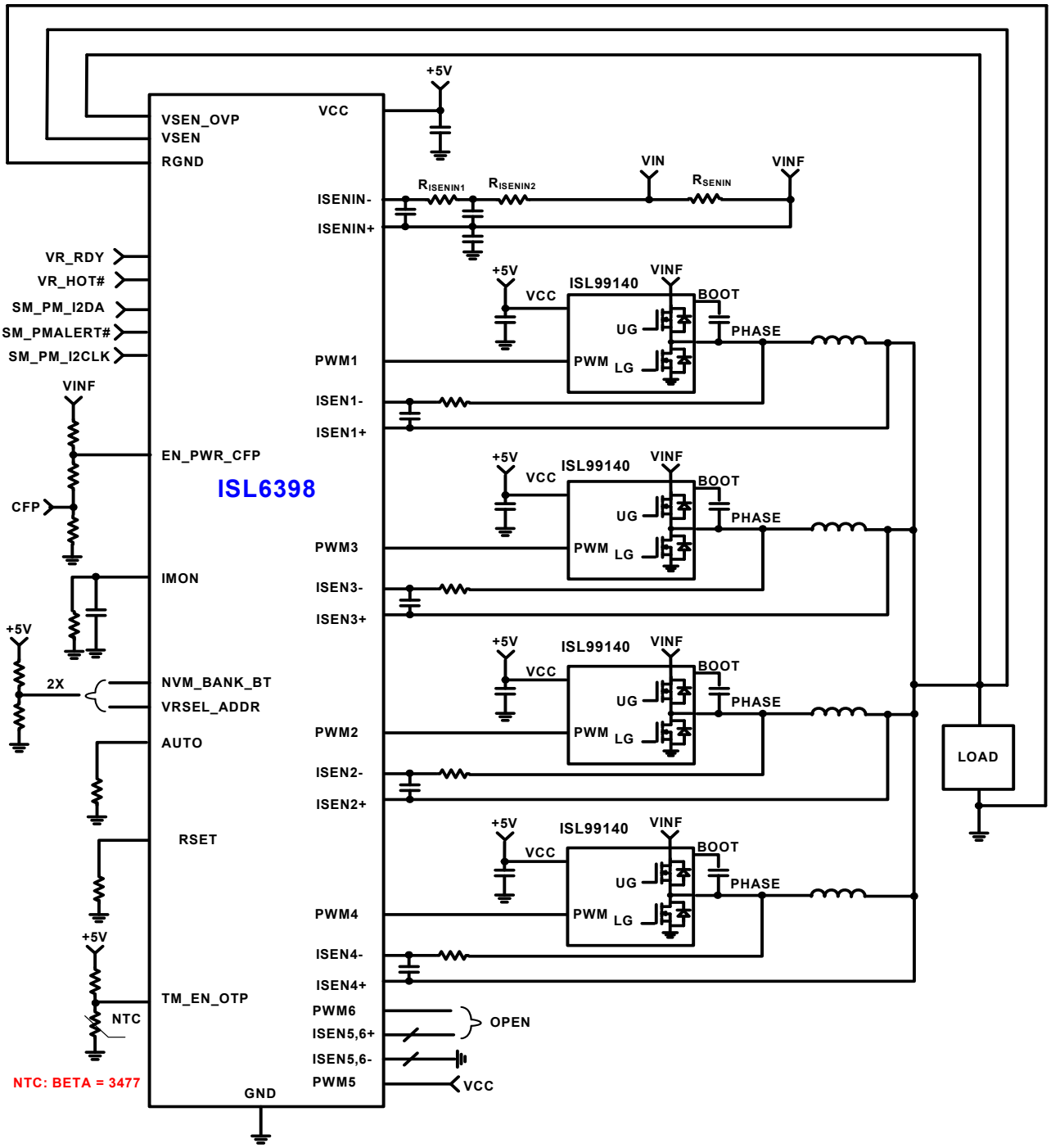
ISL6398 Internal Block Diagram



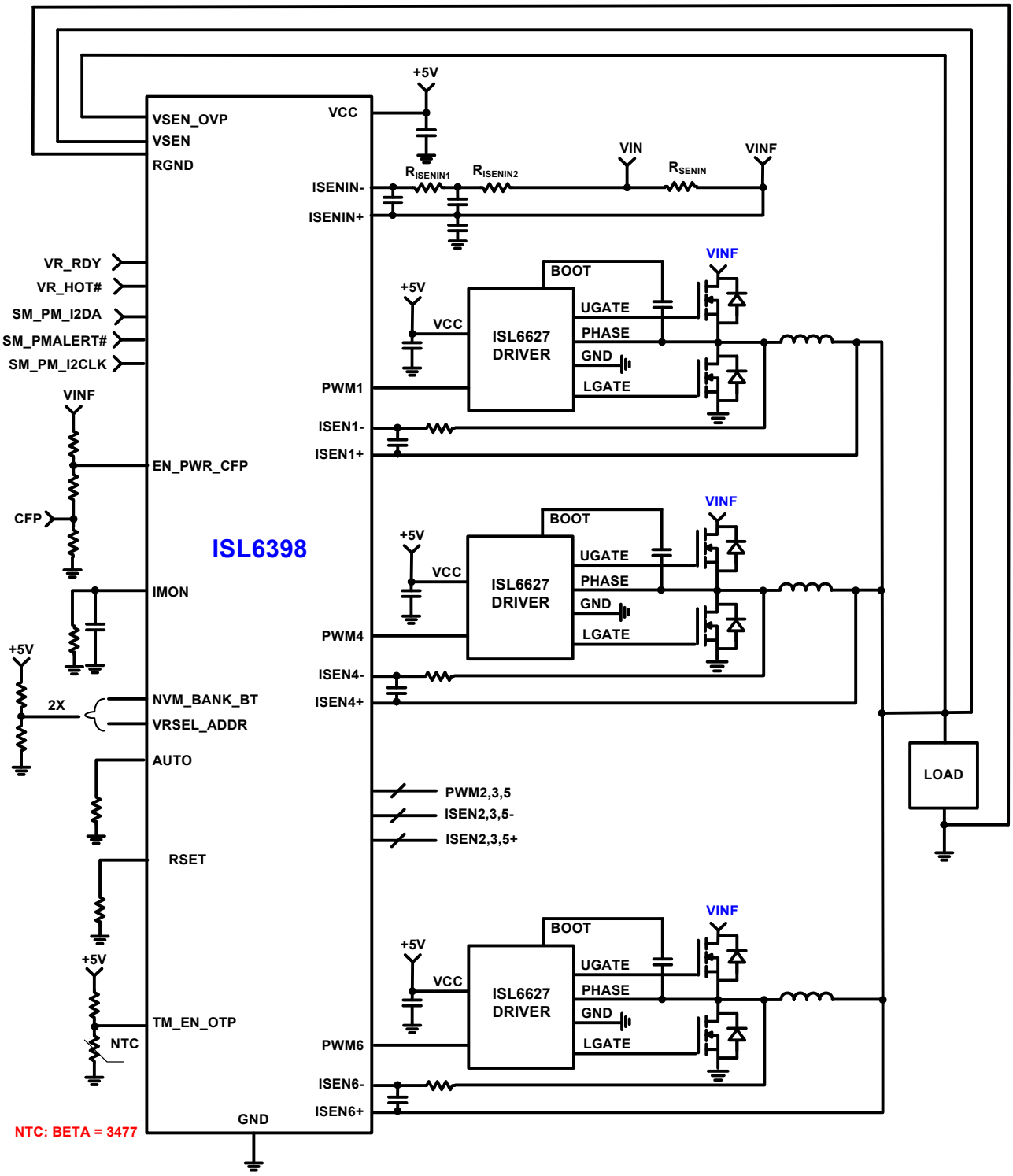
Typical Application: 6-Phase VR with DrMOS and PMBus/SMBus/I²C



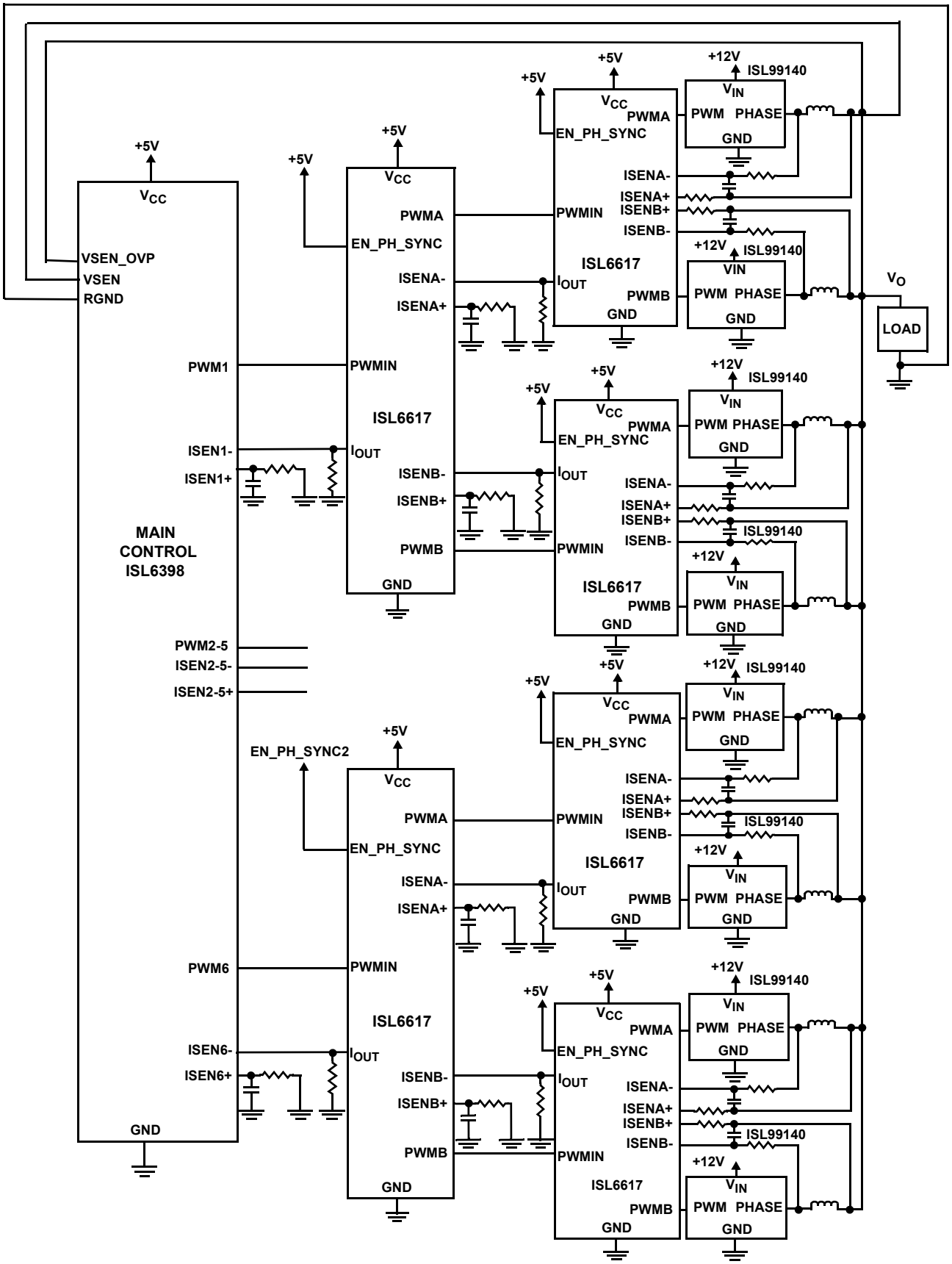
Typical Application: 4-Phase VR with DrMOS and PMBus/SMBus/I²C



Typical Application: 6-Phase VR for General Processor Power



Typical Application: 12-Phase VR for Over-clocking Applications



Absolute Maximum Ratings

VCC, VR_RDY . . . . . +6V
ISENIN± . . . . . .GND -0.3V to 27V
All Other Pins . . . . . .GND -0.3V to V_{CC} + 0.3V

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . .+5V ±5%
EEPROM Write and Store Command Temperature . . . . . .-40°C to +85°C
Ambient Temperature
ISL6398HRTZ . . . . . .-10°C to +100°C
ISL6398IRTZ . . . . . .-40°C to +85°C

Thermal Information

Thermal Resistance (Notes 4, 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
40 Ld 5x5 TQFN Package	29	1

Maximum Junction Temperature . . . . . .+150°C
Maximum Storage Temperature Range . . . . . .-65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, V_{CC} = 5V, Unless Otherwise specified. **Boldface limits apply across the operating temperature range.**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
V_{CC} SUPPLY CURRENT					
Nominal Supply	V_{CC} = 5VDC; EN_PWR = 5VDC; F_{SW} = 400kHz	-	35	**45**	mA
Shutdown Supply	V_{CC} = 5VDC; EN_PWR = 0VDC; F_{SW} = 400kHz	-	27	**33**	mA
POWER-ON RESET AND ENABLE					
V_{CC} Rising POR Threshold		**4.22**	4.35	**4.55**	V
V_{CC} Falling POR Threshold		**4.00**	4.10	**4.22**	V
EN_PWR_CFP High Level Turn-OFF Threshold	Externally Driven	**3.5**	3.6	**3.7**	V
EN_PWR_CFP High Level Turn-ON Threshold	Externally Driven	**3.33**	3.52	**3.58**	V
EN_PWR_CFP Latch-OFF Level	Internally Driven, 5mA Load	**4.80**	-	**-**	V
EN_PWR_CFP Internal Pull-Up Impedance		**-**	12	**34**	Ω
EN_PWR_CFP Rising Threshold		**0.83**	0.85	**0.87**	V
EN_PWR_CFP Falling Threshold		**0.70**	0.77	**0.84**	V
DAC (VID+OFFSET)					
System Accuracy of Commercial Temperature (T_J = 0°C to +70°C, Note 6, Closed-Loop)	DAC = 1.5V to 3.04 V	**-0.5**	-	**0.5**	%VID
	DAC = 0.8V to 1.49V	**-5**	-	**5**	mV
	DAC = 0.25V to 0.795V	**-8**	-	**8**	mV
System Accuracy of ISL6398HRTZ (T_J = -10°C to +100°C, Note 6, Closed-Loop)	DAC = 1.5V to 3.04 V	**-0.55**	-	**0.55**	%VID
	DAC = 0.8V to 1.49V	**-7**	-	**7**	mV
	DAC = 0.25V to 0.795V	**-9**	-	**9**	mV
System Accuracy of ISL6398IRTZ (T_J = -40°C to +85°C, Note 6, Closed-Loop)	DAC = 1.5V to 3.04 V	**-0.6**	-	**0.6**	%VID
	DAC = 0.8V to 1.49V	**-10**	-	**10**	mV
	DAC = 0.25V to 0.795V	**-10**	-	**10**	mV

Electrical Specifications Recommended Operating Conditions, V_{CC} = 5V, Unless Otherwise specified. **Boldface limits apply across the operating temperature range. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
OSCILLATORS					
Accuracy of Switching Frequency Setting	390kHz, F3[2:0] = 0h = Original, ISL6398HRTZ	**355**	390	**425**	kHz
	390kHz, F3[2:0] = 0h = Original, ISL6398IRTZ	**348**	390	**425**	kHz
Maximum Switching Frequency		**-**	2.025	-	MHz
Minimum Switching Frequency		**-**	0.120	**-**	MHz
Soft-start Ramp Rate	DVID = 0.3125mV/µs, Minimum	**0.3125**	-	**-**	mV/µs
	DVID = 2.5mV/µs	**2.5**	3.0	**3.4**	mV/µs
	DVID = 5.0mV/µs	**5.0**	6.0	**7.0**	mV/µs
	DVID = 13.25mV/µs, Maximum	**13.25**	-	**-**	mV/µs
Minimum Dynamic VID Slew Rate	DVID = 0.3125mV/µs, Minimum	**0.3125**	-	**-**	mV/µs
Maximum Dynamic VID Slew Rate	DVID = 13.25mV/µs, Maximum	**13.25**	-	**-**	mV/µs
Maximum Duty Cycle Per PWM	390kHz	**95**	98	**99**	%
PWM GENERATOR					
Sawtooth Amplitude	VR_{RAMP_ADJ} = 0.7V, ISENIN+ = 12V	**-**	0.7	-	V
	VR_{RAMP_ADJ} = 1.0V, ISENIN+ = 12V	**-**	1.0	-	V
	VR_{RAMP_ADJ} = 1.2V, ISENIN+ = 12V	**-**	1.2	-	V
	VR_{RAMP_ADJ} = 1.5V, ISENIN+ = 12V	**-**	1.5	-	V
BUFFERED COMP AMPLIFIER					
Open-Loop Gain	R_L = 10kΩ to ground	**-**	96	-	dB
Open-Loop Bandwidth		**-**	20	-	MHz
Maximum Output Voltage	No Load	**3.6**	4.0	**-**	V
Output High Voltage	1mA Load	**3.4**	3.9	**-**	V
Output Low Voltage	1mA Load	**1.88**		**1.99**	V
PWM OUTPUT (PWM[6:1])					
PWM[6:1] Sink Impedance	PWM = Low with 1mA Load, for Fast Transition	**-**	80	-	Ω
	PWM = Low with 1mA Load, ISL6398HRTZ	**170**	285	**425**	Ω
	PWM = Low with 1mA Load, ISL6398IRTZ	**170**	285	**400**	Ω
PWM[6:1] Source Impedance	PWM = High, Forced to 3.7V	**60**	125	**210**	Ω
PWM Mid-Level	0.4mA Load, 5V PWM	**36**	40	**44**	%VCC
PWM Mid-Level	0.4mA Load, 3.3V PWM	**24**	28	**31**	%VCC
CURRENT SENSE AND OVERCURRENT PROTECTION					
Sensed Current Tolerance CS Offset and Mirror Error Included, R_{SET} = 12.8kΩ	(T_J = 0°C to +70°C)	**73**	78	**82.5**	µA
	(T_J = -40°C to +100°C, HRTZ, IRTZ)	**72**	78	**83**	µA
Average OC Trip Level at Normal CCM PWM Mode CS Offset and Mirror Error Included, R_{SET} = 12.8kΩ	(T_J = 0°C to +70°C)	**96**	103	**111**	µA
	(T_J = -40°C to +100°C, HRTZ, IRTZ)	**95**	103	**112**	µA
Average Overcurrent Trip Level at PSI1/2/3 Mode CS Offset and Mirror Error Included, R_{SET} = 12.8kΩ	(T_J = 0°C to +70°C)	**92**	107	**122**	µA
	(T_J = -40°C to +100°C, HRTZ, IRTZ)	**90**	125	**124**	µA

Electrical Specifications Recommended Operating Conditions, V_{CC} = 5V, Unless Otherwise specified. **Boldface limits apply across the operating temperature range. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Peak Current Limit for Individual Channel CS Offset and Mirror Error Included, R_{SET} = 12.8kΩ	(T_J = 0°C to +70°C)	**118**	125	**133**	µA
	(T_J = -40°C to +100°C, HRTZ, IRTZ)	**116**	125	**134**	µA
IMON OCP Trip Level		**2.9**	3.0	**3.1**	V
IMON VOLTAGE IMAX (FF) TRIP POINT	Higher than this will be “FF”	**2.45**	2.5	**2.56**	V
READ_IIN (1F) Maximum Threshold		**-**	10	**-**	µA
Input Peak Current Trip Level		**13.9**	15	**16.5**	µA
THERMAL MONITORING					
VR_HOT# Pull-down Impedance		**-**	9.2	**13**	Ω
TM Voltage at VR_HOT# Trip	TMAX = +100°C (see Table 6), Programmable via Tmax	**-**	39.12	-	%VCC
VR_HOT# and Thermal Alert# Hysteresis		**-**	3	-	°C
Leakage Current of VR_HOT#	With external pull-up resistor connected to V_{CC}	**-**	-	**1**	µA
Over-Temperature Shutdown Threshold		**0.91**	0.94	**0.97**	V
Over-Temperature Shutdown Reset Threshold		**1.04**	1.07	**1.11**	V
VR READY AND PROTECTION MONITORS					
Leakage Current of VR_RDY	With pull-up resistor externally connected to V_{CC}	**-**	-	**1**	µA
VR READY Low Voltage	4mA Load	**-**	-	**0.3**	V
Undervoltage Protection Threshold (UVP) Can Be Disabled by DFh	Voltage below VID E1[3:0] = 0h)	**65**	105	**146**	mV
	Voltage below VID E1[3:0] = 1h)	**93**	141	**191**	mV
	Voltage below VID E1[3:0] = 2h)	**121**	178	**236**	mV
	Voltage below VID E1[3:0] = 3h)	**149**	214	**281**	mV
	Voltage below VID E1[3:0] = 4h)	**177**	252	**330**	mV
	Voltage below VID E1[3:0] = 5h)	**207**	291	**378**	mV
	Voltage below VID E1[3:0] = 6h)	**233**	328	**426**	mV
	Voltage below VID E1[3:0] = 7h)	**288**	402	**519**	mV
Undervoltage Warning Threshold (UVP Warning) Can Be Disable by DFh	Voltage below VID E1[3:0] = 0h)	**10**	41	**72**	mV
	Voltage below VID E1[3:0] = 1h)	**35**	72	**109**	mV
	Voltage below VID E1[3:0] = 2h)	**61**	103	**146**	mV
	Voltage below VID E1[3:0] = 3h)	**84**	135	**186**	mV
	Voltage below VID E1[3:0] = 4h)	**109**	168	**226**	mV
	Voltage below VID E1[3:0] = 5h)	**133**	202	**268**	mV
	Voltage below VID E1[3:0] = 6h)	**157**	234	**307**	mV
	Voltage below VID E1[3:0] = 7h)	**201**	298	**389**	mV
Undervoltage Protection Reset Hysteresis	Higher than UVP	**-**	19	**-**	mV
Undervoltage Warning Reset Hysteresis	Higher than UVP Warning	**-**	17	**-**	mV

Electrical Specifications Recommended Operating Conditions, V_{CC} = 5V, Unless Otherwise specified. **Boldface limits apply across the operating temperature range. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Overvoltage Protection Threshold (OVP) Can Be Disabled by DFh	Prior to the End of Soft-start (D8h[4:3] = 0h)	**1.51**	1.58	**1.70**	V
	Prior to the End of Soft-start (D8h[4:3] = 1h)	**1.75**	1.86	**1.95**	V
	Prior to the End of Soft-start (D8h[4:3] = 2h)	**2.20**	2.29	**2.40**	V
	Prior to the End of Soft-start (D8h[4:3] = 3h)	**3.10**	3.32	**3.50**	V
	End of Soft-start, the voltage above VID D8[2:0] = 0h)	**91**	135	**177**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 1h)	**125**	177	**225**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 2h)	**158**	218	**274**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 3h)	**191**	260	**323**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 4h)	**254**	342	**424**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 5h)	**318**	425	**526**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 6h)	**347**	460	**580**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 7h)	**395**	549	**697**	mV
Overvoltage Protection Reset Hysteresis	Prior to the end of Soft-start, lower than OVP	**55**	110	**180**	mV
	During operation, lower than OVP	-	83	-	mV
Overvoltage Warning Threshold (OVP) Can Be Disabled by DFh	End of Soft-start, the voltage above VID D8[2:0] = 0h)	**22**	54	**83**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 1h)	**60**	96	**129**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 2h)	**97**	138	**176**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 3h)	**132**	179	**225**	mV
	End of soft-start, the voltage above VID D8[2:0] = 4h)	**205**	264	**324**	mV
	End of soft-start, the voltage above VID D8[2:0] = 5h)	**273**	347	**427**	mV
	End of soft-start, the voltage above VID D8[2:0] = 6h)	**308**	389	**476**	mV
	End of soft-start, the voltage above VID D8[2:0] = 7h)	**377**	474	**578**	mV
Overvoltage Warning Reset Hysteresis	Lower than OVP Warning	-	42	-	mV
SMBus/PMBus/I^{2}C					
Signal Input Low Voltage		-	-	**0.8**	V
Signal Input High Voltage		**2.1**	-	**VCC**	V
Signal Output Low Voltage	4mA loading on Alert#	-	-	**0.4**	V
ALERT# Pull-down Impedance		-	28	**50**	Ω
DATA Pull-down Impedance		-	28	**50**	Ω
CLOCK Maximum Speed		**1.5**	-	-	MHz
CLOCK Minimum Speed		-	-	**0.05**	MHz
Time-out		25	30	35	ms
EEPROM					
Number of NVM_BANK		-	8	-	
NVM_BANK Loading Time	Including POR delay and Resistor Reading Time	-	16	**20**	ms

NOTES:

6. These parts are designed and adjusted for accuracy with all errors in the voltage loop included.
7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Functional Pin Descriptions

Refer to Table 19 on page 53 for Design and Layout Considerations.

VCC - Supplies the power necessary to operate the chip. Connect this pin directly to a +5V supply with a high quality ceramic bypass capacitor. The controller start to operate, when the voltage on this pin exceeds the rising POR threshold and shuts down when the voltage on this pin drops below the falling POR threshold.

GND - The bottom metal base of ISL6398 is return of VCC supply. It is also the return of the PMBus as well as all PWM output drivers. Connect it to system ground; also externally connect pins 13, 14, and 15 to system GND.

ISENIN+, ISENIN- - These pins are current sense inputs to the differential amplifier of the input supply. The sensed current is used for input power monitoring and power management of the system. When not used, connect ISENIN+ to VIN and a resistor divider with a ratio of 1/3 on ISENIN± pin, say 499kΩ in between ISENIN± pins and then 1.5MΩ from ISENIN- to ground (see Figure 29). Refer to "Input Current Sensing" on page 30 for configuration details. Regardless input current sense is used or not, ISENIN+ should be connected to input voltage (V_{IN}) for feed-forward compensation to maintain a constant loop gain over the input line variation.

EN_PWR_CFP - This pin is a threshold-sensitive enable input and a catastrophic failure protection (CFP) output. Connecting the power train input supply to this through an appropriate resistor divider provides input undervoltage protection and a means to synchronize the power sequencing of the controller and the MOSFET driver ICs. When EN_PWR_CFP is driven above 0.85V but below 3.3V, the controller is actively depending on status of the TM_EN_OTP, the internal POR, and pending fault states. Driving EN_PWR_CFP below 0.75V or above 3.7V will turn off the controller, clear all fault states (except for CFP fault) and prepare the ISL6398 to soft-start when re-enabled. In addition, this pin will be latched high (VCC) by the input overcurrent (monitored by ISENIN±) or VR overvoltage event. The latch resets by cycling VCC and cannot reset by TM_EN_OTP or EN_PWR_CFP since when the catastrophic failure (CFP) is triggered, the input power is removed from VR so is the VTT voltage rail and it is PGOOD signal. To keep CFP active, VCC should be biased with a standby supply. This feature means to provide protection to the case that the VR with shorted high-side MOSFET draws insufficient current to trigger the input supply's over current trip level, this pin will send an active high signal (CFP) to disconnect the input supply before catching fire or further damage of PCB. Refer "Catastrophic Fault Protection" on page 30 for more details.

VSEN_OVP - This pin monitors the regulator output for overvoltage protection. Connect this pin to the positive rail remote sensing point of the microprocessor or load. This pin tracks with the VSEN pin. If a resistive divider is placed on the VSEN pin, a resistive divider with the same ratio should be placed on the VSEN_OVP pin to track UVP and OVP.

VSEN - This pin compensates the voltage drop between the load and local output rail for precision regulation. Connect this pin to the positive rail remote sensing point of the microprocessor or load. It also is the APA level sensing input.

RGND - This pin compensates the offset between the remote ground of the load and the local ground of this device for precision regulation. Connect this pin to the negative rail remote sensing point of the microprocessor or load.

VR_RDY - VR_RDY indicates that soft-start has completed and the output remains in normal operation. It is an open-drain logic output. When OCP, UVP, OVP, or CFP occurs, VR_RDY is pulled low.

TM_EN_OTP - Input pin for the temperature measurement. Connect this pin through an NTC thermistor to GND and a resistor to VCC of the controller. The voltage at this pin is inversely proportional to the VR temperature. The device monitors the VR temperature based on the voltage at the TM pin. Combined with "TCOMP" setting, the sensed current is thermally compensated. The VR_HOT# asserts low if the sensed temperature at this pin is higher than the maximum desired temperature, "TMAX". The NTC should be placed close to the current sensing element, the output inductor or dedicated sense resistor on Phase 1. A decoupling capacitor (0.1µF) is typically needed in close proximity to the controller. In addition, the controller is disabled when this pin's voltage drops below 0.95 (typically) and is active when it is above 1.05V (typically); it can serve as Enable and Over-Temperature functions, however, when it is used as an Enable toggle input, bit2 of STATUS_BYTE (78h) will flag OT; CLEAR_FAULTS (03h) command must be sent to clear the fault after VR start-up. If not used, connect a 1MΩ/2MΩ resistor divider or tie to V_{CC}.

PWM[6:1] - Pulse width modulation outputs. Connect these pins to the PWM input pins of the Intersil driver IC(s). The number of active channels is determined by the state of PWM[6:2]. Tie PWM(N+1) to VCC to configure for N-phase operation. The PWM firing order is sequential from 1 to N with N being the number of active phases. If PWM1 is tied high, the VR is disabled.

ISEN[6:1]+, ISEN[6:1] - The ISEN+ and ISEN- pins are current sense inputs to individual differential amplifiers of VR. The sensed current is used for channel current balancing, overcurrent protection, and droop regulation. Inactive channels should have their respective current sense inputs, ISEN[6:#]- grounded, and ISEN[6:#]+ open. For example, ground ISEN[6:5]- and open ISEN[6:5]+ for 4-phase operation. DO NOT ground ISEN[6:1]+. For DCR sensing, connect each ISEN- pin to the node between the RC sense elements. Tie the ISEN+ pin to the other end of the sense capacitor (typically output rail). The voltage across the sense capacitor is proportional to the inductor current. Therefore, the sensed current is proportional to the inductor current and scaled by the DCR of the inductor and R_{SET}.

BUF_COMP - Buffered output of internal COMP.

VR_HOT# - Indicator of VR temperature reaching above TMAX set by PMBus E8[2:0]. It is an open-drain logic output. Normally open if the measured VR temperature is less than TMAX, and pulled low when the measured VR temperature exceeds TMAX.

RSET - A resistor connected from this pin to ground sets the current gain of the current sensing amplifier. The RSET resistor value can be set from 3.84kΩ to 60.4kΩ and is 64x of the equivalent R_{ISEN} resistor value. Therefore, the effective current sense resistor value can be set between 60Ω and 943Ω.

IMON - IMON is the output pin of sensed, thermally compensated (if internal thermal compensation is used) average current of VR0. The voltage at the IMON pin is proportional to the load current and the resistor value. When it reaches to 3.0V, it initiates an overcurrent shutdown, while 2.5V IMON voltage corresponds to READ_IOUT (8Ch) maximum reading. By choosing the proper value for the resistor at IMON pin, the overcurrent trip level can be set lower than the fixed internal overcurrent threshold. During dynamic VID, the OCP function of this pin is disabled to avoid false triggering. Tie it to GND if not used. Refer to "Current Sense Output" on page 25 for more details.

AUTO - A resistor from the pin to ground sets the current threshold of phase dropping for operation. The AUTO mode can be permanently disabled by pulling this pin to ground or PMBus D4h[2]. See Table 2 on page 17 and Table 8 on page 32 for more details.

SM_PM_I2CLK - Synchronous clock signal input of SMBus/PMBus/I^2C.

SM_PM_I2DATA - I/O pin for transferring data signals SMBus/PMBus/I^2C and VR controller.

SM_PMALERT# - Output pin for transferring the active low signal driven asynchronously from the VR controller to SMBus/PMBus.

VRSEL_ADDR - Register pin used to program VR address (PMBus) and to determine 5m/step or 10mV/step mode.

NVM_BANK_BT - Register pin to select NVM memory bank to use (up to 8 configuration banks) and boot voltage, which can be set by this pin or the value stored in NVM bank.

Operation

The ISL6398 is the **smallest** 6-Phase PWM controller. It utilizes Intersil's proprietary Advanced Linear EAPP (Enhanced Active Pulse Positioning) digital control scheme that can process voltage and current information in real time for fast control and high speed protection and realize digital power management capability and flexibility. It achieves the extremely fast linear transient response with fewer output capacitors and overcomes many hurdles of traditional digital approach, which uses non-linear, discrete control method for both voltage loop and current balance loop and runs into beat frequency oscillation and non-linear response. The ISL6398 is designed to cloud computing, networking, datacenter, and POL applications. The system parameters and required registers are programmable and can be stored into selected NVM_BANK via PMBus, no firmware required. It allows up to 8 memory banks, i.e., 8 different applications. This greatly simplifies the system design for various platforms and lowers inventory complexity and cost by using a single device.

In addition, this controller is compatible with phase doublers (ISL6611A and ISL6617), which can double or quadruple the phase count. For instance, the multi-phase PWM can realize up to 24-phase count system. A higher phase count system can improve thermal distribution and power conversion efficiency at heavy load.

The ISL6398 also supports coupled (2-Phase CI) inductor design. Refer to Intersil's application note, AN1268 for detailed coupled inductor discussion.

Multiphase Power Conversion

High Power processor load current profiles have changed to the point that the advantages of multiphase power conversion are impossible to ignore. The technical challenges associated with producing a single-phase converter (which are both cost-effective and thermally viable), have forced a change to the cost-saving approach of multiphase. The ISL6398 controller helps reduce the complexity of implementation by integrating vital functions and requiring minimal output components. The typical application circuits diagrams on pages 6 through 9 provide the top level views of multiphase power conversion using the ISL6398 controller.

Interleaving

The switching of each channel in a multiphase converter is timed to be symmetrically out-of-phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the 3-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase, as illustrated in Figure 1. The three channel currents (IL1, IL2 and IL3) combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM pulse is terminated 1/3 of a cycle after the PWM pulse of the previous phase. The DC components of the inductor currents combine to feed the load.

To understand the reduction of ripple current amplitude in the multiphase circuit, examine Equation 1, which represents an individual channel's peak-to-peak inductor current.

$$I_{p\text{-}p} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{L \cdot F_{SW} \cdot V_{IN}} \quad \text{(EQ. 1)}$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and F_{SW} is the switching frequency.

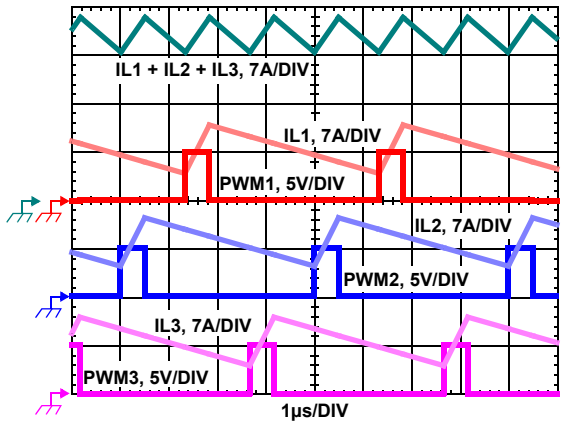


FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

In the case of multiphase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2, the peak-to-peak overall ripple current $I_{C(P-P)}$ decreases with the increase in the number of channels, as shown in Figure 2.

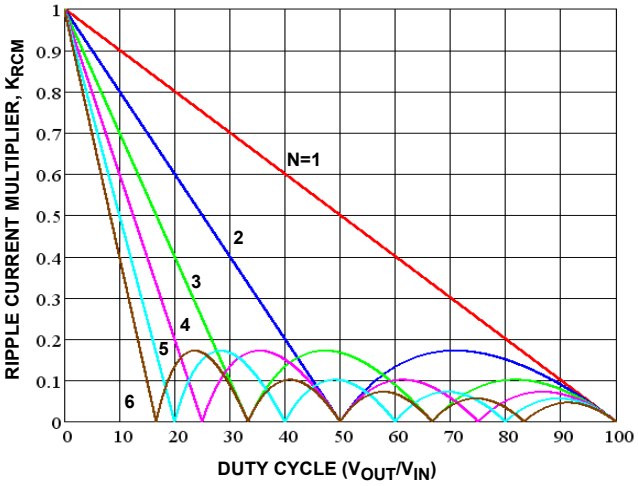


FIGURE 2. RIPPLE CURRENT MULTIPLIER VS. DUTY CYCLE

Output voltage ripple is a function of capacitance, capacitor Equivalent Series Resistance (ESR), and the summed inductor ripple current. Increased ripple frequency and lower ripple amplitude means that the designer can use less per-channel inductance and few or less costly output capacitors for any performance specification.

$$I_{c(p-p)} = \frac{V_{OUT}}{L \cdot F_{SW}} K_{RCM} \quad \text{(EQ. 2)}$$

$$K_{RCM} = \frac{(N \cdot D - m + 1) \cdot (m - (N \cdot D))}{N \cdot D}$$

$$\text{for} \quad m - 1 \le N \cdot D \le m$$

$$m = \text{ROUNDUP}(N \cdot D, 0)$$

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multiphase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitors. The example in Figure 3 illustrates input currents from a three-phase converter combining to reduce the total input ripple current.

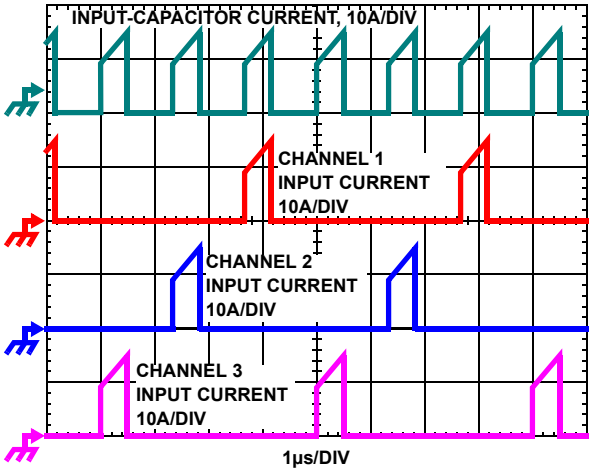


FIGURE 3. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

The converter depicted in Figure 3 delivers 36A to a 1.5V load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has $11.9A_{RMS}$ input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent three-phase converter.

Figures 37, 38 and 39, as described in "Input Capacitor Selection" on page 52, can be used to determine the input capacitor RMS current based on load current, duty cycle, and the number of channels. They are provided as aids in determining the optimal input capacitor solution. Figure 40 shows the single phase input-capacitor RMS current for comparison.

PWM Modulation Scheme

The ISL6398 adopts Intersil's proprietary Enhanced Active Pulse Positioning (EAPP) modulation scheme to improve transient performance. The EAPP is a unique dual-edge PWM modulation scheme with both PWM leading and trailing edges being independently moved to give the best response to transient loads. The EAPP has an inherited function, similar to Intersil's proprietary Adaptive Phase Alignment (APA) technique, to turn on all phases together to further improve the transient response, when there are sufficiently large load step currents. The EAPP is a variable frequency architecture, providing linear control over transient events and evenly distributing the pulses among all phases to achieve very good current balance and eliminate beat frequency oscillation over a wide range of load transient frequencies.

To further improve the line and load transient responses, the multi-phase PWM features feed-forward function to change the up ramp with the input line (voltage on ISENIN+ pin) to maintain a constant overall loop gain over a wide range input voltage. The up ramp of the internal sawtooth is defined in Equation 3.

$$V_{RAMP} = \frac{V_{IN} \cdot V_{RAMP\_ADJ}}{12V} \quad \text{(EQ. 3)}$$

With EAPP control and feed-forward function, the ISL6398 can achieve excellent transient performance over wide frequency range of load step, resulting in lower demand on the output capacitors.

Under steady state conditions, the operation of the ISL6398 PWM modulator is similar to a conventional trailing edge modulator. Conventional analysis and design methods can therefore be used for steady state and small signal analysis.

PWM Operation

The timing of each channel is set by the number of active channels. The default channel setting for the ISL6398 is six. The switching cycle is defined as the time between PWM pulse termination signals of each channel. The cycle time of the pulse signal is the inverse of the switching frequency. The PWM signals command the MOSFET driver to turn on/off the channel MOSFETs.

The ISL6398 can work in a 0 to 6-Phase configuration. Tie PWM(N+1) to VCC to configure for N-phase operation. PWM firing order is sequential from 1 to N with N being the number of active phases, as summarized in Table 1. For 6-phase operation, the channel firing sequence is 1-2-3-4-5-6, and they are evenly spaced over 1/6 of a cycle. Connecting PWM6 to V_{CC} configures 5-phase operation, the channel firing order is 1-2-3-4-5 and the phase spacing is 1/5 of a cycle. If PWM2 is connected to V_{CC}, only Channel 1 operation is selected. If PWM1 is connected to V_{CC}, the VR operation is turned off.

TABLE 1. PHASE NUMBER AND PWM FIRING SEQUENCE

N	PHASE SEQUENCE	PWM# TIED TO V_{CC}	ACTIVE PHASE AT 0A LOAD
5	1-2-3-4-5	None	PWM1/3
4	1-2-3-4	PWM5	PWM1/3
3	1-2-3	PWM4	PWM1/2
2	1-2	PWM3	PWM1/2
1	1	PWM2	PWM1
0	OFF	PWM1	OFF

The controller starts phase shedding the next switching cycle. The controller reduces the number of active phases according to the logic state on Table 2. “NPSI” register and AUTO pin program the controller in operation of standard (SI), 2-phase coupled, or (N-x)-phase coupled inductors. Different cases yield different PWM output behaviors on both dropped phase(s) and operational phase(s) as load changes. When APA is triggered, it pulls the controller back to full phase operation to sustain an immediate heavy transient load. Note that “N-x” means N-x phase(s) coupled and x phase(s) are uncoupled.

For 2-Phase coupled inductor (CI) operation, both coupled phases should be 180° out-of-phase. In low power conditions, it drops to 2-phase and the opposite phase of the operational phase turns on its low-side MOSFET to circulate inductor current to minimize conduction loss when Phase 1 is high.

In low power condition, VR is in single-phase CCM operation with PWM1, or 2-phase CCM operation with PWM1 and 2, 3 or 4, as shown in Table 1. The number of operational phases is configured by “NPSI” register, shown in Table 2.

TABLE 2. PHASE DROPPING CONFIGURATION AT LOW POWER

NPSI D2[1:0]	CODE		AUTO MINIMUM PHASE COUNT
0h	SI1	SI, (N-1)-CI	1-Phase
1h	SI2	SI, (N-2)-CI	2-Phase
2h	CI1	2-Phase CI	1-Phase
3h	CI2	2-Phase CI	2-Phase

NOTE: For 2-Phase CI option, the dropped coupled phase turns on LGATE to circulate current when PWM1 is high. Programmable via PMBus.

While the controller is operational (V_{CC} above POR, TM_EN_OTP and EN_PWR_CFP are both high, valid VID inputs), it can pull the PWM pins to ~40% of V_{CC} (~2V for 5V V_{CC} bias, for 5V PWM) or ~28% of V_{CC} (for 3.3V PWM) during various stages, such as soft-start delay, phase shedding operation, or fault conditions (OC or OV events). The matching driver's internal PWM resistor divider can further raise the PWM potential, but not lower it below the level set by the controller IC. Therefore, the controller's PWM outputs are designed to be compatible with DrMOS and Intersil drivers that require 3.3V and 5V PWM signal amplitudes, programmed by PMBus.

DrMOS and Driver Compatibility

In operational mode, the ISL6398 can actively drive PWM into tri-state level (mid level), which can be programmed to be compatible with 3.3V or 5V PWM input DrMOS or Drivers. The ISL6398’s PWM “LOW” level is 0V and PWM “HIGH” level is V_{CC} (5V). The PWM “HIGH” minimum threshold of the DrMOS should be higher than 33% of V_{CC} for 3.3V PWM logic and 44% of V_{CC} for 5V PWM logic, while the PWM “LOW” maximum threshold of the DrMOS should be lower than 26% of V_{CC} for 3.3V PWM logic and 36% of V_{CC} for 5V PWM logic. Since most of industrial DrMOS devices are not compatible with Intersil’s PWM protocol for diode emulation, therefore, the diode emulation mode should be disabled in both controller and DrMOS. Coupling with the ISL6627, zero current shutdown can be achieved, which minimizes the power stage stress.

Phase Doubler Compatibility

The ISL6398 is compatible with phase doublers (ISL6611A and ISL6617), which can double or quadruple the phase count. For instance, the multi-phase PWM can realize up to 24-phase count system. A higher phase count system can improve thermal distribution and power conversion efficiency at heavy load. Non-Intersil Phase doubler typically does not have current balance and is not compatible with Intersil’s multi-phase controllers.

Precharged Start-up Capability

Since the ISL6398 uses 5V bias and the high efficiency power train mostly uses 5V driver, this makes the ISL6398 digital power system much more robust and reliable for power-up and down as well as precharged start-up, which is typically hardly managed for a system that deals with 3.3V, 5V, and 12V supplies.

Switching Frequency

The VR’s switching frequency is programmable from 120kHz to 2.025MHz via PMBus. It is 15kHz/step with a slew rate of step/20µs.

Current Sensing

The ISL6398 senses current continuously for fast response. The ISL6398 supports inductor DCR sensing, or resistive sensing techniques. The associated channel current sense amplifier uses the ISEN inputs to reproduce a signal proportional to the inductor current, I_L. The sense current, I_{SEN}, is proportional to the inductor current. The sensed current is used for current balance, load-line regulation, and overcurrent protection.

The internal circuitry, shown in Figures 4 and 5, represents one channel of the VR output, respectively. The ISEN± circuitry is repeated for each channel, but may not be active depending on the status of the PWM[6:2] pins, as described in "PWM Operation" on page 17. The input bias current of the current sensing amplifier is typically 25nA; less than 8kΩ input impedance is preferred to minimized the offset error, i.e., a larger C value as needed.

INDUCTOR DCR SENSING

An inductor's winding is characteristic of a distributed resistance, as measured by the Direct Current Resistance (DCR) parameter. Consider the inductor DCR as a separate lumped quantity, as shown in Figure 4. The channel current I_L, flowing through the inductor, will also pass through the DCR. Equation 4 shows the S-domain equivalent voltage across the inductor V_L.

$$V_L(s) = I_L \cdot (s \cdot L + DCR) \quad \text{(EQ. 4)}$$

A simple R-C network across the inductor extracts the DCR voltage, as shown in Figure 4.

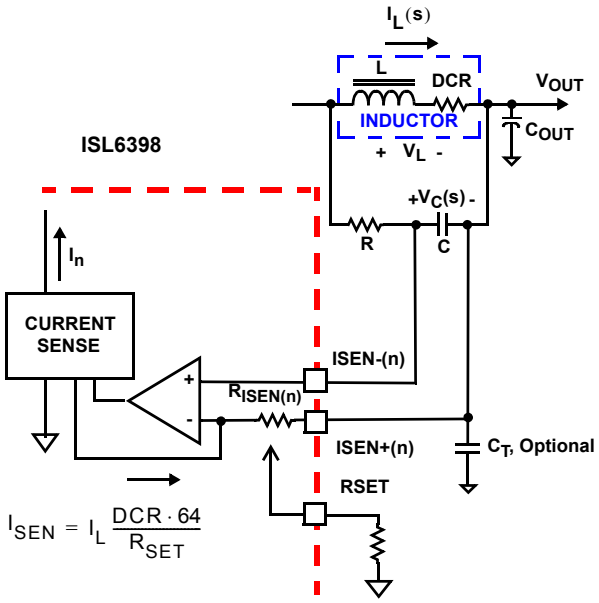


FIGURE 4. DCR SENSING CONFIGURATION

The voltage on the capacitor V_C, can be shown to be proportional to the channel current I_L(see Equation 5).

$$V_C(s) = \frac{\left(s \cdot \frac{L}{DCR} + 1\right) \cdot (DCR \cdot I_L)}{(s \cdot RC + 1)} \quad \text{(EQ. 5)}$$

If the R-C network components are selected such that the RC time constant matches the inductor time constant (R*C = L/DCR), the voltage across the capacitor V_C is equal to the voltage drop across the DCR, i.e., proportional to the channel current.

With the internal low-offset current amplifier, the capacitor voltage V_C is replicated across the sense resistor R_{ISEN}. Therefore, the current out of the ISENS+ pin, I_{SEN}, is proportional to the inductor current.

Equation 6 shows that the ratio of the channel current to the sensed current, I_{SEN}, is driven by the value of the sense resistor and the DCR of the inductor.

$$I_{SEN} = I_L \cdot \frac{DCR}{R_{ISEN}} = I_L \frac{DCR \cdot 64}{R_{SET}} \quad \text{(EQ. 6)}$$

RESISTIVE SENSING

For more accurate current sensing, a dedicated current-sense resistor R_{SENSE} in series with each output inductor can serve as the current sense element (see Figure 5). This technique however reduces overall converter efficiency due to the additional power loss on the current sense element R_{SENSE}.

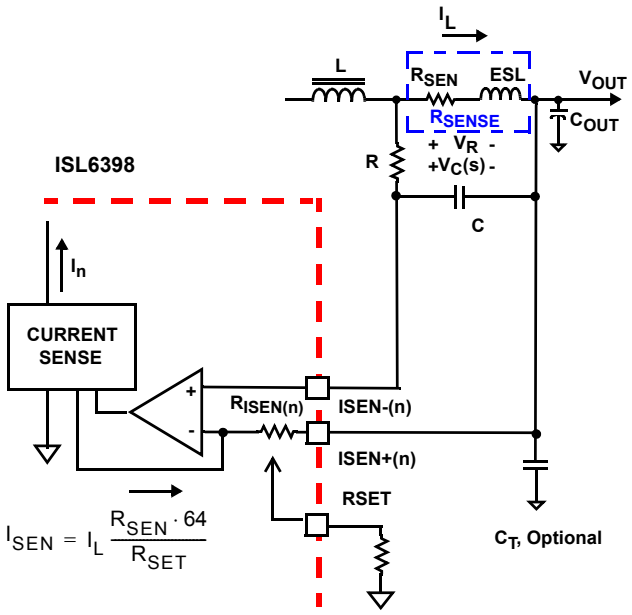


FIGURE 5. SENSE RESISTOR IN SERIES WITH INDUCTORS

A current sensing resistor has a distributed parasitic inductance, known as ESL (equivalent series inductance, typically less than 1nH) parameter. Consider the ESL as a separate lumped quantity, as shown in Figure 5. The channel current I_L, flowing through the inductor, will also pass through the ESL. Equation 7 shows the s-domain equivalent voltage across the resistor V_R.

$$V_R(s) = I_L \cdot (s \cdot ESL + R_{SEN}) \quad \text{(EQ. 7)}$$

A simple R-C network across the current sense resistor extracts the R_{SEN} voltage, as shown in Figure 5.

The voltage on the capacitor V_C, can be shown to be proportional to the channel current I_L (see Equation 8).

$$V_C(s) = \frac{\left(s \cdot \frac{ESL}{R_{SEN}} + 1\right) \cdot (R_{SEN} \cdot I_L)}{(s \cdot RC + 1)} \quad \text{(EQ. 8)}$$

If the R-C network components are selected such that the RC time constant matches the ESL-R_{SEN} time constant ($R*C = ESL/R_{SEN}$), the voltage across the capacitor V_C is equal to the voltage drop across the R_{SEN}, i.e., proportional to the channel current. As an example, a typical 1mΩ sense resistor can use R = 348 and C = 820pF for the matching. Figures 6 and 7 show the sensed waveforms with and without matching RC when using resistive sense.

FIGURE 6. VOLTAGE ACROSS R WITHOUT RC

FIGURE 7. VOLTAGE ACROSS C WITH MATCHING RC

Equation 9 shows that the ratio of the channel current to the sensed current, I_{SEN}, is driven by the value of the sense resistor and the R_{ISEN}.

$$I_{SEN} = I_L \cdot \frac{R_{SEN}}{R_{ISEN}} = I_L \frac{R_{SEN} \cdot 64}{R_{SET}} \quad \text{(EQ. 9)}$$

However, the R_{ISEN} resistor of each channel is integrated, while its value is determined by the R_{SET} resistor. The RSET resistor value can be from 3.84kΩ to 60.4kΩ and is 64x of the required I_{SEN} resistor value. Therefore, the current sense gain resistor (Integrated R_{ISEN}) value can be effectively set at 60Ω to 943Ω.

The inductor DCR value will increase as the temperature increases. Therefore, the sensed current will increase as the temperature of the current sense element increases. In order to compensate the temperature effect on the sensed current signal, a Negative Temperature Coefficient (NTC) resistor can be used for thermal compensation, or the integrated temperature compensation function of the ISL6398 should be utilized. The integrated temperature compensation function is described in “Temperature Compensation” on page 28.

Decoupling capacitor (C_T) on ISEN[6:1]- pins are optional and might be required for long sense traces and a poor layout.

L/DCR OR ESL/R_{SEN} MATCHING

Assuming the compensator design is correct, Figure 8 shows the expected load transient response waveforms if L/DCR or ESL/R_{SEN} is matching the R-C time constant. When the load current I_{OUT} has a square change, the output voltage V_{OUT} also has a square response, except for the overshoot at load release. However, there is always some PCB contact impedance of current sensing components between the two current sensing points; it hardly accounts into the L/DCR or ESL/R_{SEN} matching calculation. Fine tuning the matching is necessarily done in the board level to improve overall transient performance and system reliability.

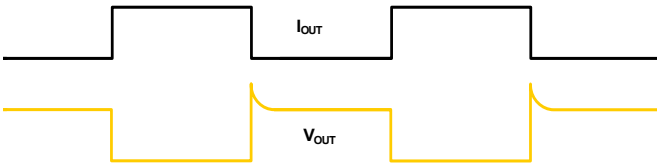


FIGURE 8. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS

If the R-C timing constant is too large or too small, $V_C(s)$ will not accurately represent real-time $I_{OUT}(s)$ and will worsen the transient response. Figure 9 shows the load transient response when the R-C timing constant is too small. V_{OUT} will sag excessively upon load insertion and may create a system failure or early overcurrent trip. Figure 10 shows the transient response when the R-C timing constant is too large. V_{OUT} is sluggish in drooping to its final value. There will be excessive overshoot if load insertion occurs during this time, which may potentially hurt the reliability.

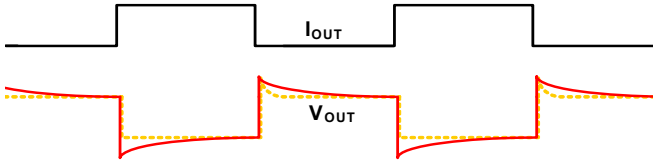


FIGURE 9. LOAD TRANSIENT RESPONSE WHEN R-C TIME CONSTANT IS TOO SMALL

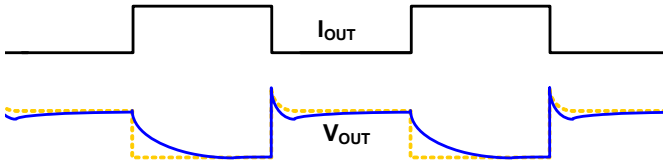


FIGURE 10. LOAD TRANSIENT RESPONSE WHEN R-C TIME CONSTANT IS TOO LARGE

R_{SET} AND L/DCR MATCHING FOR COUPLED INDUCTOR

The current sense circuitry operates in a very similar manner for negative current feedback, where inductor current is flowing from the output of the regulator to the PHASE node, opposite of flow pictured in Figures 4 and 5. However, the range of proper operation with negative current sensing has a limitation. The worst-case peak-to-peak inductor ripple current should be kept less than 80% of the OCP trip point (~80µA). Care should be taken to avoid operation with negative current feedback exceeding this threshold, as this may lead to momentary loss of current balance between phases and disruption of normal circuit operation. Note that the negative current can especially affect coupled inductor designs, where the effective inductance is the leakage between the two channels, much lower than the specified mutual inductance (LM) and self inductance (L). To limit the impact, a higher RSET value (1.5x to 2x) is often used to reduce the effective negative current seen by the controller in coupled inductor designs.

Refer to Intersil’s application note, AN1268 for detailed coupled inductor discussion and ripple current calculation.

As explained in application note, AN1268 the leakage inductance (not self inductance or mutual inductance) of the coupled inductor should be used as the inductance in the time constant calculation. Therefore, the leakage, self, and mutual inductance should be well controlled for a good coupled inductor design.

Channel-current Balance

The sensed current I_n from each active channel is summed together and divided by the number of active channels. The resulting average current I_{AVG} provides a measure of the total load current. Channel current balance is achieved by comparing the sensed current of each channel to the average current to make an appropriate adjustment to the PWM duty cycle of each channel with Intersil's patented current-balance method.

Channel current balance is essential in achieving the thermal advantage of multiphase operation. With good current balance, the power loss is equally dissipated over multiple devices and a greater area. The ISL6398 can adjust the thermal/current balance of the VR via registers F7 to FC.

Voltage Regulation (5mV and 10mV Mode)

The compensation network shown in Figure 11 assures that the steady-state error in the output voltage is limited only to the error in the reference voltage (DAC and OFFSET) and droop current source, remote sense, and error amplifier.

The sensed average current I_{DROOP} is tied to FB internally and will develop a voltage drop across the resistor between FB and V_{OUT} for droop control. This current can be disconnected from the FB node via PMBus for non-droop applications.

The output of the error amplifier, V_{COMP}, is compared to the internal sawtooth waveforms to generate the PWM signals. The PWM signals control the timing of the Intersil MOSFET drivers and regulate the converter output to the specified reference voltage.

For remote sensing, connect the load sensing pins to the non-inverting input, VSEN, and inverting input, RGND, of the error amplifier. This configuration effectively removes the voltage error encountered when measuring the output voltage relative to the local controller ground reference point.

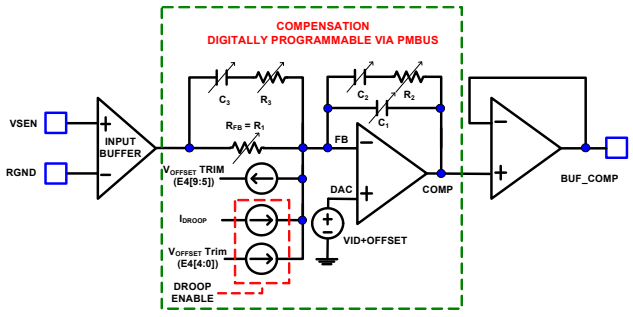


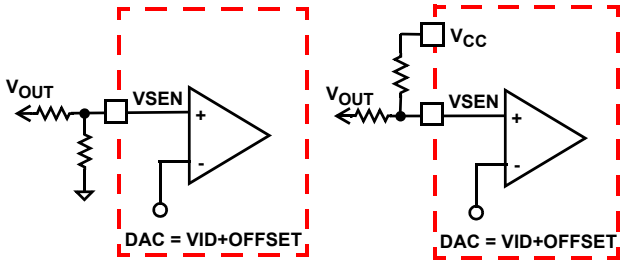
FIGURE 11. OUTPUT VOLTAGE AND LOAD-LINE REGULATION

A digital-to-analog converter (DAC) generates a reference voltage, which is programmable via PMBus bus. The DAC decodes the PMBus set VID command into one of the discrete voltages shown in Table 4. In addition, the output voltage can be margined in ±5mV step between -640mV and 635mV, ±10mV step between -1280mV and 1270mV, as shown in Table 4. For a finer than 5mV or 10mV offset, a large ratio resistor divider can be placed on the VSEN pin between the output and GND for positive offset or V_{CC} for negative offset, as in Figure 12. The VR operational mode is programmed by the "VRSEL_ADDR" pin. Table 3 shows the difference between 5mV and 10mV modes. VOUT_MAX and VBOOT registers must be programmed accordingly to support each mode, otherwise, the VR might NOT power-up correctly.

Furthermore, the PMBus register (E4h[9:5]) can program the additional droop current (range from -4µA to 3.75µA) into R_1 for DC offset calibration; a negative current will yield a negative offset, while a positive current will yield a positive offset: OFFSET = R_1* I(E4[9:5]). In droop applications, E4[4:0] can add current out of IMON pin and droop current through R_1 simultaneously (the negative current yields positive offset, and vice versa).

TABLE 3. 5mV vs 10mV DAC Resolution

MODE (VRSEL)	MAXIMUM DAC (V)	VOUT_MAX (24h)	MAXIMUM VBOOT ("BT" pin)	MAXIMUM VBOOT (E6)
5mV	2.155	Table 18	1.50	1.52
10mV	3.011	Table 4 Follow DAC	3.00	3.04



A. V_{OUT} HIGHER THAN DAC B. V_{OUT} LOWER THAN DAC

FIGURE 12. EXTERNAL PROGRAMMABLE REGULATION

TABLE 4. 5mV OR 10mV VID 8-BIT

BINARY CODE	HEX CODE	5mV VID (V)	10mV VID (V)	5mV OFFSET (mV)	10mV OFFSET (mV)
00000000	0	OFF	OFF	0	0
00000001	1	0.250	0.500	5	10
00000010	2	0.255	0.510	10	20
00000011	3	0.260	0.520	15	30
00000100	4	0.265	0.530	20	40
00000101	5	0.270	0.540	25	50
00000110	6	0.275	0.550	30	60
00000111	7	0.280	0.560	35	70
00001000	8	0.285	0.570	40	80
00001001	9	0.290	0.580	45	90
00001010	A	0.295	0.590	50	100
00001011	B	0.300	0.600	55	110
00001100	C	0.305	0.610	60	120
00001101	D	0.310	0.620	65	130

TABLE 4. 5mV OR 10mV VID 8-BIT (Continued)

BINARY CODE	HEX CODE	5mV VID (V)	10mV VID (V)	5mV OFFSET (mV)	10mV OFFSET (mV)
00001110	E	0.315	0.630	70	140
00001111	F	0.320	0.640	75	150
00010000	10	0.325	0.650	80	160
00010001	11	0.330	0.660	85	170
00010010	12	0.335	0.670	90	180
00010011	13	0.340	0.680	95	190
00010100	14	0.345	0.690	100	200
00010101	15	0.350	0.700	105	210
00010110	16	0.355	0.710	110	220
00010111	17	0.360	0.720	115	230
00011000	18	0.365	0.730	120	240
00011001	19	0.370	0.740	125	250
00011010	1A	0.375	0.750	130	260
00011011	1B	0.380	0.760	135	270
00011100	1C	0.385	0.770	140	280
00011101	1D	0.390	0.780	145	290
00011110	1E	0.395	0.790	150	300
00011111	1F	0.400	0.800	155	310
00100000	20	0.405	0.810	160	320
00100001	21	0.410	0.820	165	330
00100010	22	0.415	0.830	170	340
00100011	23	0.420	0.840	175	350
00100100	24	0.425	0.850	180	360
00100101	25	0.430	0.860	185	370
00100110	26	0.435	0.870	190	380
00100111	27	0.440	0.880	195	390
00101000	28	0.445	0.890	200	400
00101001	29	0.450	0.900	205	410
00101010	2A	0.455	0.910	210	420
00101011	2B	0.460	0.920	215	430
00101100	2C	0.465	0.930	220	440
00101101	2D	0.470	0.940	225	450
00101110	2E	0.475	0.950	230	460
00101111	2F	0.480	0.960	235	470
00110000	30	0.485	0.970	240	480
00110001	31	0.490	0.980	245	490
00110010	32	0.495	0.990	250	500
00110011	33	0.500	1.000	255	510
00110100	34	0.505	1.010	260	520
00110101	35	0.510	1.020	265	530
00110110	36	0.515	1.030	270	540
00110111	37	0.520	1.040	275	550
00111000	38	0.525	1.050	280	560
00111001	39	0.530	1.060	285	570
00111010	3A	0.535	1.070	290	580

TABLE 4. 5mV OR 10mV VID 8-BIT (Continued)

BINARY CODE	HEX CODE	5mV VID (V)	10mV VID (V)	5mV OFFSET (mV)	10mV OFFSET (mV)
00111011	3B	0.540	1.080	295	590
00111100	3C	0.545	1.090	300	600
00111101	3D	0.550	1.100	305	610
00111110	3E	0.555	1.110	310	620
00111111	3F	0.560	1.120	315	630
01000000	40	0.565	1.130	320	640
01000001	41	0.570	1.140	325	650
01000010	42	0.575	1.150	330	660
01000011	43	0.580	1.160	335	670
01000100	44	0.585	1.170	340	680
01000101	45	0.590	1.180	345	690
01000110	46	0.595	1.190	350	700
01000111	47	0.600	1.200	355	710
01001000	48	0.605	1.210	360	720
01001001	49	0.610	1.220	365	730
01001010	4A	0.615	1.230	370	740
01001011	4B	0.620	1.240	375	750
01001100	4C	0.625	1.250	380	760
01001101	4D	0.630	1.260	385	770
01001110	4E	0.635	1.270	390	780
01001111	4F	0.640	1.280	395	790
01010000	50	0.645	1.290	400	800
01010001	51	0.650	1.300	405	810
01010010	52	0.655	1.310	410	820
01010011	53	0.660	1.320	415	830
01010100	54	0.665	1.330	420	840
01010101	55	0.670	1.340	425	850
01010110	56	0.675	1.350	430	860
01010111	57	0.680	1.360	435	870
01011000	58	0.685	1.370	440	880
01011001	59	0.690	1.380	445	890
01011010	5A	0.695	1.390	450	900
01011011	5B	0.700	1.400	455	910
01011100	5C	0.705	1.410	460	920
01011101	5D	0.710	1.420	465	930
01011110	5E	0.715	1.430	470	940
01011111	5F	0.720	1.440	475	950
01100000	60	0.725	1.450	480	960
01100001	61	0.730	1.460	485	970
01100010	62	0.735	1.470	490	980
01100011	63	0.740	1.480	495	990
01100100	64	0.745	1.490	500	1000
01100101	65	0.750	1.500	505	1010
01100110	66	0.755	1.510	510	1020
01100111	67	0.760	1.520	515	1030

TABLE 4. 5mV OR 10mV VID 8-BIT (Continued)

BINARY CODE	HEX CODE	5mV VID (V)	10mV VID (V)	5mV OFFSET (mV)	10mV OFFSET (mV)
01101000	68	0.765	1.530	520	1040
01101001	69	0.770	1.540	525	1050
01101010	6A	0.775	1.550	530	1060
01101011	6B	0.780	1.560	535	1070
01101100	6C	0.785	1.570	540	1080
01101101	6D	0.790	1.580	545	1090
01101110	6E	0.795	1.590	550	1100
01101111	6F	0.800	1.600	555	1110
01110000	70	0.805	1.610	560	1120
01110001	71	0.810	1.620	565	1130
01110010	72	0.815	1.630	570	1140
01110011	73	0.820	1.640	575	1150
01110100	74	0.825	1.650	580	1160
01110101	75	0.830	1.660	585	1170
01110110	76	0.835	1.670	590	1180
01110111	77	0.840	1.680	595	1190
01111000	78	0.845	1.690	600	1200
01111001	79	0.850	1.700	605	1210
01111010	7A	0.855	1.710	610	1220
01111011	7B	0.860	1.720	615	1230
01111100	7C	0.865	1.730	620	1240
01111101	7D	0.870	1.740	625	1250
01111110	7E	0.875	1.750	630	1260
01111111	7F	0.880	1.760	635	1270
10000000	80	0.885	1.770	-640	-1280
10000001	81	0.890	1.780	-635	-1270
10000010	82	0.895	1.790	-630	-1260
10000011	83	0.900	1.800	-625	-1250
10000100	84	0.905	1.810	-620	-1240
10000101	85	0.910	1.820	-615	-1230
10000110	86	0.915	1.830	-610	-1220
10000111	87	0.920	1.840	-605	-1210
10001000	88	0.925	1.850	-600	-1200
10001001	89	0.930	1.860	-595	-1190
10001010	8A	0.935	1.870	-590	-1180
10001011	8B	0.940	1.880	-585	-1170
10001100	8C	0.945	1.890	-580	-1160
10001101	8D	0.950	1.900	-575	-1150
10001110	8E	0.955	1.910	-570	-1140
10001111	8F	0.960	1.920	-565	-1130
10010000	90	0.965	1.930	-560	-1120
10010001	91	0.970	1.940	-555	-1110
10010010	92	0.975	1.950	-550	-1100
10010011	93	0.980	1.960	-545	-1090
10010100	94	0.985	1.970	-540	-1080

TABLE 4. 5mV OR 10mV VID 8-BIT (Continued)

BINARY CODE	HEX CODE	5mV VID (V)	10mV VID (V)	5mV OFFSET (mV)	10mV OFFSET (mV)
10010101	95	0.990	1.980	-535	-1070
10010110	96	0.995	1.990	-530	-1060
10010111	97	1.000	2.000	-525	-1050
10011000	98	1.005	2.010	-520	-1040
10011001	99	1.010	2.020	-515	-1030
10011010	9A	1.015	2.030	-510	-1020
10011011	9B	1.020	2.040	-505	-1010
10011100	9C	1.025	2.050	-500	-1000
10011101	9D	1.030	2.060	-495	-990
10011110	9E	1.035	2.070	-490	-980
10011111	9F	1.040	2.080	-485	-970
10100000	A0	1.045	2.090	-480	-960
10100001	A1	1.050	2.100	-475	-950
10100010	A2	1.055	2.110	-470	-940
10100011	A3	1.060	2.120	-465	-930
10100100	A4	1.065	2.130	-460	-920
10100101	A5	1.070	2.140	-455	-910
10100110	A6	1.075	2.150	-450	-900
10100111	A7	1.080	2.160	-445	-890
10101000	A8	1.085	2.170	-440	-880
10101001	A9	1.090	2.180	-435	-870
10101010	AA	1.095	2.190	-430	-860
10101011	AB	1.100	2.200	-425	-850
10101100	AC	1.105	2.210	-420	-840
10101101	AD	1.110	2.220	-415	-830
10101110	AE	1.115	2.230	-410	-820
10101111	AF	1.120	2.240	-405	-810
10110000	B0	1.125	2.250	-400	-800
10110001	B1	1.130	2.260	-395	-790
10110010	B2	1.135	2.270	-390	-780
10110011	B3	1.140	2.280	-385	-770
10110100	B4	1.145	2.290	-380	-760
10110101	B5	1.150	2.300	-375	-750
10110110	B6	1.155	2.310	-370	-740
10110111	B7	1.160	2.320	-365	-730
10111000	B8	1.165	2.330	-360	-720
10111001	B9	1.170	2.340	-355	-710
10111010	BA	1.175	2.350	-350	-700
10111011	BB	1.180	2.360	-345	-690
10111100	BC	1.185	2.370	-340	-680
10111101	BD	1.190	2.380	-335	-670
10111110	BE	1.195	2.390	-330	-660
10111111	BF	1.200	2.400	-325	-650
11000000	C0	1.205	2.410	-320	-640
11000001	C1	1.210	2.420	-315	-630

TABLE 4. 5mV OR 10mV VID 8-BIT (Continued)

BINARY CODE	HEX CODE	5mV VID (V)	10mV VID (V)	5mV OFFSET (mV)	10mV OFFSET (mV)
11000010	C2	1.215	2.430	-310	-620
11000011	C3	1.220	2.440	-305	-610
11000100	C4	1.225	2.450	-300	-600
11000101	C5	1.230	2.460	-295	-590
11000110	C6	1.235	2.470	-290	-580
11000111	C7	1.240	2.480	-285	-570
11001000	C8	1.245	2.490	-280	-560
11001001	C9	1.250	2.500	-275	-550
11001010	CA	1.255	2.510	-270	-540
11001011	CB	1.260	2.520	-265	-530
11001100	CC	1.265	2.530	-260	-520
11001101	CD	1.270	2.540	-255	-510
11001110	CE	1.275	2.550	-250	-500
11001111	CF	1.280	2.560	-245	-490
11010000	D0	1.285	2.570	-240	-480
11010001	D1	1.290	2.580	-235	-470
11010010	D2	1.295	2.590	-230	-460
11010011	D3	1.300	2.600	-225	-450
11010100	D4	1.305	2.610	-220	-440
11010101	D5	1.310	2.620	-215	-430
11010110	D6	1.315	2.630	-210	-420
11010111	D7	1.320	2.640	-205	-410
11011000	D8	1.325	2.650	-200	-400
11011001	D9	1.330	2.660	-195	-390
11011010	DA	1.335	2.670	-190	-380
11011011	DB	1.340	2.680	-185	-370
11011100	DC	1.345	2.690	-180	-360
11011101	DD	1.350	2.700	-175	-350
11011110	DE	1.355	2.710	-170	-340
11011111	DF	1.360	2.720	-165	-330
11100000	E0	1.365	2.730	-160	-320
11100001	E1	1.370	2.740	-155	-310
11100010	E2	1.375	2.750	-150	-300
11100011	E3	1.380	2.760	-145	-290
11100100	E4	1.385	2.770	-140	-280
11100101	E5	1.390	2.780	-135	-270
11100110	E6	1.395	2.790	-130	-260
11100111	E7	1.400	2.800	-125	-250
11101000	E8	1.405	2.810	-120	-240
11101001	E9	1.410	2.820	-115	-230
11101010	EA	1.415	2.830	-110	-220
11101011	EB	1.420	2.840	-105	-210
11101100	EC	1.425	2.850	-100	-200
11101101	ED	1.430	2.860	-95	-190

TABLE 4. 5mV OR 10mV VID 8-BIT (Continued)

BINARY CODE	HEX CODE	5mV VID (V)	10mV VID (V)	5mV OFFSET (mV)	10mV OFFSET (mV)
11101110	EE	1.435	2.870	-90	-180
11101111	EF	1.440	2.880	-85	-170
11110000	F0	1.445	2.890	-80	-160
11110001	F1	1.450	2.900	-75	-150
11110010	F2	1.455	2.910	-70	-140
11110011	F3	1.460	2.920	-65	-130
11110100	F4	1.465	2.930	-60	-120
11110101	F5	1.470	2.940	-55	-110
11110110	F6	1.475	2.950	-50	-100
11110111	F7	1.480	2.960	-45	-90
11111000	F8	1.485	2.970	-40	-80
11111001	F9	1.490	2.980	-35	-70
11111010	FA	1.495	2.990	-30	-60
11111011	FB	1.500	3.000	-25	-50
11111100	FC	1.505	3.010	-20	-40
11111101	FD	1.510	3.020	-15	-30
11111110	FE	1.515	3.030	-10	-20
11111111	FF	1.520	3.040	-5	-10

Load-line Regulation

Some applications require a precisely controlled output resistance. This dependence of output voltage on load current is often termed “droop” or “load-line” regulation. By adding a well controlled output impedance, the output voltage can effectively be level shifted in a direction, which works to achieve the load-line regulation required by these manufacturers.

In other cases, the designer may determine that a more cost-effective solution can be achieved by adding droop. Droop can help to reduce the output-voltage spike that results from fast load-current demand changes.

The magnitude of the spike is dictated by the ESR and ESL of the output capacitors selected. By positioning the no-load voltage level near the upper specification limit, a larger negative spike can be sustained without crossing the lower limit. By adding a well controlled output impedance, the output voltage under load can effectively be level shifted down so that a larger positive spike can be sustained without crossing the upper specification limit.

As shown in Figure 11, a current proportional to the average current of all active channels, I_{AVG}, flows from FB through a load-line regulation resistor R_{FB}, i.e., R_1. The resulting voltage drop across R_{FB} is proportional to the output current, effectively creating an output voltage droop with a steady-state value defined, as shown in Equation 10:

$$V_{DROOP} = I_{AVG} \cdot R_{FB} \quad \text{(EQ. 10)}$$

The regulated output voltage is reduced by the droop voltage V_{DROOP}. The output voltage as a function of load current is derived by combining Equation 10 with the appropriate sample current expression defined by the current sense method employed, as shown in Equation 11:

$$V_{OUT} = V_{REF} - \left(\frac{I_{LOAD}}{N}\frac{R_X}{R_{ISEN}}R_{FB}\right) \quad \text{(EQ. 11)}$$

where V_{REF} is the reference voltage (DAC), I_{LOAD} is the total output current of the converter, R_{ISEN} is the sense resistor connected to the ISEN+ pin, and R_{FB} is the feedback resistor, N is the active channel number, and R_X is the DCR, or R_{SENSE} depending on the sensing method.

Therefore, the equivalent loadline impedance, i.e. Droop impedance, is equal to Equation 12:

$$R_{LL} = \frac{R_{FB}}{N}\frac{R_X}{R_{ISEN}} \quad \text{(EQ. 12)}$$

The major regulation error comes from the current sensing elements. To improve load-line regulation accuracy, a tight DCR tolerance of inductor or a precision sensing resistor should be considered.

In addition, the overall load-line can be programmed to fit the application needed by the PMBus registers: B0h[7:0] for Load-Line and E4h[9:5] for DC offset. Curve 3 shown in Figure 13, makes a steeper load line than the target to fully utilize the total tolerance band, reduce the output capacitor count and cost.

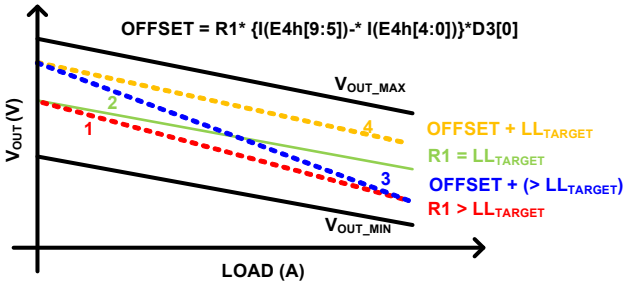


FIGURE 13. PROGRAMMABLE LOAD-LINE REGULATION

Dynamic VID

Some applications need to make changes to their voltage as part of normal operation. They direct the core-voltage regulator to do this by making changes to the VID during regulator operation. The power management solution is required to monitor the DAC and respond to on-the-fly VID changes in a controlled manner. Supervising the safe output voltage transition within the DAC range of the load without discontinuity or disruption is a necessary function of the voltage regulator.

Sixteen different slew rates can be selected for soft-start and during Dynamic VID (DVID) transition for VR.

TABLE 5. SLEW RATE OPTIONS

DVID F6h[4:0]	DVID SLEW RATE (MINIMUM RATE) (mV/µs)	DVID F6h[4:0]	DVID SLEW RATE (MINIMUM RATE) (mV/µs)
0h	0.315	8h	4.0
1h	0.625	9h	4.44
2h	1.25	Ah	5.0
3h	2.5	Bh	5.6
4h	2.85	Ch	6.66
5h	3.07	Dh	8.0
6h	3.33	Eh	10
7h	3.63	Fh	13.25

During dynamic VID transition and VID step up, the overcurrent trip point increases by 140% to avoid falsely triggering OCP circuits, while the overvoltage trip point will follow the DAC+OVP level, programmable via PMBus (D8h[2:0]).

Operation Initialization

Prior to converter initialization, proper conditions must exist on the enable inputs and V_{CC}. When the conditions are met, the controller begins soft-start. Once the output voltage is within the proper window of operation, VR_RDY asserts logic high.

Enable and Disable

While in shutdown mode, the PWM outputs are held in a high-impedance state (or pulled to 40% of V_{CC}) to assure the drivers remain off. The following input conditions must be met before the ISL6398 is released from shutdown mode.

1. The bias voltage applied at V_{CC} must reach the internal power-on reset (POR) rising threshold. Once this threshold is reached, proper operation of all aspects of the ISL6398 is guaranteed. Hysteresis between the rising and falling thresholds assure that once enabled, ISL6398 will not inadvertently turn off unless the bias voltage drops substantially (see “Electrical Specifications” on page 10).
2. The ISL6398 features an enable input (EN_PWR_CFP) for power sequencing between the controller bias voltage and another voltage rail. The enable comparator holds the ISL6398 in shutdown until the voltage at EN_PWR_CFP rises above 0.85V. The enable comparator has about 100mV of hysteresis to prevent bounce. It is important that the drivers reach their POR level before the ISL6398 becomes enabled. The schematic in Figure 14 demonstrates sequencing the ISL6398 with ISL99140 DrMOS and the ISL66xx family of Intersil MOSFET drivers.
3. The voltage on TM_EN_OTP must be higher than 1.08V (typically) to enable the controller. This pin is typically connected to the output of VTT VR. However, since the TM_EN_OTP pin is also used for thermal monitoring, it will assert SM_PMALERT# pin low due to thermal alert prior to start-up, therefore, it needs to use CLEAR_FAULT (03h) command to clear the SM_PMALERT# pin and STATUS_BYTE (78h) after power-up. There is no effect on normal operation if SM_PMALERT# and STATUS_BYTE are not used.

When all conditions previously mentioned are satisfied, the ISL6398 begins the soft-start and ramps the output voltage to the Boot Voltage set by hard-wired “BT” registers. After remaining at the boot voltage for some time, the ISL6398 reads the VID code. If the VID code is valid, ISL6398 will regulate the output to the final VID setting. If the VID code is “OFF” code, ISL6398 will remain shut down.

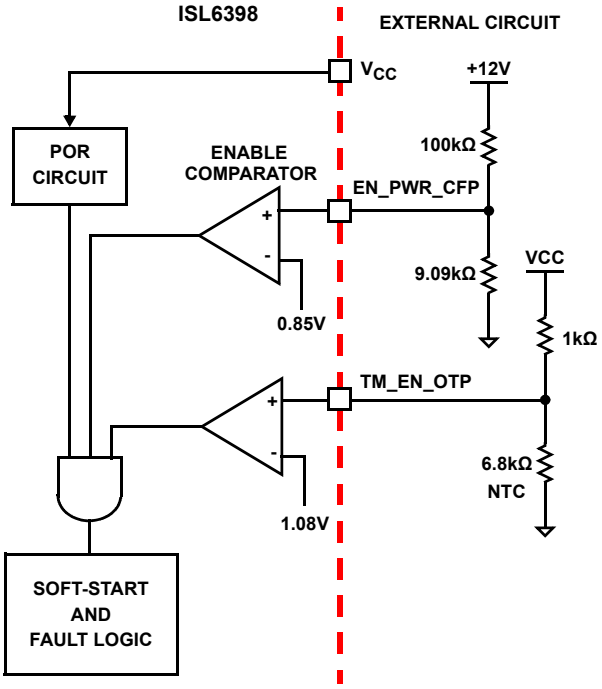


FIGURE 14. POWER SEQUENCING USING THRESHOLD-SENSITIVE ENABLE (EN) FUNCTION

Soft-start

The ISL6398 based VR has 4 periods during soft-start, as shown in Figure 15. After V_{CC}, TM_EN_OTP and EN_PWR_CFP reach their POR/enable thresholds and the NVM_BANK loading time (typically 16ms, and worst case 20ms) expired, the controller will have a fixed delay period t_{D1}. After this delay period, the VR will begin first soft-start ramp until the output voltage reaches the V_{BOOT} voltage at a fixed slew rate, as in Table 5. Then, the controller will regulate the VR voltage at V_{BOOT} for another period t_{D3} until PMBus sends a new VID command. If the VID code is valid, ISL6398 will initiate the second soft-start ramp at a slew rate, set by DVID command in Table 5, until the voltage reaches the new VID voltage. The soft-start time is the sum of the 4 periods, as shown in Equation 13.

$$t_{SS} = t_{D1} + t_{D2} + t_{D3} + t_{D4} \quad \text{(EQ. 13)}$$

t_{D1} is a fixed delay with the typical value as 20µs. t_{D3} is determined by the time to obtain a new valid VID voltage from PMBus. If the VID is valid before the output reaches the boot voltage, the output will turn around to respond to the new VID code.

During t_{D2} and t_{D4}, the ISL6398 digitally controls the DAC voltage change at 5mV per step. The soft-start ramp time t_{D2} and t_{D4} can be calculated based on Equations 14 and 15:

$$t_{D2} = \frac{V_{BOOT}}{DVIDRATE}(\mu s) \quad \text{(EQ. 14)}$$

$$t_{D4} = \frac{V_{VID} - V_{BOOT}}{DVID\ RATE}(\mu s) \quad \text{(EQ. 15)}$$

For example, when the V_{BOOT} is set at 1.1V and DVID slew rate is set at 5mV/µs, the first soft-start ramp time t_{D2} will be around 220µs and the second soft-start ramp time t_{D4} will be at maximum of 80µs if an SET_VID command for 1.5V is received after t_{D3}.

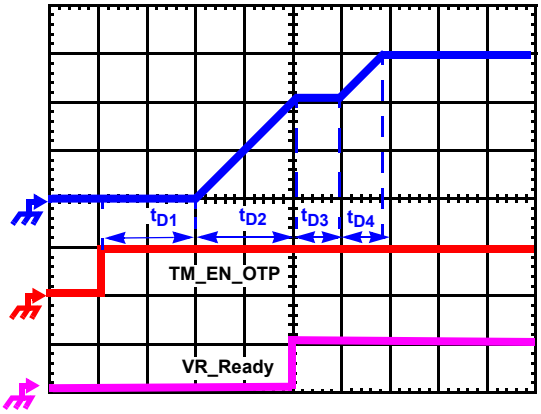


FIGURE 15. SOFT-START WAVEFORMS

Current Sense Output

The current flowing out of the IMON pin is equal to the sensed average current inside the ISL6398. In typical applications, a resistor is placed from the IMON pin to GND to generate a voltage, which is proportional to the load current and the resistor value, as shown in Equation 16:

$$V_{IMON} = \frac{R_{IMON}}{N}\frac{R_X}{R_{ISEN}}I_{LOAD} \quad \text{(EQ. 16)}$$

where V_{IMON} is the voltage at the IMON pin, R_{IMON} is the resistor between the IMON pin and GND, I_{LOAD} is the total output current of the converter, R_{ISEN} is the sense resistor connected to the ISEN+ pin, N is the active channel number, and R_X is the DC resistance of the current sense element, either the DCR of the inductor or R_{SENSE} depending on the sensing method.

The resistor from the IMON pin to GND should be chosen to ensure that the voltage at the IMON pin is typically 2.5V at the maximum load current, typically corresponding to the I_{CCMAX} register. The IMON voltage is linearly digitized every 88µs and stored in the READ_IOUT register (8Ch). When the IMON voltage reaches 2.5V or higher, the digitized I_{OUT} will reach the maximum value of ICCMAX and the SM_PMALERT# pin is pulled low.

$$R_{IMON} = \frac{2.5V\,R_{ISEN}}{R_X}\frac{N}{I_{CC\_MAX\_21h}} \quad \text{(EQ. 17)}$$

A small capacitor can be placed between the IMON pin and GND to reduce the noise impact and provide averaging. If this pin is not used, tie it to GND.