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Buck-Boost Narrow VDC Battery Charger with SMBus Interface and USB OTG

ISL9237

The ISL9237 is a buck-boost Narrow Output Voltage DC (NVDC) charger utilizing Intersil's advanced R3™ Technology to provide high light-load efficiency, fast transient response and seamless DCM/CCM transitions for a variety of mobile and industrial applications.

In Charge mode, the ISL9237 takes input power from a wide range of DC power sources (conventional AC/DC charger adapters, USB PD ports, travel adapters, etc.) and safely charges battery packs with up to 3 cells in a series configuration.

ISL9237 supports On-the-Go (OTG) function for 2- and 3-cell battery applications. When OTG function is enabled, the ISL9237 operates in the reverse Buck mode to provide 5V at the USB port.

As a NVDC topology charger, it also regulates the system output to a narrow DC range for stable system bus voltage. The system power can be provided from the adapter, battery or a combination of both. The ISL9237 can operate with only a battery, only an adapter or both connected. For Intel IMVP8 compliant systems, the ISL9237 includes PSYS functionality, which provides an analog signal representing total platform power. The PSYS output will connect to a wide range of Intersil IMVP8 core regulators to provide an IMVP8 compliant power domain function.

The ISL9237 has serial communication via SMBus/I^2C that allows programming of many critical parameters to deliver a customized solution. These programming parameters include, but are not limited to: Adapter current limit, charger current limit, system voltage setting and trickle charging current limit.

Features

- Buck-boost NVDC charger for 1-, 2- or 3-cell Li-ion batteries
- Input voltage range 3.2V to 23.4V (no dead zone)
- System output voltage 2.4V to 13.824V
- System power monitor PSYS output, IMVP-8 compliant
- Up to 1MHz switching frequency
- LDO output for charger VDD
- Adapter current monitor (AMON)
- Battery discharging current monitor (BMON)
- PROCHOT# open-drain output, IMVP-8 compliant
- Allows trickle charging of depleted battery
- Optional ASGATE FET control
- Ideal diode control in Turbo mode
- Supports OTG function for 2- and 3-cell batteries
- SMBus and auto-increment I^2C compatible
- Two-level adapter current limit available
- Pb-free (RoHS compliant)
- Package 4x4 32 Ld QFN

Applications

- Mobile devices with rechargeable batteries
- Industrial devices with rechargeable batteries

Related Literature

- UG075, "ISL9237EVAL2Z Evaluation Board User Guide"

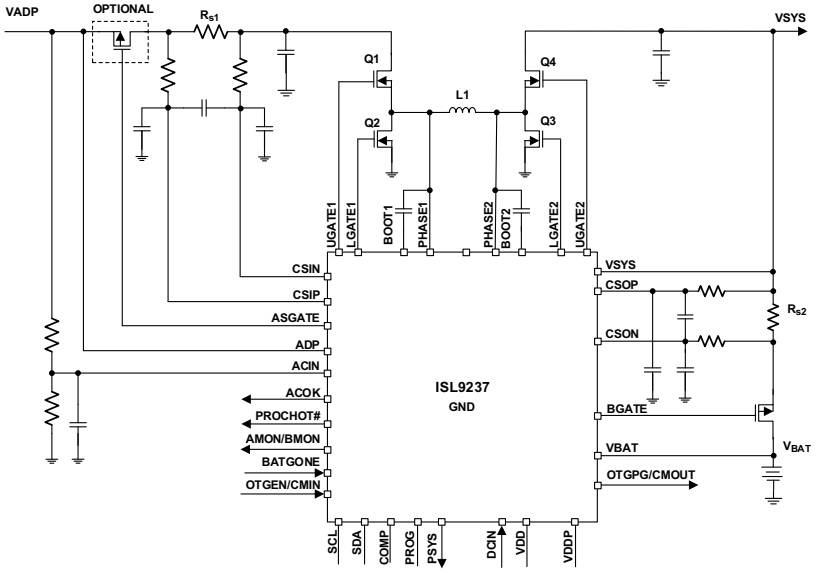

FIGURE 1. TYPICAL APPLICATION CIRCUIT

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Ordering Information

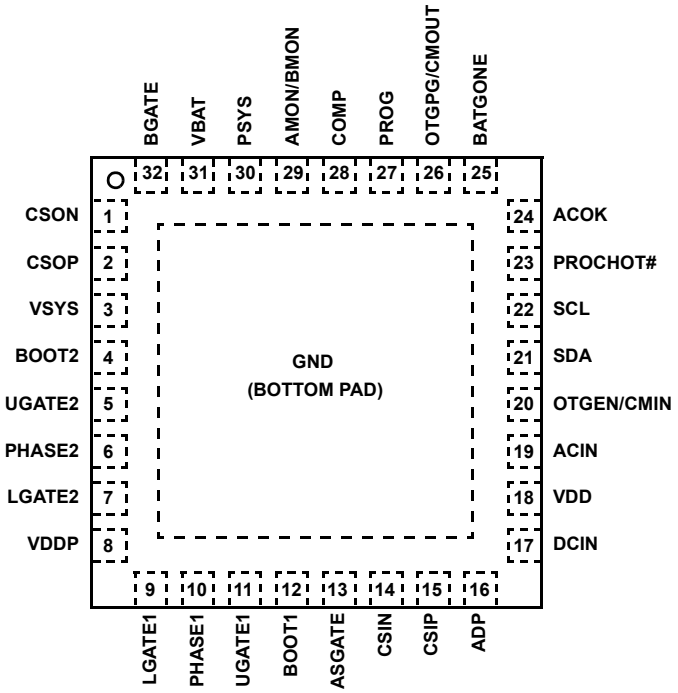
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL9237HRZ	923 7HRZ	-10 to +100	32 Ld 4x4 QFN	L32.4x4A
ISL9237EVAL2Z	Evaluation Board			

NOTES:

1. Add “-T” suffix for 6k unit, “-TK” suffix for 1k unit, or “-T7A” suffix for 250 unit Tape and Reel options. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for ISL9237. For more information on MSL, please see tech brief TB363.

Pin Configuration

ISL9237
(32 LD 4x4 QFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
BOTTOM PAD	GND	Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pin. It should also be used as the thermal pad for heat dissipation.
1	CSON	Battery current sense “–” input. Connect to battery current resistor negative input. Place a 0.1µF ceramic capacitor between CSOP to CSON to provide differential mode filtering.
2	CSOP	Battery current sense “+” input. Connect to battery current resistor positive input. Place a 0.1µF ceramic capacitor between CSOP to CSON to provide differential mode filtering.
3	VSYS	Provides feedback voltage for MaxSystemVoltage regulation.

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	DESCRIPTION
4	BOOT2	High-side MOSFET Q4 gate driver supply. Connect an MLCC capacitor across the BOOT2 pin and the PHASE2 pin. The boot capacitor is charged through an internal boot diode connected from the VDDP pin to the BOOT2 pin when the PHASE2 pin drops below VDDP minus the voltage drop across the internal boot diode.
5	UGATE2	High-side MOSFET Q4 gate drive.
6	PHASE2	Current return path for the high-side MOSFET Q4 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q4 source, the low-side MOSFET Q3 drain and the one terminal of the inductor.
7	LGATE2	Low-side MOSFET Q3 gate drive.
8	VDDP	Power supply for the gate drivers. Connect to VDD pin through a 4.7Ω resistor and connect a 1µF ceramic capacitor to GND.
9	LGATE1	Low-side MOSFET Q2 gate drive.
10	PHASE1	Current return path for the high side MOSFET Q1 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q1 source, the low-side MOSFET Q2 drain and the input terminal of the inductor.
11	UGATE1	High-side MOSFET Q1 gate drive.
12	BOOT1	High-side MOSFET Q1 gate driver supply. Connect an MLCC capacitor across the BOOT1 pin and the PHASE1 pin. The boot capacitor is charged through an internal boot diode connected from the VDDP pin to the BOOT1 pin when the PHASE1 pin drops below VDDP minus the voltage drop across the internal boot diode.
13	ASGATE	Gate drive output to the P-channel adapter FET. The use of ASGATE FETs is optional, if not used, leave ASGATE pin floating. When ASGATE turns on, it is clamped 10V below ADP pin voltage.
14	CSIN	Adapter current sense “-” input.
15	CSIP	Adapter current sense “+” input. The modulator also uses this for sensing input voltage in forward mode and output voltage in reverse mode.
16	ADP	Adapter input. Used to sense adapter voltage. When adapter voltage is higher than 3.2V, AGATE is turned on. ADP pin is also one of the two internal low power LDO inputs.
17	DCIN	Input of an internal LDO; provides power to the IC. Connect a diode OR from adapter and system outputs. Bypass this pin with an MLCC capacitor.
18	VDD	Output of the internal LDO; provides the bias power for the internal analog and digital circuit. Connect a 1µF ceramic capacitor to GND. If VDD is pulled below 2V for more than 1ms, ISL9237 will reset all the SMBus register values to the default.
19	ACIN	Adapter voltage sense. Use a resistor divider externally to detect adapter voltage. The adapter voltage is valid if the ACIN pin voltage is greater than 0.8V.
20	OTGEN/ CMIN	OTG function enable pin or stand-alone comparator input pin. Pull high to enable OTG function. The OTG function is enabled when the control register is written to select OTG mode and when the battery voltage is above 5.8V. When OTG function is not selected, this pin is the general purpose stand-alone comparator input.
21	SDA	SMBus data I/O. Connect to the data line from the host controller or smart battery. Connect a 10k pull-up resistor according to SMBus specification.
22	SCL	SMBus clock I/O. Connect to the clock line from the host controller or smart battery. Connect a 10k pull-up resistor according to SMBus specification.
23	PROCHOT#	Open-drain output. Pulled low when ACProchot#, DCProchot# or Low_VSYS event is detected. IMVP-8 compliant.
24	ACOK	Adapter presence indicator output to indicate the adapter is ready.
25	BATGONE	Input pin to the IC. Logic high on this pin indicates the battery has been removed. Logic low on this pin indicates the battery is present. BATGONE pin logic high will force BGATE FET to turn off in any circumstance.
26	OTGPG/ CMOUT	Open-drain output. OTG function output power-good indicator or the stand-alone comparator output. When OTG function is enabled, low if OTG output voltage is not within regulation window. When OTG function is not used, it is the general purpose comparator output.

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	DESCRIPTION
27	PROG	A resistor from PROG pin to GND sets the following configurations: 1. Default number of the battery cells in series, 1-, 2- or 3-cell. 2. Default switching frequency 733kHz or 1MHz. 3. Default adapter current limit value 0.476A or 1.5A. Refer to Table 18 for programming options.
28	COMP	Error amplifier output. Connect a compensation network externally from COMP to GND.
29	AMON/ BMON	Adapter current monitor output or battery discharging current monitor output. V_{AMON} = 18 x (V_{CSIP} - V_{CSIN}); V_{BMON} = 18 x (V_{CSON} - V_{CSOP})
30	PSYS	Current source output that indicates the whole platform power consumption.
31	VBAT	Battery voltage sensing. Used for trickle charging detection and ideal diode mode control. The VBAT pin is also one of the two internal low power LDO inputs.
32	BGATE	Gate drive output to the P-channel FET connecting the system and the battery. This pin can go high to disconnect the battery, low to connect the battery or operate in a linear mode to regulate trickle charge current during trickle charge. ISL9237 pulls down BGATE to GND to turn on BGATE PFET. Therefore, BGATE PFET gate-to-source voltage rating should be higher than the battery voltage.

Simplified Application Circuit

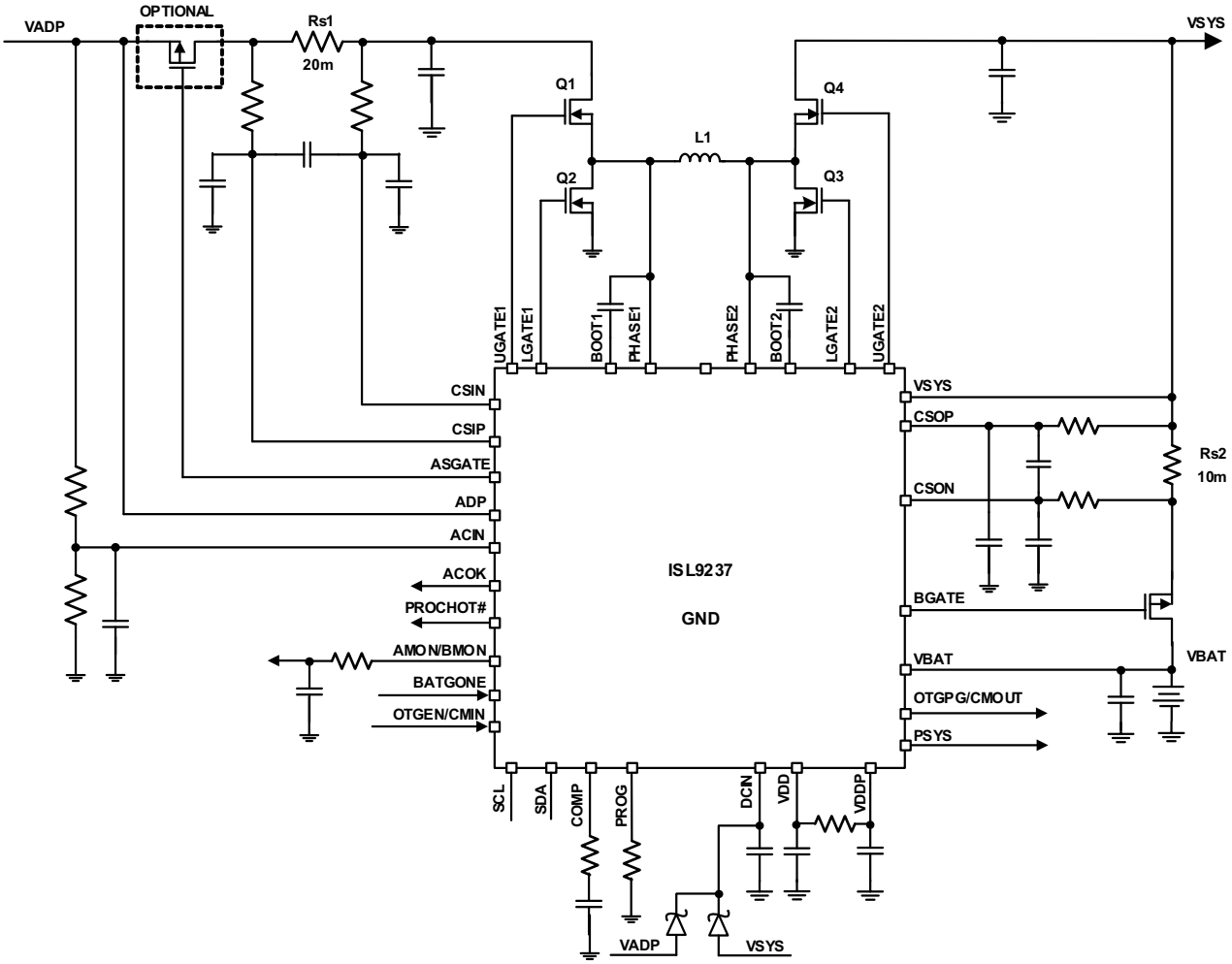


FIGURE 2. SIMPLIFIED APPLICATION DIAGRAM

Absolute Maximum Ratings

CSIP, CSIN, DCIN, ADP, ASGATE . . . . . -0.3V to +28V
PHASE1 . . . . . (GND - 0.3V) to +28V
PHASE1 . . . . . GND-2V(<20ns) to +28V
BOOT1, UGATE1 . . . . . (GND - 0.3V) to +33V
PHASE2 . . . . . (GND - 0.3V) to +15V
PHASE2 . . . . . GND - 2V(<20ns) to +15V
BOOT2, UGATE2 . . . . . (GND - 0.3V) to +20V
LGATE1, LGATE2 . . . . . (GND - 0.3V) to +6.5V
LGATE1, LGATE2 . . . . . GND - 2V(<20ns) to +6.5V
VBAT, VSYS, CSOP, CSON, BGATE . . . . . -0.3V to +15V
VDD, VDDP. . . . . -0.3V to +6.5V
COMP . . . . . -0.3V to +6.5V
AMON/BMON, PSYS. . . . . -0.3V to +6.5V
OTGEN, BATGONE . . . . . -0.3V to +6.5V
ACIN, ACOK, PROCHOT#, OTGPG . . . . . -0.3V to +6.5V
CLK, DAT . . . . . -0.3V to +6.5V
BOOT1-PHASE1, BOOT2-PHASE2. . . . . -0.3V to +6.5V
CSIP-CSIN, CSOP-CSON . . . . . -0.5V to +0.5V
VDD. 70mA
ACIN, SDA, SCL, DCIN, ACOK. 2mA
ESD Rating
  Human Body Model (Tested per JESD22-A114E). 2kV
  Machine Model (Tested per JESD22-A115-A). 200V
  Charged Device Model (Tested per JESD22-C101A) 1kV
Latch-Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld QFN Package (Notes 4, 5)	38	3.5

Ambient Temperature Range (T_A) . . . . . -10°C to +100°C
Junction Temperature Range (T_J) . . . . . -10°C to +150°C
Storage Temperature Range (T_S) . . . . . -65°C to +175°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature . . . . . -10°C to +100°C
Junction Temperature . . . . . -10°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the ceramic on the package underside.

Electrical Specifications

Operating conditions: ADP = CSIP = CSIN = 5V and 20V, VSYS = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
UVLO/ACOK						
VADP UVLO Rising (Note 7)	VADP_UVLO_r		**3.1**	3.2	**3.4**	V
VADP UVLO Hysteresis (Note 7)	VADP_UVLO_h			600		mV
V_{BAT} UVLO Rising	VBAT_UVLO_r		**2.30**	2.45	**2.60**	V
V_{BAT} UVLO Hysteresis	VBAT_UVLO_h			350		mV
V_{BAT} 5P8V Rising	VBAT_5P8_r		**5.50**	5.95	**6.45**	V
V_{BAT} 5P8V Hysteresis	VBAT_5P8_h			600		mV
VDD 2P7 POR Rising, SMBus and BGATE/BMON Active Threshold	VDD_2P7_r		**2.55**	2.70	**2.85**	V
VDD 2P7 POR Hysteresis (Note 7)	VDD_2P7_h			150		mV
VDD 3P8 POR Rising, Modulator and Gate Driver Active (Note 7)	VDD_3P8_r			3.8		V
VDD 3P8 POR Hysteresis (Note 7)	VDD_3P8_h			150		mV
ACIN Rising	ACIN_r		**0.775**	0.8	**0.825**	V
ACIN Hysteresis	ACIN_h			50		mV

Electrical Specifications Operating conditions: ADP = CSIP = CSIN = 5V and 20V, VSYS = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
LINEAR REGULATOR						
VDD Output Voltage	VDD	6V < V_{DCIN} < 23V, no load	**4.5**	5.0	**5.5**	V
VDD Dropout Voltage	VDD_dp	30mA, V_{DCIN} = 4V		110		mV
VDD Overcurrent Threshold	VDD_OC		**40**	70	**110**	mA
Battery Current	I_{BAT1}	Battery only, BGATE on, PSYS OFF, BMON OFF, V_{BAT} = 12V, DCIN current comes from battery, $I_{BAT} = I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{VSYS}$		12	30	µA
	I_{BAT2}	Battery only, BGATE on, PSYS OFF, BMON ON, V_{BAT} = 12V, DCIN current comes from battery, $I_{BAT} = I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{VSYS}$		74		µA
	I_{BAT3}	Battery only, BGATE on, PSYS ON, BMON OFF, V_{BAT} = 12V, DCIN current comes from battery, $I_{BAT} = I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{VSYS}$		940	1025	µA
INPUT CURRENT REGULATION, R_{S1} = 20mΩ						
Input Current Accuracy		CSIP - CSIN = 80mV		4		A
			-2		**2**	%
		CSIP - CSIN = 40mV		2		A
			-2.5		**2.5**	%
		CSIP - CSIN = 10mV		0.5		A
			-10		**10**	%
Adapter Current PROCHOT# Threshold R_{S1} = 20mΩ	$I_{ADP\_HOT\_TH10}$	ACProchot = 0x0A80H (2688mA)		2688		mA
			-3.0		**3.0**	%
		ACProchot = 0x0400H (1024mA)		1027		mA
			-6.0		**6.0**	%
VOLTAGE REGULATION						
Maximum System Voltage Regulation Accuracy		MaxSystemVoltage for 1-cell, (4.2V)	**-0.75**		**0.75**	%
		MaxSystemVoltage for 2-cell and 3-cell	**-0.50**		**0.50**	%
Minimum System Voltage Regulation Accuracy			**-3**		**3**	%
Input Voltage Regulation Accuracy			**-3**		**3**	%
CHARGE CURRENT REGULATION, R_{S2} = 10mΩ						
Charge Current Accuracy		CSOP - CSON = 60mV		6		A
			-2.5		**2.5**	%
		CSOP - CSON = 20mV		2		A
			-5		**5**	%
		CSOP - CSON = 10mV		1		A
			-10		**10**	%
		CSOP - CSON = 5mV		0.5		A
			-20		**20**	%

Electrical Specifications Operating conditions: ADP = CSIP = CSIN = 5V and 20V, VSYS = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
TRICKLE CHARGING CURRENT REGULATION, R_{S2} = 10mΩ						
Trickle Charge Current Accuracy		Trickle, options 256mA and 512mA	**-20**		**20**	%
		Trickle, option 128mA	**-30**		**30**	%
Fast Charge to Trickle Charge Threshold		V_{BGATE} rising	**1.5**	1.7	**1.9**	V
Trickle Charge to Fast Charge Threshold Hysteresis			**65**	92	**125**	mV
IDEAL DIODE MODE						
Entering Ideal Diode Mode VSYS Voltage Threshold		BGATE off, VSYS falling V_{VBAT} - V_{VSYS}		150		mV
Exiting Ideal Diode Mode Battery Current Threshold		R_{S2} = 10mΩ		150		mA
BGATE Source		VSYS - BGATE = 2V	**12**	17	**20**	mA
BGATE Sink		BGATE - GND = 2V	**4**	6	**10**	mA
AMON/BMON						
INPUT CURRENT SENSE AMPLIFIER, R_{S1} = 20mΩ						
AMON Gain				17.91		V/V
AMON Accuracy V_{AMON} = 17.91 (CSIP - CSIN)		V_{CSIP} - V_{CSIN} = 100mV (5A), CSIP = 5V, 20V	**-2**		**2**	%
		V_{CSIP} - V_{CSIN} = 20mV (1A), CSIP = 5V, 20V	**-5.0**	0.4	**5.0**	%
		V_{CSIP} - V_{CSIN} = 10mV (0.5A), CSIP = 5V, 20V	**-10**	1	**10**	%
		V_{CSIP} - V_{CSIN} = 2mV (0.1A), CSIP = 5V, 20V	**-40**	4	**40**	%
AMON Minimum Output Voltage		V_{CSIP} - V_{CSIN} = 0V			**30**	mV
DISCHARGE CURRENT SENSE AMPLIFIER, R_{S2} = 10mΩ						
BMON Gain				17.95		V/V
BMON Accuracy V_{BMON} = 17.95 (V_{CSON} - V_{CSOP})		V_{CSON} - V_{CSOP} = 100mV (10A), V_{CSON} = 8V	**-2.00**	-0.15	**2.00**	%
		V_{CSON} - V_{CSOP} = 20mV (2A), V_{CSON} = 8V	**-5.00**	-0.68	**5.00**	%
		V_{CSON} - V_{CSOP} = 10mV (1A), V_{CSON} = 8V	**-10.0**	-1.3	**10.0**	%
		V_{CSON} - V_{CSOP} = 6mV (0.6A), V_{CSON} = 8V	**-20.0**	-2.2	**20.0**	%
BMON Minimum Output Voltage		V_{CSON} - V_{CSOP} = 0V			**30**	mV
Discharging Current PROCHOT# Threshold, R_{S2} = 10mΩ	$I_{DIS\_HOT\_TH5}$	DCProchot = 0x1000H (4096mA)		4096		mA
			-3		**3**	%
		DCProchot = 0x0C00H (3072mA)		3072		mA
			-5		**5**	%
AMON/BMON Source Resistance					**5**	Ω
AMON/BMON Sink Resistance					**5**	Ω
ACOK, PROCHOT#, OTGPG/CMOUT (OPEN-DRAIN)						
Open-Drain Current					**1**	µA
BATGONE AND OTGEN						
High-Level Input Voltage			**0.9**			V
Low-Level Input Voltage					**0.4**	V
Input Leakage Current		$V_{BATGONE}$ = 3.3V, 5V; V_{OTGEN} = 3.3V, 5V			**1**	µA
PROCHOT#						
PROCHOT# Debounce Time (Note 7)		Prochot# Debounce register Bit<1:0> = 11		1		ms
		Prochot# Debounce register Bit<1:0> = 10		500		µs

Electrical Specifications Operating conditions: ADP = CSIP = CSIN = 5V and 20V, VSYS = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
PROCHOT# Duration Time (Note 7)		Prochot# Duration register Bit<2:0> = 011		10		ms
		Prochot# Duration register Bit<2:0> = 001		20		ms
Low VSYS PROCHOT# Trip Threshold	$V_{LOW\_VSYS\_HOT}$	Control1 register Bit<9:8> = 00	**5.8**	6.0	**6.2**	V
		Control1 register Bit<9:8> = 01	**6.1**	6.3	**6.5**	V
		Control1 register Bit<9:8> = 10	**6.4**	6.6	**6.8**	V
		Control1 register Bit<9:8> = 11	**6.7**	6.9	**7.1**	V
PSYS						
PSYS Output Current R_{S1} = 20mΩ R_{S2} = 10mΩ	I_{PSYS}	V_{CSIP} = 19V, $V_{CSIP-CSIN}$ = 80mV, V_{BAT} = 12V, $V_{CSOP-CSON}$ = 0mV		109		µA
			-5		5	%
		V_{CSIP} = 19V, $V_{CSIP-CSIN}$ = 0mV, V_{BAT} = 12V, $V_{CSOP-CSON}$ = 20mV		36		µA
			-6		6	%
		V_{CSIP} = 19V, $V_{CSIP-CSIN}$ = 0mV, V_{BAT} = 8.4V, $V_{CSOP-CSON}$ = -20mV		24		µA
			-7		7	%
		V_{CSIP} = 0V, $V_{CSIP-CSIN}$ = 0mV, V_{BAT} = 8.4V, $V_{CSOP-CSON}$ = -10mV		12		µA
			-8.5		8.5	%
Maximum PSYS Output Voltage	V_{PSYS_MAX}	I_{PSYS} = 200µA		2		V
OTG						
OTG Voltage		OTGVoltage register = 5.12V	**5.04**	5.11	**5.18**	V
OTG Current		OTGCurrent register = 512mA	**435**	512	**589**	mA
		OTGCurrent register = 1024mA	**922**	1024	**1126**	mA
		OTGCurrent register = 4096mA	**3975**	4096	**4220**	mA
GENERAL PURPOSE COMPARATOR						
General Purpose Comparator Rising Threshold		Reference = 1.2V	**1.15**	1.20	**1.25**	V
		Reference = 2V	**1.95**	2.00	**2.05**	V
General Purpose Comparator Hysteresis		Reference = 1.2V	**25**	40	**65**	mV
		Reference = 2V	**25**	40	**65**	mV
PROTECTION						
VSYS Overvoltage Rising Threshold		MaxSystemVoltage register value = 8.4V	**8.79**	8.96	**9.18**	V
VSYS Overvoltage Hysteresis			**185**	280	**380**	mV
Adapter Way Overcurrent Rising Threshold			**8**	12	**18**	A
Adapter Way Overcurrent Hysteresis			**2.8**	3.5	**4.2**	A
Battery Discharge Way Overcurrent Rising Threshold (Note 7)		R_{S1} = 20mΩ	**10**	15	**24**	A
Battery Discharge Way Overcurrent Hysteresis (Note 7)		R_{S2} = 10mΩ	**2.56**	3.20	**3.84**	A
Over-Temperature Threshold (Note 7)			**140**	150	**160**	°C
Adapter Overvoltage Rising Threshold			**22.5**	23.4	**24**	V
Adapter Overvoltage Hysteresis			**200**	400	**600**	mV
MISCELLANEOUS						
Switching Frequency Accuracy		All programmed f_{SW} settings	**-15**		**15**	%
1MHz Oscillator			**0.85**	1.00	**1.15**	MHz
Digital Debounce Time Accuracy (Note 7)			**-15**		**15**	%
BGATE_Low Voltage		VSYS = 8V	**-10**	0	**10**	mV

Electrical Specifications

Operating conditions: ADP = CSIP = CSIN = 5V and 20V, VSYS = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
ASGATE_Low Voltage Clamp		VADP = 23V, VADP - ASGATE	**8**	11	**12**	V
Battery Learn Mode Auto-Exit Threshold		MinSystemVoltage = 5.376V Control1 register Bit<13> = 1	**5.05**		**5.70**	V
Battery Learn Mode Auto-Exit Hysteresis (Note 7)			**80**	160	**320**	mV
SMBus						
SDA/SCL Input Low Voltage					**0.8**	V
SDA/SCL Input High Voltage			**2**			V
SDA/SCL Input Bias Current					**1**	µA
SDA, Output Sink Current		SDA = 0.4V, on	**4**			mA
GATE DRIVER (Note 7)						
UGATE1 Pull-Up Resistance	$UG1_{RPU}$	100mA source current		800	**1200**	mΩ
UGATE1 Source Current	$UG1_{SRC}$	UGATE1 - PHASE1 = 2.5V	**1.3**	2		A
UGATE1 Pull-Down Resistance	$UG1_{RPD}$	100mA sink current		350	**475**	mΩ
UGATE1 Sink Current	$UG1_{SNK}$	UGATE1 - PHASE1 = 2.5V	**1.9**	2.8		A
LGATE1 Pull-Up Resistance	$LG1_{RPU}$	100mA source current		800	**1200**	mΩ
LGATE1 Source Current	$LG1_{SRC}$	LGATE1 - GND = 2.5V	**1.3**	2		A
LGATE1 Pull-Down Resistance	$LG1_{RPD}$	100mA sink current		300	**450**	mΩ
LGATE1 Sink Current	$LG1_{SNK}$	LGATE1 - GND = 2.5V	**2.3**	3.5		A
LGATE2 Pull-Up Resistance	$LG2_{RPU}$	100mA source current		800	**1200**	mΩ
LGATE2 Source Current	$LG2_{SRC}$	LGATE2 - GND = 2.5V	**1.3**	2		A
LGATE2 Pull-Down Resistance	$LG2_{RPD}$	100mA sink current		300	**450**	mΩ
LGATE2 Sink Current	$LG2_{SNK}$	LGATE2 - GND = 2.5V	**2.3**	3.5		A
UGATE2 Pull-Up Resistance	$UG2_{RPU}$	100mA source current		800	**1200**	mΩ
UGATE2 Source Current	$UG2_{SRC}$	UGATE2 - PHASE2 = 2.5V	**1.3**	2		A
UGATE2 Pull-Down Resistance	$UG2_{RPD}$	100mA sink current		350	**475**	mΩ
UGATE2 Sink Current	$UG2_{SNK}$	UGATE2 - PHASE2 = 2.5V	**1.9**	2.8		A
UGATE1 to LGATE1 Dead Time	$t_{UG1LG1DEAD}$		**10**	20	**40**	ns
LGATE1 to UGATE1 Dead Time	$t_{LG1UG1DEAD}$		**15**	25	**45**	ns
LGATE2 to UGATE2 Dead Time	$t_{LG2UG2DEAD}$		**15**	22	**40**	ns
UGATE2 to LGATE2 Dead Time	$t_{UG2LG2DEAD}$		**10**	20	**40**	ns

SMBUS Timing Specification (Note 7)

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
SMBus Frequency	f_{SMB}		**10**		**400**	kHz
Bus Free Time	t_{BUF}		**4.7**			µs
Start Condition Hold Time from SCL	$t_{HD:STA}$		**4**			µs
Start Condition Set-Up Time from SCL	$t_{SU:STA}$		**4.7**			µs
Stop Condition Set-Up Time from SCL	$t_{SU:STO}$		**4**			µs
SDA Hold Time from SCL	$t_{HD:DAT}$		**300**			ns
SDA Set-up Time from SCL	$t_{SU:DAT}$		**250**			ns
SCL Low Period	t_{LOW}		**4.7**			µs
SCL High Period	t_{HIGH}		**4**			µs

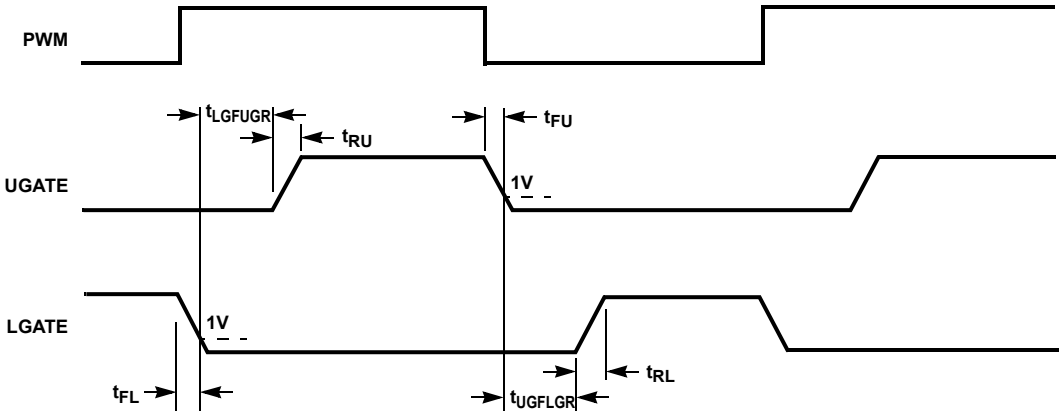
SMBUS Timing Specification (Note 7)

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
SMBus Inactivity Timeout		Maximum charging period without a SMBus Write to MaxSystemVoltage or ChargeCurrent register		175		s

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Limits established by characterization and are not production tested.

Buck Mode Gate Driver Timing Diagram



$t_{LGFUGR} = t_{LG1UG1DEAD}$

$t_{UGFLGR} = t_{UG1LG1DEAD}$

FIGURE 3. BUCK MODE GATE DRIVER TIMING DIAGRAM

Typical Performance

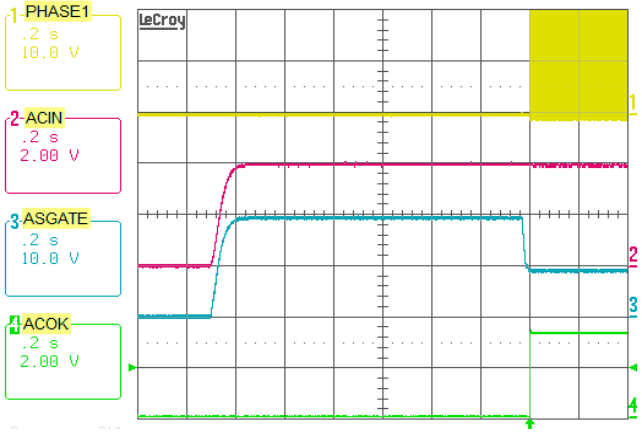


FIGURE 4. ADAPTER INSERTION, V_{ADP} = 20V, V_{BAT} = 7.5V, CHARGECURRENT = 0A, ADAPTER INSERTION DEBOUNCE = 1.3s

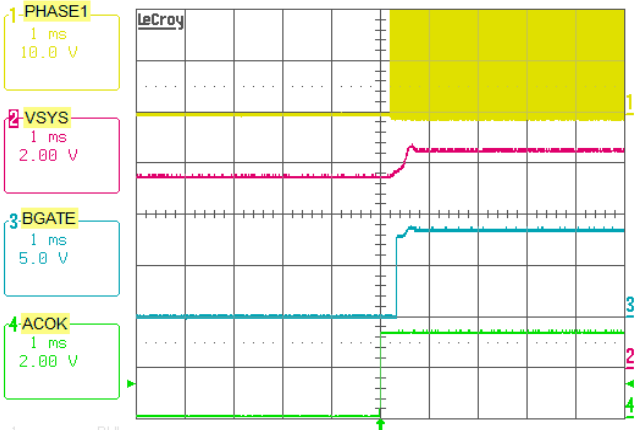


FIGURE 5. ADAPTER INSERTION, V_{ADP} = 20V, V_{BAT} = 7.5V, CHARGECURRENT = 0A

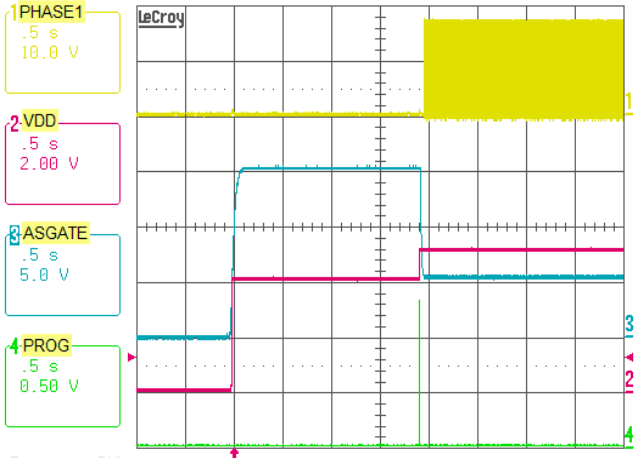


FIGURE 6. ADAPTER INSERTION, V_{ADP} = 20V, V_{BAT} = 7.5V, CHARGECURRENT = 0A, ADAPTER INSERTION DEBOUNCE = 1.3s

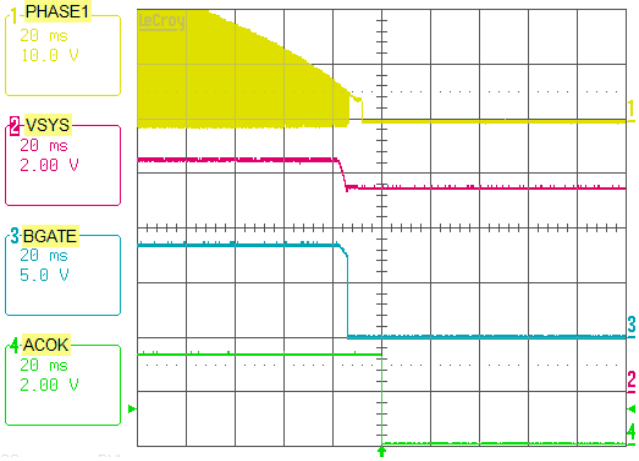


FIGURE 7. ADAPTER REMOVAL, V_{ADP} = 20V, V_{BAT} = 7.5V, CHARGECURRENT = 0A

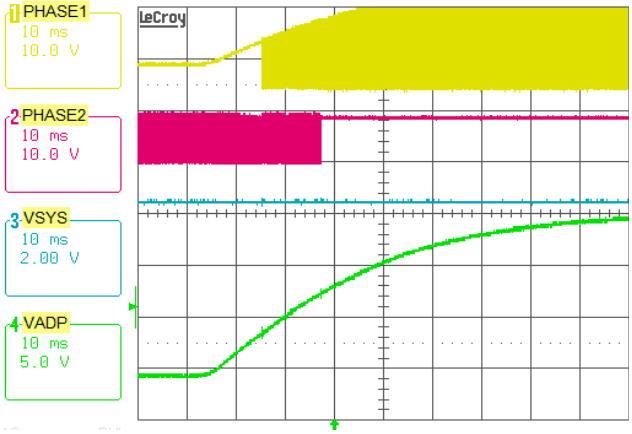


FIGURE 8. ADAPTER VOLTAGE RAMPS UP, BOOST -> BUCK-BOOST -> BUCK OPERATION MODE TRANSITION

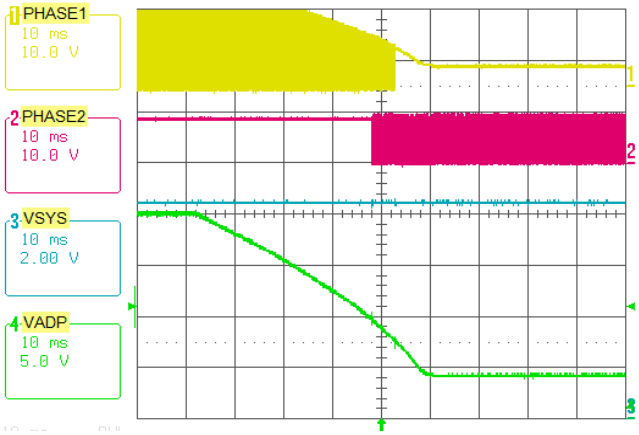


FIGURE 9. ADAPTER VOLTAGE RAMPS DOWN, BUCK -> BUCK-BOOST -> BOOST OPERATION MODE TRANSITION

Typical Performance (Continued)

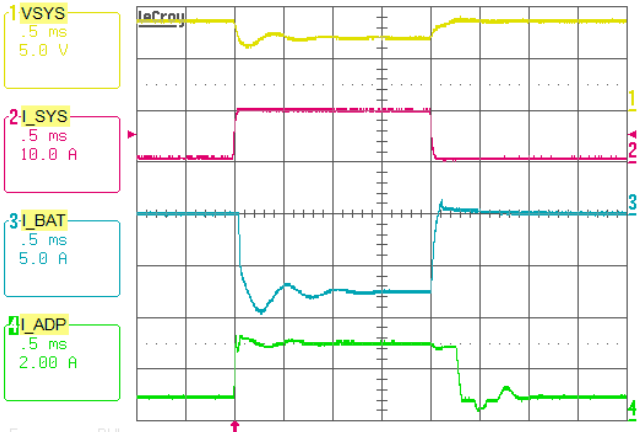


FIGURE 10. BOOST MODE, OUTPUT VOLTAGE LOOP TO ADAPTER CURRENT LOOP TRANSITION. V_{ADP} = 5V, MAXSYSTEMVOLTAGE = 8.496V, V_{BAT} = 7V, SYSTEM LOAD 0.5A TO 10A STEP, ADAPTERCURRENTLIMIT = 3A, CHARGECURRENT = 0A

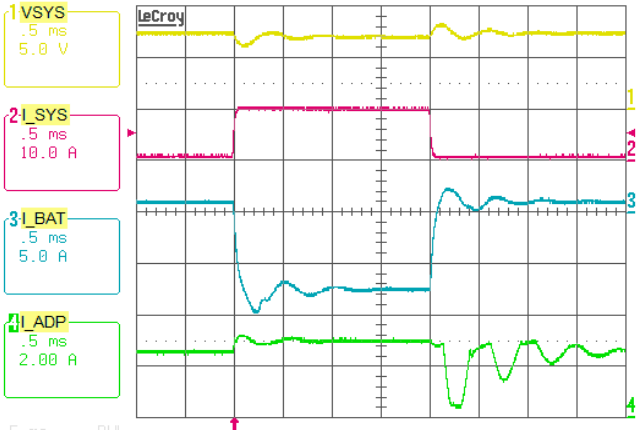


FIGURE 11. BOOST MODE, CHARGING CURRENT LOOP TO ADAPTER CURRENT LOOP TRANSITION. V_{ADP} = 5V, MAXSYSTEMVOLTAGE = 8.496V, V_{BAT} = 7V, SYSTEM LOAD 0.5A TO 10A STEP, ADAPTERCURRENTLIMIT = 3A, CHARGECURRENT = 1A

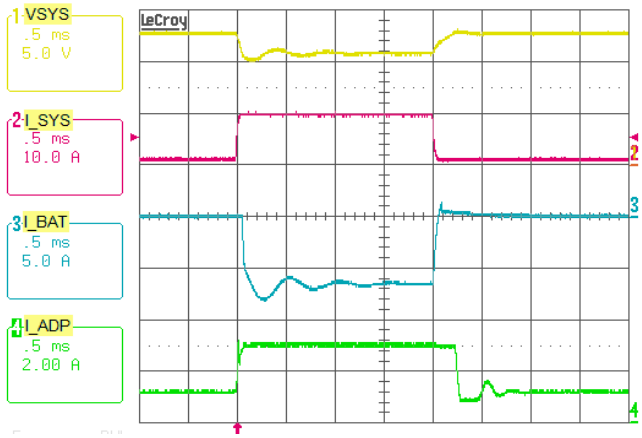


FIGURE 12. BUCK-BOOST MODE, OUTPUT VOLTAGE LOOP TO ADAPTER CURRENT LOOP TRANSITION. V_{ADP} = 12V, MAXSYSTEMVOLTAGE = 12.6V, V_{BAT} = 11V, SYSTEM LOAD 1A TO 10A STEP, ADAPTERCURRENTLIMIT = 3A, CHARGECURRENT = 0A

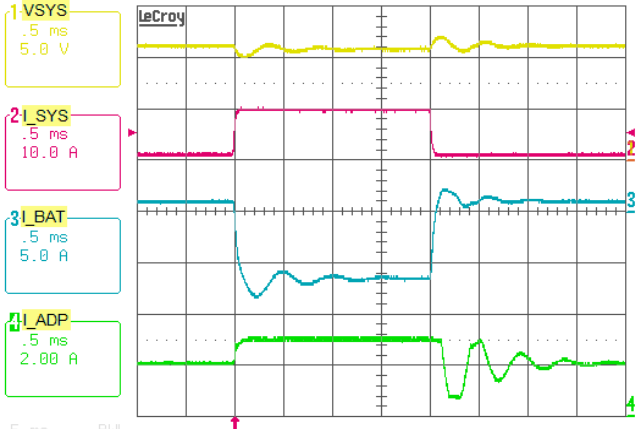


FIGURE 13. BUCK-BOOST MODE, CHARGING CURRENT LOOP TO ADAPTER CURRENT LOOP TRANSITION. V_{ADP} = 12V, MAXSYSTEMVOLTAGE = 12.6V, V_{BAT} = 11V, SYSTEM LOAD 1A TO 10A STEP, ADAPTERCURRENTLIMIT = 3A, CHARGECURRENT = 1A

Typical Performance (Continued)

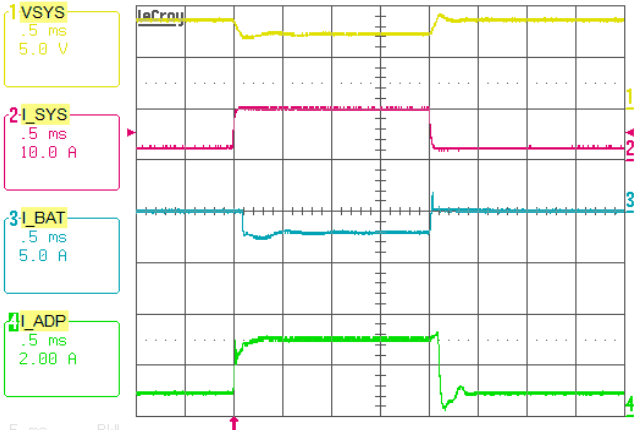


FIGURE 14. BUCK MODE, OUTPUT VOLTAGE LOOP TO ADAPTER CURRENT LOOP TRANSITION. V_{ADP} = 20V, MAXSYSTEMVOLTAGE = 8.496V, V_{BAT} = 7V, SYSTEM LOAD 2A TO 10A STEP, ADAPTERCURRENTLIMIT = 3A, CHARGECURRENT = 0A

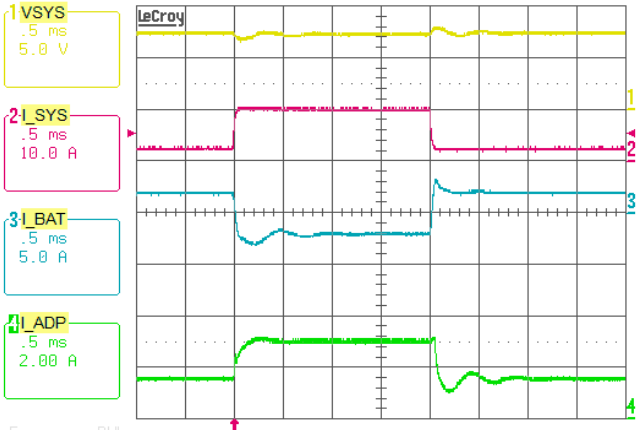


FIGURE 15. BUCK MODE, CHARGING CURRENT LOOP TO ADAPTER CURRENT LOOP TRANSITION. V_{ADP} = 20V, MAXSYSTEMVOLTAGE = 8.496V, V_{BAT} = 7V, SYSTEM LOAD 2A TO 10A STEP, ADAPTERCURRENTLIMIT = 3A, CHARGECURRENT = 2A

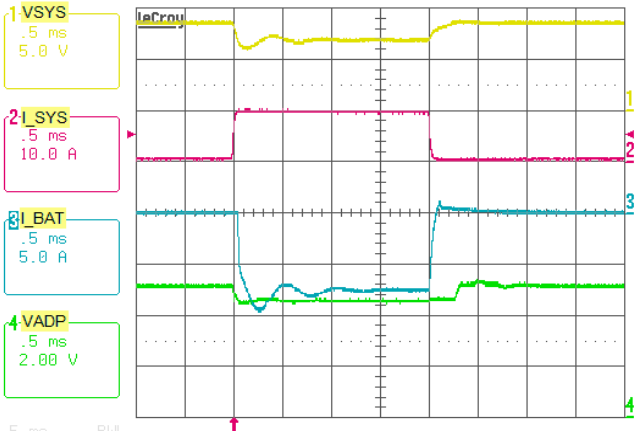


FIGURE 16. BOOST MODE, OUTPUT VOLTAGE LOOP TO INPUT VOLTAGE LOOP TRANSITION. V_{ADP} = 5V, MAXSYSTEMVOLTAGE = 8.496V, V_{BAT} = 7V, VINDAC = 4.5V, SYSTEM LOAD 0.5A TO 10A STEP, CHARGECURRENT = 0A

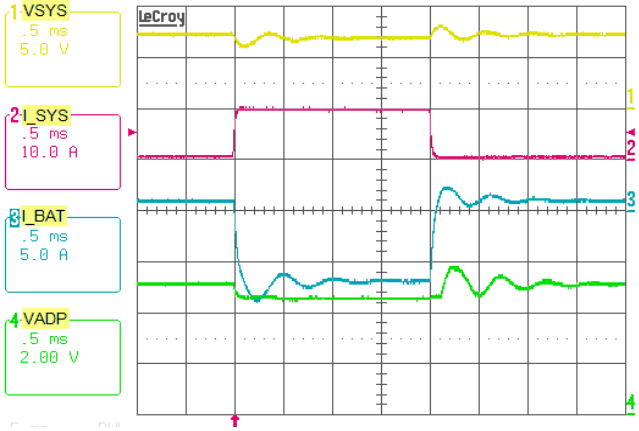


FIGURE 17. BOOST MODE, CHARGING CURRENT LOOP TO INPUT VOLTAGE LOOP TRANSITION. V_{ADP} = 5V, MAXSYSTEMVOLTAGE = 8.496V, V_{BAT} = 7V, VINDAC = 4.5V, SYSTEM LOAD 0.5A TO 10A STEP, CHARGECURRENT = 1A

Typical Performance (Continued)

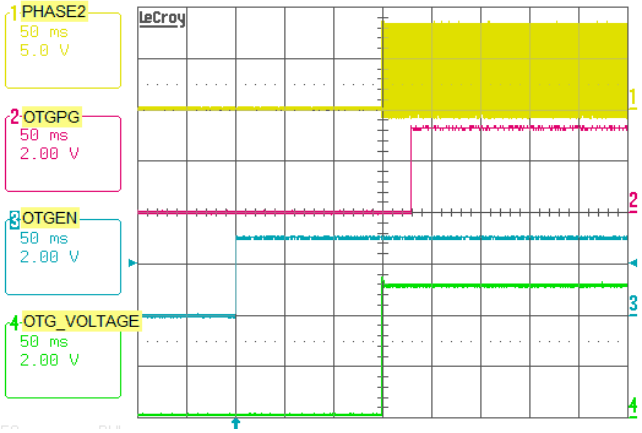


FIGURE 18. OTG MODE ENABLE, OTG ENABLE 150ms DEBOUNCE TIME

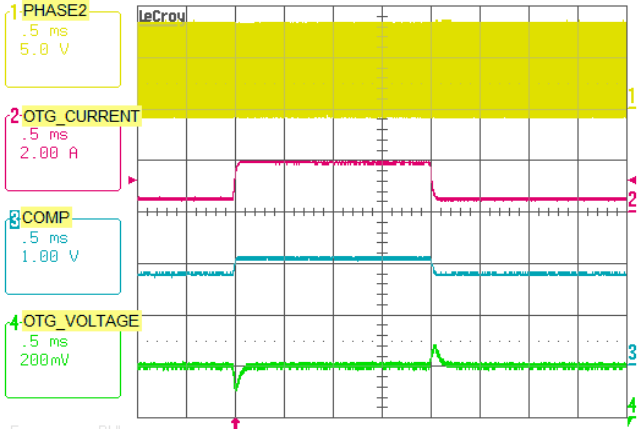


FIGURE 19. OTG MODE 0.5A TO 2A TRANSIENT LOAD, OTG VOLTAGE = 5.12V

General SMBus Architecture

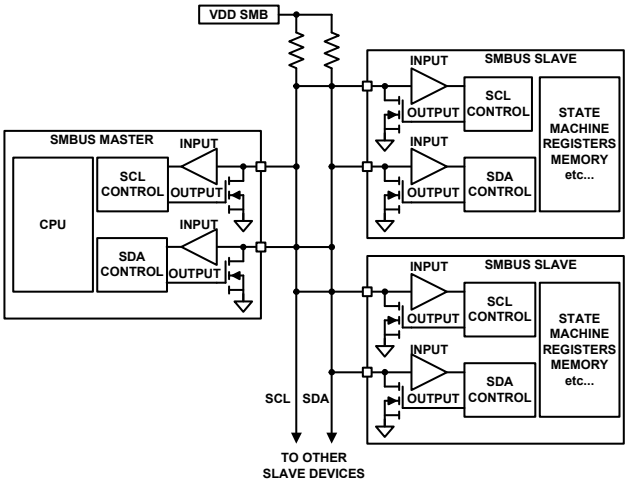


FIGURE 20. GENERAL SMBus ARCHITECTURE

Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. Refer to Figure 21.

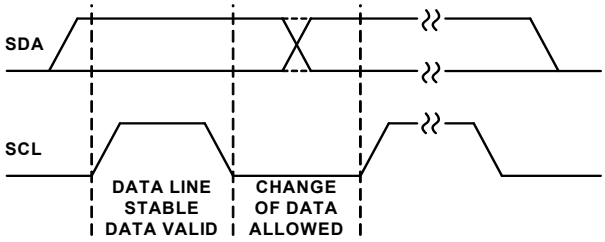


FIGURE 21. DATA VALIDITY

START and STOP Conditions

Figure 22 START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

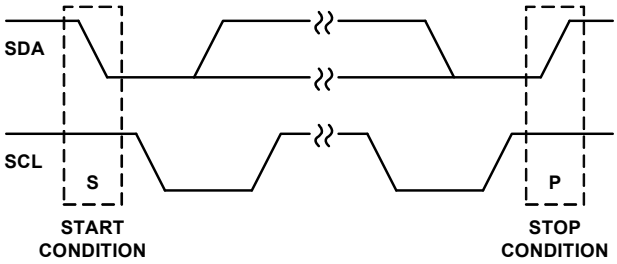


FIGURE 22. START AND STOP WAVEFORMS

Acknowledge

Each address and data transmission uses 9 clock pulses. The ninth pulse is the acknowledge bit (ACK). After the start condition, the master sends 7 slave address bits and a R/W bit during the next 8 clock pulses. During the 9 clock pulse, the device that recognizes its own address holds the data line low to acknowledge (Refer to Figure 23). The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

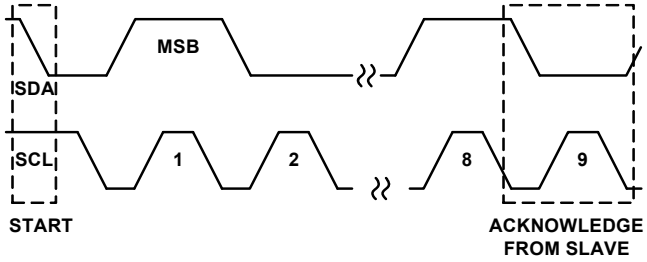


FIGURE 23. ACKNOWLEDGE ON THE SMBus

SMBus Transactions

All transactions start with a control byte sent from the SMBus master device. The control byte begins with a Start condition, followed by 7 bits of slave address (0001001 for the ISL9237) and the R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a WRITE or 1 for a READ. If any slave device on the SMBus bus recognizes its address, it will acknowledge by pulling the serial data (SDA) line low for the last clock cycle in the control byte. If no slave exists at that address or it is not ready to communicate, the data line will be one, indicating a Not Acknowledge condition.

Once the control byte is sent and the ISL9237 acknowledges it, the second byte sent by the master must be a register address byte such as 0x14 for the ChargeCurrent register. The register address byte tells the ISL9237 which register the master will write or read. See Table 1 on page 17 for details of the registers. Once the ISL9237 receives a register address byte, it will respond with an acknowledge.

Byte Format

Every byte put on the SDA line must be 8 bits long and must be followed by an acknowledge bit. Data is transferred with the Most Significant Bit first (MSB) and the Least Significant Bit (LSB) last. The LO BYTE data is transferred before the HI BYTE data. For example, when writing 0x41A0, 0xA0 is written first and 0x41 is written second.

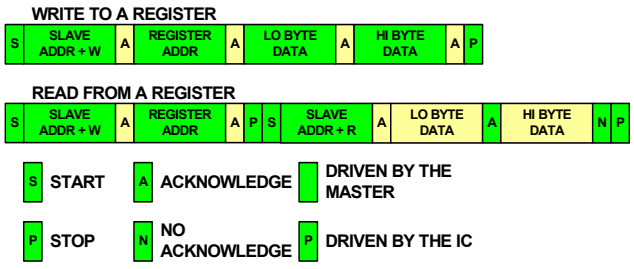


FIGURE 24. SMBus READ AND WRITE PROTOCOL

SMBus and I²C Compatibility

The ISL9237 SMBus minimum input logic high voltage is 2V, so it is compatible with an I²C with higher than 2V pull-up power supply.

The ISL9237 SMBus registers are 16 bits, so it is compatible with a 16-bit I²C or an 8-bit I²C with auto-increment capability.

ISL9237 SMBus Commands

The ISL9237 receives control inputs from the SMBus interface after Power-On Reset (POR). The serial interface complies with the System Management Bus Specification, which can be downloaded from www.smbus.org. The ISL9237 uses the SMBus Read-word and Write-word protocols (see Figure 24 on page 16) to communicate with the host system and a smart battery. The ISL9237 is an SMBus slave device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001_:

Read address = 0b00010011 (0x13H) and

Write address = 0b00010010 (0x12H).

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors for SDA and SCL to achieve rise times according to the SMBus specifications.

The illustration in this datasheet is based on current sensing resistors R_{S1} = 20mΩ and R_{S2} = 10mΩ unless otherwise specified.

TABLE 1. REGISTER SUMMARY

REGISTER NAMES	REGISTER ADDRESS	READ/ WRITE	NUMBER OF BITS	DESCRIPTION	DEFAULT
ChargeCurrentLimit	0x14	R/W	11	[12:2] 11-bit, LSB size 4mA, maximum range 6080mA for 10mΩ R_{S2}.	0A
AdapterCurrentLimit1	0x3F	R/W	11	[12:2] 11-bit, LSB size 4mA, maximum range 6080mA for 20mΩ R_{S1}.	Set by PROG pin
AdapterCurrentLimit2	0x3B	R/W	11	[12:2] 11-bit, LSB size 4mA, maximum range 6080mA for 20mΩ R_{S1}.	1500mA
MaxSystemVoltage	0x15	R/W	11	[13:3] 11-bit, LSB size 8mV, maximum range 13.824V.	4.192V for 1-cell
					8.384V for 2-cell
					12.576V for 3-cell
MinSystemVoltage	0x3E	R/W	11	[13:3] 11-bit, LSB size 8mV, maximum range 13.824V.	2.688V for 1-cell
					5.376V for 2-cell
					8.064V for 3-cell
ACProchot#	0x47	R/W	6	[12:7] adapter current Prochot# threshold. LSB size 128mA, maximum 6.4A for 20mΩ Rs1.	3.072A
DCProchot#	0x48	R/W	6	[13:8] Battery discharging current Prochot# threshold. LSB size 256mA, maximum 12.8A for 10mΩ R_{S2}.	4.096A
T1 and T2	0x38	R/W	6	Configure two-level adapter current limit duration	0x000h
Control0	0x39	R/W	8	Configure various charger options	0x0000h
Control1	0x3C	R/W	16	Configure various charger options	0x0000h
Control2	0x3D	R/W	16	Configure various charger options	0x0000h
Information	0x3A	R	16	Indicate various charger status	0x0000h
OTGVoltage	0x49	R/W	6	[12:7] 6-bit, OTG mode output voltage reference. LSB size 128mV, maximum 5.376V and minimum 4.864V.	5.12V
OTGCurrent	0x4A	R/W	6	[12:7] 6-bit, OTG mode output current limit. LSB size 128mA, maximum 4.096A for 20mΩ R_{S1}.	512mA
ManufacturerID	0xFE	R	8	Manufacturers ID register – 0x49 - Read only	0x0049h
DeviceID	0xFF	R	8	Device ID register - 0x0A- Read only	0x000Ah

Setting Charging Current Limit

To set the charging current limit, write a 16-bit ChargeCurrentLimit command (0x14H or 0b00010100) using the Write-word protocol shown in Figure 24 on page 16 and the data format shown in Table 2 for a 10mΩ R_{S2} or Table 3 for a 5mΩ R_{S2}.

The ISL9237 limits the charging current by limiting the CSOP-CSON voltage. By using the recommended current sense resistor values R_{S1} = 20mΩ and R_{S2} = 10mΩ, the register's LSB always translates to 1mA of charging current. The ChargeCurrentLimit register accepts any charging current command but only the valid register bits will be written to the register and the maximum value is clamped at 6080mA for R_{S2} = 10mΩ.

After POR, the ChargeCurrentLimit register is reset to 0x0000H. To set the battery charging current value, write a non-zero number to the ChargeCurrentLimit register. The ChargeCurrentLimit register can be read back to verify its content.

Table 2 shows the conditions to enable fast charging according to the ChargeCurrentLimit register setting.

TABLE 2. ChargeCurrentLimit REGISTER 0x14H (11-BIT, 4mA STEP, 10mΩ SENSE RESISTOR, x36)

BIT	DESCRIPTION
<1:0>	Not used
<2>	0 = Add 0mA of charge current limit. 1 = Add 4mA of charge current limit.
<3>	0 = Add 0mA of charge current limit. 1 = Add 8mA of charge current limit.
<4>	0 = Add 0mA of charge current limit. 1 = Add 16mA of charge current limit.
<5>	0 = Add 0mA of charge current limit. 1 = Add 32mA of charge current limit.
<6>	0 = Add 0mA of charge current limit. 1 = Add 64mA of charge current limit.
<7>	0 = Add 0mA of charge current limit. 1 = Add 128mA of charge current limit.
<8>	0 = Add 0mA of charge current limit. 1 = Add 256mA of charge current limit.
<9>	0 = Add 0mA of charge current limit. 1 = Add 512mA of charge current limit.
<10>	0 = Add 0mA of charge current limit. 1 = Add 1024mA of charge current limit.
<11>	0 = Add 0mA of charge current limit. 1 = Add 2048mA of charge current limit.
<12>	0 = Add 0mA of charge current limit. 1 = Add 4096mA of charge current limit.
<13:15>	Not used
Maximum	<12:2> = 10111110000, 6080mA

TABLE 3. ChargeCurrentLimit REGISTER 0x14H (11-BIT, 8mA STEP, 5mΩ SENSE RESISTOR, x36)

BIT	DESCRIPTION
<1:0>	Not used
<2>	0 = Add 0mA of charge current limit. 1 = Add 8mA of charge current limit.
<3>	0 = Add 0mA of charge current limit. 1 = Add 16mA of charge current limit.
<4>	0 = Add 0mA of charge current limit. 1 = Add 32mA of charge current limit.
<5>	0 = Add 0mA of charge current limit. 1 = Add 64mA of charge current limit.
<6>	0 = Add 0mA of charge current limit. 1 = Add 128mA of charge current limit.
<7>	0 = Add 0mA of charge current limit. 1 = Add 256mA of charge current limit.
<8>	0 = Add 0mA of charge current limit. 1 = Add 512mA of charge current limit.
<9>	0 = Add 0mA of charge current limit. 1 = Add 1024mA of charge current limit.
<10>	0 = Add 0mA of charge current limit. 1 = Add 2048mA of charge current limit.
<11>	0 = Add 0mA of charge current limit. 1 = Add 4096mA of charge current limit.
<12>	0 = Add 0mA of charge current limit. 1 = Add 8192mA of charge current limit.
<13:15>	Not used
Maximum	<12:2> = 10111110000, 12160mA

Setting Adapter Current Limit

To set the adapter current limit, write a 16-bit AdapterCurrentLimit1 command (0x3FH or 0b00111111) and/or AdapterCurrentLimit2 command (0x3BH or 0b00111011) using the Write-word protocol shown in Figure 24 and the data format shown in Table 4 for a 20mΩ R_{S1} or Table 5 for a 10mΩ R_{S1}.

The ISL9237 limits the adapter current by limiting the CSIP-CSIN voltage. By using the recommended current sense resistor values, the register's LSB always translates to 1mA of adapter current. Any adapter current limit command will be accepted but only the valid register bits will be written to the AdapterCurrentLimit1 and AdapterCurrentLimit2 registers, and the maximum value is clamped at 6080mA for R_{S1} = 20mΩ.

After adapter POR, the AdapterCurrentLimit1 register is reset to the value programmed through the PROG pin resistor. The AdapterCurrentLimit2 register is set to its default value of 1.5A or keep the value that is written to it previously if battery is present first. The AdapterCurrentLimit1 and AdapterCurrentLimit2 registers can be read back to verify their content.

To set a second level adapter current limit, write a 16-bit AdapterCurrentLimit2 (0x3BH or 0b00111011) command using the Write-word protocol shown in Figure 24 and the data format as shown in Table 4 for a 20mΩ R_{S1} or Table 5 for a 10mΩ R_{S1}.

The AdapterCurrentLimit2 register has the same specification as the AdapterCurrentLimit1 register. Refer to "Two-Level Adapter Current Limit" on page 30 for detailed operation.

TABLE 4. AdapterCurrentLimit1 REGISTER 0x3FH AND AdapterCurrentLimit2 REGISTER 0x3BH (11-BIT, 4mA STEP, 20mΩ SENSE RESISTOR, x16)

BIT	DESCRIPTION
<1:0>	Not used
<2>	0 = Add 0mA of adapter current limit. 1 = Add 4mA of adapter current limit.
<3>	0 = Add 0mA of adapter current limit. 1 = Add 8mA of adapter current limit.
<4>	0 = Add 0mA of adapter current limit. 1 = Add 16mA of adapter current limit.
<5>	0 = Add 0mA of adapter current limit. 1 = Add 32mA of adapter current limit.
<6>	0 = Add 0mA of adapter current limit. 1 = Add 64mA of adapter current limit.
<7>	0 = Add 0mA of adapter current limit. 1 = Add 128mA of adapter current limit.
<8>	0 = Add 0mA of adapter current limit. 1 = Add 256mA of adapter current limit.
<9>	0 = Add 0mA of adapter current limit. 1 = Add 512mA of adapter current limit.
<10>	0 = Add 0mA of adapter current limit. 1 = Add 1024mA of adapter current limit.
<11>	0 = Add 0mA of adapter current limit. 1 = Add 2048mA of adapter current limit.
<12>	0 = Add 0mA of adapter current limit. 1 = Add 4096mA of adapter current limit.
<13:15>	Not used
Maximum	<12:4> = 10111110000, 6080mA

TABLE 5. AdapterCurrentLimit1 REGISTER 0x3FH AND AdapterCurrentLimit2 REGISTER 0x3BH (11-BIT, 8mA STEP, 10mΩ SENSE RESISTOR, x16)

BIT	DESCRIPTION
<1:0>	Not used.
<2>	0 = Add 0mA of adapter current limit. 1 = Add 8mA of adapter current limit.
<3>	0 = Add 0mA of adapter current limit. 1 = Add 16mA of adapter current limit.
<4>	0 = Add 0mA of adapter current limit. 1 = Add 32mA of adapter current limit.
<5>	0 = Add 0mA of adapter current limit. 1 = Add 64mA of adapter current limit.
<6>	0 = Add 0mA of adapter current limit. 1 = Add 128mA of adapter current limit.
<7>	0 = Add 0mA of adapter current limit. 1 = Add 256mA of adapter current limit.

TABLE 5. AdapterCurrentLimit1 REGISTER 0x3FH AND AdapterCurrentLimit2 REGISTER 0x3BH (11-BIT, 8mA STEP, 10mΩ SENSE RESISTOR, x16) (Continued)

BIT	DESCRIPTION
<8>	0 = Add 0mA of adapter current limit. 1 = Add 512mA of adapter current limit.
<9>	0 = Add 0mA of adapter current limit. 1 = Add 1024mA of adapter current limit.
<10>	0 = Add 0mA of adapter current limit. 1 = Add 2048mA of adapter current limit.
<11>	0 = Add 0mA of adapter current limit. 1 = Add 4096mA of adapter current limit.
<12>	0 = Add 0mA of adapter current limit. 1 = Add 8192mA of adapter current limit.
<13:15>	Not used
Maximum	<12:4> = 10111110000, 12160mA

Setting Two-Level Adapter Current Limit Duration

For a two-level adapter current limit, write a 16-bit T1 and T2 command (0x38H or 0b00111000) using the Write-word protocol shown in Figure 24 and the data format as shown in Table 6 to set the AdapterCurrentLimit1 duration T1. Write a 16-bit T2 command (0x38H or 0b00111000) to set AdapterCurrentLimit2 duration T2. T1 and T2 register accepts any command, however, only the valid register bits will be written. Refer to "Two-Level Adapter Current Limit" on page 30 for detailed operation.

TABLE 6. T1 AND T2 REGISTER 0x38H

BIT	DESCRIPTION
T1 <2:0>	000 = 10ms 001 = 20ms 010 = 15ms 011 = 5ms 100 = 1ms 101 = 0.5ms 110 = 0.1ms 111 = 0ms
T2 <10:8>	000 = 10µs (default) 001 = 100µs 010 = 500µs 011 = 1ms 100 = 300µs 101 = 750µs 110 = 2ms 111 = 10ms

Setting Maximum Charging Voltage or System Regulating Voltage

To set the maximum charging voltage or the system regulating voltage, write a 16-bit MaxSystemVoltage command (0x15H or 0b00010101) using the Write-word protocol shown in Figure 24 and the data format as shown in Table 7.

The MaxSystemVoltage register accepts any voltage command however, only the valid register bits will be written to the register and the maximum value is clamped at 13.824V.

The MaxSystemVoltage register sets the battery full charging voltage limit. The MaxSystemVoltage register setting also is the system bus voltage regulation point when battery is absent or battery is present, however, is not in charging mode. See "System Voltage Regulation" on page 31 for details.

The VSYS pin is used to sense the battery voltage for maximum charging voltage regulation. VSYS pin is also the system bus voltage regulation sense point.

TABLE 7. MaxSystemVoltage REGISTER 0x15H (8mV STEP)

BIT	DESCRIPTION
<2:0>	Not used
<3>	0 = Add 0mV of charge voltage. 1 = Add 8mV of charge voltage.
<4>	0 = Add 0mV of charge voltage. 1 = Add 16mV of charge voltage.
<5>	0 = Add 0mV of charge voltage. 1 = Add 32mV of charge voltage.
<6>	0 = Add 0mV of charge voltage. 1 = Add 64mV of charge voltage.
<7>	0 = Add 0mV of charge voltage. 1 = Add 128mV of charge voltage.
<8>	0 = Add 0mV of charge voltage. 1 = Add 256mV of charge voltage.
<9>	0 = Add 0mV of charge voltage. 1 = Add 512mV of charge voltage.
<10>	0 = Add 0mV of charge voltage. 1 = Add 1024mV of charge voltage.
<11>	0 = Add 0mV of charge voltage. 1 = Add 2046mV of charge voltage.
<12>	0 = Add 0mV of charge voltage. 1 = Add 4096mV of charge voltage.
<13>	0 = Add 0mV of charge voltage. 1 = Add 8192mV of charge voltage.
<15:14>	Not used
Maximum	<13:3> = 11011000000, 13824mV

Setting Minimum System Voltage

To set the minimum system voltage, write a 16-bit MinSystemVoltage command (0x3EH or 0b00111110) using the Write-word protocol shown in Figure 24 and the data format as shown in Table 8.

The MinSystemVoltage register accepts any voltage command, however, only the valid register bits will be written to the register, and the maximum value is clamped at 13.824V. The MinSystemVoltage register value should be set lower than the MaxSystemVoltage register value.

The MinSystemVoltage register sets the battery voltage threshold for entry and exit of the trickle charging mode and for entry and exit of the Learn mode. The VBAT pin is used to sense the battery voltage to compare with the MinSystemVoltage register setting. Refer to "Trickle Charging" on page 31 and "Battery Learn Mode" on page 29 for details.

The MinSystemVoltage register setting also is the system voltage regulation point when it is in trickle charging mode. The CSON pin is the system voltage regulation sense point in trickle charging mode. Refer to "System Voltage Regulation" on page 31" for details.

TABLE 8. MinSystemVoltage REGISTER 0x3EH

BIT	DESCRIPTION
<2:0>	Not used
<3>	0 = Add 0mV of charge voltage. 1 = Add 8mV of charge voltage.
<4>	0 = Add 0mV of charge voltage. 1 = Add 16mV of charge voltage.
<5>	0 = Add 0mV of charge voltage. 1 = Add 32mV of charge voltage.
<6>	0 = Add 0mV of charge voltage. 1 = Add 64mV of charge voltage.
<7>	0 = Add 0mV of charge voltage. 1 = Add 128mV of charge voltage.
<8>	0 = Add 0mV of charge voltage. 1 = Add 256mV of charge voltage.
<9>	0 = Add 0mV of charge voltage. 1 = Add 512mV of charge voltage.
<10>	0 = Add 0mV of charge voltage. 1 = Add 1024mV of charge voltage.
<11>	0 = Add 0mV of charge voltage. 1 = Add 2046mV of charge voltage.
<12>	0 = Add 0mV of charge voltage. 1 = Add 4096mV of charge voltage.
<13>	0 = Add 0mV of charge voltage. 1 = Add 8192mV of charge voltage.
<15:14>	Not used
Maximum	<13:3> = 11011000000, 13824mV

Setting PROCHOT# Threshold for Adapter Overcurrent Condition

To set the PROCHOT# assertion threshold for adapter overcurrent condition, write a 16-bit ACProchot# command (0x47H or 0b01000111) using the Write-word protocol shown in Figure 24 and the data format shown in Table 9 on page 21. By using the recommended current sense resistor values, the register's LSB always translates to 1mA of adapter current. The ACProchot# register accepts any current command, however, only the valid register bits will be written to the register, and the maximum value is clamped at 6400mA for R_{S1} = 20mΩ.

After POR, the ACProchot# register is reset to 0x0C00H. The ACProchot# register can be read back to verify its content.

If the adapter current exceeds the ACProchot# register setting, PROCHOT# signal will assert after the debounce time programmed by the Control2 register Bit<10:9> and latch on for a minimum time programmed by Control2 register Bit<8:6>.

TABLE 9. ACProchot# REGISTER 0x47H (20mΩ SENSING RESISTOR, 128mA STEP, x18 GAIN)

BIT	DESCRIPTION
<6:0>	Not used
<7>	0 = Add 0mA of ACProchot# threshold. 1 = Add 128mA of ACProchot# threshold.
<8>	0 = Add 0mA of ACProchot# threshold. 1 = Add 256mA of ACProchot# threshold.
<9>	0 = Add 0mA of ACProchot# threshold. 1 = Add 512mA of ACProchot# threshold.
<10>	0 = Add 0mA of ACProchot# threshold. 1 = Add 1024mA of ACProchot# threshold.
<11>	0 = Add 0mA of ACProchot# threshold. 1 = Add 2048mA of ACProchot# threshold.
<12>	0 = Add 0mA of ACProchot# threshold. 1 = Add 4096mA of ACProchot# threshold.
<15:13>	Not used
Maximum	<12:7> = 110010, 6400mA

Setting PROCHOT# Threshold for Battery Over Discharging Current Condition

To set the PROCHOT# signal assertion threshold for battery over discharging current condition, write a 16-bit DCProchot# command (0x48H or 0b01001000) using the Write-word protocol shown in Figure 24 and the data format shown in Table 10. By using the recommended current sense resistor values, the register's LSB always translates to 1mA of adapter current. The DCProchot# register accepts any current command, however, only the valid register bits will be written to the register and the maximum value is clamped at 12.8A for R_{S2} = 10mΩ.

After POR, the DCProchot# register is reset to 0x1000H. The DCProchot# register can be read back to verify its content.

If the battery discharging current exceeds the DCProchot# register setting, the PROCHOT# signal will assert after the debounce time programmed by the Control2 register Bit<10:9> and latch on for a minimum time programmed by Control2 register Bit<8:6>.

In battery only and Low Power mode, the DCProchot# threshold is set by Control0 register Bit<4:3>.

In battery only mode, DCProchot# function works only when PSYS is enabled, since enabling PSYS will activate the internal comparator reference. The Information register Bit<15> indicates if the internal comparator reference is active or not. When adapter is present, the internal comparator reference is always active.

TABLE 10. DCPROCHOT# REGISTER 0x48H (10mΩ SENSING RESISTOR, 256mA STEP, x18 GAIN)

BIT	DESCRIPTION
<7:0>	Not used
<8>	0 = Add 0mA of DCProchot# threshold. 1 = Add 256mA of DCProchot# threshold.
<9>	0 = Add 0mA of DCProchot# threshold. 1 = Add 512mA of DCProchot# threshold.
<10>	0 = Add 0mA of DCProchot# threshold. 1 = Add 1024mA of DCProchot# threshold.
<11>	0 = Add 0mA of DCProchot# threshold. 1 = Add 2048mA of DCProchot# threshold.
<12>	0 = Add 0mA of DCProchot# threshold. 1 = Add 4096mA of DCProchot# threshold.
<13>	0 = Add 0mA of DCProchot# threshold. 1 = Add 8192mA of DCProchot# threshold.
<15:14>	Not used
Maximum	<13:8> = 110010, 12800mA

Setting PROCHOT# Debounce Time and Duration Time

Control2 register Bit<10:9> configures the PROCHOT# signal debounce time before its assertion for ACProchot# and DCProchot#. The low system voltage Prochot# has a fixed debounce time of 10µs.

Control2 register Bit<8:6> configures the minimum duration of Prochot# signal once asserted.

Control Registers

Control0, Control1 and Control2 registers configure the operation of the ISL9237. To change certain functions or options after POR, write an 8-bit control command to Control0 register (0x39H or 0b00111001) or a 16-bit control command to Control1 register (0x3CH or 0b00111100) or Control2 register (0x3DH or 0b00111101) using the Write-word protocol shown in Figure 24 and the data format shown in Tables 11, 12 and 13, respectively.

TABLE 11. CONTROL0 REGISTER 0x39H

<table>
<tr><th>BIT</th><th>BIT NAME</th><th>DESCRIPTION</th></tr>
<tr><td><15:8></td><td></td><td>Not used</td></tr>
<tr><td><7></td><td>SMBus Timeout</td><td>The ISL9237 includes a timer to insure the SMBus master is active and to prevent overcharging the battery. If the adapter is present and if the ISL9237 does not receive a write to the MaxChargeVoltage or ChargeCurrentLimit register within 175s, ISL9237 will terminate charging. If a timeout occurs, writing the MaxChargeVoltage or ChargeCurrentLimit register will re-enable charging.
0 = Enable the SMBus timeout function (default).
1 = Disable the SMBus timeout function.</td></tr>
<tr><td><6:5></td><td>High-Side FET Short Detection Threshold</td><td>Bit<6:5> configures the high-side FET short detection PHASE node voltage threshold during low-side FET turning on.
00 = 400mV (default)
01 = 500mV
10 = 600mV
11 = 800mV</td></tr>
<tr><td><4:3></td><td>DCProchot# Threshold in Battery Only Low Power Mode</td><td>Bit<4:3> only configures the battery discharging current DCProchot# threshold in battery only Low Power mode indicated by the Information register 0x3A Bit<15>. If PSYS is enabled, battery discharge current DCProchot# threshold is set by the DCProchot# register 0x48 setting.
<table>
<tr><th>BIT<4:3></th><th>R_{S2} = 10mΩ (A)</th><th>R_{S2} = 20mΩ (A)</th><th>R_{S2} = 5mΩ (A)</th></tr>
<tr><td>00</td><td>12 (Default)</td><td>6</td><td>24</td></tr>
<tr><td>01</td><td>10</td><td>5</td><td>20</td></tr>
<tr><td>10</td><td>8</td><td>4</td><td>16</td></tr>
<tr><td>11</td><td>6</td><td>3</td><td>12</td></tr>
</table></td></tr>
<tr><td><2></td><td>Input Voltage Regulation Loop</td><td>Bit<2> disables or enables the input voltage regulation loop.
0 = Enable (default)
1 = Disable</td></tr>
<tr><td><1:0></td><td>Input Voltage Regulation Reference</td><td>Bit<1:0> configures the input voltage loop regulation reference.
00 = 3.9V (default)
01 = 4.2V
10 = 4.5V
11 = 4.8V</td></tr>
</table>

TABLE 12. CONTROL1 REGISTER 0x3CH

BIT	BIT NAME	DESCRIPTION
<15:14>	General Purpose Comparator Assertion Debounce Time	Bit<15:14> configures the general purpose comparator assertion debounce time. 00 = 2µs (default) 01 = 12µs 10 = 2ms 11 = 5s
13	Exit Learn Mode Option	Bit<12> provides the option to exit Learn mode when battery voltage is lower than MinSystemVoltage register setting. 0 = Stay in Learn mode even if V_{BAT} < MinSystemVoltage register setting (default) 1 = Exit Learn mode if V_{BAT} < MinSystemVoltage register setting
12	Learn Mode	Bit<13> enables or disables the Battery Learn mode. 0 = Disable (default) 1 = Enable To enter Learn mode, BATGONE pin needs to be low, i.e., battery must be present.
11	OTG Function	Bit<11> enables or disables OTG function. 0 = Disable (default) 1 = Enable
10	Audio Filter	Bit<10> enables or disables the audio filter function. 0 = Disable (default) 1 = Enable

TABLE 12. CONTROL1 REGISTER 0x3CH

BIT	BIT NAME	DESCRIPTION
<9:7>	Switching Frequency	Bit<9:7> configures the switching frequency and overrides the switching frequency set by PROG pin. 000 = Switching frequency set by PROG pin (default) 001 = 913kHz 010 = 839kHz 011 = 777kHz 100 = 723kHz 101 = 676kHz 110 = 635kHz 111 = 599kHz To keep the switching frequency set by PROG pin resistor, leave Bit<9:7> as it is or write code 000, which sets the same frequency as the PROG pin resistor.
6	Turbo	Bit<6> enables or disables Turbo mode. When the turbo function is enabled, BGATE FET turns on in Turbo mode. Refer to Table 19 on page 30 for BGATE ON/OFF truth table. 0 = Enable (default) 1 = Disable
5	AMON/BMON Function	Bit<5> enables or disables the current monitor function AMON and BMON. 0 = Enable AMON/BMON (default) 1 = Disable AMON/BMON Bit<5> is only valid in battery only mode. When adapter is present, AMON/BMON is automatically enabled and Bit<5> becomes invalid.
4	AMON or BMON	Bit<4> selects AMON or BMON as the output of AMON/BMON pin. 0 = AMON (default) 1 = BMON
3	PSYS	Bit<3> enables or disable system power monitor PSYS function. 0 = Disable (default) 1 = Enable
2	VSYS	Bit<2> enables or disables the buck-boost charger switching VSYS output. When disabled, ISL9237 stops switching and forces BGATE FET on. 0 = Enable (default) 1 = Disable
<1:0>	Low_VSYS_Prochot# Reference	Bit<1:0> configures the Low_VSYS_Prochot# assertion threshold. 00 = 6.0V (default) 01 = 6.3V 10 = 6.6V 11 = 6.9V For 1-cell configuration, the Low_VSYS_Prochot# assertion threshold is fixed 2.4V.

TABLE 13. CONTROL2 REGISTER 0x3DH

BIT	BIT NAME	DESCRIPTION
<15:14>	Trickle Charging Current	Bit<15:14> configures the charging current in trickle charging mode. 00 = 256mA (default) 01 = 128mA 10 = 64mA 11 = 512mA
13	OTG Function Enable Debounce Time	Bit<13> configures the OTG function debounce time from when ISL9237 receives the OTG enable command. 0 = 1.3s (default) 1 = 150ms
12	Two-Level Adapter Current Limit Function	Bit<12> enables or disables the two-level adapter current limit function. 0 = Disable (default) 1 = Enable

TABLE 13. CONTROL2 REGISTER 0x3DH (Continued)

BIT	BIT NAME	DESCRIPTION
11	Adapter Insertion to ASGATE Turning On Debounce	Bit<11> configures the debounce time from adapter insertion to ASGATE turning on. 0 = 1.3s (default) 1 = 150ms After VDD POR, for the first time adapter is plugged in, the ASGATE turn-on delay is always 150ms, regardless of the Bit<11> setting. This bit only sets the ASGATE turn-on delay after ASGATE turns off at least one time when VDD is above the POR value and Bit<11> default is 0 for 1.3s.
<10:9>	Prochot# Debounce	Bit<10:9> configures the Prochot# debounce time before its assertion for ACProchot# and DCProchot#. 00: 10µs (default) 01: 100µs 10: 500µs 11: 1ms The Low_VSYS_Prochot# has fixed 10µs debounce time.
<8:6>	Prochot# Duration	Bit<8:6> configures the minimum duration of Prochot# signal once asserted. 000 = 10ms (default) 001 = 20ms 010 = 15ms 011 = 5ms 100 = 1ms 101 = 500µs 110 = 100µs 111 = 0s
5	ASGATE in OTG Mode	Bit<5> turns on or off the ASGATE FET in OTG mode. 0 = Turn ON ASGATE in OTG mode (default) 1 = Turn OFF ASGATE in OTG mode
4	CMIN Reference	Bit<4> configures the general purpose comparator reference voltage. 0 = 1.2V (default) 1 = 2V
3	General Purpose Comparator	Bit<3> enables or disabled the general purpose comparator. 0 = Enable (default) 1 = Disable
2	CMOUT Polarity	Bit<2> configures the general purpose comparator output polarity once asserted. The comparator reference voltage is connected at the inverting input node. 0 = CMOUT is high when CMIN is higher than reference (default) 1 = CMOUT is low when CMIN is higher than reference
1	WOCP Function	Bit<1> enables or disables the WOC (Way Overcurrent) fault protection function. 0 = Enable WOCP (default) 1 = Disable WOCP
0	PSYS Gain	Bit<0> configures the system power monitor PSYS output gain. 0 = 1.44µA/W (default) 1 = 0.36µA/W

OTGVoltage Register

To set the OTG mode output regulation voltage, write a 16-bit OTGVoltage command (0x49H or 0b01001001) using the Write-word protocol shown in Figure 24 on page 16 and the data format as shown in Table 14.

The OTGVoltage register accepts any voltage command, however, only the valid register bits will be written to the register, and the maximum value is clamped at 5.376V and the minimum value is clamped at 4.864V.

TABLE 14. OTGVOLTAGE REGISTER 0x49H

BIT	DESCRIPTION
<6:0>	Not used
<7>	0 = Add 0mV of OTG voltage 1 = Add 128mV of OTG voltage
<8>	0 = Add 0mV of OTG voltage 1 = Add 256mV of OTG voltage
<9>	0 = Add 0mV of OTG voltage 1 = Add 512mV of OTG voltage
<10>	0 = Add 0mV of OTG voltage 1 = Add 1024mV of OTG voltage

TABLE 14. OTGVOLTAGE REGISTER 0x49H (Continued)

BIT	DESCRIPTION
<11>	0 = Add 0mV of OTG voltage 1 = Add 2048mV of OTG voltage
<12>	0 = Add 0mV of OTG voltage 1 = Add 4096mV of OTG voltage
<15:13>	Not used
Range	<12:7> = 101010, maximum 5.376V <12:7> = 100110, minimum 4.864V

OTGCurrent Register

To set the OTG mode output current limit threshold, write a 16-bit OTGVoltage command (0x4AH or 0b01001010) using the Write-word protocol shown in Figure 24 on page 16 and the data format as shown in Table 15.

The OTGCurrent register accepts any current command, however, only the valid register bits will be written to the register, and the maximum value is clamped at 4096mA for R_{s1} = 20mΩ.

TABLE 15. OTGCURRENT 0x4AH

BIT	DESCRIPTION
<6:0>	Not used
<7>	0 = Add 0mA of OTG current 1 = Add 128mA of OTG current
<8>	0 = Add 0mA of OTG current 1 = Add 256mA of OTG current
<9>	0 = Add 0mV of OTG current 1 = Add 512mA of OTG current
<10>	0 = Add 0mV of OTG current 1 = Add 1024mA of OTG current
<11>	0 = Add 0mV of OTG current 1 = Add 2048mA of OTG current
<12>	0 = Add 0mV of OTG current 1 = Add 4096mA of OTG current
<15:13>	Not used
Maximum	<12:7> = 100000, 4096mA

Information Register

The Information Register contains SMBus readable information about manufacturing and operating modes. Table 16 identifies the bit locations of the information available.

TABLE 16. INFORMATION REGISTER 0x3AH

BIT	DESCRIPTION
<3:0>	Bit<3:0> indicates the configuration set by PROG pin resistor. In battery only mode, Bit<3:0> shows the PROG pin programmed configuration only after PROG pin resistor is read by enabling PSYS. <3:0> = Cell number, Default f_{SW}, default AdapterCurrentLimit1 register setting. 0000 = 3-cell, 1MHz, 1.5A, 0001 = 3-cell, 1MHz, 0.476A, 0010 = 3-cell, 723kHz, 1.5A 0011 = 3-cell, 723kHz, 0.476A 0100 = 3-cell, 723kHz, 0.1A 0101 = 2-cell, 1MHz, 1.5A 0110 = 2-cell, 1MHz, 0.476A 0111 = 2-cell, 723kHz, 1.5A 1000 = 2-cell, 723kHz, 0.476A 1001 = 2-cell, 723kHz, 0.1A 1010 = 1-cell, 1MHz, 0.1A 1011 = 1-cell, 1MHz, 1.5A 1100 = 1-cell, 1MHz, 0.476A 1101 = 1-cell, 723kHz, 1.5A 1110 = 1-cell, 723kHz, 0.476A 1111 = 1-cell, 723kHz, 0.1A
<4>	Bit<4> indicates if the trickle charging mode is active or not. 0 = Trickle charging mode is not active 1 = Trickle charging mode is active
<6:5>	Bit<6:5> indicates the ISL9237 operation mode. 00 = Buck mode 01 = Boost mode 10 = Buck-boost mode 11 = OTG mode
<9:7>	Bit<9:7> indicates the ISL9237 state machine status 000 = OFF 001 = BATTERY 010 = ADAPTER 011 = ACOK 100 = VSYS 101 = CHARGE 110 = ENOTG 111 = OTG
<10>	Bit<10> indicates if the Low_VSYS_Prochot# is tripped or not. 0 = Low_VSYS Prochot# is not tripped 1 = Low_VSYS Prochot# is tripped
<11>	Bit<11> indicates if the battery discharging Prochot# signal DCProchot# is tripped or not. 0 = DCProchot# is not tripped 1 = DCProchot# is tripped