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DATASHEET

Buck-Boost Narrow VDC Battery Charger with SMBus Interface and USB OTG

ISL9238, ISL9238A

The ISL9238 and ISL9238A are buck-boost Narrow Output Voltage DC (NVDC) chargers. The ISL9238 and ISL9238A provide the NVDC charging function, system bus regulation and protection features for tablet, ultrabook, notebook, power bank and any USB-C interface platform. Intersil's advanced R3™ Technology is used to provide high light-load efficiency and fast transient response.

In Charging mode the ISL9238 and ISL9238A takes input power from a wide range of DC power sources (conventional AC/DC charger adapters, USB PD ports, travel adapters, etc.) and safely charges battery packs with up to 4-series cell Li-ion batteries.

As a NVDC topology charger, it also regulates the system output to a narrow DC range for stable system bus voltage. The system power can be provided from the adapter, battery or a combination of both. The ISL9238 and ISL9238A can operate with only a battery, only an adapter or both connected. For Intel IMVP8 compliant systems the ISL9238 and ISL9238A includes PSYS (System power monitor) functionality, which provides an analog signal representing total platform power. The PSYS output will connect to a wide range of Intersil IMVP8 core regulators to provide an IMVP8 compliant power domain function.

The ISL9238 and ISL9238A support reverse buck, boost, or buck-boost operation to input port from 2- to 4-cell batteries.

The ISL9238 and ISL9238A have serial communication via SMBus/I^2C that allows programming of many critical parameters to deliver a customized solution.

The ISL9238A is exactly same as ISL9238, but it has different SMBus addresses for customers who use two battery chargers in one system.

Features

- Buck-boost NVDC charger for 1-, 2-, 3-, or 4-cell Li-ion batteries
- Input voltage range 3.2V to 23.4V (no dead zone)
- System output voltage 2.4V to 18.304V
- Autonomous charging option (automatic end of charging)
- System power monitor PSYS output, IMVP compliant
- Up to 1MHz switching frequency
- Adapter current and battery current monitor (AMON/BMON)
- PROCHOT# open-drain output, IMVP compliant
- Allows trickle charging of depleted battery
- Ideal diode control in Turbo mode
- Reverse buck, boost and buck-boost operation from battery
- Two-level adapter current limit available
- Battery Ship mode option
- SMBus and auto-increment I^2C compatible
- Package 4x4 32 Ld TQFN

Applications

- 1 to 4-cell tablet, ultrabook, notebook, power bank, and any USB-C interface portable device requiring batteries

Related Literature

- For a full list of related documents please visit our web pages
  - ISL9238, ISL9238A product pages

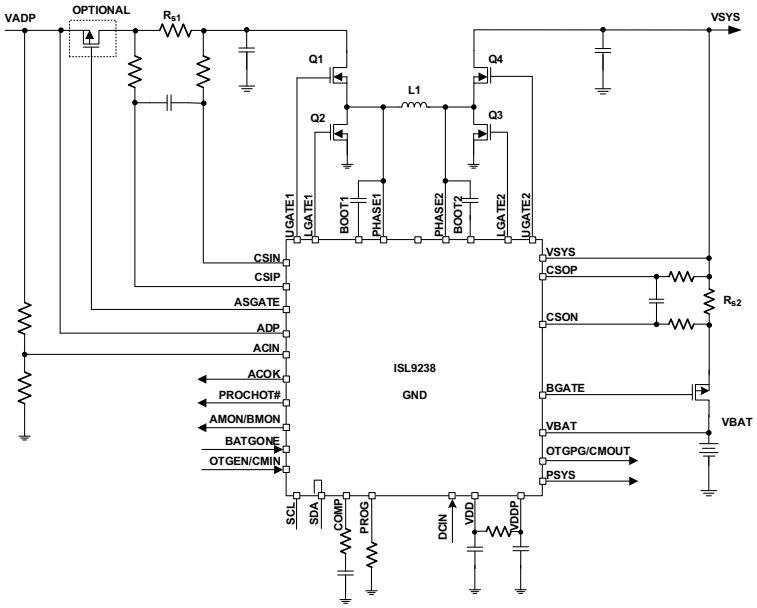

FIGURE 1. TYPICAL APPLICATION CIRCUIT

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Ordering Information

PART NUMBER (Notes 4, 5)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL9238HRTZ (Note 1)	9238H	-10 to +100	32 Ld 4x4 TQFN	L32.4x4D
ISL9238IRTZ (Note 2)	9238I	-40 to +100	32 Ld 4x4 TQFN	L32.4x4D
ISL9238AHRTZ (Note 3)	9238AH	-10 to +100	32 Ld 4x4 TQFN	L32.4x4D
ISL9238EVAL1Z	Evaluation Board			

NOTES:

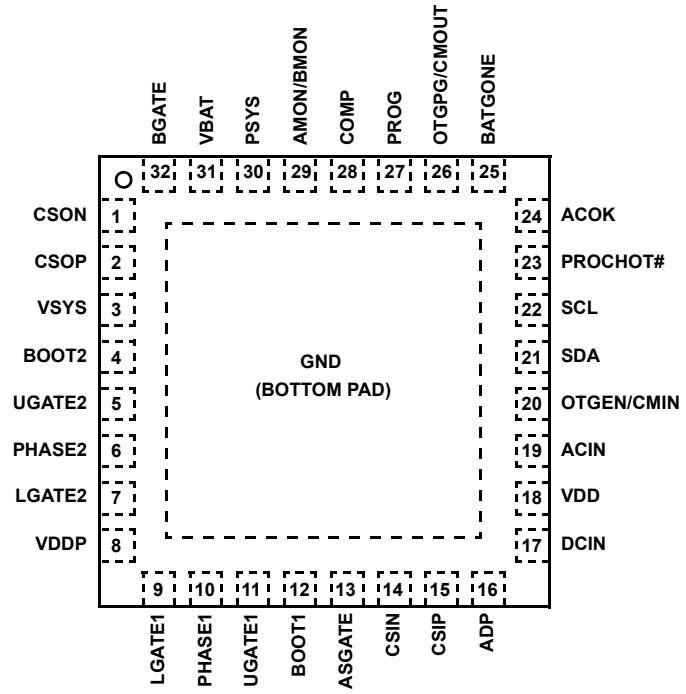
1. Add “-T” suffix for 6k unit, “-TK” suffix for 1k unit, or “-T7A” suffix for 250 unit tape and reel options. Refer to TB347 for details on reel specifications.
2. Add “-T” suffix for 6k unit tape and reel option. Refer to TB347 for details on reel specifications.
3. Add “-T” suffix for 6k unit or “-TK” suffix for 1k unit tape and reel options. Refer to TB347 for details on reel specifications.
4. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
5. For Moisture Sensitivity Level (MSL), see product information page for ISL9238, ISL9238A. For more information on MSL, see tech brief TB363.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	I^2C READ ADDRESS	I^2C WRITE ADDRESS
ISL9238	0b00010011 (0x13H)	0b00010010 (0x12H)
ISL9238A	0b00011011 (0x1BH)	0b00011010 (0x1AH)

Pin Configuration

ISL9238, ISL9238A
(32 LD 4x4 TQFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
BOTTOM PAD	GND	Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pin. It should also be used as the thermal pad for heat dissipation.
1	CSON	Battery current sense “–” input. Connect to battery current resistor negative input. Place a 0.1µF ceramic capacitor between CSOP to CSON to provide Differential mode filtering.
2	CSOP	Battery current sense “+” input. Connect to battery current resistor positive input. Place a 0.1µF ceramic capacitor between CSOP to CSON to provide Differential mode filtering.
3	VSYS	Provides feedback voltage for MaxSystemVoltage regulation.
4	BOOT2	High-side MOSFET Q4 gate driver supply. Connect an MLCC capacitor across the BOOT2 and PHASE2 pins. The boot capacitor is charged through an internal boot diode connected from the VDDP to BOOT2 pins when the PHASE2 pin drops below VDDP minus the voltage drop across the internal boot diode.
5	UGATE2	High-side MOSFET Q4 gate drive.
6	PHASE2	Current return path for the high-side MOSFET Q4 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q4 source, the low-side MOSFET Q3 drain and the one terminal of the inductor.
7	LGATE2	Low-side MOSFET Q3 gate drive.
8	VDDP	Power supply for the gate drivers. Connect to VDD pin through a 4.7Ω resistor and connect a 1µF ceramic capacitor to GND.
9	LGATE1	Low-side MOSFET Q2 gate drive.
10	PHASE1	Current return path for the high-side MOSFET Q1 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q1 source, the low-side MOSFET Q2 drain and the input terminal of the inductor.
11	UGATE1	High-side MOSFET Q1 gate drive.
12	BOOT1	High-side MOSFET Q1 gate driver supply. Connect an MLCC capacitor across the BOOT1 and PHASE1 pins. The boot capacitor is charged through an internal boot diode connected from the VDDP to BOOT1 pins when the PHASE1 pin drops below VDDP minus the voltage drop across the internal boot diode.

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
13	ASGATE	Gate drive output to the P-channel adapter FET. The use of ASGATE FETs is optional, if it is not used, leave ASGATE pin floating. When ASGATE turns on, it is clamped 10V below ADP pin voltage.
14	CSIN	Adapter current sense “-” input.
15	CSIP	Adapter current sense “+” input. The modulator also uses this for sensing input voltage in forward mode and output voltage in reverse mode.
16	ADP	Adapter input. Used to sense adapter voltage. When adapter voltage is higher than 3.2V, AGATE is turned on. ADP pin is also one of the two internal low power LDO inputs.
17	DCIN	Input of an internal LDO providing power to the IC. Connect a diode OR from adapter and system outputs. Bypass this pin with an MLCC capacitor.
18	VDD	Output of the internal LDO; provide the bias power for the internal analog and digital circuit. Connect a 1µF ceramic capacitor to GND. If VDD is pulled below 2V more than 1ms, ISL9238 and ISL9238A will reset all the SMBus register values to the default.
19	ACIN	Adapter voltage sense. Use a resistor divider externally to detect adapter voltage. The adapter voltage is valid if the ACIN pin voltage is greater than 0.8V.
20	OTGEN/ CMIN	OTG function enable pin or stand-alone comparator input pin. Pull high to enable OTG function. The OTG function is enabled when the control register is written to select OTG mode and when the battery voltage is above 5.2V. When OTG function is not selected, this pin is the general purpose stand-alone comparator input.
21	SDA	SMBus data I/O. Connect to the data line from the host controller or smart battery. Connect a 10k pull-up resistor according to SMBus specification.
22	SCL	SMBus clock I/O. Connect to the clock line from the host controller or smart battery. Connect a 10k pull-up resistor according to SMBus specification.
23	PROCHOT#	Open-drain output. Pulled low when ACHOT, DCHOT or Low_VSYS is detected. IMVP-8 compliant. SMBus command to pull low with OTGCURRENT, BAGONE, ACOK, and general purpose comparator (refer to Table 15 on page 28).
24	ACOK	Adapter presence indicator output to indicate the adapter is ready.
25	BATGONE	Input pin to the IC. Logic high on this pin indicates the battery has been removed. Logic low on this pin indicates the battery is present. BATGONE pin logic high will force BGATE FET to turn-off in any circumstances.
26	OTGPG/ CMOUT	Open-drain output. OTG function output power-good indicator or the stand-alone comparator output. When OTG function is enabled, low if OTG output voltage is not within regulation window. When OTG function is not used, it is the general purpose comparator output.
27	PROG	A resistor from PROG pin to GND sets the following configurations: 1. Default number of the battery cells in series, 1-, 2-, 3-, or 4-cell. 2. Default switching frequency 733kHz or 1MHz. 3. Default adapter current limit value 0.476A or 1.5A. 4. Autonomous Charging mode enable or disable Refer to Table 23 for programming options.
28	COMP	Error amplifier output. Connect a compensation network externally from COMP to GND.
29	AMON/ BMON	Adapter current, OTG output current, battery charging current, or battery discharging current monitor output. $V_{AMON} = 18x(V_{CSIP}-V_{CSIN})$ for adapter current monitor $V_{OTGCMON} = 18x(V_{CSIN}-V_{CSIP})$ for OTG output current monitor $V_{BMON\_DISCHARGING} = 18x(V_{CSON}-V_{CSOP})$ for battery discharging current monitor $V_{BMON\_CHARGING} = 36x(V_{CSOP}-V_{CSON})$ for battery charging current monitor
30	PSYS	Current source output that indicates the whole platform power consumption. PSYS gain = 1.44µA/W (default) or 0.723µA/W
31	VBAT	Battery voltage sensing. Used for trickle charging detection and Ideal Diode mode control. Connect to >1µF ceramic capacitor from VBAT pin to GND. VBAT pin is also one of the two internal low power LDO inputs.
32	BGATE	Gate drive output to the P-channel FET connecting the system and the battery. This pin can go high to disconnect the battery, low to connect the battery or operate in a Linear mode to regulate trickle charge current during trickle charge. When BGATE turns on, it is clamped 10V below VSYS pin voltage.

Block Diagram

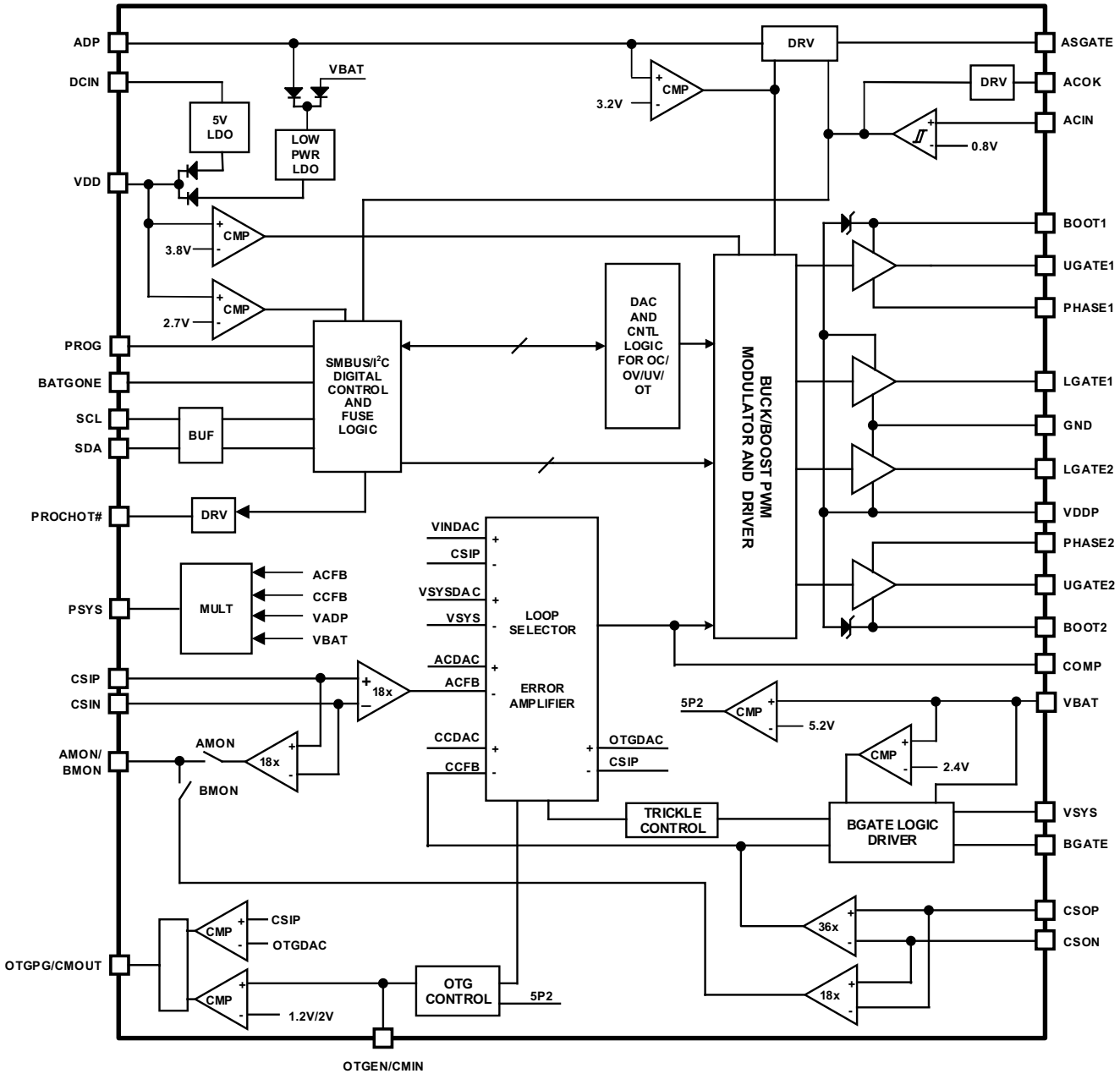


FIGURE 2. BLOCK DIAGRAM

Simplified Application Circuit

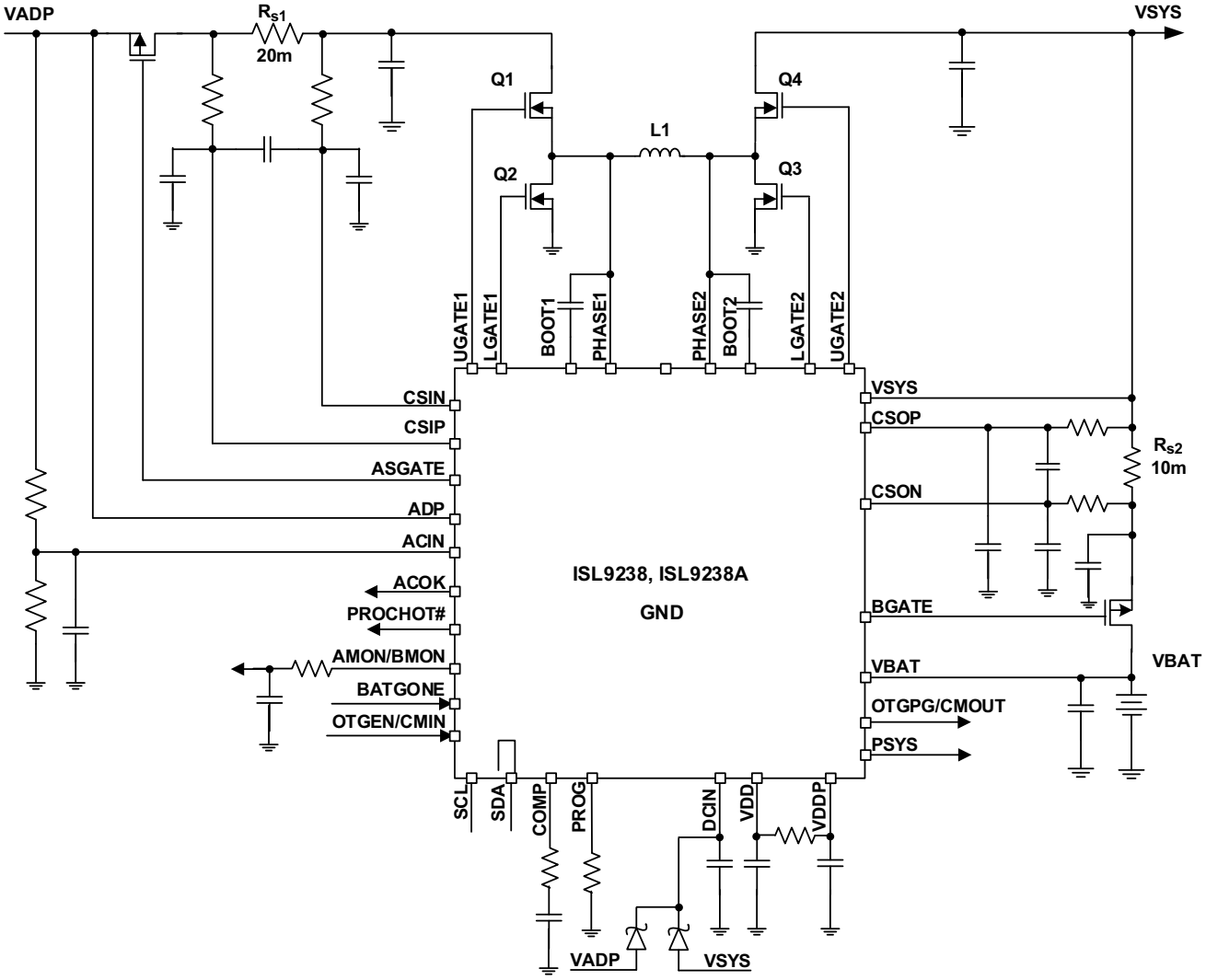


FIGURE 3. SIMPLIFIED APPLICATION DIAGRAM

Absolute Maximum Ratings

CSIP, CSIN, DCIN, ADP, ASGATE . . . . . -0.3V to +28V
PHASE1 . . . . . (GND - 0.3V) to +28V
PHASE1 . . . . . GND-2V(<20ns) to +28V
BOOT1, UGATE1 . . . . . (GND - 0.3V) to +33V
PHASE2 . . . . . (GND - 0.3V) to +24V
PHASE2 . . . . . GND - 2V(<20ns) to +24V
BOOT2, UGATE2 . . . . . (GND - 0.3V) to +29V
LGATE1, LGATE2 . . . . . (GND - 0.3V) to +6.5V
LGATE1, LGATE2 . . . . . GND - 2V(<20ns) to +6.5V
VBAT, VSYS, CSOP, CSON, BGATE . . . . . -0.3V to +24V
VDD, VDDP. . . . . -0.3V to +6.5V
COMP . . . . . -0.3V to +6.5V
AMON/BMON, PSYS. . . . . -0.3V to +6.5V
OTGEN, BATGONE . . . . . -0.3V to +6.5V
ACIN, ACOK, PROCHOT#, OTGPG . . . . . -0.3V to +6.5V
CLK, DAT . . . . . -0.3V to +6.5V
BOOT1-PHASE1, BOOT2-PHASE2. . . . . -0.3V to +6.5V
CSIP-CSIN, CSOP-CSON . . . . . -0.5V to +0.5V
VDD. 70mA
ACIN, SDA, SCL, DCIN, ACOK. 2mA
ESD Rating
  Human Body Model (Tested per JESD22-A114E). 2kV
  Machine Model (Tested per JESD22-A115-A). 200V
  Charged Device Model (Tested per JESD22-C101A) 1kV
Latch-Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JB} (°C/W)
32 Ld TQFN Package (Notes 6, 7)	37	2

Ambient Temperature Range (T_A) . . . . . -10°C to +100°C
Junction Temperature Range (T_J) . . . . . -10°C to +125°C
Storage Temperature Range (T_S) . . . . . -65°C to +175°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature
  HRTZ . . . . . -10°C to +100°C
  IRTZ . . . . . -40°C to +100°C
Junction Temperature . . . . . -10°C to +125°C
Adapter voltage. . . . . +4V to +23V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
7. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating conditions: ADP = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
UVLO/ACOK						
VADP UVLO Rising	VADP_UVLO_r		**3.1**	3.3	**3.5**	V
VADP UVLO Hysteresis	VADP_UVLO_h			600		mV
V_{BAT} UVLO Rising	VBAT_UVLO_r		**2.30**	2.45	**2.65**	V
V_{BAT} UVLO Hysteresis	VBAT_UVLO_h			400		mV
V_{BAT} 5P2V Rising	VBAT_5P2_r		**5.05**	5.20	**5.65**	V
V_{BAT} 5P2V Hysteresis	VBAT_5P2_h			490		mV
VDD 2P7 POR Falling, SMBus and BGATE/BMON Active Threshold	VDD_2P7_f		**2.50**	2.70	**2.9**	V
VDD 2P7 POR Hysteresis	VDD_2P7_h			150		mV
VDD 3P8 POR Rising, Modulator and Gate Driver Active	VDD_3P8_r		**3.6**	3.8	**3.9**	V
VDD 3P8 POR Hysteresis	VDD_3P8_h			150		mV
ACIN Rising	ACIN_r		**0.775**	0.800	**0.825**	V
ACIN Hysteresis	ACIN_h			50		mV

Electrical Specifications Operating conditions: ADP = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
LINEAR REGULATOR						
VDD Output Voltage	VDD	6V < V_{DCIN} < 23V, no load	**4.5**	5.0	**5.5**	V
VDD Dropout Voltage	VDD_dp	30mA, V_{DCIN} = 4V		85		mV
VDD Overcurrent Threshold	VDD_OC	HRTZ	**80**	115	**150**	mA
VDD Overcurrent Threshold		IRTZ	**75**	115	**150**	mA
Battery Current	I_{BAT1}	Battery only, BGATE on, PSYS OFF, BMON OFF, V_{BAT} = 16.8V, DCIN current comes from battery, I_{BAT} = I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{VSYS}		24	**50**	µA
	I_{BAT2}	Battery only, BGATE on, PSYS OFF, BMON ON, V_{BAT} = 16.8V, DCIN current comes from battery, I_{BAT} = I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{VSYS}		74		µA
	I_{BAT3}	Battery only, BGATE on, PSYS ON, BMON OFF, V_{BAT} = 16.8V, DCIN current comes from battery, I_{BAT} = I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{VSYS}		905	**1055**	µA
ADAPTER CURRENT REGULATION, R_{S1} = 20mΩ						
Adapter Current Accuracy		CSIP-CSIN = 80mV		4		A
			-2		**2**	%
		CSIP-CSIN = 40mV		2		A
			-2.5		**2.5**	%
		CSIP-CSIN = 10mV		0.5		A
			-10		**10**	%
Adapter Current PROCHOT# Threshold R_{S1} = 20mΩ	$I_{ADP\_HOT\_TH10}$	ACProchot = 0x1580H (5504mA)		5504		mA
			-1.5		**1.5**	%
		ACProchot = 0x0A80H (2688mA)		2688		mA
			-3.0		**3.0**	%
		ACProchot = 0x0400H (1024mA)		1024		mA
			-6.0		**6.0**	%
SYSTEM VOLTAGE REGULATION						
Maximum System Voltage Accuracy	HRTZ	MaxSystemVoltage for 1-cell (4.2V)	**-0.75**		**0.75**	%
		MaxSystemVoltage for 1-cell (8.4V)	**-0.6**		**0.6**	%
		MaxSystemVoltage for 3-cell and 4-cell (12.6V and 16.8V)	**-0.5**		**0.5**	%
	IRTZ	MaxSystemVoltage for 1-cell (4.2V)	**-0.85**		**0.85**	%
		MaxSystemVoltage for 1-cell (8.4V)	**-0.7**		**0.7**	%
		MaxSystemVoltage for 3-cell and 4-cell (12.6V and 16.8V)	**0.55**		**0.50**	%
Minimum System Voltage Accuracy			**-3**		**3**	%
Input Voltage Regulation Accuracy		4.096V	**3.98**		**4.22**	%

Electrical Specifications Operating conditions: ADP = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
CHARGE CURRENT REGULATION, R_{S2} = 10mΩ (LIMITS APPLY ACROSS TEMPERATURE RANGE OF 0°C TO +85°C)						
Charge Current Accuracy		CSOP-CSON = 60mV		6.03		A
			-2		**2**	%
		CSOP-CSON = 20mV		2.01		A
			-4		**4**	%
		CSOP-CSON = 10mV		1.005		A
			-5		**6**	%
		CSOP-CSON = 5mV		0.501		A
			-10		**12**	%
BGATE CLAMP						
VSYS-VBGATE ON		Charging enabled	**6.80**	8.30	**9.16**	V
VSYS-VBGATE OFF		Charging disabled		0		V
ASGATE CLAMP						
VADP-VASGATE ON				12		V
VSYS-VBGATE OFF				0		V
TRICKLE CHARGING CURRENT REGULATION, R_{S2} = 10mΩ (LIMITS APPLY ACROSS TEMPERATURE RANGE OF 0°C TO +85°C)						
Trickle Charge Current Accuracy		Trickle, options 512mA	**410**	512	**614**	mA
		Trickle, options 256mA	**205**	256	**334**	mA
		Trickle, 128mA	**77**	128	**192**	mA
		Trickle, 64mA	**16**	64	**128**	mA
Fast Charge to Trickle Charge Threshold		V_{SYS} - V_{BGATE}	**4.23**	5.18	**5.97**	V
Trickle Charge to Fast Charge Threshold Hysteresis		V_{SYS} - V_{BGATE}	**55**	130	**210**	mV
Fast Charge to Trickle Charge BGATE Threshold		V_{SYS} > 7V, V_{FB} >> V_{REF}		1.15		V
Trickle Charge to Fast Charge BGATE Threshold Hysteresis		V_{SYS} > 7V, V_{FB} >> V_{REF}		50		mV
IDEAL DIODE MODE						
Entering Ideal Diode Mode VSYS Voltage Threshold		BGATE off, VSYS falling V_{VBAT} - V_{VSYS}	**100**	150	**200**	mV
Exiting Ideal Diode Mode Battery Discharging Current Threshold		R_{S2} = 10mΩ	**110**	200	**290**	mA
Exiting Ideal Diode Mode Battery Charging Current Threshold		R_{S2} = 10mΩ	**50**	130	**200**	mA
BGATE Source		VSYS - BGATE = 2V, charging disabled	**4**	6	**10**	mA
BGATE Sink		BGATE - GND = 2V, charging enabled	**20**	30	**40**	µA
BGATE Sink		BGATE - GND = 2V, in Ideal Diode mode		6		µA
AMON/BMON						
INPUT CURRENT SENSE AMPLIFIER, R_{S1} = 20mΩ						
CSIP/CSIN Input Voltage Range	$V_{CSIP/N}$		**4**		**23**	V/V
AMON Gain				17.97		V/V
AMON Accuracy V_{AMON} = 17.9 * (CSIP - CSIN)		V_{CSIP} - V_{CSIN} = 100mV (5A), CSIP = 5V - 20V	**-2**		**2**	%
		V_{CSIP} - V_{CSIN} = 20mV (1A), CSIP = 5V - 20V	**-5**		**5**	%
		V_{CSIP} - V_{CSIN} = 10mV (0.5A), CSIP = 5V - 20V	**-10**		**10**	%
		V_{CSIP} - V_{CSIN} = 2mV (0.1A), CSIP = 5V - 20V	**-40**		**40**	%

Electrical Specifications Operating conditions: ADP = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
Reverse AMON Gain				17.9		V/V
AMON Accuracy V_{AMON} = 17.9 * (CSIN - CSIP)		V_{CSIN} - V_{CSIP} = 80mV (4A), CSIP = 4V - 22V	**-2.5**		**2.5**	%
		V_{CSIN} - V_{CSIP} = 20mV (1A), CSIP = 4V - 22V	**-6.5**		**4.5**	%
		V_{CSIN} - V_{CSIP} = 10mV (0.5A), CSIP = 4V - 22V	**-12**		**9**	%
		V_{CSIN} - V_{CSIP} = 5.12mV (0.256A), CSIP = 4V - 22V	**-25**		**25**	%
AMON Minimum Output Voltage		V_{CSIP} - V_{CSIN} = 0V			**30**	mV
DISCHARGE CURRENT SENSE AMPLIFIER, R_{S2} = 10mΩ						
BMON Gain (Battery Discharging)				17.78		V/V
BMON Accuracy V_{BMON} = 17.9 * (V_{CSON} - V_{CSOP})		V_{CSON} - V_{CSOP} = 100mV (10A), V_{CSON} = 8V	**-2**		**2**	%
		V_{CSON} - V_{CSOP} = 20mV (2A), V_{CSON} = 8V	**-7.0**	-1.5	**3.0**	%
		V_{CSON} - V_{CSOP} = 10mV (1A), V_{CSON} = 8V	**-10.5**	-2.5	**5.5**	%
		V_{CSON} - V_{CSOP} = 6mV (0.6A), V_{CSON} = 8V	**-17**	-4	**12**	%
BMON Gain (Battery Charging)		Limits apply across temperature range of 0°C to +85°C		35.7		V/V
BMON Accuracy V_{BMON} = 35.7* (V_{CSON} - V_{CSOP})		V_{CSOP} - V_{CSON} = 60mV (6A), V_{CSON} = 8V	**-3**		**3**	%
		V_{CSOP} - V_{CSON} = 40mV (4A), V_{CSON} = 8V	**-4**		**4**	%
		V_{CSOP} - V_{CSON} = 10mV (1A), V_{CSON} = 8V	**-10**		**10**	%
		V_{CSOP} - V_{CSON} = 5mV (0.5A), V_{CSON} = 8V	**-25**		**25**	%
BMON Minimum Output Voltage		V_{CSOP} - V_{CSON} = 0V			**30**	mV
Discharging Current PROCHOT# Threshold, R_{S2} = 10mΩ	$I_{DIS\_HOT\_TH}$	DCProchot = 2.048A	**1.77**	2.08	**2.39**	A
Discharging Current PROCHOT# Threshold, Battery Only, R_{S2} = 10mΩ	$I_{DIS\_HOT\_TH}$	DCProchot = 12A	**10.8**	13.5	**17**	A
		DCProchot = 6A	**5.35**	6.5	**8**	A
AMON/BMON Source Resistance		(Note 9)			**5**	Ω
AMON/BMON Sink Resistance		(Note 9)			**5**	Ω
BATGONE AND OTGEN						
High-Level Input Voltage			**0.9**			V
Low-Level Input Voltage					**0.4**	V
Input Leakage Current		$V_{BATGONE}$ = 3.3V, 5V; V_{OTGEN} = 3.3V, 5V			**1**	µA
PROCHOT#						
PROCHOT# Debounce Time		Prochot# Debounce register Bit<1:0> = 11	**0.85**	1	**1.15**	ms
		Prochot# Debounce register Bit<1:0> = 10	**425**	500	**575**	µs
PROCHOT# Duration Time		Prochot# Duration register Bit<2:0> = 011	**8.5**	10	**11.5**	ms
		Prochot# Duration register Bit<2:0> = 001	**17**	20	**23**	ms
Low VSYS PROCHOT# Trip Threshold	$V_{LOW\_VSYS\_HOT}$	Control1 register Bit<1:0> = 00	**5.8**	6.0	**6.2**	V
		Control1 register Bit<1:0> = 01	**6.1**	6.3	**6.5**	V
		Control1 register Bit<1:0> = 10	**6.4**	6.6	**6.8**	V
		Control1 register Bit<1:0> = 11	**6.7**	6.9	**7.1**	V

Electrical Specifications Operating conditions: ADP = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
PSYS						
PSYS Output Current R_{S1} = 20mΩ R_{S2} = 10mΩ I_{PSYS}= 1.493 x Power + 1.43µA	I_{PSYS} Control3 Bit<9> = 1	V_{CSIP} = 19V, $V_{CSIP-CSIN}$ = 80mV, V_{BAT} = 12V, $V_{CSOP-CSON}$ = 10mV	**-5**		**5**	%
		V_{CSIP} = 19V, $V_{CSIP-CSIN}$ = 80mV, V_{BAT} = 12V, $V_{CSOP-CSON}$ = -10mV	**-5.3**		**5.3**	%
	I_{PSYS} Control3 Bit<9> = 0	V_{CSIP} = 19V, $V_{CSIP-CSIN}$ = 0mV, V_{BAT} = 8.4V, $V_{CSOP-CSON}$ = 20mV	**-7**		**7**	%
		V_{CSIP} = 19V, $V_{CSIP-CSIN}$ = 0mV, V_{BAT} = 4.2V, $V_{CSOP-CSON}$ = 10mV	**-15**		**15**	%
Maximum PSYS Output Voltage	V_{PSYS_MAX}		**4**			V
OTG						
OTG Voltage		OTGVoltage register = 5.12V	**4.95**	5.03	**5.12**	V
OTG Current (5V to 12V)		OTGCurrent register = 512mA	**435**	512	**589**	mA
		OTGCurrent register = 1024mA	**922**	1024	**1126**	mA
		OTGCurrent register = 4096mA	**3975**	4096	**4240**	mA
GENERAL PURPOSE COMPARATOR						
General Purpose Comparator Rising Threshold		Reference = 1.2V	**1.15**	1.2	**1.25**	V
		Reference = 2V	**1.95**	2	**2.05**	V
General Purpose Comparator Hysteresis		Reference = 1.2V	**30**	60	**90**	mV
		Reference = 2V	**30**	60	**90**	mV
PROTECTION						
VSYS Overvoltage Rising Threshold		MaxSystemVoltage register value = 8.4V	**8.95**	9.15	**9.35**	V
VSYS Overvoltage Hysteresis			**250**	400	**550**	mV
Adapter Way Overcurrent Rising Threshold (Note 9)		R_{S1} = 20mΩ	**7.5**	12	**18**	A
Adapter Way Overcurrent Hysteresis			**5**	6.6	**8**	A
Battery Discharge Way Overcurrent Rising Threshold (Note 9)		R_{S2} = 10mΩ	**10**	20	**32**	A
Battery Discharge Way Overcurrent Hysteresis (Note 9)			**7.5**	9	**10.5**	A
Over-Temperature Threshold (Note 9)			**140**	150	**160**	°C
Adapter Overvoltage Rising Threshold			**22.5**	23.4	**24**	V
Adapter Overvoltage Hysteresis			**150**	350	**500**	mV
OTG Undervoltage Falling Threshold		OTG voltage = 5.004V	**3.45**	3.80	**4.25**	V
OTG Overvoltage Rising Threshold		OTG voltage = 5.004V	**5.8**	6.2	**6.6**	V

Electrical Specifications

Operating conditions: ADP = CSIP = CSIN = 5V and 20V, V_{SYS} = V_{BAT} = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
OSCILLATOR						
Oscillator Frequency. Digital Core Only			**0.85**	1	**1.15**	MHz
Digital Debounce Time Accuracy (Note 9)			**-15**		**15**	%
MISCELLANEOUS						
Switching Frequency Accuracy		COMP>1.7V and not in period stretching	**-15**		**15**	%
Battery Learn Mode Auto-Exit Threshold		MinSystemVoltage = 5.376V Control1 register Bit<13> = 1	**5.05**	5.35	**5.7**	V
Battery Learn Mode Auto-Exit Hysteresis (Note 9)			**180**	330	**480**	mV
SMBus						
SDA/SCL Input Low Voltage		3.3V			**0.8**	V
SDA/SCL Input High Voltage		3.3V	**2**			V
SDA/SCL Input Bias Current		3.3V			**1**	µA
SDA, Output Sink Current		SDA = 0.4V, on	**4**			mA
SMBus Frequency	f_{SMB}		**10**		**400**	kHz
GATE DRIVER						
UGATE1 Pull-Up Resistance	$UG1_{RPU}$	100mA source current		800	**1200**	mΩ
UGATE1 Source Current	$UG1_{SRC}$	UGATE1 - PHASE1 = 2.5V	**1.3**	2		A
UGATE1 Pull-Down Resistance	$UG1_{RPD}$	100mA sink current		350	**475**	mΩ
UGATE1 Sink Current	$UG1_{SNK}$	UGATE1 - PHASE1 = 2.5V	**1.9**	2.8		A
LGATE1 Pull-Up Resistance	$LG1_{RPU}$	100mA source current		800	**1200**	mΩ
LGATE1 Source Current	$LG1_{SRC}$	LGATE1 - GND = 2.5V	**1.3**	2		A
LGATE1 Pull-Down Resistance	$LG1_{RPD}$	100mA sink current		300	**450**	mΩ
LGATE1 Sink Current	$LG1_{SNK}$	LGATE1 - GND = 2.5V	**2.3**	3.5		A
LGATE2 Pull-Up Resistance	$LG2_{RPU}$	100mA source current		800	**1200**	mΩ
LGATE2 Source Current	$LG2_{SRC}$	LGATE2 - GND = 2.5V	**1.3**	2		A
LGATE2 Pull-Down Resistance	$LG2_{RPD}$	100mA sink current		300	**450**	mΩ
LGATE2 Sink Current	$LG2_{SNK}$	LGATE2 - GND = 2.5V	**2.3**	3.5		A
UGATE2 Pull-Up Resistance	$UG2_{RPU}$	100mA source current		800	**1200**	mΩ
UGATE2 Source Current	$UG2_{SRC}$	UGATE2 - PHASE2 = 2.5V	**1.3**	2		A
UGATE2 Pull-Down Resistance	$UG2_{RPD}$	100mA sink current		300	**450**	mΩ
UGATE2 Sink Current	$UG2_{SNK}$	UGATE2 - PHASE2 = 2.5V	**2.3**	3.5		A
UGATE1 to LGATE1 Dead Time	$t_{UG1LG1DEAD}$		**10**	20	**40**	ns
LGATE1 to UGATE1 Dead Time	$t_{LG1UG1DEAD}$		**10**	20	**40**	ns
LGATE2 to UGATE2 Dead Time	$t_{LG2UG2DEAD}$		**10**	20	**40**	ns
UGATE2 to LGATE2 Dead Time	$t_{UG2LG2DEAD}$		**10**	20	**40**	ns

SMBUS Timing Specification (Note 9)

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
SMBus Frequency	F_{SMB}		**10**		**400**	kHz
Bus Free Time	t_{BUF}		**4.7**			µs
Start Condition Hold Time from SCL	$t_{HD:STA}$		**4**			µs
Start Condition Set-Up Time from SCL	$t_{SU:STA}$		**4.7**			µs
Stop Condition Set-Up Time from SCL	$t_{SU:STO}$		**4**			µs
SDA Hold Time from SCL	$t_{HD:DAT}$		**300**			ns
SDA Set-Up Time from SCL	$t_{SU:DAT}$		**250**			ns
SCL Low Period	t_{LOW}		**4.7**			µs
SCL High Period	t_{HIGH}		**4**			µs
SMBus Inactivity Timeout		Maximum charging period without a SMBus Write to MaxSystemVoltage or ChargeCurrent register		175		s

NOTES:

8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. Limits established by characterization and are not production tested.

Gate Driver Timing Diagram

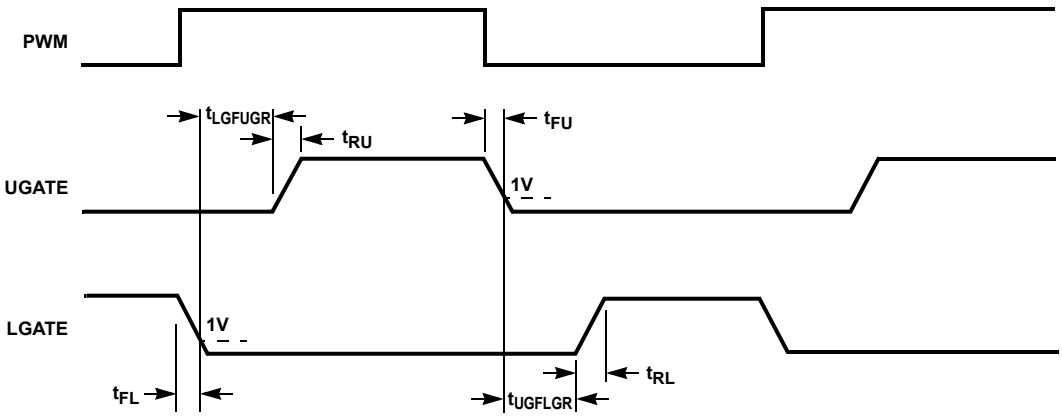


FIGURE 4. GATE DRIVER TIMING DIAGRAM

Typical Performance

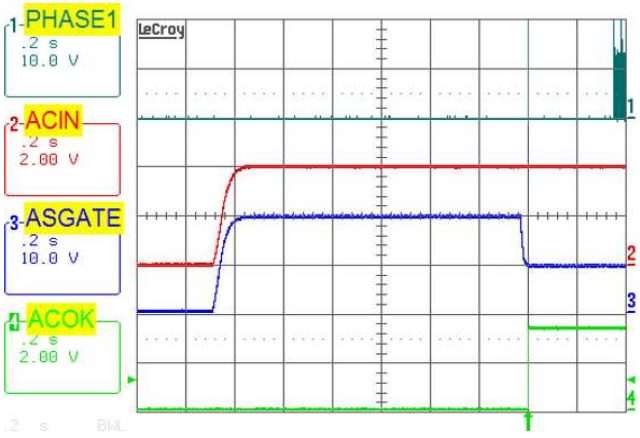


FIGURE 5. ADAPTER INSERTION, V_{ADP} = 20V, V_{BAT} = 11V, CHARGECURRENT = 0A

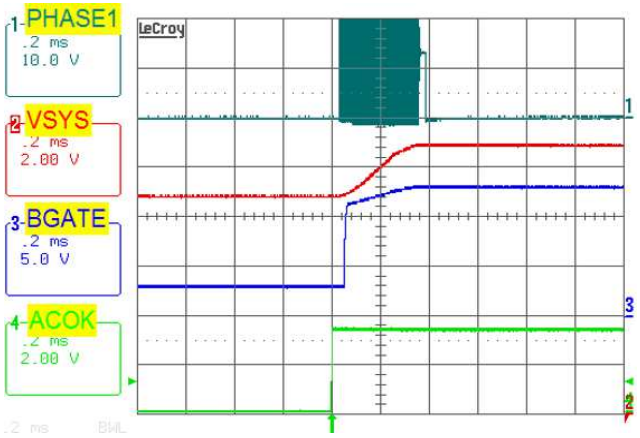


FIGURE 6. ADAPTER INSERTION, V_{ADP} = 20V, V_{BAT} = 11V, CHARGECURRENT = 0A (Figure 5 ZOOM IN)

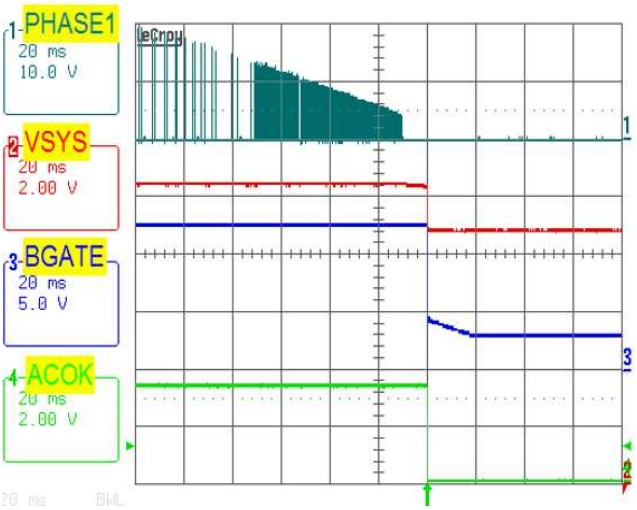


FIGURE 7. ADAPTER REMOVAL, V_{ADP} = 20V, V_{BAT} = 11V, CHARGECURRENT = 0A

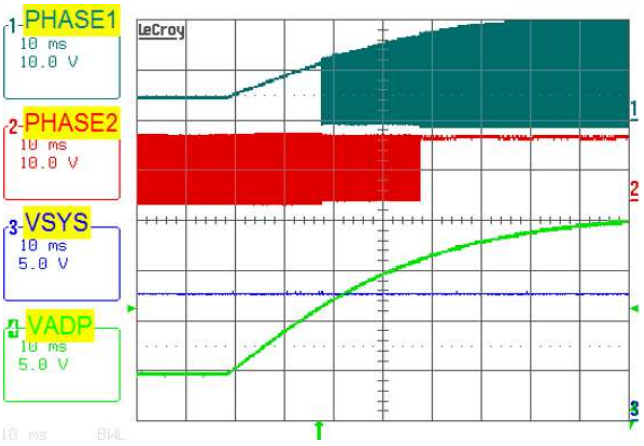


FIGURE 8. ADAPTER VOLTAGE RAMPS UP, BOOST -> BUCK-BOOST -> BUCK OPERATION MODE TRANSITION

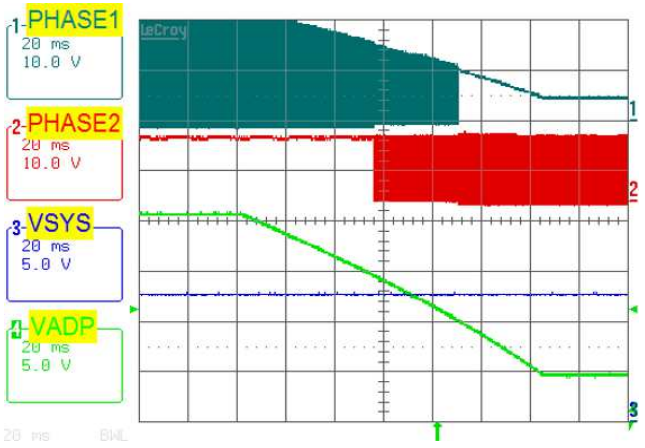


FIGURE 9. ADAPTER VOLTAGE RAMPS DOWN, BUCK -> BUCK-BOOST -> BOOST OPERATION MODE TRANSITION

Typical Performance (Continued)

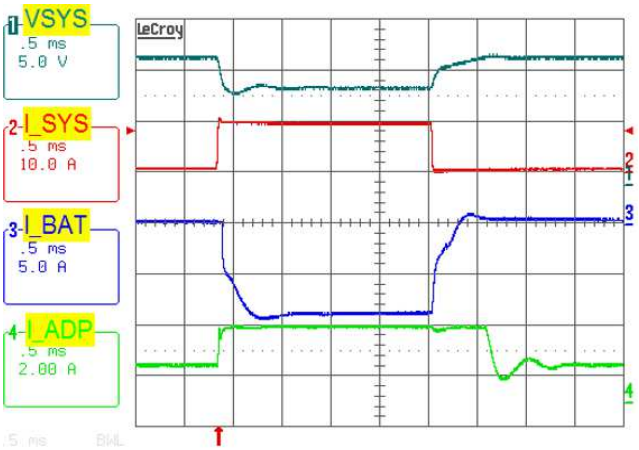


FIGURE 10. BOOST MODE, OUTPUT VOLTAGE LOOP TO ADAPTER CURRENT LOOP TRANSITION. V_{ADP} = 5V, MAXSYSTEMVOLTAGE = 12.576V, V_{BAT} = 11V, SYSTEM LOAD 0.5A TO 10A STEP, ADAPTERCURRENTLIMIT = 3A, CHARGECURRENT = 0A

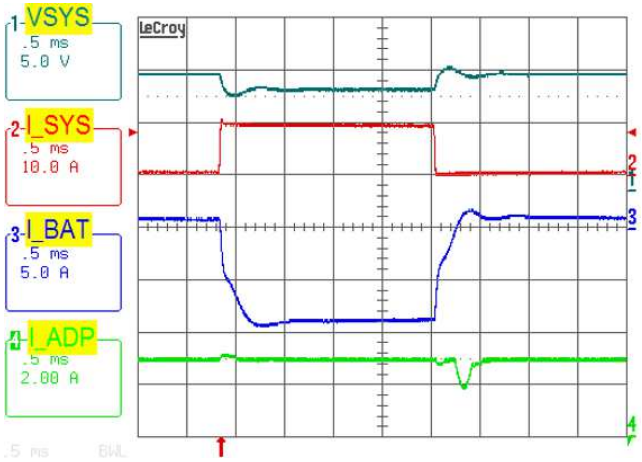


FIGURE 11. BOOST MODE, CHARGING CURRENT LOOP TO ADAPTER CURRENT LOOP TRANSITION. V_{ADP} = 5V, MAXSYSTEMVOLTAGE = 12.5766V, V_{BAT} = 11V, SYSTEM LOAD 0.5A TO 10A STEP, ADAPTERCURRENTLIMIT = 3A, CHARGECURRENT = 1A

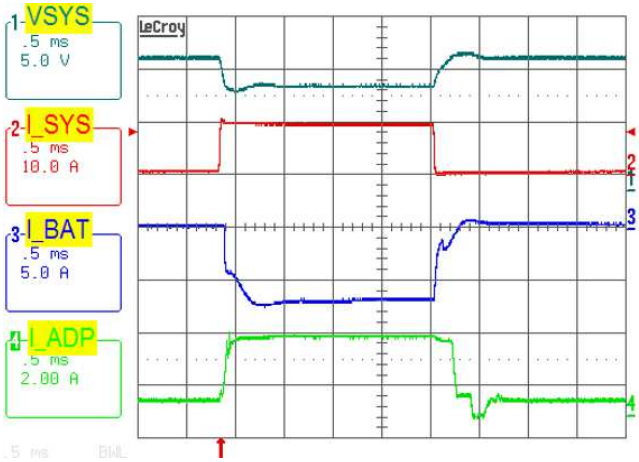


FIGURE 12. BUCK-BOOST MODE, OUTPUT VOLTAGE LOOP TO ADAPTER CURRENT LOOP TRANSITION. V_{ADP} = 12V, MAXSYSTEMVOLTAGE = 12.576V, V_{BAT} = 11V, SYSTEM LOAD 1A TO 10A STEP, ADAPTERCURRENTLIMIT = 3A, CHARGECURRENT = 0A

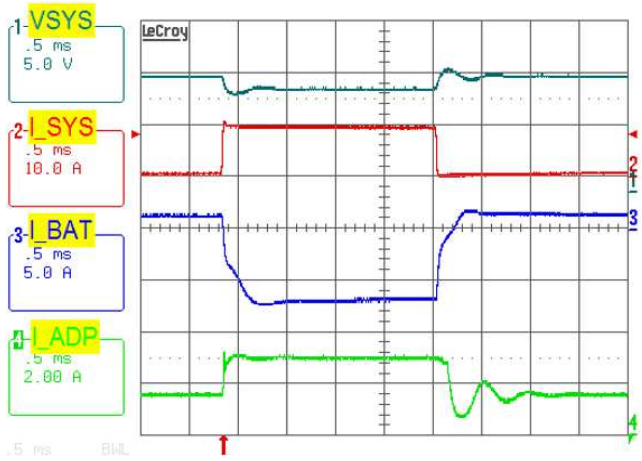


FIGURE 13. BUCK-BOOST MODE, CHARGING CURRENT LOOP TO ADAPTER CURRENT LOOP TRANSITION. V_{ADP} = 12V, MAXSYSTEMVOLTAGE = 12.576V, V_{BAT} = 11V, SYSTEM LOAD 1A TO 10A STEP, ADAPTERCURRENTLIMIT = 3A, CHARGECURRENT = 1A

Typical Performance (Continued)

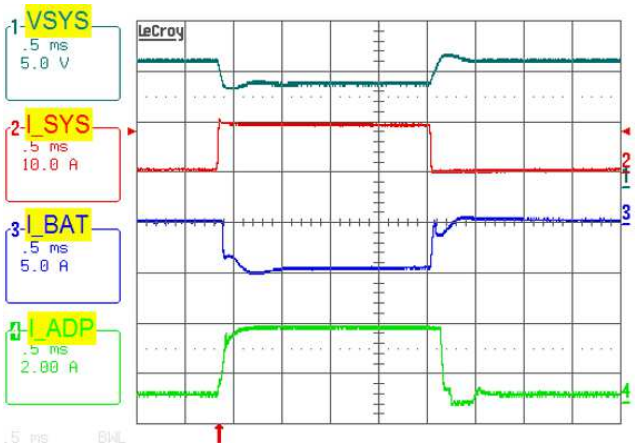


FIGURE 14. BUCK MODE, OUTPUT VOLTAGE LOOP TO ADAPTER CURRENT LOOP TRANSITION. V_{ADP} = 20V, MAXSYSTEMVOLTAGE = 12.576V, V_{BAT} = 11V, SYSTEM LOAD 2A TO 10A STEP, ADAPTERCURRENTLIMIT = 3A, CHARGECURRENT = 0A

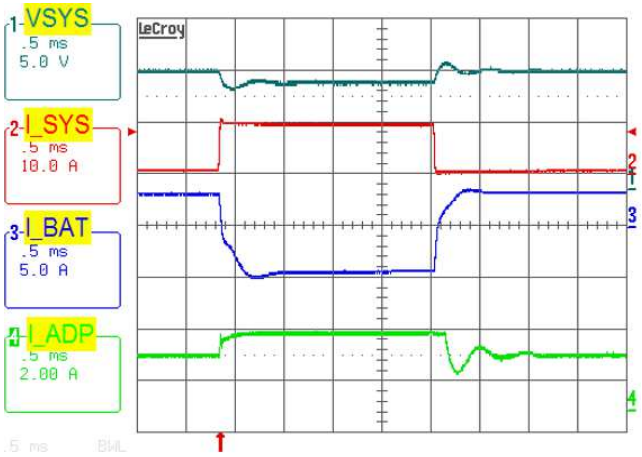


FIGURE 15. BUCK MODE, CHARGING CURRENT LOOP TO ADAPTER CURRENT LOOP TRANSITION. V_{ADP} = 20V, MAXSYSTEMVOLTAGE = 12.576V, V_{BAT} = 11V, SYSTEM LOAD 2A TO 10A STEP, ADAPTERCURRENTLIMIT = 3A, CHARGECURRENT = 3A

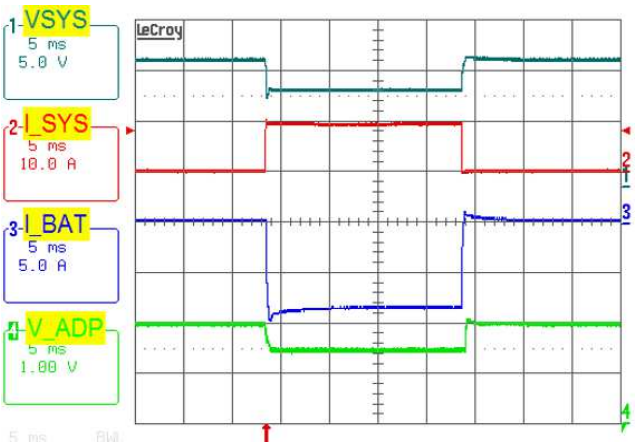


FIGURE 16. BOOST MODE, OUTPUT VOLTAGE LOOP TO INPUT VOLTAGE LOOP TRANSITION. V_{ADP} = 5.004V, MAXSYSTEMVOLTAGE = 12.576V, V_{BAT} = 11V, VINDAC = 4.437V, SYSTEM LOAD 0A TO 10A STEP, CHARGECURRENT = 0A

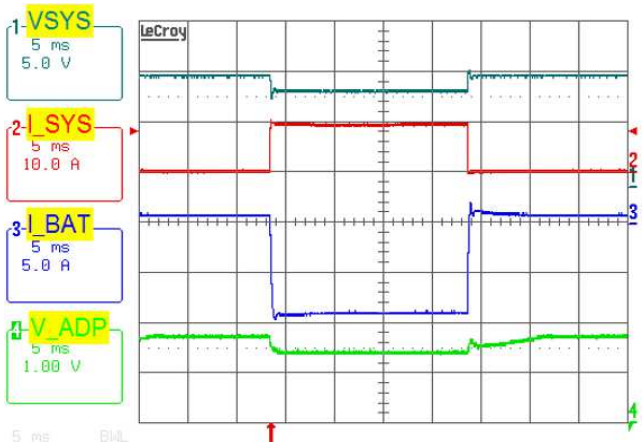


FIGURE 17. BOOST MODE, CHARGING CURRENT LOOP TO INPUT VOLTAGE LOOP TRANSITION. V_{ADP} = 5.004V, MAXSYSTEMVOLTAGE = 12.576V, V_{BAT} = 11V, VINDAC = 4.437V, SYSTEM LOAD 0A TO 10A STEP, CHARGECURRENT = 0.5A

Typical Performance (Continued)

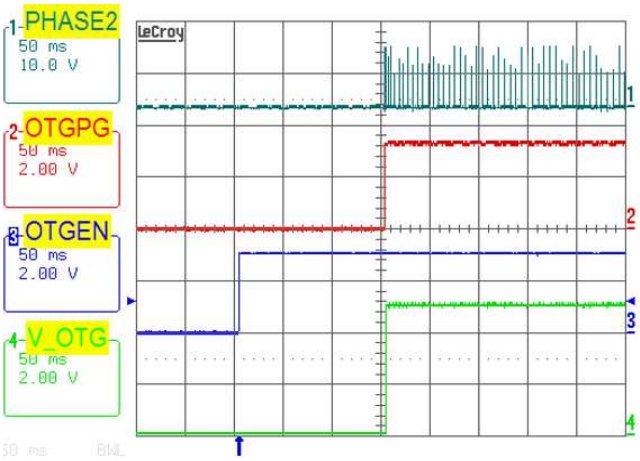


FIGURE 18. OTG MODE ENABLE, OTG ENABLE 150ms DEBOUNCE TIME

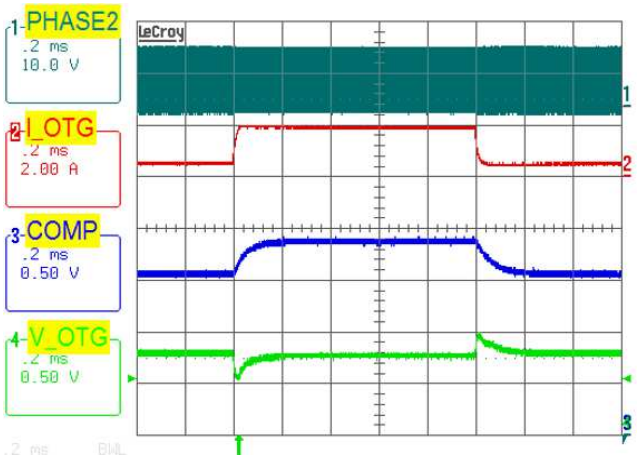


FIGURE 19. OTG MODE 0.5A TO 2A TRANSIENT LOAD, OTG VOLTAGE = 5.12V

General SMBus Architecture

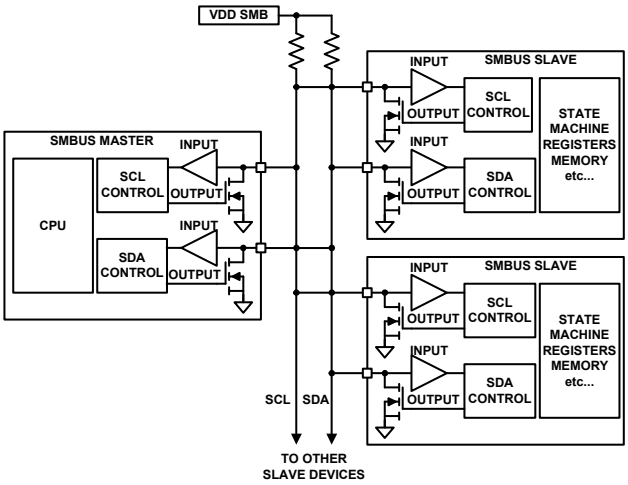


FIGURE 20. GENERAL SMBus ARCHITECTURE

Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. Refer to Figure 21.

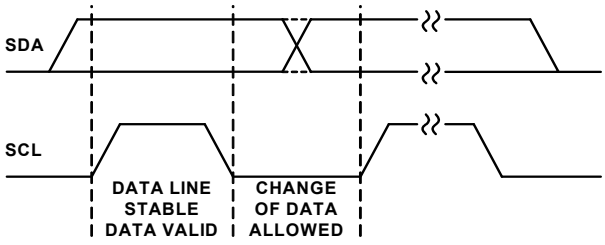


FIGURE 21. DATA VALIDITY

START and STOP Conditions

Figure 22 START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

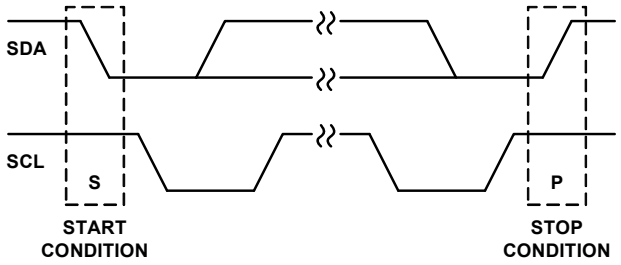


FIGURE 22. START AND STOP WAVEFORMS

Acknowledge

Each address and data transmission uses 9 clock pulses. The ninth pulse is the Acknowledge bit (ACK). After the start condition, the master sends 7 slave address bits and a R/$\overline{W}$ bit during the next 8 clock pulses. During the 9th clock pulse, the device that recognizes its own address holds the data line low to acknowledge (Refer to Figure 23). The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

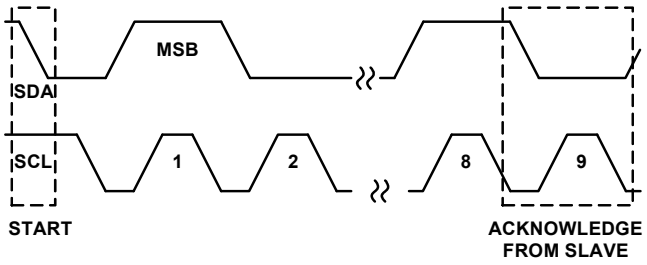


FIGURE 23. ACKNOWLEDGE ON THE SMBus

SMBus Transactions

All transactions start with a control byte sent from the SMBus master device. The control byte begins with a Start condition, followed by 7 bits of slave address (0001001 for the ISL9238 and 0001101 for the ISL9238A) and the R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a WRITE or 1 for a READ. If any slave device on the SMBus bus recognizes its address, it will acknowledge by pulling the Serial Data (SDA) line low for the last clock cycle in the control byte. If no slave exists at that address or it is not ready to communicate, the data line will be one, indicating a not acknowledge condition.

Once the control byte is sent and the ISL9238 and ISL9238A acknowledges it, the second byte sent by the master must be a register address byte such as 0x14 for the ChargeCurrent register. The register address byte tells the ISL9238 and ISL9238A which register the master will write or read. See Table 2 on page 20 for details of the registers. Once the ISL9238 and ISL9238A receives a register address byte, it will respond with an acknowledge.

Byte Format

Every byte put on the SDA line must be 8 bits long and must be followed by an acknowledge bit. Data is transferred with the Most Significant Bit first (MSB) and the least significant bit last (LSB). The LO BYTE data is transferred before the HI BYTE data. For example, when writing 0x41A0, 0xA0 is written first and 0x41 is written second.

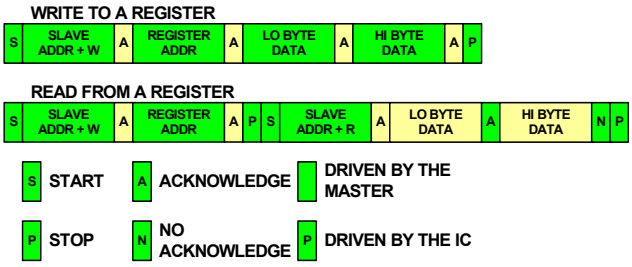


FIGURE 24. SMBus READ AND WRITE PROTOCOL

SMBus and I^{2}C Compatibility

The ISL9238 and ISL9238A SMBus minimum input logic high voltage is 2V, so it is compatible with I^{2}C with higher than 2V pull-up power supply.

The ISL9238 and ISL9238A SMBus registers are 16 bits, so it is compatible with 16 bits I^{2}C or 8 bits I^{2}C with auto-increment capability.

ISL9238 and ISL9238A SMBus Commands

The ISL9238 and ISL9238A receives control inputs from the SMBus interface after Power-On Reset (POR). The serial interface complies with the System Management Bus Specification, which can be downloaded from www.smbus.org. The ISL9238 and ISL9238A uses the SMBus Read-word and Write-word protocols (see Figure 24) to communicate with the host system and a smart battery. The ISL9238 and ISL9238A is an SMBus slave device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001_(ISL9238) /0b0001101_(ISL9238A) as follows:

Read and Write address for ISL9238/ISL9238A is

Read address = 0b00010011 (0X13H)/0b00011011 (0X1BH)

Write address = 0b00010010 (0X12H)/0b00011010 (0X1AH)

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors for SDA and SCL to achieve rise times according to the SMBus specifications.

The illustration in this datasheet is based on current sensing resistors R_{S1} = 20mΩ and R_{S2} = 10mΩ unless otherwise specified.

TABLE 2. REGISTER SUMMARY

REGISTER NAMES	REGISTER ADDRESS	READ/ WRITE	NUMBER OF BITS	DESCRIPTION	DEFAULT
ChargeCurrentLimit	0x14	R/W	11	[12:2]11-bit, LSB size 4mA, total range 6080mA with 10mΩ R_{S2}	0A
MaxSystemVoltage	0x15	R/W	12	[14:3]12-bit, LSB size 8mV, total range 18.304V	4.192V for 1-cell
					8.384V for 2-cell
					12.576V for 3-cell
					16.768V for 4-cell
T1 and T2	0x38	R/W	6	Configure two-level adapter current limit duration	0x000h
Control0	0x39	R/W	16	Configure various charger options	0x0000h
Information1	0x3A	R	16	Indicate various charger status	0x0000h
AdapterCurrentLimit2	0x3B	R/W	11	[12:2]11-bit, LSB size 4mA, total range 6080mA with 20mΩ R_{S1}	1500mA
Control1	0x3C	R/W	16	Configure various charger options	0x0000h
Control2	0x3D	R/W	16	Configure various charger options	0x0000h
MinSystemVoltage	0x3E	R/W	6	[13:8]6-bit, LSB size 256mV, total range 13.824V	2.56V for 1-cell
					5.12V for 2-cell
					7.68V for 3-cell
					10.24V for 4-cell
AdapterCurrentLimit1	0x3F	R/W	11	[12:2]11-bit, LSB size 4mA, total range 6080mA with 20mΩ R_{S1}	Set by PROG pin
ACProchot#	0x47	R/W	6	[12:7] adapter current Prochot# threshold Default 3.072A, 128mA resolution for 20mΩ R_{s1}.	3.072A
DCProchot#	0x48	R/W	6	[13:8] Battery discharging current Prochot# threshold Default 4.096A, 256mA resolution for 10mΩ R_{S2}.	4.096A
OTG Voltage	0x49	R/W	12	[14:3] 12-bit, LSB size 12mV, total range 27.456V OTG mode voltage reference	5.004V
OTG Current	0x4A	R/W	6	[12:7] 6-bit, LSB size 128mAV, total range 4.096A OTG mode maximum current limit	0.512A
V_{IN} Voltage	0x4B	R/W	6	[13:8] 6-bit, LSB size 341.3mV, total range 18.432mV V_{IN} loop voltage reference	4.096V
Control3	0x4C	R/W	16	Configure various charger options	0x0000h
Information2	0x4D	R	16	Indicate various charger status	0x0000h
Control4	0x4E	R/W	8	[7:0] 8-bit, Configure various charger options	0x0000h
Manufacturer ID	0xFE	R	8	Manufacturers ID register – 0x49 - Read only	0x0049h
Device ID	0xFF	R	8	Device ID register - 0x0C- Read only	0x000Ch

Setting Charging Current Limit

To set the charging current limit, write a 16-bit ChargeCurrentLimit command (0x14H or 0b00010100) using the Write-word protocol shown in Figure 24 on page 19 and the data format shown in Table 3 for a 10mΩ R_{S2} or Table 4 for a 5mΩ R_{S2}.

The ISL9238 and ISL9238A limits the charging current by limiting the CSOP-CSON voltage. By using the recommended current sense resistor values R_{S1} = 20mΩ and R_{S2} = 10mΩ, the register's LSB always translates to 4mA of charging current. The ChargeCurrentLimit register accepts any charging current command but only the valid register bits will be written to the register and the maximum values is clamped at 6080mA for R_{S2} = 10mΩ.

After POR, the ChargeCurrentLimit register is reset to 0x0000H. To set the battery charging current value, write a non-zero number to the ChargeCurrentLimit register. The ChargeCurrentLimit register can be read back to verify its content.

Table 24 shows the conditions to enable fast charging according to the ChargeCurrentLimit register setting.

TABLE 3. ChargeCurrentLimit REGISTER 0x14H (11-BIT, 4mA STEP, 10mΩ SENSE RESISTOR, x36)

BIT	DESCRIPTION
<1:0>	Not used
<2>	0 = Add 0mA of charge current limit. 1 = Add 4mA of charge current limit.
<3>	0 = Add 0mA of charge current limit. 1 = Add 8mA of charge current limit.
<4>	0 = Add 0mA of charge current limit. 1 = Add 16mA of charge current limit.
<5>	0 = Add 0mA of charge current limit. 1 = Add 32mA of charge current limit.
<6>	0 = Add 0mA of charge current limit. 1 = Add 64mA of charge current limit.
<7>	0 = Add 0mA of charge current limit. 1 = Add 128mA of charge current limit.
<8>	0 = Add 0mA of charge current limit. 1 = Add 256mA of charge current limit.
<9>	0 = Add 0mA of charge current limit. 1 = Add 512mA of charge current limit.
<10>	0 = Add 0mA of charge current limit. 1 = Add 1024mA of charge current limit.
<11>	0 = Add 0mA of charge current limit. 1 = Add 2048mA of charge current limit.
<12>	0 = Add 0mA of charge current limit. 1 = Add 4096mA of charge current limit.
<13:15>	Not used
Maximum	<12:2> = 10111110000 6080mA

TABLE 4. ChargeCurrentLimit REGISTER 0x14H (11-BIT, 8mA STEP, 5mΩ SENSE RESISTOR, x36)

BIT	DESCRIPTION
<1:0>	Not used
<2>	0 = Add 0mA of charge current limit. 1 = Add 8mA of charge current limit.
<3>	0 = Add 0mA of charge current limit. 1 = Add 16mA of charge current limit.
<4>	0 = Add 0mA of charge current limit. 1 = Add 32mA of charge current limit.
<5>	0 = Add 0mA of charge current limit. 1 = Add 64mA of charge current limit.
<6>	0 = Add 0mA of charge current limit. 1 = Add 128mA of charge current limit.
<7>	0 = Add 0mA of charge current limit. 1 = Add 256mA of charge current limit.
<8>	0 = Add 0mA of charge current limit. 1 = Add 512mA of charge current limit.
<9>	0 = Add 0mA of charge current limit. 1 = Add 1024mA of charge current limit.
<10>	0 = Add 0mA of charge current limit. 1 = Add 2048mA of charge current limit.
<11>	0 = Add 0mA of charge current limit. 1 = Add 4096mA of charge current limit.
<12>	0 = Add 0mA of charge current limit. 1 = Add 8192mA of charge current limit.
<13:15>	Not used
Maximum	<12:2> = 10111110000 12160mA

Setting Adapter Current Limit

To set the adapter current limit, write a 16-bit AdapterCurrentLimit1 command (0x3FH or 0b00111111) and/or AdapterCurrentLimit2 command (0x3BH or 0b00111011) using the Write-word protocol shown in Figure 24 on page 19 and the data format shown in Table 5 on page 22 for a 20mΩ R_{S1} or Table 6 on page 22 for a 10mΩ R_{S1}.

The ISL9238 and ISL9238A limits the adapter current by limiting the CSIP-CSIN voltage. By using the recommended current sense resistor values, the register's LSB always translates to 4mA of adapter current. Any adapter current limit command will be accepted but only the valid register bits will be written to the AdapterCurrentLimit1 and AdapterCurrentLimit2 registers and the maximum values is clamped at 6080mA for R_{S1} = 20mΩ.

After adapter POR, the AdapterCurrentLimit1 register is reset to the value programmed through the PROG pin resistor. The AdapterCurrentLimit2 register is set to its default value of 1.5A or keep the value that is written to it previously if battery is present first. The AdapterCurrentLimit1 and AdapterCurrentLimit2 registers can be read back to verify their content.

To set a second level adapter current limit, write a 16-bit AdapterCurrentLimit2 (0x3BH or 0b00111011) command using the Write-word protocol shown in Figure 24 and the data format as shown in Table 5 for a 20mΩ R_{S1} or Table 6 for a 10mΩ R_{S1}.

The AdapterCurrentLimit2 register has the same specification as the AdapterCurrentLimit1 register. Refer to "Two-Level Adapter Current Limit" on page 36 for detailed operation.

TABLE 5. AdapterCurrentLimit1 REGISTER 0x3FH AND AdapterCurrentLimit2 REGISTER 0x3BH (11-BIT, 4mA STEP, 20mΩ SENSE RESISTOR, x18)

BIT	DESCRIPTION
<1:0>	Not used
<2>	0 = Add 0mA of adapter current limit. 1 = Add 4mA of adapter current limit.
<3>	0 = Add 0mA of adapter current limit. 1 = Add 8mA of adapter current limit.
<4>	0 = Add 0mA of adapter current limit. 1 = Add 16mA of adapter current limit.
<5>	0 = Add 0mA of adapter current limit. 1 = Add 32mA of adapter current limit.
<6>	0 = Add 0mA of adapter current limit. 1 = Add 64mA of adapter current limit.
<7>	0 = Add 0mA of adapter current limit. 1 = Add 128mA of adapter current limit.
<8>	0 = Add 0mA of adapter current limit. 1 = Add 256mA of adapter current limit.
<9>	0 = Add 0mA of adapter current limit. 1 = Add 512mA of adapter current limit.
<10>	0 = Add 0mA of adapter current limit. 1 = Add 1024mA of adapter current limit.
<11>	0 = Add 0mA of adapter current limit. 1 = Add 2048mA of adapter current limit.
<12>	0 = Add 0mA of adapter current limit. 1 = Add 4096mA of adapter current limit.
<13:15>	Not used
Maximum	<12:4> = 10111110000 6080mA

TABLE 6. AdapterCurrentLimit1 REGISTER 0x3FH AND AdapterCurrentLimit2 REGISTER 0x3BH (11-BIT, 8mA STEP, 10mΩ SENSE RESISTOR, x18)

BIT	DESCRIPTION
<1:0>	Not used.
<2>	0 = Add 0mA of adapter current limit. 1 = Add 8mA of adapter current limit.
<3>	0 = Add 0mA of adapter current limit. 1 = Add 16mA of adapter current limit.
<4>	0 = Add 0mA of adapter current limit. 1 = Add 32mA of adapter current limit.
<5>	0 = Add 0mA of adapter current limit. 1 = Add 64mA of adapter current limit.
<6>	0 = Add 0mA of adapter current limit. 1 = Add 128mA of adapter current limit.
<7>	0 = Add 0mA of adapter current limit. 1 = Add 256mA of adapter current limit.
<8>	0 = Add 0mA of adapter current limit. 1 = Add 512mA of adapter current limit.
<9>	0 = Add 0mA of adapter current limit. 1 = Add 1024mA of adapter current limit.
<10>	0 = Add 0mA of adapter current limit. 1 = Add 2048mA of adapter current limit.
<11>	0 = Add 0mA of adapter current limit. 1 = Add 4096mA of adapter current limit.
<12>	0 = Add 0mA of adapter current limit. 1 = Add 8192mA of adapter current limit.
<13:15>	Not used
Maximum	<12:4> = 10111110000 12160mA

Setting Two-Level Adapter Current Limit Duration

For a two-level adapter current limit, write a 16-bit T1 and T2 command (0x38H or 0b00111000) using the Write-word protocol shown in Figure 24 and the data format shown in Table 5 or Table 6 to set the AdapterCurrentLimit1 duration t1. Write a 16-bit T2 command (0x38H or 0b00111000) to set AdapterCurrentLimit2 duration t2. T1 and T2 register accepts any command but only the valid register bits will be written. Refer to "Two-Level Adapter Current Limit" on page 36 for detailed operation.

TABLE 7. T1 AND T2 REGISTER 0x38H

BIT	DESCRIPTION
<2:0> T1	000 = 10ms (default) 001 = 20ms 010 = 15ms 011 = 5ms 100 = 1ms 101 = 0.5ms 110 = 0.1ms 111 = 0ms
<7:3>	Not used
<10:8> T2	000 = 10µs (default) 001 = 100µs 010 = 500µs 011 = 1ms 100 = 300µs 101 = 750µs 110 = 2ms 111 = 10ms
<15:11>	Not used

Setting Maximum Charging Voltage or System Regulating Voltage

To set the maximum charging voltage or the system regulating voltage, write a 16-bit MaxSystemVoltage command (0x15H or 0b00010101) using the Write-word protocol shown in Figure 24 on page 19 and the data format as shown in Table 8.

The maximum system voltage range is 8mV to 18.304V. The MaxSystemVoltage register accepts any voltage command but only the valid register bits will be written to the register and the maximum values is clamped at 18.304V. ISL9238 and ISL9238A accepts 0V command, but register value does not change.

The MaxSystemVoltage register sets the battery full charging voltage limit. The MaxSystemVoltage register setting also is the system bus voltage regulation point when battery is absent or battery is present but is not in Charging mode. See "System Voltage Regulation" on page 37 for details.

The VSYS pin is used to sense the battery voltage for maximum charging voltage regulation. The VSYS pin is also the system bus voltage regulation sense point.

TABLE 8. MaxSystemVoltage REGISTER 0x15H (8mV STEP)

BIT	DESCRIPTION
<2:0>	Not used
<3>	0 = Add 0mV of charge voltage. 1 = Add 8mV of charge voltage.
<4>	0 = Add 0mV of charge voltage. 1 = Add 16mV of charge voltage.
<5>	0 = Add 0mV of charge voltage. 1 = Add 32mV of charge voltage.
<6>	0 = Add 0mV of charge voltage. 1 = Add 64mV of charge voltage.
<7>	0 = Add 0mV of charge voltage. 1 = Add 128mV of charge voltage.
<8>	0 = Add 0mV of charge voltage. 1 = Add 256mV of charge voltage.
<9>	0 = Add 0mV of charge voltage. 1 = Add 512mV of charge voltage.
<10>	0 = Add 0mV of charge voltage. 1 = Add 1024mV of charge voltage.
<11>	0 = Add 0mV of charge voltage. 1 = Add 2046mV of charge voltage.
<12>	0 = Add 0mV of charge voltage. 1 = Add 4096mV of charge voltage.
<13>	0 = Add 0mV of charge voltage. 1 = Add 8192mV of charge voltage.
<14>	0 = Add 0mV of charge voltage. 1 = Add 16384mV of charge voltage.
<15>	Not used
Maximum	18304mV

Setting Minimum System Voltage

To set the minimum system voltage, write a 16-bit MinSystemVoltage command (0x3EH or 0b00111110) using the Write-word protocol shown in Figure 24 on page 19 and the data format as shown in Table 9.

The minimum system voltage range is 256mV to 13.824V. The MinSystemVoltage register accepts any voltage command but only the valid register bits will be written to the register. The MinSystemVoltage register value should be set lower than the MaxSystemVoltage register value and the maximum value is clamped at 13.824V.

The MinSystemVoltage register sets the battery voltage threshold for entry and exit of the Trickle Charging mode and for entry and exit of the Learn mode. The VBAT pin is used to sense the battery voltage to compare with the MinSystemVoltage register setting. Refer to "Trickle Charging" on page 37 and "Battery Learn Mode" on page 36 for details.

The MinSystemVoltage register setting also is the system voltage regulation point when it is in Trickle Charging mode. The CSON pin is the system voltage regulation sense point in Trickle Charging mode. Refer to "System Voltage Regulation" on page 37" for details.

TABLE 9. MinSystemVoltage REGISTER 0x3EH

BIT	DESCRIPTION
<7:0>	Not used
<8>	0 = Add 0mV of charge voltage. 1 = Add 256mV of charge voltage.
<9>	0 = Add 0mV of charge voltage. 1 = Add 512mV of charge voltage.
<10>	0 = Add 0mV of charge voltage. 1 = Add 1024mV of charge voltage.
<11>	0 = Add 0mV of charge voltage. 1 = Add 2046mV of charge voltage.
<12>	0 = Add 0mV of charge voltage. 1 = Add 4096mV of charge voltage.
<13>	0 = Add 0mV of charge voltage. 1 = Add 8192mV of charge voltage.
<15:14>	Not used
Maximum	13824mV

Setting PROCHOT# Threshold for Adapter Overcurrent Condition

To set the PROCHOT# assertion threshold for adapter overcurrent condition, write a 16-bit ACProchot# command (0x47H or 0b01000111) using the Write-word protocol shown in Table 24 on page 19 and the data format shown in Table 10 on page 24. By using the recommended current sense resistor values, the register's LSB always translates to 128mA of adapter current. The ACProchot# register accepts any current command but only the valid register bits will be written to the register and the maximum value is clamped at 6400mA for R_{S1} = 20mΩ.

After POR, the ACProchot# register is reset to 0x0C00H. The ACProchot# register can be read back to verify its content.

If the adapter current exceeds the ACProchot# register setting, PROCHOT# signal will assert after the debounce time programmed by the Control2 register Bit<10:9> and latch on for a minimum time programmed by Control2 register Bit<8:6>.

TABLE 10. ACProchot# REGISTER 0x47H (20mΩ SENSING RESISTOR, 128mA STEP, x18 GAIN)

BIT	DESCRIPTION
<6:0>	Not used
<7>	0 = Add 0mA of ACProchot# threshold. 1 = Add 128mA of ACProchot# threshold.
<8>	0 = Add 0mA of ACProchot# threshold. 1 = Add 256mA of ACProchot# threshold.
<9>	0 = Add 0mA of ACProchot# threshold. 1 = Add 512mA of ACProchot# threshold.
<10>	0 = Add 0mA of ACProchot# threshold. 1 = Add 1024mA of ACProchot# threshold.
<11>	0 = Add 0mA of ACProchot# threshold. 1 = Add 2048mA of ACProchot# threshold.
<12>	0 = Add 0mA of ACProchot# threshold. 1 = Add 4096mA of ACProchot# threshold.
<15:13>	Not used
Maximum	<12:7> = 110010, 6400mA

Setting PROCHOT# Threshold for Battery Over Discharging Current Condition

To set the PROCHOT# signal assertion threshold for battery over discharging current condition, write a 16-bit DCProchot# command (0x48H or 0b01001000) using the Write-word protocol shown in Figure 24 on page 19 and the data format shown in Table 11. By using the recommended current sense resistor values, the register's LSB always translates to 256mA of adapter current. The DCProchot# register accepts any current command but only the valid register bits will be written to the register and the maximum values is clamped at 12.8A for R_{S2} = 10mΩ.

After POR, the DCProchot# register is reset to 0x1000H. The DCProchot# register can be read back to verify its content.

If the battery discharging current exceeds the DCProchot# register setting, the PROCHOT# signal will assert after the debounce time programmed by the Control2 register Bit<10:9> and latch on for a minimum time programmed by Control2 register Bit<8:6>.

In battery only and Low Power mode, the DCProchot# threshold is set by Control0 register Bit<4:3>.

In battery only mode, DCProchot# function works only when PSYS is enabled, since enabling PSYS will activate the internal comparator reference. The Information register Bit<15> indicates if the internal comparator reference is active or not. When the adapter is present, the internal comparator reference is always active.

TABLE 11. DCPROCHOT# REGISTER 0x48H (10mΩ SENSING RESISTOR, 256mA STEP, x18 GAIN)

BIT	DESCRIPTION
<7:0>	Not used
<8>	0 = Add 0mA of DCProchot# threshold. 1 = Add 256mA of DCProchot# threshold.
<9>	0 = Add 0mA of DCProchot# threshold. 1 = Add 512mA of DCProchot# threshold.
<10>	0 = Add 0mA of DCProchot# threshold. 1 = Add 1024mA of DCProchot# threshold.
<11>	0 = Add 0mA of DCProchot# threshold. 1 = Add 2048mA of DCProchot# threshold.
<12>	0 = Add 0mA of DCProchot# threshold. 1 = Add 4096mA of DCProchot# threshold.
<13>	0 = Add 0mA of DCProchot# threshold. 1 = Add 8192mA of DCProchot# threshold.
<15:14>	Not used.
Maximum	<13:8> = 110010, 12800mA

Setting PROCHOT# Debounce Time and Duration Time

Control2 register Bit<10:9> configures the PROCHOT# signal debounce time before its assertion for ACProchot# and DCProchot#. The low system voltage Prochot# has a fixed debounce time of 10µs.

Control2 register Bit<8:6> configures the minimum duration of Prochot# signal once asserted.

Control Registers

Control0, Control1, Control2, Control3 and Control4 registers configure the operation of the ISL9238 and ISL9238A. To change certain functions or options after POR, write an 8-bit control command to Control0 register (0x39H or 0b00111001) or a 16-bit control command to Control1 register (0x3CH or 0b00111100) or Control2 register (0x3DH or 0b00111101) or Control3 register (0x4CH or 0b00111100) or Control4 register (0x4EH or 0b00111101) using the Write-word protocol shown in Figure 24 on page 19 and the data format shown in Tables 12, 13, 14 and 15 on page 16, respectively.

TABLE 12. CONTROLO REGISTER 0x39H

<table>
<tr><th>BIT</th><th>BIT NAME</th><th>DESCRIPTION</th></tr>
<tr><td><15:13></td><td>Forward Buck and Buck-Boost Phase Comparator Threshold Offset</td><td>Bit<15:13> adjusts phase comparator threshold offset for forward buck and buck-boost
000 = 0mV
001 = 0.5mV
010 = 1mV
011 = 1.5mV
100 = -2mV
101 = -1.5mV
110 = -1mV
111 = -0.5mV</td></tr>
<tr><td><12:10></td><td>Forward and Reverse Boost Phase Comparator Threshold Offset</td><td>Bit<12:10> adjusts phase comparator threshold offset for forward and reverse boost
000 = 0mV
001 = 0.5mV
010 = 1mV
011 = 1.5mV
100 = -2mV
101 = -1.5mV
110 = -1mV
111 = -0.5mV</td></tr>
<tr><td><9:8></td><td>Reverse Buck and Buck-Boost Phase Comparator Threshold Offset</td><td>Bit<9:8> adjusts phase comparator threshold offset for forward and reverse boost
00 = 0mV
01 = 1mV
10 = -2mV
11 = -1mV</td></tr>
<tr><td><7></td><td>SMBus Timeout</td><td>The ISL9238 and ISL9238A includes a timer to insure the SMBus master is active and to prevent overcharging the battery. If the adapter is present and if the ISL9238 and ISL9238A does not receive a write to the MaxChargeVoltage or ChargeCurrentLimit register within 175s, ISL9238 and ISL9238A will terminate charging. If a timeout occurs, writing the MaxChargeVoltage or ChargeCurrentLimit register will re-enable charging.
0 = Enable the SMBus timeout function.
1 = Disable the SMBus timeout function.</td></tr>
<tr><td><6:5></td><td>High-Side FET Short Detection Threshold</td><td>Bit<6:5> configures the high-side FET short detection PHASE node voltage threshold during low-side FET turning on.
00 = 400mV (default)
01 = 500mV
10 = 600mV
11 = 800mV</td></tr>
<tr><td><4:3></td><td>DCProchot# Threshold in Battery Only Low Power Mode</td><td>Bit<4:3> only configures the battery discharging current DCProchot# threshold in battery only Low Power mode indicated by the Information1 register 0x3A Bit<15>. If PSYS is enabled, battery discharge current DCProchot# threshold is set by the DCProchot# register 0x48 setting.
<table>
<tr><th>Bit<4:3></th><th>R_{s2} = 10mΩ (A)</th><th>R_{s2} = 20mΩ (A)</th><th>R_{s2} = 5mΩ (A)</th></tr>
<tr><td>00</td><td>12 (Default)</td><td>6</td><td>24</td></tr>
<tr><td>01</td><td>10</td><td>5</td><td>20</td></tr>
<tr><td>10</td><td>8</td><td>4</td><td>16</td></tr>
<tr><td>11</td><td>6</td><td>3</td><td>12</td></tr>
</table></td></tr>
<tr><td><2></td><td>Input Voltage Regulation Loop</td><td>Bit<2> disables or enables the input voltage regulation loop.
0 = Enable (default)
1 = Disable</td></tr>
<tr><td><1:0></td><td></td><td>Not used</td></tr>
</table>