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Multi-Cell Li-Ion Battery Manager

ISL94212

The ISL94212 Li-ion battery manager IC supervises up to 12 series connected cells. The part provides accurate monitoring, cell balancing and extensive system diagnostics functions. Three cell balancing modes are provided: Manual Balancing mode, Timed Balancing mode and Auto Balance mode. The Auto Balance mode terminates balancing functions when a charge transfer value has been met.

The ISL94212 communicates to a host microcontroller via an SPI interface and to other ISL94212 devices using a robust, proprietary, two-wire Daisy Chain system.

The ISL94212 is offered in a 64 Ld TQFP package and is specified for an operational temperature range of -40°C to +85°C.

Applications

- Light electric vehicle (LEV); E-Moto; E-Bike
- Battery backup systems; Energy Storage Systems (ESS)
- Solar Farms
- Portable and semi-portable equipment

Features

- Up to 12-cell voltage monitors, support Li-Ion CoO_2, Li-ion Mn_2O_4, and Li-ion FePO4 chemistries
- Cell voltage measurement accuracy ±10mV
- 13-bit cell voltage measurement
- Pack voltage measurement accuracy ±180mV
- 14-bit pack voltage and temperature measurements
- Cell voltage scan rate of 19.5µs per cell (234µs to scan 12 cells)
- Internal temperature monitoring
- Up to four external temperature inputs
- Robust daisy chain communications system
- Integrated system diagnostics for all key internal functions
- Hardwired and communications based fault notification
- Integrated watchdog shuts down device if communication is lost
- 7µA shutdown current: Enable = V_{SS}
- 2Mbps SPI

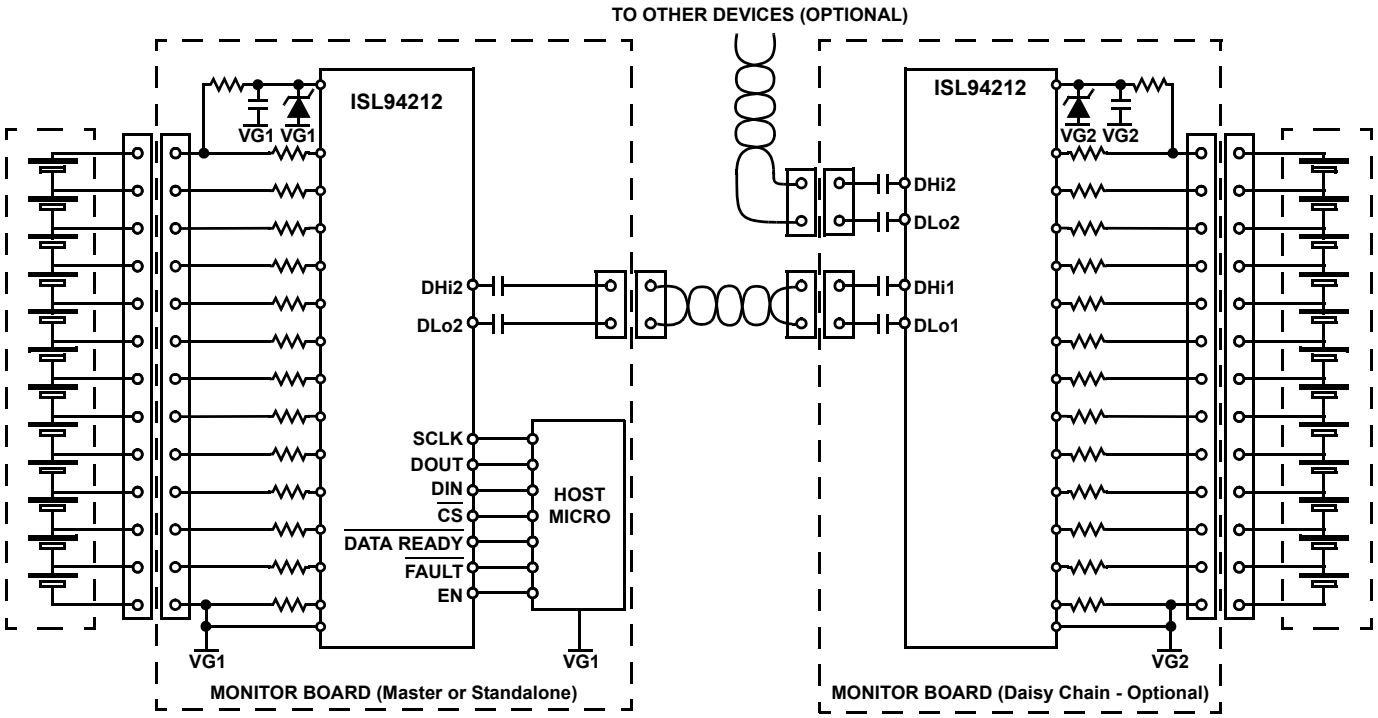

FIGURE 1. TYPICAL APPLICATION

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Ordering Information

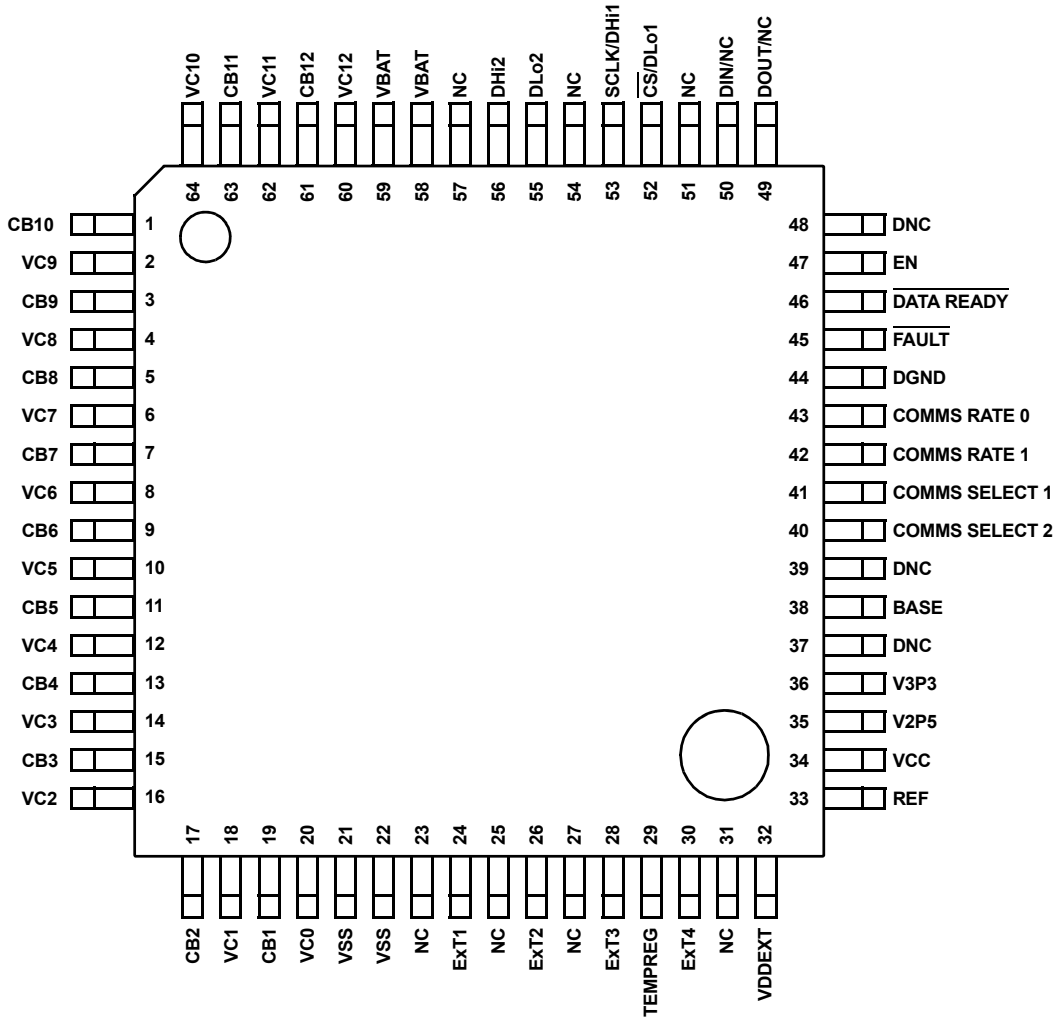
PART NUMBER (Notes 2, 3, 4)	PART MARKING	TRIM VOLTAGE, V_{NOM} (V)	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL94212INZ (Note 1)	ISL94212INZ	3.3	-40 to +85	64 Ld TQFP	Q64.10x10D
ISL94212EVKIT1Z	Evaluation Kit				

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level Rating (MSL) for the package, please see the Intersil ISL94212. For more information on handling and processing moisture sensitive devices, please see Techbrief TB363.
4. For other trim options, please contact Marketing.

Pin Configuration

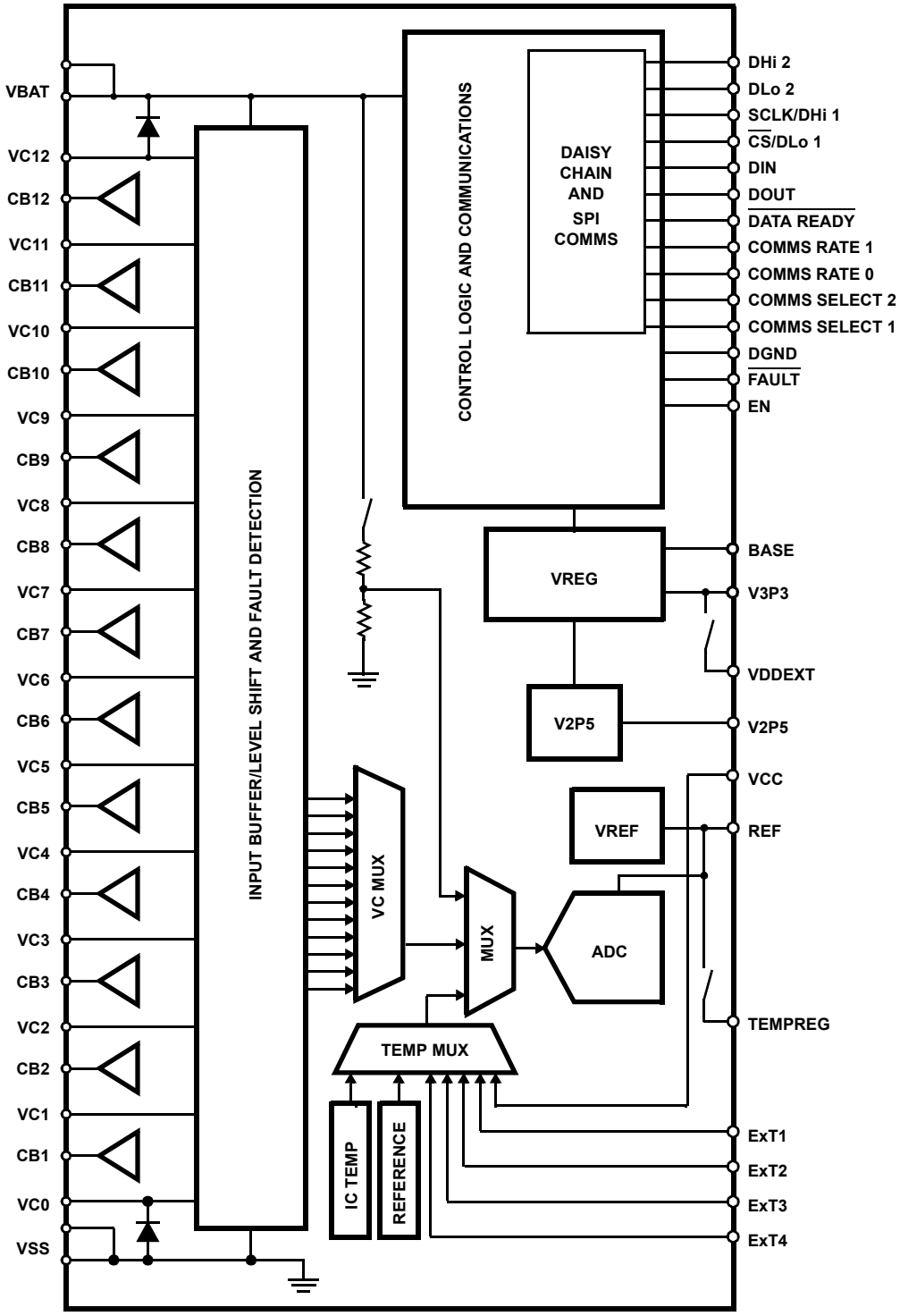
ISL94212
(64 LD 10x10 TQFP)
TOP VIEW



Pin Descriptions

SYMBOL	PIN NUMBER	DESCRIPTION
VC0, VC1, VC2, VC3, VC4, VC5, VC6, VC7, VC8, VC9, VC10, VC11, VC12	20, 18, 16, 14, 12, 10, 8, 6, 4, 2, 64, 62, 60	Battery cell voltage inputs. VCn connects to the positive terminal of CELLn and the negative terminal of CELLn+1. (VC12 connects only to the positive terminal of CELL12 and VC0 only connects with the negative terminal of CELL1.)
CB1, CB2, CB3, CB4, CB5, CB6, CB7, CB8, CB9, CB10, CB11, CB12	19, 17, 15, 13, 11, 9, 7, 5, 3, 1, 63, 61	Cell Balancing FET control outputs. Each output controls an external FET which provides a current path around the cell for balancing.
VBAT	58, 59	Main IC Supply pins. Connect to the most positive terminal in the battery string.
VSS	21, 22	Ground. These pins connect to the most negative terminal in the battery string.
ExT1, ExT2, ExT3, ExT4	24, 26, 28, 30	External temperature monitor or general purpose inputs. The temperature inputs are intended for use with external resistor networks using NTC type thermistor sense elements but may also be used as general purpose analog inputs at the user's discretion. 0V to 2.5V input range.
TEMPREG	29	Temperature monitor voltage regulator output. This is a switched 2.5V output, which supplies a reference voltage to external NTC thermistor circuits to provide ratiometric ADC inputs for temperature measurement.
VDDEXT	32	External V3P3 supply input/output. Connected to the V3P3 pin via a switch, this pin may be used to power external circuits from the V3P3 supply. The switch is open when the ISL94212 is placed in **Sleep mode**.
REF	33	2.5V voltage reference decoupling pin. Connect a 2.0µF to 2.5µF X7R capacitor to VSS. Do not connect any additional external load to this pin.
VCC	34	Analog supply voltage input. Connect to V3P3 via a 33Ω resistor. Connect a 1µF capacitor to ground.
V2P5	35	Internal 2.5V digital supply decoupling pin. Connect a 1µF capacitor to DGND.
V3P3	36	3.3V digital supply voltage input. Connect the emitter of the external NPN regulator transistor to this pin. Connect a 1µF capacitor to DGND.
Base	38	Regulator control pin. Connect the external NPN transistor's base. Do not let this pin float,
DNC	37, 39, 48	Do not connect. Leave pins floating.
Comms Select 1	41	Communications port 1 mode select pin. Connect via a 1kΩ resistor to V3P3 for Daisy Chain communications on port 1 or to DGND for SPI operation on port 1.
Comms Select 2	40	Communications port 2 mode select pin. Connect via a 1kΩ resistor to V3P3 to enable port 2 or to DGND to disable this port.
Comms Rate 0, Comms Rate 1	43, 42	Daisy Chain communications data rate setting. Connect via a 1kΩ resistor to DGND ('0') or to V3P3 ('1') to select between various communication data rates.
DGND	44	Digital Ground.
$\overline{\text{Fault}}$	45	Logic fault output. Asserted low if a fault condition exists.
$\overline{\text{Data Ready}}$	46	SPI data ready. Asserted low when the device is ready to transmit data to the host microcontroller.
EN	47	Enable input. Tie to V3P3 to enable the part. Tie to DGND to disable (all IC functions are turned off).
DOUT/NC	49	Serial Data Output (SPI) or NC (Daisy Chain). 0V to 3.3V push-pull output.
DIN/NC	50	Serial Data Input (SPI) or NC (Daisy Chain). 0V to 3.3V input.
$\overline{\text{CS}}$/DLo1	52	Chip-Select, active low 3.3V input (SPI) or Daisy Chain port 1 Lo connection.
SCLK/DHi1	53	Serial-Clock Input (SPI) or Daisy Chain port 1 Hi connection.
DHi2	56	Daisy Chain port 2 Hi connection.
DLo2	55	Daisy Chain port 2 Lo connection.
NC	23, 25, 27, 31, 51, 54, 57	No internal connection.

Block Diagram



Absolute Maximum Ratings

Unless otherwise specified. With respect to VSS.

DIN, SCLK, $\overline{CS}$, DOUT, $\overline{Data\ Ready}$, Comms Select n, ExTn, TEMPREG, REF, V3P3, VCC, $\overline{Fault}$, Comms Rate n, Base, EN, VDDEXT. . . . . -0.2V to 4.1V
V2P5. . . . . -0.2V to 2.9V
VBAT . . . . . -0.5V to 63V
Dhi1, DLo1, DHi2, DLo2 . . . . . -0.5V to (VBAT + 0.5V)
VC0 . . . . . -0.5V to + 9.0V
VC1 . . . . . -0.5V to + 18V
VC2 . . . . . -0.5V to + 18V
VC3 . . . . . -0.5V to + 27V
VC4 . . . . . -0.5V to + 27V
VC5 . . . . . -0.5V to + 36V
VC6 . . . . . -0.5V to + 36V
VC7 . . . . . -0.5V to + 45V
VC8 . . . . . -0.5V to + 45V
VC9 . . . . . -0.5V to + 54V
VC10 . . . . . -0.5V to + 63V
VC11 . . . . . -0.5V to + 63V
VC12 . . . . . -0.5V to + 63V
VCn (for n = 0 to 12). . . . . -0.5 to VBAT + 0.5V
CBn (for n = 1 to 12) . . . . . -0.5 to VBAT + 0.5V
CBn (for n = 1 to 9) . . . . . V(VCn-1) - 0.5V to V(VCn-1) + 9V
CBn (for n = 10 to 12). . . . . V(VCn) - 9V to V(VCn) + 0.5V
Current into VCn, VBAT, VSS (Latch up Test) . . . . . ±100mA
ESD Rating
  Human Body Model (Tested per JESD22-A114F) 2kV
  Machine Model (Tested per JESD22A115-A) 200V
  Charge Device Model (Tested per JESD22-C101D) 750V
Latch-up (Tested per JESD-78B; Class 2, Level A) 100mA

NOTE: DOUT, $\overline{Data\ Ready}$, and $\overline{Fault}$ are digital outputs and should not be driven from external sources. V2P5, REF, TEMPREG and BASE are analog outputs and should not be driven from external sources.

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (C/W)	θ_{JC} (C/W)
64 Ld TQFP Package (Notes 5, 6)	42	9

Max Continuous Package Power Dissipation 400mW
Storage Temperature . . . . . -55°C to +125°C
Max Operating Junction Temperature . . . . . +125°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

T_A, Ambient Temperature Range . . . . . -40°C to +85°C
V_{BAT} . . . . . 6V to 60V
V_{BAT} (Daisy Chain Operation) . . . . . 10V to 60V
VCn (for n = 1 to 12) . . . . . V(VCn-1) to V(VCn-1) + 5V
VC0 . . . . . -0.1V to 0.1V
CBn (for n = 1 to 9) . . . . . V(VCn-1) to V(VCn-1) + 9V
CBn (for n = 10 to 12). . . . . V(VCn) - 9V to V(VCn)
DIN, SCLK, $\overline{CS}$, DOUT, $\overline{Data\ Ready}$, Comms Select 1, Comms Select 2, TEMPREG, REF, V3P3, VCC, $\overline{Fault}$, Comms Rate 0, Comms Rate 1, EN, VDDEXT. . . . . 0V to 3.6V
ExT1,ExT2,ExT3,Ext4 . . . . . 0V to 2.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V_{BAT} = 6 to 60V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Power-up Condition Threshold	V_{POR}	V_{BAT} voltage (rising)	**4.8**	5.1	**5.6**	V
Power-up Condition Hysteresis	V_{PORhys}			400		mV
Initial Power-up Delay	t_{POR}	Time after VPOR condition V_{REF} from 0V to 0.95 x V_{REF}(nom) (EN tied to V3P3) Device can now communicate			**27.125**	ms
Enable Pin Power-up Delay	t_{PUD}	Delay after EN = 1 to V_{REF} from 0V to 0.95 x V_{REF}(nom) (V_{BAT} = 39.6V) - Device can now communicate			**27.125**	ms

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN (Note 7)	TYP	MAX (Note 7)	UNITS
V_{BAT} Supply Current	I_{VBAT}	Non-daisy chain configuration. Device enabled. No communications, ADC, measurement, balancing or open wire detection activity.	6V	**10**	35	**75**	µA
			39.6V	**10**	64	**220**	µA
			60V	**10**	90	**230**	µA
	$I_{VBATMASTER}$	Daisy chain configuration – master device. Enabled. No communications, ADC, measurement, balancing or open wire detection activity.	6V	**400**	530	**660**	µA
			39.6V	**500**	680	**900**	µA
			60V	**550**	750	**1000**	µA
		Peak current when daisy chain transmitting			18		mA
	$I_{VBATMID}$	Daisy chain configuration – mid stack device. Enabled. No communications, ADC, measurement, balancing or open wire detection activity.	6V	**700**	1020	**1300**	µA
			39.6V	**900**	1250	**1600**	µA
			60V	**1000**	1400	**1700**	µA
		Peak current when daisy chain transmitting			18		mA
	$I_{VBATTOP}$	Daisy chain configuration – top device. Enabled. No communications, ADC, measurement, balancing or open wire detection activity.	6V	**400**	530	**660**	µA
			39.6V	**500**	680	**900**	µA
			60V	**550**	750	**1000**	µA
		Peak current when daisy chain transmitting			18		mA
	$I_{VBATSLEEP1}$	Sleep mode (EN = 1, daisy chain configuration).		**10**	19	**36**	µA
	$I_{VBATSLEEP2}$	Sleep mode (EN = 1, standalone, non-daisy chain)		**5**	9	**18**	µA
	$I_{VBATSHDN}$	Shutdown. device “off” (EN = 0) (daisy chain and non-daisy chain configurations)		**5**	7	**18**	µA
V_{BAT} Supply Current Tracking. Sleep Mode.	$I_{VBATΔSLEEP}$	EN = 1, daisy chain sleep mode configuration. V_{BAT} current difference between any two devices operating at the same temperature and supply voltage.		**0**		**10.5**	µA
V_{BAT} Incremental Supply Current, Balancing	$I_{VBATBAL}$	All balancing circuits on. Incremental current: Add to non-balancing V_{BAT} current. V_{BAT} = 39.6V		**200**	300	**400**	µA
V3P3 Regulator Voltage (Normal)	V_{3P3N}	EN = 1, load current range 0 to 5 mA. V_{BAT} = 39.6V		**3.2**	3.35	**3.5**	V
V3P3 Regulator Voltage (Sleep)	V_{3P3S}	EN = 1, load current range. No load. (SLEEP). V_{BAT} = 39.6V		**2.4**	2.7	**3.05**	V
V3P3 Regulator Control Current	I_{Base}	Current sourced from base output. V_{BAT} = 6V		**1**	1.5		mA
V3P3 Supply Current	I_{V3P3}	Device enabled No measurement activity, normal mode		**0.8**	1	**1.3**	mA
V_{REF} Reference Voltage	V_{REF}	EN = 1, no load, normal mode			2.5		V

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
VDDEXT Switch Resistance	R_{VDDEXT}	Switch ON-resistance, V_{BAT} = 39.6V	**5**	12	**22**	Ω
VCC Supply Current	I_{VCC}	Device enabled (EN = 1). Standalone or daisy configuration. No ADC or daisy chain communications active.	**2.0**	3.25	**5.0**	mA
	$I_{VCCACTIVE1}$	Device enabled (EN = 1). Standalone or daisy configuration. Average current during 16ms scan continuous operation. V_{BAT} = 39.6V		6.0		mA
	$I_{VCCSLEEP}$	Device enabled (EN = 1). Sleep mode. V_{BAT} = 39.6V		2.4		µA
	$I_{VCCSHDN}$	Device disabled (EN = 0). Shutdown mode.	**0**	1.2	**9.0**	µA
MEASUREMENT SPECIFICATIONS						
Cell Voltage Input Measurement Range	V_{CELL}	VC(N) - VC(N-1). For design reference.	**0**		**5**	V
Cell Monitor Voltage Resolution	$V_{CELLRES}$	[VC(N)-VC(N-1)] LSB step size (13-bit signed number), 5V full scale value		0.61		mV
ISL94212 Cell Monitor Voltage Error (Absolute)	ΔV_{CELLA}	Absolute cell measurement error (Cell measurement error compared with applied voltage with 1k series resistor.) Temperature = 0°C to +50°C, V_{CELL} = 2.6V to 4.0V	-10		10	mV
		Temperature = +50°C to +85°C, V_{CELL} = 2.0V to 4.3V	-25		25	mV
		Temperature = -40°C to 0°C, V_{CELL} = 2.0V to 4.3V	-35		35	mV
ISL94212 Cell Monitor Voltage Error (Relative)	ΔV_{CELLB}	Relative cell measurement error (Max absolute cell measurement error Min absolute cell measurement error) Temperature = 0°C to +50°C	0		7.5	mV
		Temperature = -40°C to 0°C	0		7.5	mV
		Temperature = +50°C to +85°C	0		20	mV
Cell Input Current. Note: Cell accuracy figures assume a fixed 1kΩ resistor is placed in series with each VCn pin (n = 0 to 12)	I_{VCELL}	VC0 input	**-2.0**	-1	**-0.5**	µA
		VC1, VC2, VC3 inputs	**-3.0**	-2	**-0.9**	µA
		VC4 input	**-0.8**	0	**0.9**	µA
		VC5, VC6, VC7, VC8, VC9, VC10, VC11 inputs	**0.5**	2	**3.2**	µA
		VC12 input	**0.4**	1	**2.0**	µA
V_{BAT} Monitor Voltage Resolution	$VBAT_{RES}$	ADC resolution referred to input (V_{BAT}) level. 14b unsigned number. Full scale value = 79.67V.		4.863		mV
V_{BAT} Monitor Voltage Error	ΔV_{BAT}	Temperature = 0°C to +50°C, Measured at V_{BAT} = 31.2V to 43.2V	-180		180	mV
		Temperature = 0°C to +50°C, Measured at V_{BAT} = 24V to 48V	-230		230	mV
		Temperature = 0°C to +50°C, Measured at V_{BAT} = 6V to 59.4V	-390		390	mV
		Temperature = -40°C to +85°C, Measured at V_{BAT} = 31.2V to 39.6V	-320		320	mV
		Temperature = -40°C to +85°C, Measured at V_{BAT} = 6V to 48V	-440		440	mV
		Temperature = -40°C to +85°C, Measured at V_{BAT} = 6V to 59.4V	-650		650	mV

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
External Temperature Monitoring Regulator	V_{TEMP}	Voltage on TEMPREG output. (0 to 2mA load)	**2.475**	2.5	**2.525**	V
External Temperature Output Impedance	R_{TEMP}	Output impedance at TEMPREG pin.	**0**	0.1	**0.2**	Ω
External Temperature Input Range	V_{EXT}	ExTn input voltage range. For design reference.	**0**		**2344**	mV
External Temperature Input Pull-up	$R_{EXTTEMP}$	Pull-up resistor to $V_{TEMPREG}$ applied to each input during measurement		10		MΩ
External Temperature Input Offset	V_{EXTOFF}	V_{BAT} = 39.6V	**-12**		**12**	mV
External Temperature Input INL	V_{EXTINL}		**-0.65**		**0.65**	mV
External Temperature Input Gain Error	V_{EXTG}		**-8**		**18.5**	mV
Internal Temperature Monitor Error	V_{INTMON}			±10		°C
Internal Temperature Monitor Resolution	T_{INTRES}	Output resolution (LSB/°C). 14b number.		31.9		LSB/°C
Internal Temperature Monitor Output	T_{INT25}	Output count at +25°C		9180		Decimal
OVER-TEMPERATURE PROTECTION SPECIFICATIONS						
Internal Temperature Limit Threshold	T_{INTSD}	Balance stops and auto scan stops. Temperature rising or falling.		150		°C
External Temperature Limit Threshold	T_{XT}	Corresponding to 0V (min) and $V_{TEMPREG}$ (max) External temperature input voltages higher than 15/16 $V_{TEMPREG}$ are registered as open input faults.	**0**		**16383**	Decimal
FAULT DETECTION SYSTEM SPECIFICATIONS						
Undervoltage Threshold	V_{UV}	Programmable. Corresponding to 0V (min) and 5V (max)	**0**		**8191**	Decimal
Overvoltage Threshold	V_{OV}	Programmable. Corresponding to 0V (min) and 5V (max)	**0**		**8191**	Decimal
V3P3 Power-good Window	V_{3PH}	3.3V Power-good window high threshold. V_{BAT} = 39.6V	**3.7**	3.90	**4.05**	V
	V_{3PL}	3.3V Power-good window low threshold. V_{BAT} = 39.6V	**2.5**	2.65	**2.8**	V
V2P5 Power-good Window	V_{2PH}	2.5V Power-good window high threshold. V_{BAT} = 39.6V	**2.55**	2.7	**2.9**	V
	V_{2PL}	2.5V Power-good window low threshold. V_{BAT} = 39.6V	**1.90**	2.0	**2.15**	V
VCC Power-good Window	V_{VCCH}	VCC Power-good window high threshold. V_{BAT} = 39.6V	**3.6**	3.75	**4.0**	V
	V_{VCCL}	VCC Power-good window low threshold. V_{BAT} = 39.6V	**2.55**	2.7	**2.85**	V
V_{REF} Power-good Window	V_{RPH}	V_{REF} Power-good window high threshold. V_{BAT} = 39.6V	**2.525**	2.7	**2.9**	V
	V_{RPL}	V_{REF} Power-good window low threshold. V_{BAT} = 39.6V	**2.0**	2.30	**2.50**	V

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
V_{REF} Reference Accuracy Error	V_{RACC}	V_{REF} value calculated using stored coefficients. V_{BAT} = 39.6V, V_{REF} typical = 2.5V (See "Voltage Reference Check Calculation" on page 86.) Temperature = 0°C to +50°C	-15		15	mV
		Temperature = -40°C to 0°C	-40		40	mV
		Temperature = +50°C to +85°C	-22		22	mV
Voltage Reference Check Timeout	t_{VREF}	Time to check voltage reference value from power-on, enable or wake up		20		ms
Oscillator Check Timeout	t_{OSC}	Time to check main oscillator frequency from power-on, enable or wake up		20		ms
Oscillator Check Filter Time	t_{OSCF}	Minimum duration of fault required for detection		100		ms
CELL OPEN WIRE DETECTION (See sections "Scan Wires" on page 22, "ISCN, PIN37, PIN39" on page 30, and "Open Wire Test" on page 45.)						
Open Wire Current	I_{OW}	ISCN bit = 0; V_{BAT} = 39.6V	**0.125**	0.15	**0.175**	mA
		ISCN bit = 1; V_{BAT} = 39.6V	**0.85**	1.0	**1.15**	mA
Open Wire Detection Time	t_{OW}	Open wire current source "on" time		4.6		ms
Open VC0 Detection Threshold	V_{VC0}	CELL1 negative terminal (with respect to VSS) V_{BAT} = 39.6V	**1.2**	1.5	**1.8**	V
Open VC1 Detection Threshold	V_{VC1}	CELL1 positive terminal (with respect to VSS) V_{BAT} = 39.6V	**0.6**	0.7	**0.8**	V
Primary Detection Threshold, VC2 to VC12	V_{VC2_12P}	V(VC(n - 1)) - V(VCn), n = 2 to 12 V_{BAT} = 39.6V	**-2**	-1.5	**0**	V
Secondary Detection Threshold, VC2 to VC12	V_{VC2_12S}	Via ADC. VC2 to VC12 only V_{BAT} = 39.6V	**-100**	-30	**50**	mV
Open V_{BAT} Fault Detection Threshold	V_{VBO}	VC12 - V_{BAT}		200		mV
Open VSS Fault Detection Threshold	V_{VSSO}	VSS - VC0		250		mV
MEASUREMENT FUNCTION TIMING (Note 8)						
Cell Sample Time Start		Time to sample the first cell (CELL12) following $\overline{CS}$ going High. Scan voltages command		65	**71.5**	µs
Cell Sample Time Duration		Time to scan all 12 cells (sample of CELL12 to sample of CELL1) scan voltages command.		233	**257**	µs
Scan Voltages Processing Time		Time from start of scan to registers loaded to $\overline{DATA\ READY}$ going low		770	**847**	µs
Scan Temperatures Processing Time		Time from start of scan to registers loaded to $\overline{DATA\ READY}$ going low		2690	**2959**	µs
Scan Mixed Processing Time		Time from start of scan to registers loaded to $\overline{DATA\ READY}$ going low		830	**913**	µs
Scan Wires Processing Time		Time from start of scan to registers loaded to $\overline{DATA\ READY}$ going low		59.4	**65.3**	ms
Scan All Processing Time		Time from start of scan to registers loaded to $\overline{DATA\ READY}$ going low		63.2	**69.5**	ms

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Measure Cell Voltage Processing Time		Time from start of measurement to register(s) loaded to $\overline{\text{DATA READY}}$ going low		180	**198**	µs
Measure V_{BAT} Voltage Processing Time		Time from start of measurement to register(s) loaded to $\overline{\text{DATA READY}}$ going low		130	**143**	µs
Measure Internal Temperature Processing Time		Time from start of measurement to register(s) loaded to $\overline{\text{DATA READY}}$ going low		110	**121**	µs
Measure External Temperature Input Processing Time		Time from start of measurement to register(s) loaded to $\overline{\text{DATA READY}}$ going low		2520	**2772**	µs
Measure Secondary Voltage Reference Time		Time from start of measurement to register(s) loaded to $\overline{\text{DATA READY}}$ going low		2520	**2772**	µs
CELL BALANCE OUTPUT SPECIFICATIONS						
Cell Balance Pin Output Impedance	R_{CBL}	CBn output off impedance between CB(n) to VC(n-1): cells 1 to 9 and between CB(n) to VC(n): cells 10 to 12.	**3**	4	**5**	MΩ
Cell Balance Output Current	I_{CBH1}	CBn output on. (CB1-CB9); V_{BAT} = 39.6V; device sinking current.	**-28**	-25	**-21**	µA
	I_{CBH2}	CBn output on. (CB10-CB12); V_{BAT} = 39.6V; device sourcing current.	**21**	25	**28**	µA
Cell Balance Output Leakage in Shutdown	I_{CBSD}	EN = GND. V_{BAT} = 39.6V.	**-500**	10	**700**	nA
External Cell Balance FET Gate Voltage	VGS	CBn Output on; External 320kΩ between VCn and CBn (n = 10 to 12) and between CBn and VCn-1 (n = 1 to 9)	**7.05**	8.0	**8.95**	V
Internal Cell Balance Output Clamp	VCBCL	I_{CB} = 100µA.	**8.9**			V
LOGIC INPUTS: SCLK, $\overline{\text{CS}}$, DIN						
Low Level Input Voltage	VIL				**0.8**	V
High Level Input Voltage	VIH		**1.75**			V
Input Hysteresis	VHYS		**100**			mV
Input Current	IIN	0V < V_{IN} < V3P3	**-1**		**+1**	µA
Input Capacitance	CIN				**10**	pF
LOGIC INPUTS: EN, COMMS SELECT1, COMMS SELECT2, COMMS RATE 0, COMMS RATE 1						
Low Level Input Voltage	VIL				**0.3*V3P3**	V
High Level Input Voltage	VIH		**0.7*V3P3**			V
Input Hysteresis	VHYS		**0.05*V3P3**			V
Input Current	IIN	0V < V_{IN} < V3P3	**-1**		**+1**	µA
Input Capacitance	CIN				**10**	pF
LOGIC OUTPUTS: DOUT, $\overline{\text{FAULT}}$, $\overline{\text{DATA READY}}$						
Low Level Output Voltage	VOL1	At 3mA sink current	**0**		**0.4**	V
	VOL2	At 6mA sink current	**0**		**0.6**	V
High Level Output Voltage	VOH1	At 3mA source current	**V3P3 – 0.4V**		**V3P3**	V
	VOH2	At 6mA source current	**V3P3 – 0.6V**		**V3P3**	V

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
SPI INTERFACE TIMING (See Figures 2 and 3)						
SCLK Clock Frequency	f_{SCLK}				**2**	MHz
Pulse Width of Input Spikes Suppressed	t_{IN1}		**50**		**200**	ns
Enable Lead Time	t_{LEAD}	Chip select low to ready to receive clock data	**200**			ns
Clock High Time	t_{HIGH}		**200**			ns
Clock Low Time	t_{LOW}		**200**			ns
Enable Lag Time	t_{LAG}	Last data read clock edge to chip select high.	**250**			ns
CHIP SELECT High Time	$t_{CS:WAIT}$	Minimum high time for $\overline{CS}$ between bytes.	**200**			ns
Slave Access Time	t_A	Chip select low to DOUT active.			**200**	ns
Data Valid Time	t_V	Clock low to DOUT valid.			**350**	ns
Data Output Hold Time	t_{HO}	Data hold time after falling edge of SCLK.	**0**			ns
DOUT Disable Time	t_{DIS}	DOUT disabled following rising edge of $\overline{CS}$.			**240**	ns
Data Setup Time	t_{SU}	Data input valid prior to rising edge of SCLK.	**100**			ns
Data Input Hold Time	t_{HI}	Data input to remain valid following rising edge of SCLK.	**80**			ns
$\overline{\text{Data Ready}}$ Start Delay Time	$t_{DR:ST}$	Chip select high to $\overline{\text{Data Ready}}$ low.	**100**			ns
$\overline{\text{Data Ready}}$ Stop Delay Time	$t_{DR:SP}$	Chip select high to $\overline{\text{Data Ready}}$ high.			**750**	ns
$\overline{\text{Data Ready}}$ High Time	$t_{DR:WAIT}$	Time between bytes.	**0.6**			µs
SPI Communications Timeout	$t_{SPI:TO}$	Time the $\overline{CS}$ remains high before SPI communications time out - requiring the start of a new command.		100		µs
DOUT Rise Time	t_R	Up to 50pF load.			**30**	ns
DOUT Fall Time	t_F	Up to 50pF load.			**30**	ns
DAISY CHAIN COMMUNICATIONS INTERFACE: DHI1, DLo1, DHI2, DLo2						
Daisy Chain Clock Frequency		Comms Rate (0, 1) = 11	**450**	500	**550**	kHz
		Comms Rate (0, 1) = 10	**225**	250	**275**	kHz
		Comms Rate (0, 1) = 01	**112.5**	125	**137.5**	kHz
		Comms Rate (0, 1) = 00	**56.25**	62.5	**68.75**	kHz
Common Mode Reference Voltage				$V_{BAT}/2$		V

NOTES:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
8. Scan and Measurement start times are synchronized by the receiver to the falling edge of the 24^{th} clock pulse (Daisy Chain systems) or to the falling edge of the 16^{th} clock pulse (non-daisy chain, single device systems) of the Scan or Measure command. Clock pulses are at the SCLK pin for master and standalone devices, and at the DHi/DLo1 pins for middle and top daisy chain devices. Max values are based on characterization of the internal clock and are not 100% tested.
9. Biasing setup as in Figure 57 on page 82 or equivalent.

Timing Diagrams

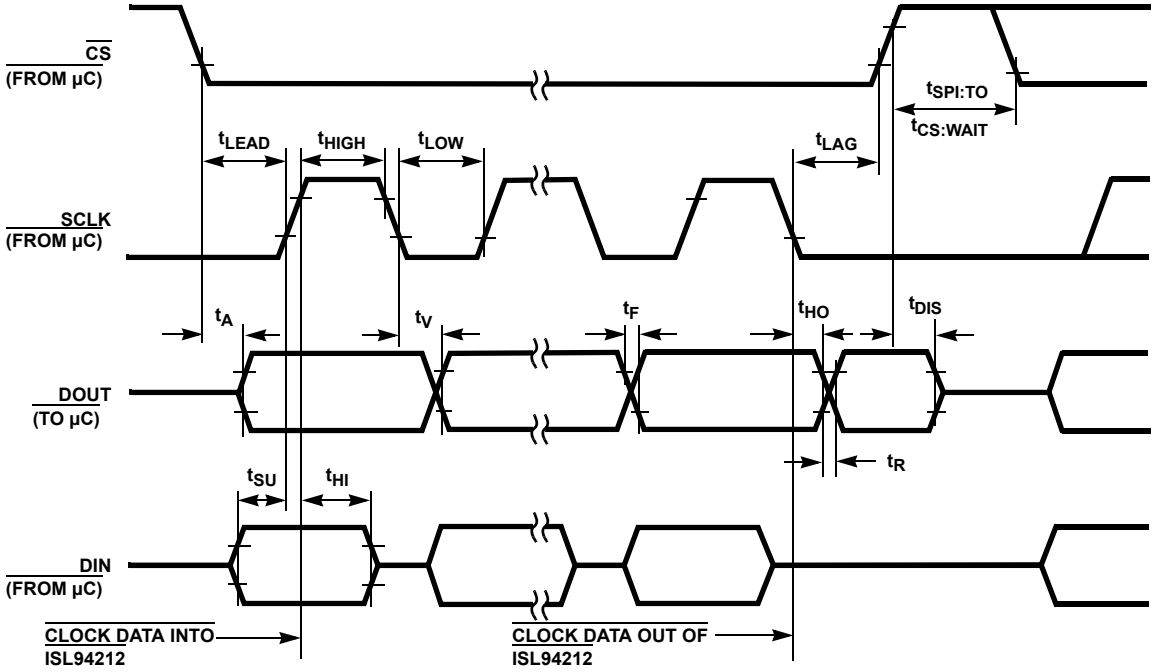


FIGURE 2. SPI FULL DUPLEX (4-WIRE) INTERFACE TIMING

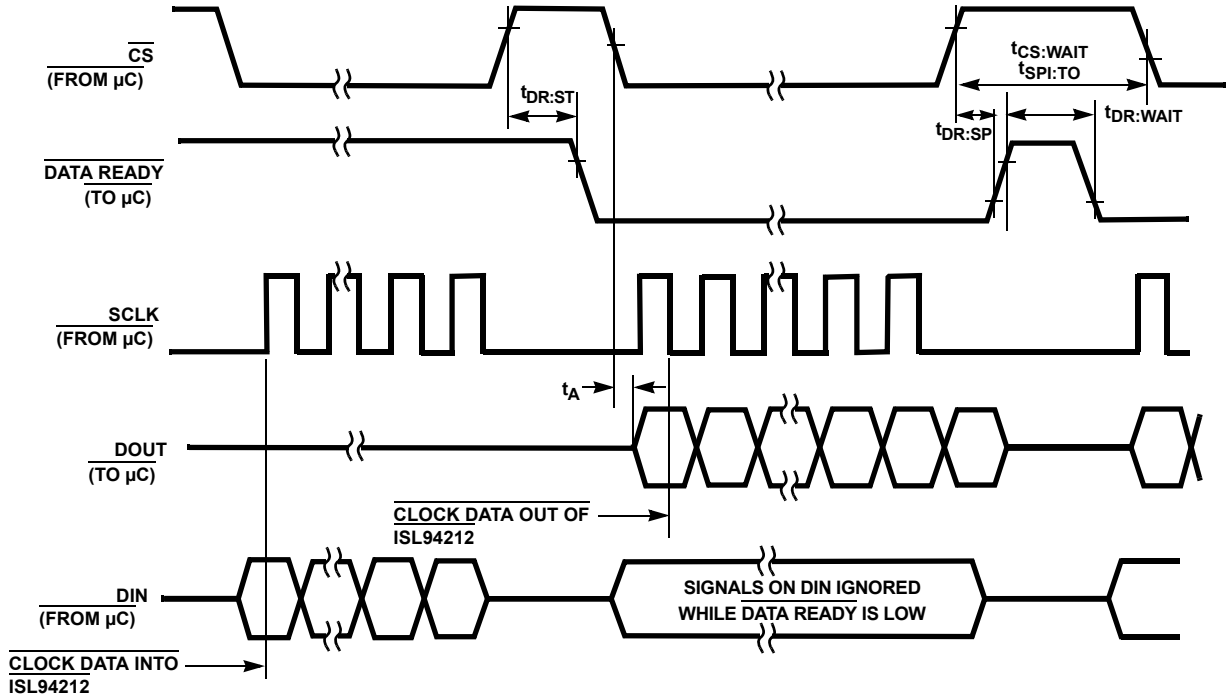


FIGURE 3. SPI HALF DUPLEX (3-WIRE) INTERFACE TIMING

Typical Performance Curves

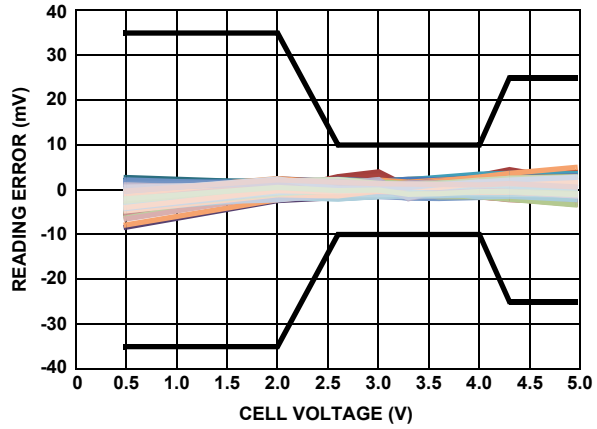


FIGURE 4. CELL VOLTAGE READING ERROR FROM 0°C TO +50°C

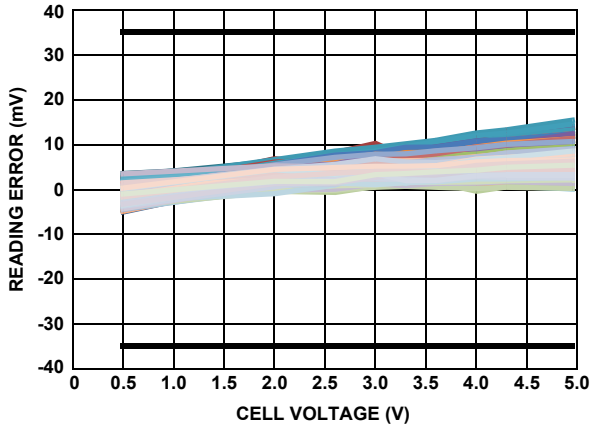


FIGURE 5. CELL VOLTAGE READING ERROR FROM -40°C TO +85°C

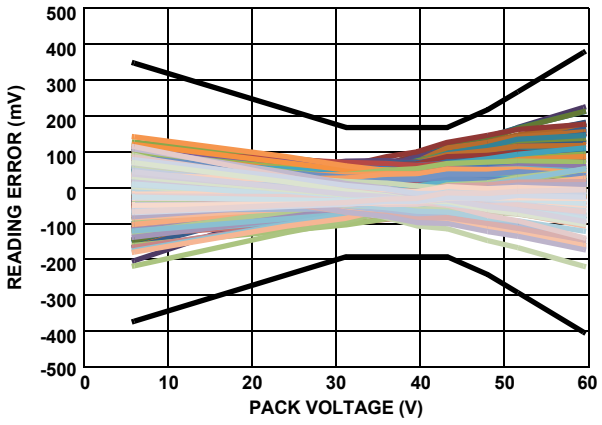


FIGURE 6. PACK VOLTAGE READING ERROR FROM 0°C TO +50°C

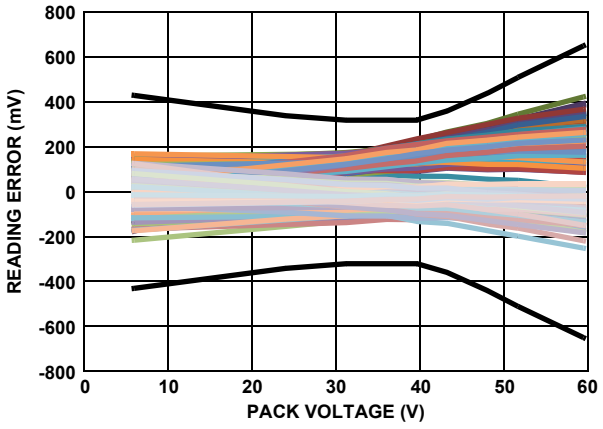


FIGURE 7. PACK VOLTAGE READING ERROR FROM -40°C TO +85°C

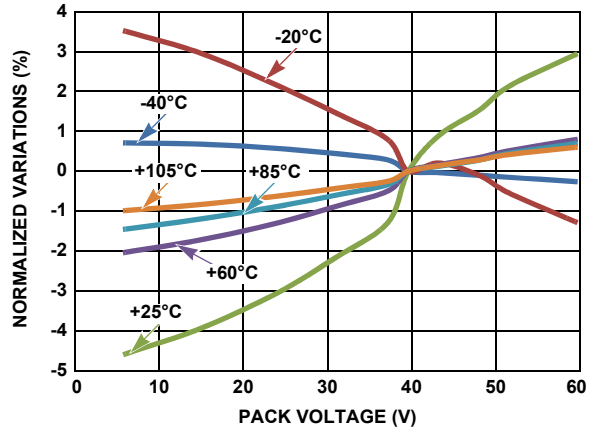


FIGURE 8. IC TEMPERATURE ERROR vs PACK VOLTAGE

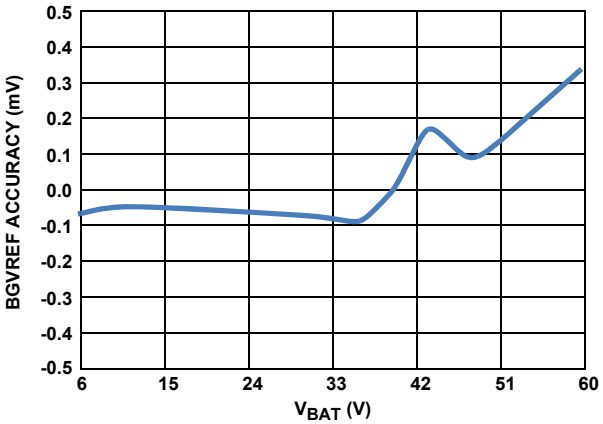


FIGURE 9. VOLTAGE REFERENCE CHECK FUNCTION vs PACK VOLTAGE (AT +25°C)

Typical Performance Curves (Continued)

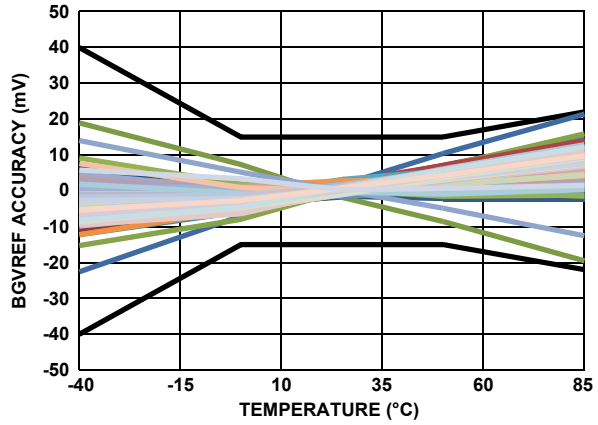


FIGURE 10. VOLTAGE REFERENCE CHECK FUNCTION vs TEMPERATURE (V_{BAT} = 39.6)

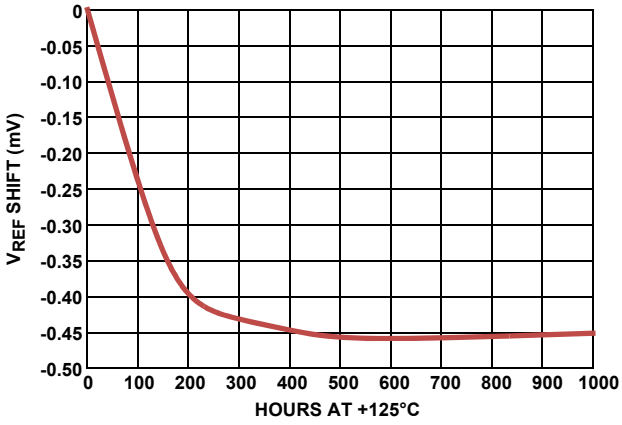


FIGURE 11. V_{REF} SHIFT OVER HTOL

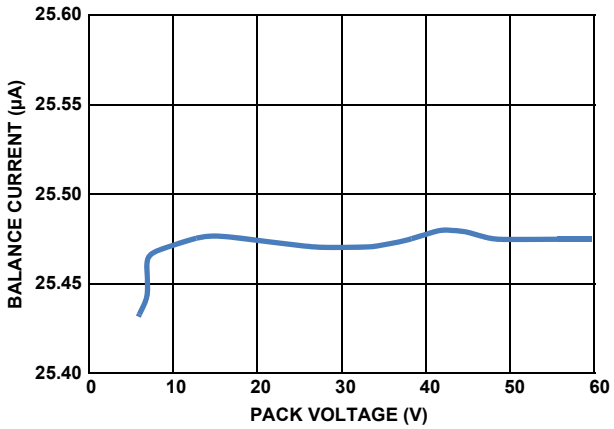


FIGURE 12. BALANCE CURRENT vs PACK VOLTAGE

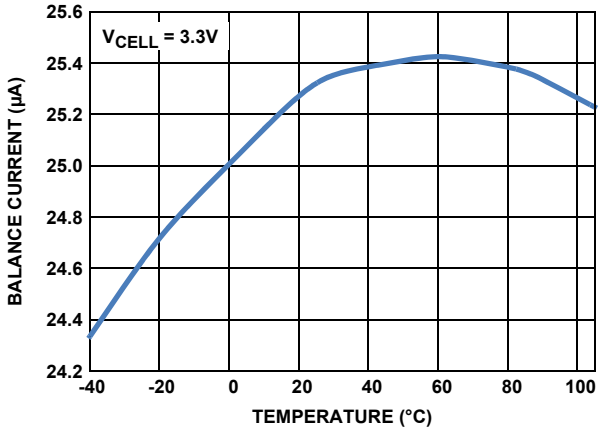


FIGURE 13. BALANCE CURRENT vs TEMPERATURE

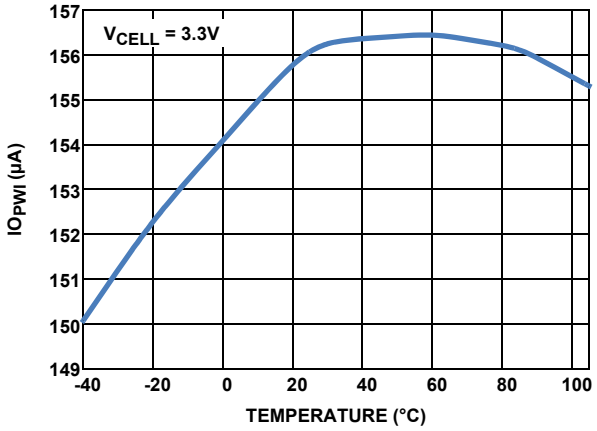


FIGURE 14. OPEN WIRE TEST CURRENT vs TEMPERATURE (150µA SETTING)

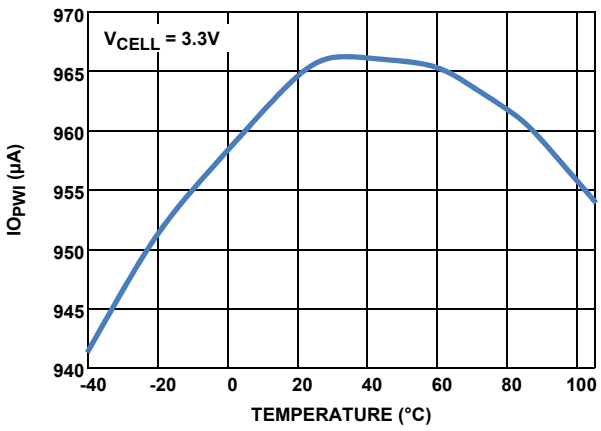


FIGURE 15. OPEN WIRE TEST CURRENT vs TEMPERATURE (1mA SETTING)

Typical Performance Curves (Continued)

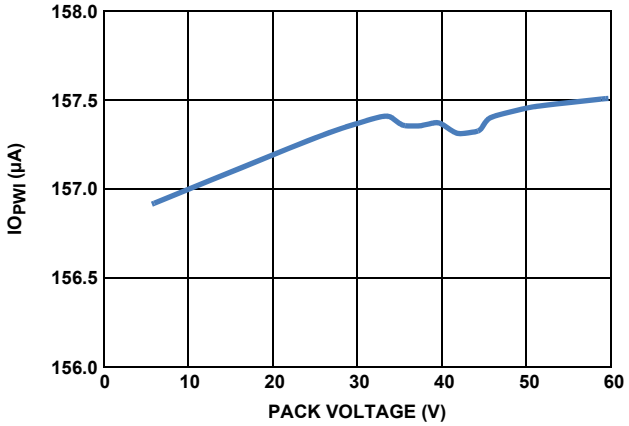


FIGURE 16. OPEN WIRE TEST CURRENT vs PACK VOLTAGE (150µA SETTING)

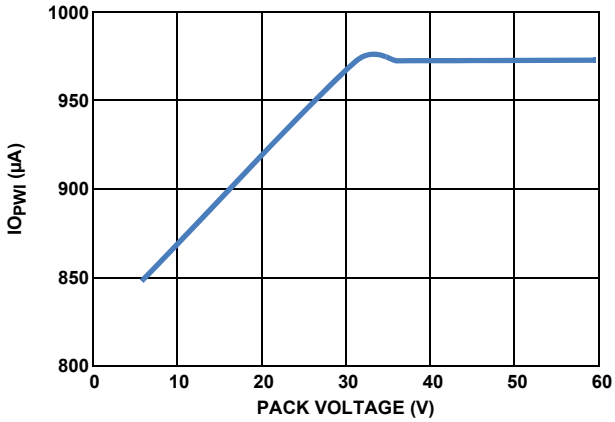


FIGURE 17. OPEN WIRE TEST CURRENT vs PACK VOLTAGE (1mA SETTING)

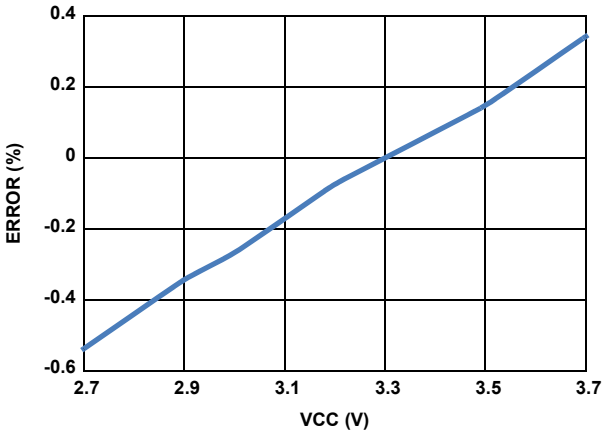


FIGURE 18. 4MHz OSCILLATOR ERROR vs VCC

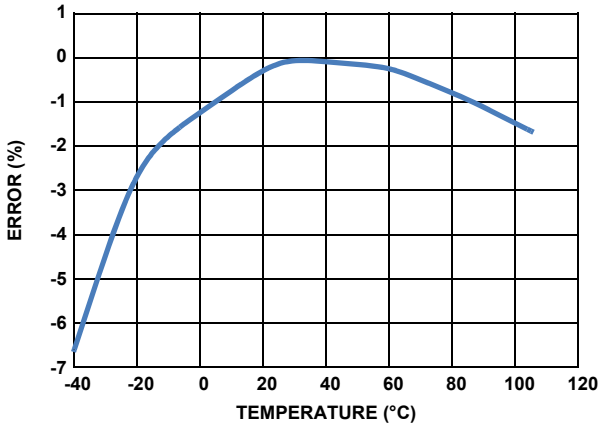


FIGURE 19. 4MHz OSCILLATOR ERROR vs TEMPERATURE

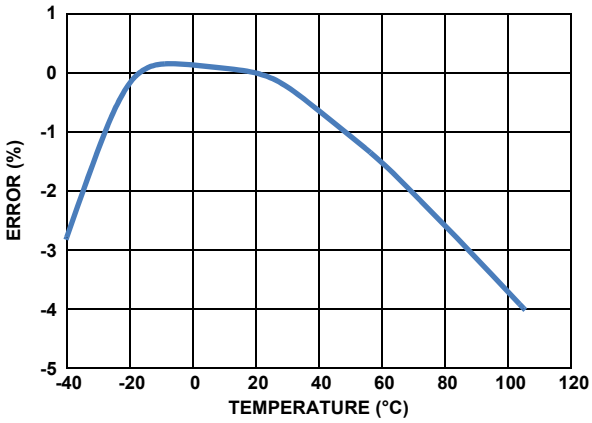


FIGURE 20. 32kHz OSCILLATOR ERROR vs TEMPERATURE

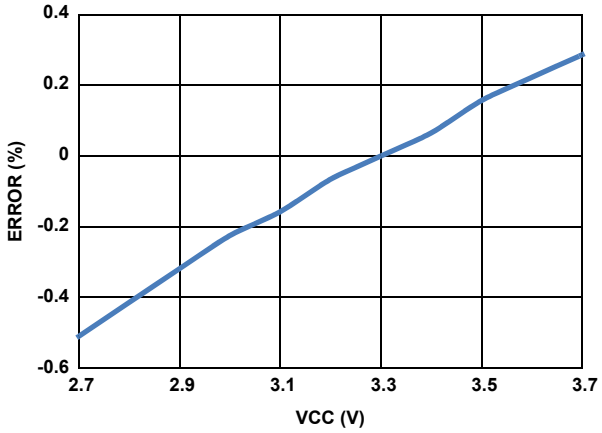


FIGURE 21. 32kHz OSCILLATOR ERROR vs VCC

Typical Performance Curves (Continued)

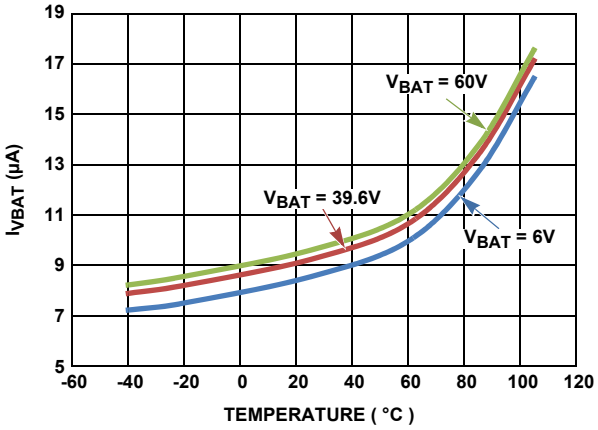


FIGURE 22A. PACK VOLTAGE SLEEP CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (STANDALONE MODE)

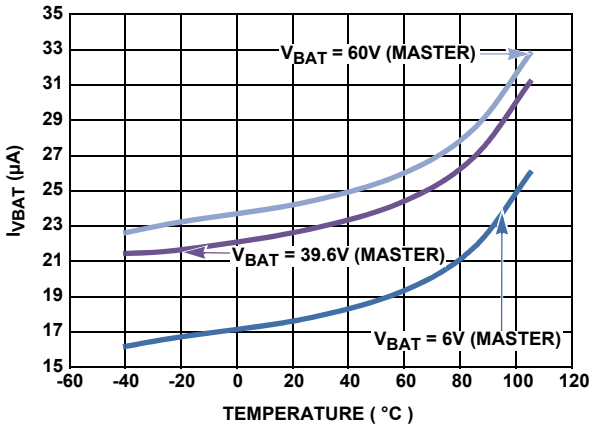


FIGURE 22B. PACK VOLTAGE SLEEP CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN MODE)

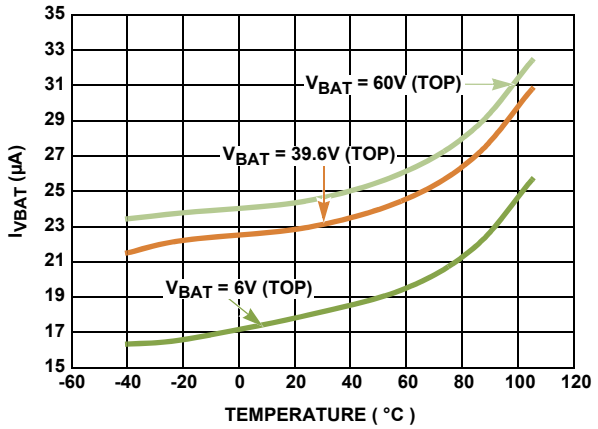


FIGURE 22C. PACK VOLTAGE SLEEP CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN MODE)

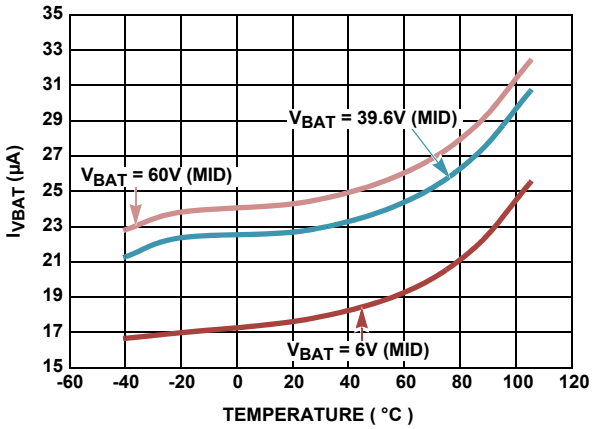


FIGURE 22D. PACK VOLTAGE SLEEP CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN MODE)

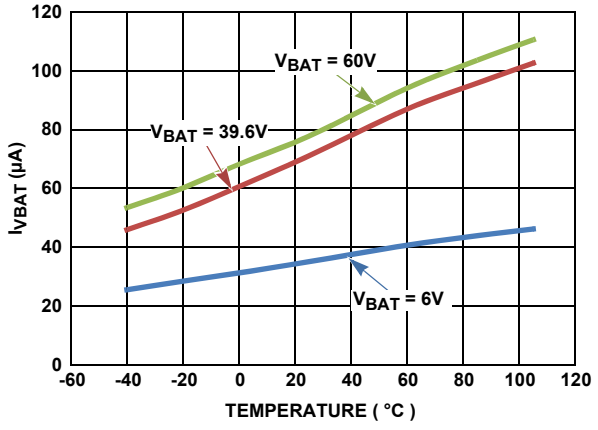


FIGURE 23A. PACK VOLTAGE SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (STANDALONE MODE)

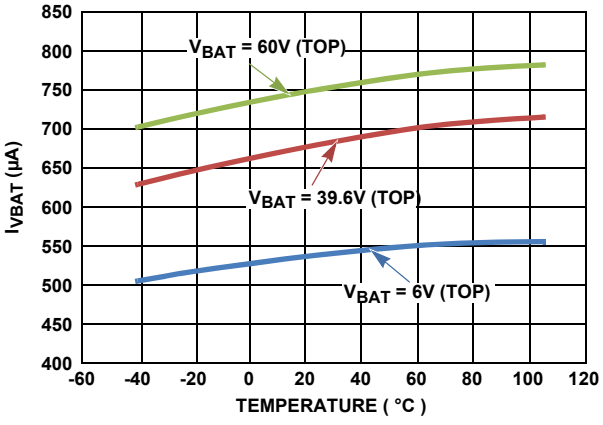


FIGURE 23B. PACK VOLTAGE SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN TOP)

Typical Performance Curves (Continued)

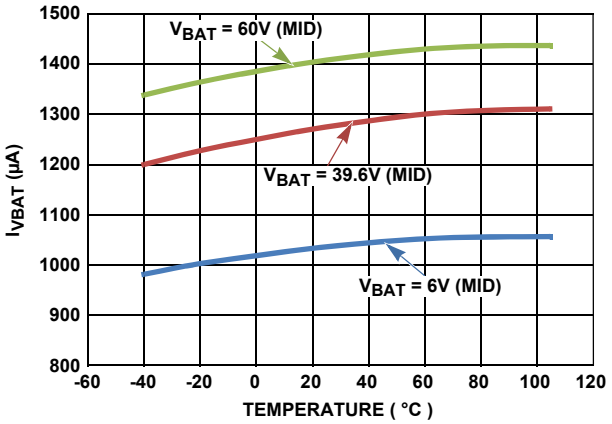


FIGURE 23C. PACK VOLTAGE SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN MIDDLE)

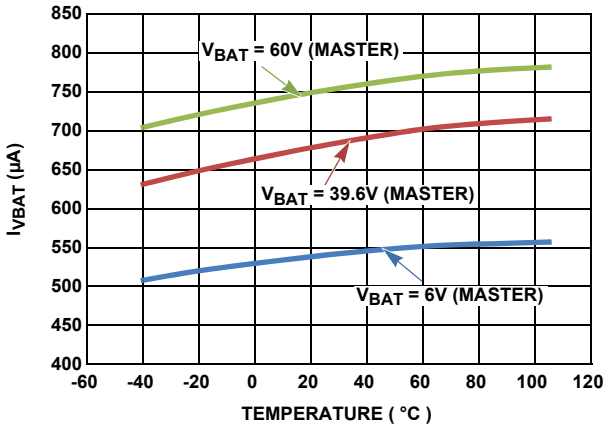


FIGURE 23D. PACK VOLTAGE SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN MASTER)

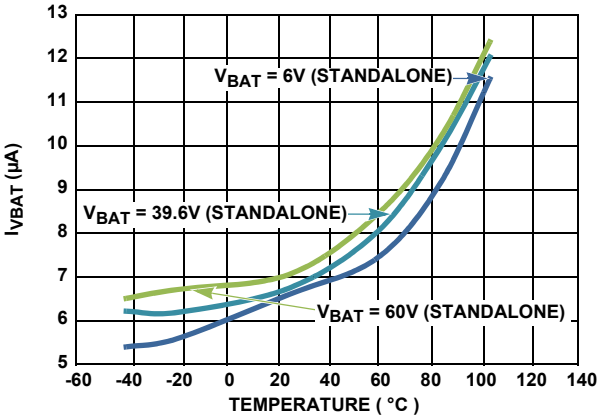


FIGURE 24A. PACK VOLTAGE SHUTDOWN CURRENT vs TEMPERATURE (EN = 0) AT 6V, 39.6V, 60V

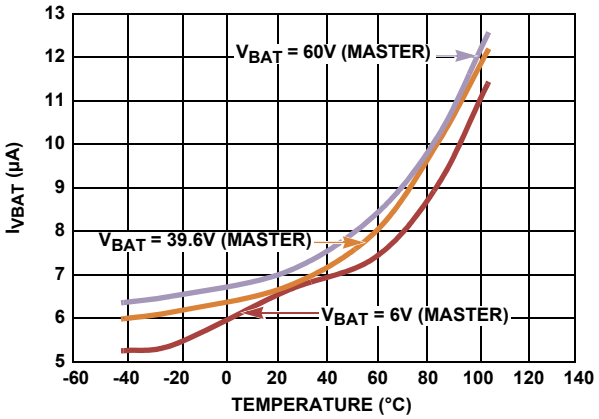


FIGURE 24B. V_{BAT} SHUTDOWN CURRENT vs TEMPERATURE (EN = 0) AT 6V, 39.6V, 60V

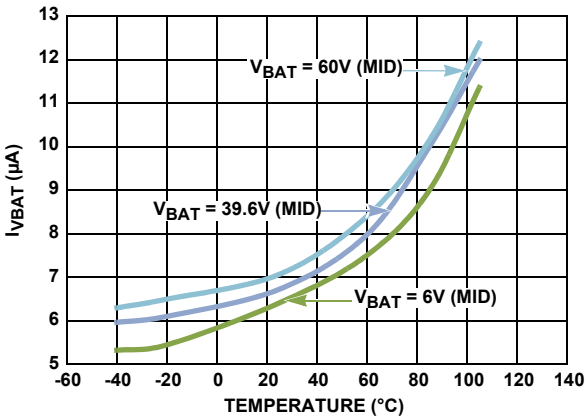


FIGURE 24C. V_{BAT} VOLTAGE SHUTDOWN CURRENT vs TEMPERATURE (EN = 0) AT 6V, 39.6V, 60V

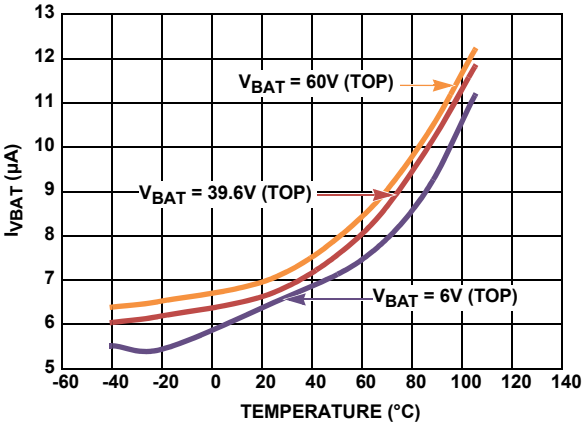


FIGURE 24D. V_{BAT} VOLTAGE SHUTDOWN CURRENT vs TEMPERATURE (EN = 0) AT 6V, 39.6V, 60V

Typical Performance Curves (Continued)

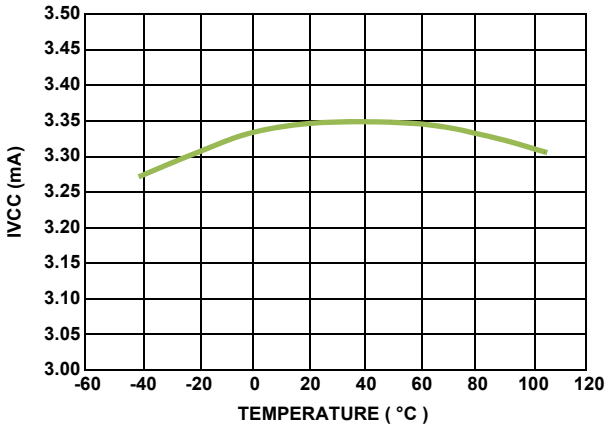


FIGURE 25. VCC SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V

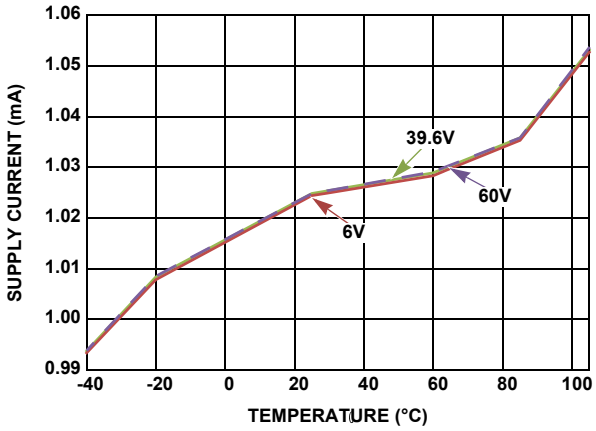


FIGURE 26. V3P3 SUPPLY CURRENT vs TEMPERATURE

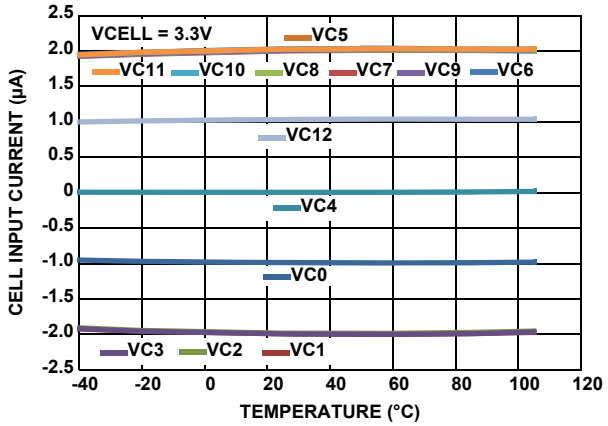


FIGURE 27. CELL INPUT CURRENT vs TEMPERATURE

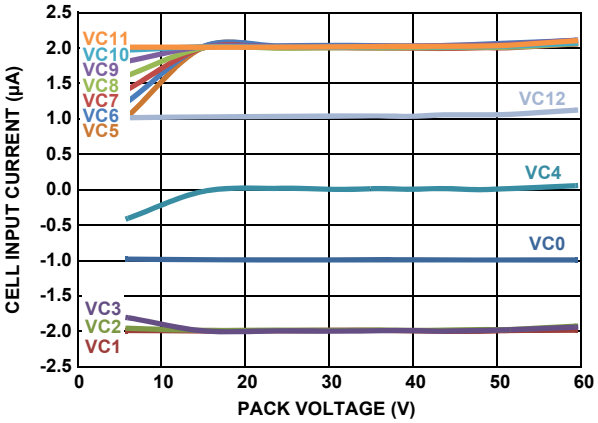


FIGURE 28. CELL INPUT CURRENT vs PACK VOLTAGE (+25°C)

Device Description and Operation

The ISL94212 is a Li-ion battery manager IC that supervises up to 12 series connected cells. Up to 14 ISL94212 devices can be connected in series to support systems with up to 168 cells. The ISL94212 provides accurate monitoring, cell balance control, and diagnostic functions. The ISL94212 includes a voltage reference, 14 bit A/D converter and registers for control and data. An external microcontroller communicates to the ISL94212 through an SPI interface. Series connected ISL94212 devices communicate to each other via a proprietary daisy chain communications interface.

The ISL94212 devices handle daisy chain communications differently depending on their position within the daisy chain. The ISL94212 at one end of the daisy chain acts as a master device for communication purposes. The master device, also called the bottom device, occupies the first position in the daisy chain and communicates to a host microcontroller using an SPI interface. A single daisy chain port then connects the master device to the next device in the daisy chain.

The device at the other end of the daisy chain from the master is the top device. The top device has a single daisy chain port connection to the device below. Devices other than the master and top devices are middle devices. Middle devices have two daisy chain port connections. The up port connects to the device above while the down port connects to the device below. The master ISL94212 device is device number 1. The top device is device number n, where n equals the total number of ISL94212 devices in the daisy chain. The middle devices are numbered 2 to (n-1) with device number 2 being connected to the master device. If n = 2, then there is a master device and a top device, with no middle device.

When multiple ISL94212 devices are connected to a series of cells, their power supply domains are normally non-overlapping. The lower (VSS) supply of each ISL94212 nominally connects to the same potential as the upper (V_{BAT}) supply of the ISL94212 device below.

The ISL94212 provides two multiple parameter measurement “scanning” modes in addition to single parameter direct measurement capability. These scanning modes provide pseudo simultaneous measurement of all cell voltages in the stack. In daisy chain applications all measurement data is sent with the corresponding device stack address (the position within the daisy chain), parameter identifier, and data address. In stand alone applications (non-daisy chain) data is sent without additional address information. This maximizes the throughput for full duplex SPI operation. Daisy chain communication throughput is maximized by allowing streamed data (accessed by a “read all data” address).

The addressed device, the top device and the bottom device act as masters for the purposes of communications timing. All other devices are repeaters, passing data up or down the chain.

The only filtering applied to the ADC measurements is that resulting from external protection circuits and the limited bandwidth of the measurement path. No additional filtering is performed within the part. This arrangement is typically needed to maintain timing integrity between the cell voltage and pack current measurements. The ISL94212 does not measure current. The system performs this separately using other measurement systems. However, the ISL94212 does apply filtering to the fault detection systems.

Power Modes

The ISL94212 has three main power modes: **Normal mode**, **Sleep mode** and **Shutdown mode** (“off”).

Sleep mode is entered in response to a *Sleep* command or after a watchdog timeout. Only the communications input circuits, low speed oscillator and internal registers are active in **Sleep mode**, allowing the part to perform timed scan and balancing activity and to wake up in response to communications.

Drive the enable pin low to place the part in **Shutdown mode**. When entering Shutdown mode, the internal bias for most of the IC is powered down except digital core, sleep mode regulators, and digital input buffers. When exiting, the device powers up and does not reload the factory programmed configuration data from EEPROM.

The **Normal mode** consists of an Active state and a Standby state. In the Standby state, all systems are powered and the device is ready and waiting to perform an operation in response to commands from the host microcontroller. In the Active state, the device performs an operation, such as ADC conversion, open wire detection, etc.

Measurement Modes

The ISL94212 provides three types of measurement modes.

- Scan Once
- Scan Continuous
- Measure

In **Scan Once mode** the part performs the requested scan a single time. In **Scan Continuous mode** the ISL94212 performs repeated scans at intervals controlled by registers settings. **Measure mode** allows a single parameter to be measured.

The ISL94212 ignores a Scan or Measure command, when the device is already in a scan mode or measure mode. But, the command passes through to other devices in the daisy chain. All other communications functions respond normally while the device is scanning or measuring.

Measurement Mode Commands

Measurement modes are activated by commands from an external microcontroller. The ISL94212 uses a memory mapped command structure. Commands are sent to the device using a memory read operation from a specific address. The addresses for the measurement mode commands[1] are shown in Table 1.

There are other commands that perform other actions, but these are discussed in other sections.

1. In this document, the terminology for a hex value (e.g., h0000) is modified by a leading value (e.g., 16’) which defines the number of bits. For the measurement mode command address, a value of 6’h02 refers to a binary value of ‘00 0010’.

TABLE 1. MEASUREMENT MODE COMMAND ADDRESSES

REGISTER ADDRESS	COMMAND SUFFIX	COMMAND
SCAN ONCE		
6'h01	6'h00	Scan Voltages
6'h02	6'h00	Scan Temperatures
6'h03	6'h00	Scan Mixed
6'h04	6'h00	Scan Wires
6'h05	6'h00	Scan All
SCAN CONTINUOUS		
6'h06	6'h00	Scan Continuous
MEASURE		
6'h08	6 bit addr of element to measure	Measure

Scan Once

Five different scan functions are available in single scan (**Scan Once mode**.) Each Scan function is activated by a command from the host microcontroller. The scan functions are:

1. Scan Voltages
2. Scan Temperatures
3. Scan Mixed
4. Scan Wires
5. Scan All

The **Scan Once** functions are synchronous: all addressed stack devices begin scanning immediately following command receipt. There is a scan start latency between subsequent stack devices of one daisy chain clock cycle (e.g., for a stack of 10 devices with a daisy chain operating at 500kHz, the scan start latency between the bottom and top stack devices is approximately 20µs).

Scan Voltages

The **Scan Voltages** command causes the addressed part (or all parts if the common address is used) to scan through the cell voltage inputs followed by the Pack Voltage. IC temperature is also recorded for use with the internal calibration routines. Cell voltages connected to each device are scanned in order from cell-12 (top) to cell-1 (bottom). Cell overvoltage and undervoltage compares are performed on each cell voltage sample. The V_{BAT} and VSS connections are also checked at the end of the scan.

Cell voltage and pack voltage data, along with any fault conditions are stored in local memory ready for reading by the system host microcontroller. If there is a fault condition, the device sets the $\overline{\text{FAULT}}$ pin and returns a fault signal (sent down the stack) on completion of a scan. Devices revert to the standby state on completion of the scan activity.

Scan Temperatures

The **Scan Temperatures** command causes the addressed part (or all parts if the common address is used) to scan through the internal and 4 external temperature signals followed by multiplexer loopback and reference measurements. The loopback and reference measurements are part of the internal diagnostics function. Over-temperature compares are performed on each temperature measurement depending on the condition of the appropriate bit in the *Fault Setup* register.

Temperature data, along with any fault conditions, are stored in local memory ready for reading by the system host microcontroller. If there is a fault condition, the device sets the $\overline{\text{FAULT}}$ pin and returns a fault signal (sent down the stack) on completion of a scan. Devices revert to the standby state on completion of the scan activity.

Scan Mixed

The **Scan Mixed** command causes the addressed part (or all parts if the common address is used) to scan through the cell voltage inputs (followed by the pack voltage) with a single external input (ExT1) interposed. IC temperature is also recorded for use with the internal calibration routines. Cell voltages connected to each device are scanned in order from cell-12 (top) to cell-1 (bottom). The external input ExT1 is scanned in the middle of the cell voltages such that half the cells are sampled before ExT1 and half after ExT1. This mode allows ExT1 to be used for an external voltage measurement, such as a current sensing and performs it along with the cell voltage measurements, reducing the latency between measurements. Cell overvoltage and cell undervoltage compares are performed on each cell voltage sample. The V_{BAT} and VSS conditions are also checked at the end of the scan.

The **Scan Mixed** command is intended for use in standalone systems, or by the Master device in stacked applications, and would typically measure a single system parameter, such as battery current. Other stack devices also measure their ExT1 input but these would normally be ignored by the host.

Cell voltage, pack voltage and ExT1 data, along with any fault conditions are stored in local memory ready for reading by the system host microcontroller. Access the data from the ExT1 measurement by a direct *Read ET1 Voltage* command or by the All Temperatures read command. If there is a fault condition, the device sets the $\overline{\text{FAULT}}$ pin and returns a fault signal (sent down the stack) on completion of a scan. Devices revert to the standby state on completion of the scan activity.

Scan Wires

The **Scan Wires** command causes the addressed part (or all parts if the common address is used) to measure all the VCn pin voltages while applying load currents to each input pin in turn. This is part of the fault detection system.

If there is a fault condition, the device sets the $\overline{\text{FAULT}}$ pin and returns a fault signal (sent down the stack) on completion of a scan. No cell voltage data is sent as a result of the *Scan Wires* command. Devices revert to the standby state on completion of this activity.

Scan All

The **Scan All** command incorporates the Scan Voltages, Scan Wires and Scan Temperatures commands and causes the addressed part (or all parts if the common address is used) to execute each of these three scan functions once, in sequence (see Figure 29 on page 25 for example on timing).

Scan Continuous

Scan Continuous mode is used primarily for fault monitoring and incorporates the scan voltages, scan temperatures and scan wires commands.

The **Scan Continuous** command causes the addressed part to set the SCAN bit in the Device Setup register and performs a succession of scans at a predetermined scan rate. Each device operates asynchronously on its own clock. This is similar to the **Scan All** command except that the scans are repeated at intervals determined by the SCN0-3 bits in the Fault Setup register. The Scan Inhibit command is used to stop scanning (i.e., receipt of this command by the target device resets the SCAN bit and stops the scan continuous function).

The ISL94212 provides an option that pauses cell balancing activity while measuring cell voltages in **Scan Continuous mode**. This is controlled by the BDDS bit in the Device Setup register. If BDDS is set, then cell balancing is inhibited during cell voltage measurement and for 10ms before the cell voltages are scanned. Balancing is reenabled at the end of the scan to allow balancing to continue. This function only applies during the scan continuous and the auto balance functions and allows the implementation of a circuit arrangement that can be used to diagnose the condition of external balancing components. It is up to the host microcontroller to manually stop balancing functions (if required) when operating a scan once or measure command.

The **Scan Continuous** scan interval is set using the SCN3:0 bits (lower nibble of the Fault Setup register.) The temperature and wire scans occur at slower rates and depend on the value of the scan interval selected. The scan system is synchronized such that the wire and temperature scans always follow a voltage scan. The three scan sequences, depending on the scans required at a particular instance, are as follows:

- Scan Voltages
- Scan Voltages, Scan Wires
- Scan Voltages, Scan Wires, Scan Temperatures.

The temperature and wire scans occur at 1/5 the voltage scan rate for voltage scan intervals above 128ms. Below this value the temperature scan interval is fixed at 512ms. The behavior of the wire scan interval is determined by the WSCN bit in the Fault Setup register. A bit value of '1' causes the wire scan to be performed at the same rate as the temperature scan. A bit value of '0' causes the wire scan rate to track the voltage scan rate for voltage scan intervals above 512ms while at and below this value the wire scan is performed at a fixed 512ms rate. Table 2 shows the various scan rate combinations available.

Data is not automatically returned while devices are in **Scan Continuous mode** except in the case where a fault condition is detected. The results of voltage and temperature scans are stored in local volatile memory and may be accessed at any time by the system host microcontroller. Devices may be operated in **Scan Continuous mode** while in **Normal mode** or in **Sleep mode**. Devices revert to the **Sleep mode** or remain in **Normal mode**, as applicable on completion of each scan.

The response to a detected fault condition is to send the fault signal, either immediately in the case of standalone devices or daisy chain devices in **Normal mode**, or following transmission of the wakeup signal if the device is being used in a daisy chain configuration and is in **Sleep mode**.

To operate the "Scan Continuous" function in **Sleep mode** the host microcontroller simply configures the ISL94212, starts the **Scan Continuous mode** and then sends the Sleep command. The ISL94212 then wakes itself up each time a scan is required. Note that for the fastest scan settings (scan interval codes 0000, 0001 and 0010) the main measurement functions do not power down between scans, since the ISL94212 remains in **Normal mode**.

TABLE 2. SCAN CONTINUOUS TIMING MODES

SCAN INTERVAL SCN3:0	SCAN INTERVAL (ms)	TEMP SCAN (ms)	WIRE SCAN WSCN = 0 (ms)	WIRE SCAN WSCN = 1 (ms)
0000	16	512	512	512
0001	32	512	512	512
0010	64	512	512	512
0011	128	512	512	512
0100	256	1024	512	1024
0101	512	2048	512	2048
0110	1024	4096	1024	4096
0111	2048	8192	2048	8192
1000	4096	16384	4096	16384
1001	8192	32768	8192	32768
1010	16384	65536	16384	65536
1011	32768	131072	32768	131072
1100	65536	262144	65536	262144

Measure

This command allows a single cell voltage, internal temperature, any of the four external temperature inputs or the secondary voltage reference measurements to be made. The command incorporates a 6-bit suffix that contains the address of the required measurement element. See Table 3 on page 24. The device matching the target address responds by conducting the single measurement and loading the result to local memory. The host microcontroller then reads from the target device to obtain the measurement result. All devices revert to the standby state on completion of this activity.

TABLE 3. MEASURE COMMAND TARGET ELEMENT ADDRESSES

MEASURE COMMAND	MEASURE ELEMENT ADDRESS (SUFFIX)	DESCRIPTION
6'h08	6'h00	V_{BAT} Voltage
	6'h01	Cell 1 Voltage
	6'h02	Cell 2 Voltage
	6'h03	Cell 3 Voltage
	6'h04	Cell 4 Voltage
	6'h05	Cell 5 Voltage
	6'h06	Cell 6 Voltage
	6'h07	Cell 7 Voltage
	6'h08	Cell 8 Voltage
	6'h09	Cell 9 Voltage
	6'h0A	Cell 10 Voltage
	6'h0B	Cell 11 Voltage
	6'h0C	Cell 12 Voltage
	6'h10	Internal temperature reading
	6'h11	External temperature input 1 reading
	6'h12	External temperature input 2 reading
	6'h13	External temperature input 3 reading
	6'h14	External temperature input 4 reading
	6'h15	Reference voltage (raw ADC) value. Use to calculate corrected reference value using reference coefficient data. See page 2 data, address 6'h38 – 6'h3A.

Cell Voltage Measurement Accuracy

The cell voltage monitoring system comprises two basic elements; a level shift to eliminate the cell common mode voltage and an analog-to-digital conversion of the cell voltage.

Each ISL94212 is calibrated at a specific cell input voltage value, V_{NOM}. Cell voltage measurement error data is given in "MEASUREMENT SPECIFICATIONS" on page 9 for various voltage and temperature ranges with voltage ranges defined with respect to V_{NOM}. Plots showing the typical error distribution over the full input range are included in the "Typical Performance Curves" section beginning on page 15.

Temperature Monitoring

One internal and four external temperature inputs are provided together with a switched bias voltage output (TEMPREG, pin 29). The voltage at the TEMPREG output is nominally equal to the ADC reference voltage such that the external voltage measurements are ratiometric to the ADC reference (see Figure 61 on page 85).

The temperature inputs are intended for use with external resistor networks using NTC type thermistor sense elements but may also be used as general purpose analog inputs. Each temperature input is applied to the ADC via a multiplexer. The ISL94212 converts the voltage at each input and loads the 14-bit result to the appropriate register.

The TEMPREG output is turned "on" in response to a **Scan temperatures** or **Measure temperature** command. A dwell time of 2.5ms is provided to allow external circuits to settle, after which the ADC measures each external input in turn. The TEMPREG output turns "off" after measurements are completed.

Figure 29 on page 25 shows an example temperature scan with the ISL94212 operating in **scan continuous mode** with a scan interval of 512ms. The preceding voltage and wire scans are shown for comparison.

The external temperature inputs are designed such that an open connection results in the input being pulled up to the full scale input level. This function is provided by a switched 10MΩ pull-up from each input to VCC. This feature is part of the fault detection system and is used to detect open pins.

The internal IC temperature, along with the auxiliary reference voltage and multiplexer loopback signals, are sampled in sequence with the external signals using the scan temperatures command.

The converted value from each temperature input is also compared to the external over-temperature limit and open connection threshold values on condition of the [*TST4:1*] bits in the Fault Setup register (see "Fault Setup:" on page 64.) If a TSTn bit is set to "1", then the temperature value is compared to the external temperature threshold and a fault occurs if the measured value is lower than the threshold value. If a TSTn bit is set to "0", then the temperature measurement is not compared to the threshold value and no fault occurs. The [TST4:1] bits are "0" by default.

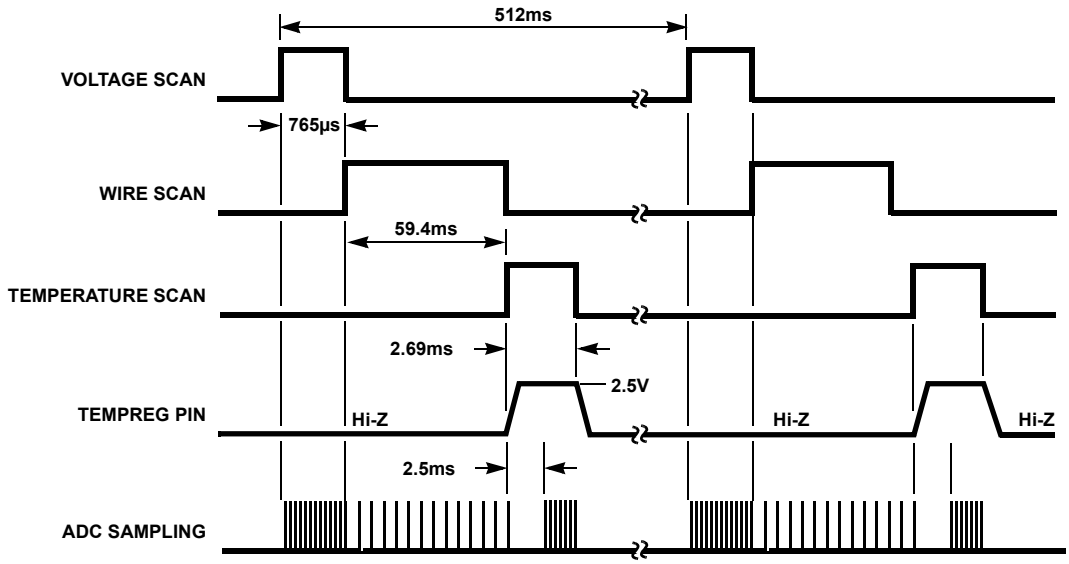


FIGURE 29. SCAN TIMING EXAMPLE DURING **SCAN CONTINUOUS MODE** AND **SCAN ALL MODE**

Cell Balancing Functions

Cell balancing is an important function in a battery pack consisting of a stack of multiple Li-ion cells. As the cells charge and discharge, differences in each cell's ability to take on and give up charge, typically leads to cells with different states of charge. The problem with a stack of cells having different states of charge is that Li-ion cells have a maximum voltage, above which it should not be charged and a minimum voltage, below which it should not be discharged. The extreme case, where one cell in the stack is at the maximum voltage and one cell is at the minimum voltage, results in a nonfunctional battery stack, since the battery stack cannot be charged or discharged.

Cell balancing is performed using external MOSFETs and external current setting resistors (see Figure 30 on page 30). Each MOSFET is controlled independently by the CB1 to CB12 pins of the ISL94212. The CB1 to CB12 outputs are controlled either directly, or indirectly by an external microcontroller through bits in various control registers.

The balancing functions within the ISL94212 are controlled by multiple registers:

- Balance Setup register (All balance modes, see Table 4)
- Balance Status register (All balance modes, see Table 7 on page 26)
- Device Setup register (auto balance mode only, see Table 13 on page 30)
- Watchdog/Balance Time register (timed and auto balance modes, see Table 9 on page 27)
- Balance Values registers (auto balance only, see example in Table 11 on page 28)

Additional registers are provided for the balance timeout (**Timed mode** and **Auto Balance mode**) and balance value (**Auto Balance mode** only).

Balance Setup Register

TABLE 4. BALANCE SETUP REGISTER (ADDRESS 6'h13)

7	6	5	4	3	2	1 9	0 8
BSP2	BSP1	BSP0	BWT2	BWT1	BWT0	BMD1	BMD0
						BEN	BSP3

The Balance Setup register (see Table 7) contents break down into 4 sub groups.

- Balance wait time: BWT[2:0] bits (also referred to as balance dwell time)
- Balance status pointer: BSP[3:0] bits
- Balance enable: BEN bit
- Balance mode: BMD[1:0] bits

BALANCE WAIT TIME

The balance wait time control bits, BWT[2:0], set the interval between balancing operations in **Auto Balance mode**, as shown in Table 5.

TABLE 5. BALANCE WAIT TIME CONTROL BITS

BWT[2:0]	SECONDS
000	0
001	1
010	2
011	4
100	8
101	16
110	32
111	64