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# 14-Bit, 250MSPS/200MSPS/130MSPS ADC

## ISLA214P

The ISLA214P is a series of low power, high performance 14-bit analog-to-digital converters. Designed with Intersil's proprietary FemtoCharge™ technology on a standard CMOS process, the series supports sampling rates of up to 250MSPS. The ISLA214P is part of a pin-compatible family of 12 to 16-bit A/Ds with maximum sample rates ranging from 130MSPS to 500MSPS.

A serial peripheral interface (SPI) port allows for extensive configurability, as well as fine control of various parameters, such as gain and offset. Digital output data is presented in selectable LVDS or CMOS formats, and can be configured as full-width, single data rate (SDR) or half-width, double data rate (DDR). The ISLA214P is available in a 72-contact QFN package with an exposed paddle. Operating from a 1.8V supply, performance is specified over the full industrial temperature range (-40°C to +85°C).

## Key Specifications

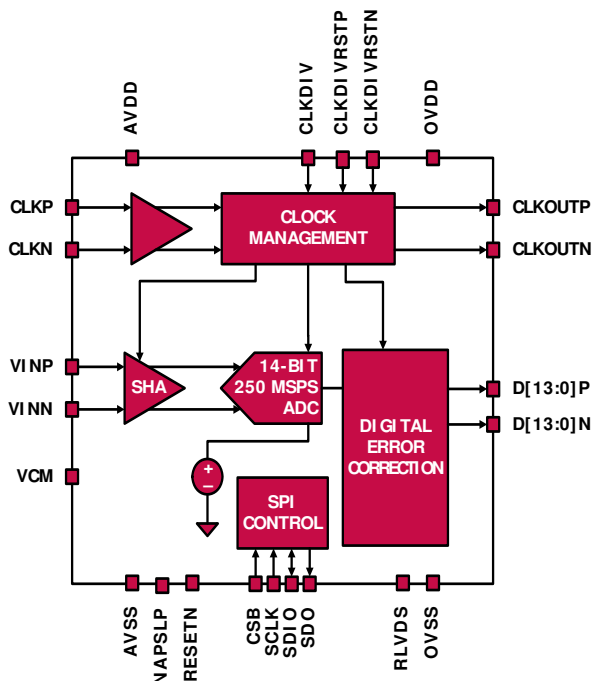
- SNR @ 250/200/130MSPS  
73.0/73.8/74.9dBFS  $f_{IN} = 30\text{MHz}$   
70.6/71.1/70.9dBFS  $f_{IN} = 363\text{MHz}$
- SFDR @ 250/200/130MSPS  
82/88/88dBc  $f_{IN} = 30\text{MHz}$   
78/82/84dBc  $f_{IN} = 363\text{MHz}$
- Total Power Consumption = 480mW @ 250MSPS

## Features

- Single supply 1.8V operation
- Clock duty cycle stabilizer
- 75fs clock jitter
- 700MHz bandwidth
- Programmable built-in test patterns
- Multi-ADC support
  - SPI programmable fine gain and offset control
  - Support for multiple ADC synchronization
  - Optimized output timing
- Nap and sleep modes
  - 200µs sleep wake-up time
- Data output clock
- SDR/DDR LVDS-compatible or LVCMOS outputs
- Selectable clock divider

## Applications

- Radar array processing
- Software defined radios
- Broadband communications
- High-performance data acquisition
- Communications test equipment



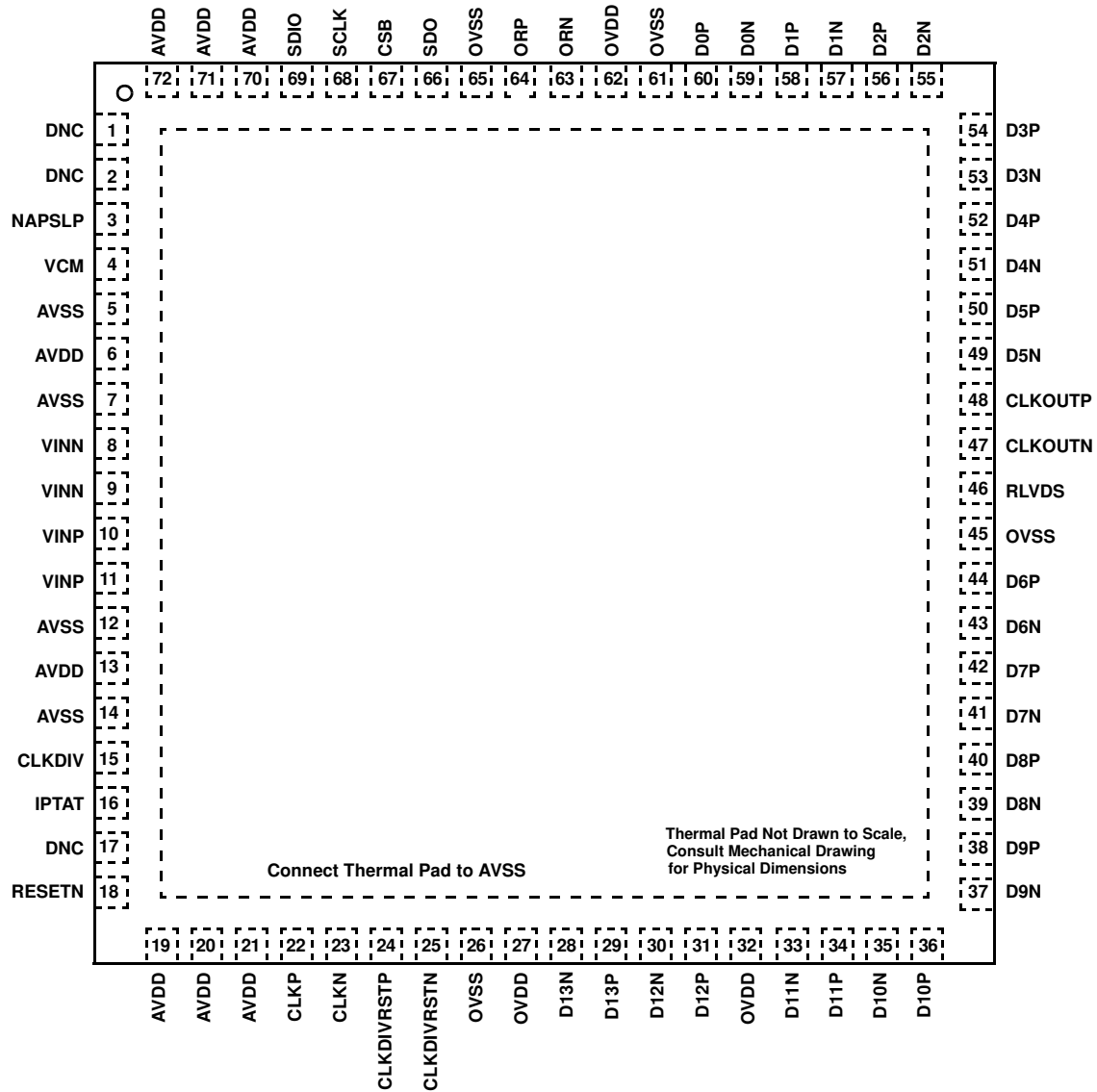
## Pin-Compatible Family

MODEL	RESOLUTION	SPEED (MSPS)
ISLA216P25	16	250
ISLA216P20	16	200
ISLA216P13	16	130
ISLA214P50	14	500
ISLA214P25	14	250
ISLA214P20	14	200
ISLA214P13	14	130
ISLA212P50	12	500
ISLA212P25	12	250
ISLA212P20	12	200
ISLA212P13	12	130

# ISLA214P

## Pin Configuration - LVDS MODE

ISLA214P  
(72 LD QFN)  
TOP VIEW



# ISLA214P

## Pin Descriptions - 72 Ld QFN, LVDS Mode

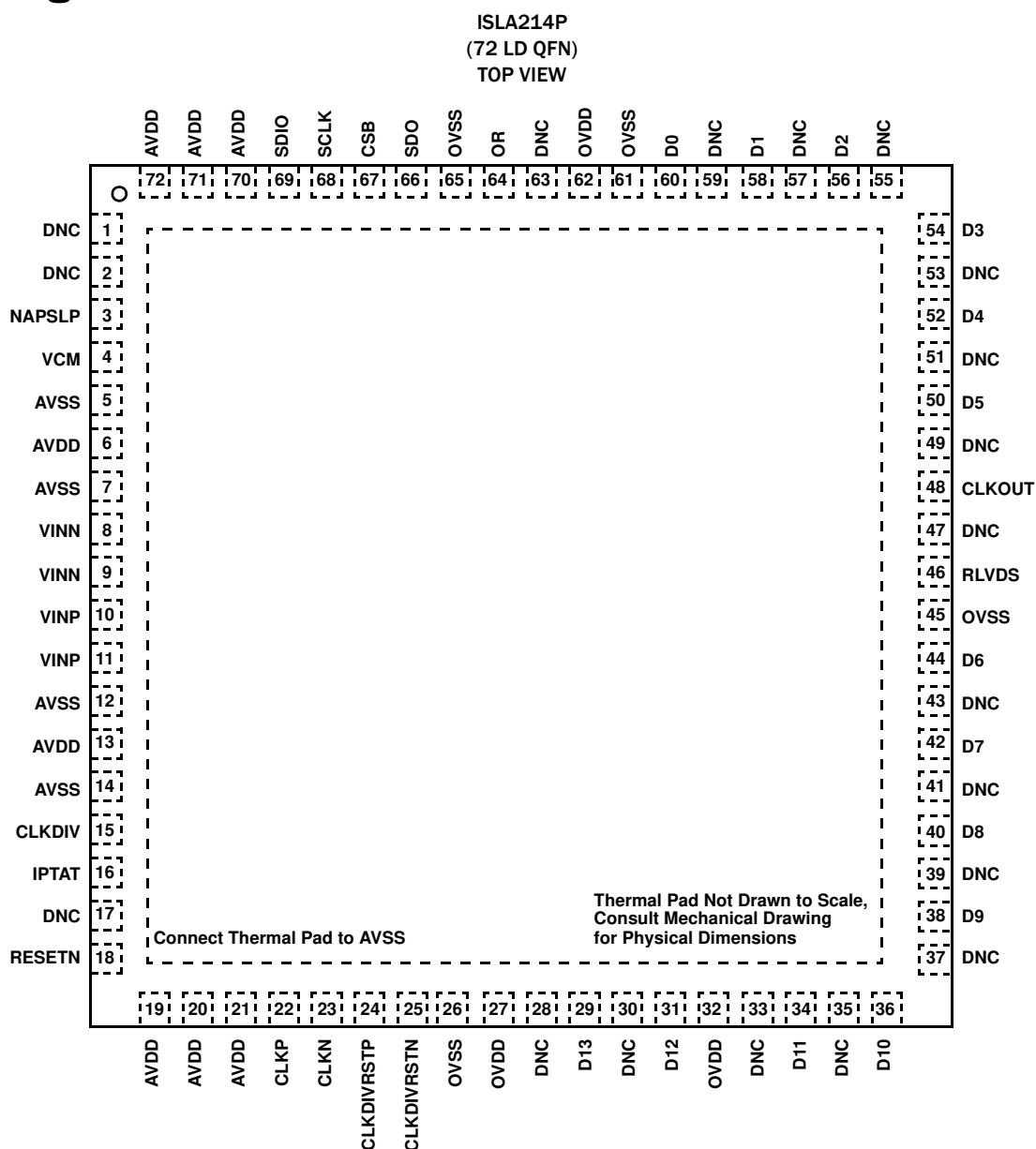
PIN NUMBER	LVDS PIN NAME	LVDS PIN FUNCTION	DDR MODE COMMENTS
1, 2, 17	DNC	Do Not Connect	
6, 13, 19, 20, 21, 70, 71, 72	AVDD	1.8V Analog Supply	
5, 7, 12, 14	AVSS	Analog Ground	
27, 32, 62	OVDD	1.8V Output Supply	
26, 45, 61, 65	OVSS	Output Ground	
3	NAPSLP	Tri-Level Power Control (Nap, Sleep modes)	
4	VCM	Common Mode Output	
8, 9	VINN	Analog Input Negative	
10, 11	VINP	Analog Input Positive	
15	CLKDIV	Tri-Level Clock Divider Control	
16	IPTAT	Temperature Monitor (Output current proportional to absolute temperature)	
18	RESETN	Power On Reset (Active Low)	
22, 23	CLKP, CLKN	Clock Input True, Complement	
24, 25	CLKDIVRSTP, CLKDIVRSTN	Synchronous Clock Divider Reset True, Complement	
28	D13N	LVDS Bit 13(MSB) Output Complement	NC in DDR Mode
29	D13P	LVDS Bit 13 (MSB) Output True	NC in DDR Mode
30	D12N	LVDS Bit 12 Output Complement	DDR Logical Bits 12, 13
31	D12P	LVDS Bit 12 Output True	DDR Logical Bits 12, 13
33	D11N	LVDS Bit 11 Output Complement	NC in DDR Mode
34	D11P	LVDS Bit 11 Output True	NC in DDR Mode
35	D10N	LVDS Bit 10 Output Complement	DDR Logical Bits 10, 11
36	D10P	LVDS Bit 10 Output True	DDR Logical Bits 10, 11
37	D9N	LVDS Bit 9 Output Complement	NC in DDR Mode
38	D9P	LVDS Bit 9 Output True	NC in DDR Mode
39	D8N	LVDS Bit 8 Output Complement	DDR Logical Bits 8, 9
40	D8P	LVDS Bit 8 Output True	DDR Logical Bits 8, 9
41	D7N	LVDS Bit 7 Output Complement	NC in DDR Mode
42	D7P	LVDS Bit 7 Output True	NC in DDR Mode
43	D6N	LVDS Bit 6 Output Complement	DDR Logical Bits 6, 7
44	D6P	LVDS Bit 6 Output True	DDR Logical Bits 6, 7
46	RLVDS	LVDS Bias Resistor (Connect to OVSS with 1% 10k $\Omega$ )	
47, 48	CLKOUTN, CLKOUTP	LVDS Clock Output Complement, True	
49	D5N	LVDS Bit 5 Output Complement	NC in DDR Mode
50	D5P	LVDS Bit 5 Output True	NC in DDR Mode
51	D4N	LVDS Bit 4 Output Complement	DDR Logical Bits 4, 5
52	D4P	LVDS Bit 4 Output True	DDR Logical Bits 4, 5
53	D3N	LVDS Bit 3 Output Complement	NC in DDR Mode
54	D3P	LVDS Bit 3 Output True	NC in DDR Mode
55	D2N	LVDS Bit 2 Output Complement	DDR Logical Bits 2, 3
56	D2P	LVDS Bit 2 Output True	DDR Logical Bits 2, 3
57	D1N	LVDS Bit 1 Output Complement	NC in DDR Mode

# ISLA214P

## Pin Descriptions - 72 Ld QFN, LVDS Mode (Continued)

PIN NUMBER	LVDS PIN NAME	LVDS PIN FUNCTION	DDR MODE COMMENTS
58	D1P	LVDS Bit 1 True	NC in DDR Mode
59	D0N	LVDS Bit 0 (LSB) Output Complement	DDR Logical Bits 0, 1
60	D0P	LVDS Bit 0 (LSB) Output True	DDR Logical Bits 0, 1
63, 64	ORN, ORP	LVDS Over Range Complement, True	DDR Over Range
66	SDO	SPI Serial Data Output	
67	CSB	SPI Chip Select (active low)	
68	SCLK	SPI Clock	
69	SDIO	SPI Serial Data Input/Output	
Exposed Paddle	AVSS	Analog Ground	

## Pin Configuration - CMOS MODE



# ISLA214P

## Pin Descriptions - 72 Ld QFN, CMOS Mode

PIN NUMBER	CMOS PIN NAME	CMOS PIN FUNCTION	DDR MODE COMMENTS
1, 2, 17, 28, 30, 33, 35, 37, 39, 41, 43, 47, 49, 51, 53, 55, 57, 59, 63	DNC	Do Not Connect	
6, 13, 19, 20, 21, 70, 71, 72	AVDD	1.8V Analog Supply	
5, 7, 12, 14	AVSS	Analog Ground	
27, 32, 62	OVDD	1.8V Output Supply	
26, 45, 61, 65	OVSS	Output Ground	
3	NAPSLP	Tri-Level Power Control (Nap, Sleep modes)	
4	VCM	Common Mode Output	
8, 9	VINN	Analog Input Negative	
10, 11	VINP	Analog Input Positive	
15	CLKDIV	Tri-Level Clock Divider Control	
16	IPTAT	Temperature Monitor (Output current proportional to absolute temperature)	
18	RESETN	Power On Reset (Active Low)	
22, 23	CLKP, CLKN	Clock Input True, Complement	
24, 25	CLKDIVRSTP, CLKDIVRSTN	Synchronous Clock Divider Reset True, Complement	
29	D13	CMOS Bit 13 (MSB) Output	NC in DDR Mode
31	D12	CMOS Bit 12 Output	DDR Logical Bits 12, 13
34	D11	CMOS Bit 11 Output	NC in DDR Mode
36	D10	CMOS Bit 10 Output	DDR Logical Bits 10, 11
38	D9	CMOS Bit 9 Output	NC in DDR Mode
40	D8	CMOS Bit 8 Output	DDR Logical Bits 8, 9
42	D7	CMOS Bit 7 Output	NC in DDR Mode
44	D6	CMOS Bit 6 Output	DDR Logical Bits 6, 7
46	RLVDS	LVDS Bias Resistor (connect to OVSS with 1% 10k $\Omega$ )	
48	CLKOUT	CMOS Clock Output	
50	D5	CMOS Bit 5 Output	NC in DDR Mode
52	D4	CMOS Bit 4 Output	DDR Logical Bits 4, 5
54	D3	CMOS Bit 3 Output	NC in DDR Mode
56	D2	CMOS Bit 2 Output	DDR Logical Bits 2, 3
58	D1	CMOS Bit 1 Output	NC in DDR Mode
60	D0	CMOS Bit 0 (LSB) Output	DDR Logical Bits 0, 1
64	OR	CMOS Over Range	DDR Over Range
66	SDO	SPI Serial Data Output	
67	CSB	SPI Chip Select (active low)	
68	SCLK	SPI Clock	
69	SDIO	SPI Serial Data Input/Output	
Exposed Paddle	AVSS	Analog Ground	

# ISLA214P

## Ordering Information

PART NUMBER (Notes 1,2)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISLA214P13IRZ	ISLA214P13 IRZ	-40°C to +85°C	72 Ld QFN	L72.10x10E
ISLA214P20IRZ	ISLA214P20 IRZ	-40°C to +85°C	72 Ld QFN	L72.10x10E
ISLA214P25IRZ	ISLA214P25 IRZ	-40°C to +85°C	72 Ld QFN	L72.10x10E
<i>Coming Soon</i> ISLA214P13IR1Z	ISLA214P13 IR1Z	-40°C to +85°C	48 Ld QFN	TBD
<i>Coming Soon</i> ISLA214P20IR1Z	ISLA214P20 IR1Z	-40°C to +85°C	48 Ld QFN	TBD
<i>Coming Soon</i> ISLA214P25IR1Z	ISLA214P25 IR1Z	-40°C to +85°C	48 Ld QFN	TBD
ISLA214IR72EV1Z	Evaluation Board			

### NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), please see respective device information page for [ISLA214P](#). For more information on MSL please see techbrief [TB363](#).

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# ISLA214P

## Absolute Maximum Ratings

AVDD to AVSS	-0.4V to 2.1V
OVDD to OVSS	-0.4V to 2.1V
AVSS to OVSS	-0.3V to 0.3V
Analog Inputs to AVSS	-0.4V to AVDD + 0.3V
Clock Inputs to AVSS	-0.4V to AVDD + 0.3V
Logic Input to AVSS	-0.4V to OVDD + 0.3V
Logic Inputs to OVSS	-0.4V to OVDD + 0.3V
Latchup (Tested per JESD-78C;Class 2,Level A)	100mA

## Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
72 Ld QFN (Notes 3, 4)	23	0.9
48 Ld QFN (Notes 3, 4)	24	1.0
Operating Temperature	-40°C to +85°C	
Storage Temperature	-65°C to +150°C	
Junction Temperature	+150°C	
Pb-Free Reflow Profile	see link below	
	<a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>	

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTES:

- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief [TB379](#).
- For  $\theta_{JC}$ , the “case temp” location is the center of the exposed metal pad on the package underside.

**Electrical Specifications** All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V,  $T_A$  = -40°C to +85°C (Typical specifications at +25°C),  $A_{IN}$  = -1dBFS,  $f_{SAMPLE}$  = Maximum Conversion Rate (per speed grade). **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	CONDITIONS	ISLA214P25			ISLA214P20			ISLA214P13			UNITS
			MIN (Note 5)	TYP	MAX (Note 5)	MIN (Note 5)	TYP	MAX (Note 5)	MIN (Note 5)	TYP	MAX (Note 5)	
<b>DC SPECIFICATIONS (Note 6)</b>												
<b>Analog Input</b>												
Full-Scale Analog Input Range	$V_{FS}$	Differential	<b>1.95</b>	2.0	<b>2.1</b>	<b>1.95</b>	2.0	<b>2.1</b>	<b>1.95</b>	2.0	<b>2.1</b>	$V_{p,p}$
Input Resistance	$R_{IN}$	Differential		600			600			600		$\Omega$
Input Capacitance	$C_{IN}$	Differential		4.5			4.5			4.5		pF
Full Scale Range Temp. Drift	$A_{VTC}$	Full Temp		108			82			74		ppm/°C
Input Offset Voltage	$V_{OS}$		<b>-5.0</b>	-1.7	<b>5.0</b>	<b>-5.0</b>	-1.7	<b>5.0</b>	<b>-5.0</b>	-1.7	<b>5.0</b>	mV
Common-Mode Output Voltage	$V_{CM}$			0.94			0.94			0.94		V
Common-Mode Input Current (per pin)	$I_{CM}$			2.6			2.6			2.6		$\mu A/MSPS$
<b>Clock Inputs</b>												
Inputs Common Mode Voltage				0.9			0.9			0.9		V
CLKP,CLKN Input Swing (Note 7)				1.8			1.8			1.8		V
<b>Power Requirements</b>												
1.8V Analog Supply Voltage	AVDD		<b>1.7</b>	1.8	<b>1.9</b>	<b>1.7</b>	1.8	<b>1.9</b>	<b>1.7</b>	1.8	<b>1.9</b>	V
1.8V Digital Supply Voltage	OVDD		<b>1.7</b>	1.8	<b>1.9</b>	<b>1.7</b>	1.8	<b>1.9</b>	<b>1.7</b>	1.8	<b>1.9</b>	V
1.8V Analog Supply Current	$I_{AVDD}$			188	<b>200</b>		174	<b>184</b>		152	<b>161</b>	mA
1.8V Digital Supply Current (Note 6)	$I_{OVDD}$	3mA LVDS (SDR)		78.5	<b>88</b>		75	<b>84</b>		68.5	<b>77</b>	mA
Power Supply Rejection Ratio	PSRR	30MHz, 30mV <sub>p,p</sub> signal on AVDD		40			40			40		dB

# ISLA214P

**Electrical Specifications** All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, TA = -40°C to +85°C (Typical specifications at +25°C), AIN = -1dBFS, fSAMPLE = Maximum Conversion Rate (per speed grade). **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	CONDITIONS	ISLA214P25			ISLA214P20			ISLA214P13			UNITS
			MIN (Note 5)	TYP	MAX (Note 5)	MIN (Note 5)	TYP	MAX (Note 5)	MIN (Note 5)	TYP	MAX (Note 5)	
<b>Total Power Dissipation</b>												
Normal Mode	PD	2mA LVDS		454			422			369		mW
		3mA LVDS (SDR)		480	<b>518</b>		448	<b>482</b>		397	<b>428</b>	mW
		3mA LVDS (DDR)		450			410			360		mW
		CMOS (SDR)		432			392			313		mW
		CMOS (DDR)		420			375			310		mW
Nap Mode	PD		55.8	<b>60</b>		52.2	<b>57</b>		48.6	<b>53</b>	mW	
Sleep Mode	PD	CSB at logic high		6	<b>11</b>		6	<b>11</b>		6	<b>10</b>	mW
Nap/Sleep Mode Wakeup Time		Sample Clock Running		200			400			630		µs
<b>AC SPECIFICATIONS</b>												
Differential Nonlinearity	DNL	fIN = 105MHz No Missing Codes	<b>-0.99</b>	±0.3	<b>2.0</b>	<b>-0.99</b>	±0.25	<b>1.4</b>	<b>-0.99</b>	±0.25	<b>1.4</b>	LSB
Integral Nonlinearity	INL	fIN = 105MHz		±2.5			±2.5			±2.5		LSB
Minimum Conversion Rate (Note 8)	fS MIN				<b>40</b>			<b>40</b>			<b>40</b>	MSPS
Maximum Conversion Rate	fS MAX		<b>250</b>			<b>200</b>			<b>130</b>			MSPS
Signal-to-Noise Ratio (Note 9)	SNR	fIN = 30MHz		73			73.8			74.9		dBFS
		fIN = 105MHz	70.1	73		72.1	73.7		73.0	74.3		dBFS
		fIN = 190MHz		72.1			72.8			73.3		dBFS
		fIN = 363MHz		70.6			71.1			70.9		dBFS
		fIN = 461MHz		69.9			70.0			69.5		dBFS
		fIN = 605MHz		68.4			68.5			67.8		dBFS
Signal-to-Noise and Distortion (Note 9)	SINAD	fIN = 30MHz		72.4			73.5			74.6		dBFS
		fIN = 105MHz	69.4	72.4		71.0	73.1		70.8	73.6		dBFS
		fIN = 190MHz		70.7			72.3			72.2		dBFS
		fIN = 363MHz		69.8			70.7			70.6		dBFS
		fIN = 461MHz		66.1			67.4			65.9		dBFS
		fIN = 605MHz		60.5			61.1			61.1		dBFS
Effective Number of Bits (Note 9)	ENOB	fIN = 30MHz		11.73			11.92			12.10		Bits
		fIN = 105MHz	11.29	11.73		11.50	11.83		11.47	11.93		Bits
		fIN = 190MHz		11.45			11.72			11.70		Bits
		fIN = 363MHz		11.30			11.45			11.44		Bits
		fIN = 461MHz		10.69			10.90			10.65		Bits
		fIN = 605MHz		9.76			9.86			9.86		Bits

# ISLA214P

**Electrical Specifications** All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T<sub>A</sub> = -40°C to +85°C (Typical specifications at +25°C), A<sub>IN</sub> = -1dBFS, f<sub>SAMPLE</sub> = Maximum Conversion Rate (per speed grade). **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	CONDITIONS	ISLA214P25			ISLA214P20			ISLA214P13			UNITS
			MIN (Note 5)	TYP	MAX (Note 5)	MIN (Note 5)	TYP	MAX (Note 5)	MIN (Note 5)	TYP	MAX (Note 5)	
Spurious-Free Dynamic Range (Note 9)	SFDR	f <sub>IN</sub> = 30MHz		82		88			88		dBc	
		f <sub>IN</sub> = 105MHz	72	83		72	84		70	83	dBc	
		f <sub>IN</sub> = 190MHz		78			84			78	dBc	
		f <sub>IN</sub> = 363MHz		78			82			84	dBc	
		f <sub>IN</sub> = 461MHz		68			71			68	dBc	
		f <sub>IN</sub> = 605MHz		61			62			61	dBc	
Spurious-Free Dynamic Range Excluding H2, H3	SFDRX23	f <sub>IN</sub> = 30MHz		89		93			99		dBc	
		f <sub>IN</sub> = 105MHz		91			90			95	dBc	
		f <sub>IN</sub> = 190MHz		88			89			91	dBc	
		f <sub>IN</sub> = 363MHz		87			90			95	dBc	
		f <sub>IN</sub> = 461MHz		88			93			94	dBc	
		f <sub>IN</sub> = 605MHz		88			88			87	dBc	
Intermodulation Distortion	IMD	f <sub>IN</sub> = 70MHz		87		86			87		dBFS	
		f <sub>IN</sub> = 170MHz		97		104			101		dBFS	
Word Error Rate	WER			10 <sup>-12</sup>		10 <sup>-12</sup>			10 <sup>-12</sup>			
Full Power Bandwidth	FPBW			700		700			700		MHz	

**NOTES:**

- Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
- Digital Supply Current is dependent upon the capacitive loading of the digital outputs. I<sub>OVDD</sub> specifications apply for 10pF load on each digital output
- See "Clock Input" on page 20.
- The DLL Range setting must be changed for low-speed operation.
- Minimum specification guaranteed when calibrated at +85°C.

**Digital Specifications** Boldface limits apply over the operating temperature range, -40°C to +85°C.

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
<b>INPUTS</b> (Note 10)						
Input Current High (RESETN)	I <sub>IH</sub>	V <sub>IN</sub> = 1.8V	<b>0</b>	1	<b>10</b>	μA
Input Current Low (RESETN)	I <sub>IL</sub>	V <sub>IN</sub> = 0V	<b>-25</b>	-12	<b>-8</b>	μA
Input Current High (SDIO)	I <sub>IH</sub>	V <sub>IN</sub> = 1.8V		4	<b>12</b>	μA
Input Current Low (SDIO)	I <sub>IL</sub>	V <sub>IN</sub> = 0V	<b>-600</b>	-415	<b>-300</b>	μA
Input Current High (CSB)	I <sub>IH</sub>	V <sub>IN</sub> = 1.8V	<b>40</b>	58	<b>75</b>	
Input Current Low (CSB)	I <sub>IL</sub>	V <sub>IN</sub> = 0V		5	<b>10</b>	
Input Current High (CLKDIV)	I <sub>IH</sub>		<b>16</b>	25	<b>34</b>	μA
Input Current Low (CLKDIV)	I <sub>IL</sub>		<b>-34</b>	-25	<b>-16</b>	μA
Input Voltage High (SDIO, RESETN)	V <sub>IH</sub>		<b>1.17</b>			V
Input Voltage Low (SDIO, RESETN)	V <sub>IL</sub>				<b>0.63</b>	V
Input Capacitance	C <sub>DI</sub>			4		pF

# ISLA214P

## Digital Specifications **Boldface limits apply over the operating temperature range, -40 °C to +85 °C. (Continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
<b>LVDS INPUTS (CLKDIVRSTP, CLKDIVRSTN)</b>						
Input Common Mode Range	$V_{ICM}$		<b>825</b>		<b>1575</b>	mV
Input Differential Swing (peak to peak, single-ended)	$V_{ID}$		<b>250</b>		<b>450</b>	mV
CLKDIVRSTP Input Pull-down Resistance	$R_{Ipd}$			100		k $\Omega$
CLKDIVRSTN Input Pull-up Resistance	$R_{Ipu}$			100		k $\Omega$
<b>LVDS OUTPUTS</b>						
Differential Output Voltage (Note 11)	$V_T$	3mA Mode		612		mV <sub>p-p</sub>
Output Offset Voltage	$V_{OS}$	3mA Mode	<b>1120</b>	1150	<b>1200</b>	mV
Output Rise Time	$t_R$			240		ps
Output Fall Time	$t_F$			240		ps
<b>CMOS OUTPUTS</b>						
Voltage Output High	$V_{OH}$	$I_{OH} = -500\mu A$	<b>OVDD - 0.3</b>	OVDD - 0.1		V
Voltage Output Low	$V_{OL}$	$I_{OL} = 1mA$		0.1	<b>0.3</b>	V
Output Rise Time	$t_R$			1.8		ns
Output Fall Time	$t_F$			1.4		ns

### NOTES:

- The Tri-Level Inputs internal switching thresholds are approximately, 0.43V and 1.34V. It is advised to float the inputs, tie to ground or AVDD depending on desired function.
- The voltage is expressed in peak-to-peak differential swing. The peak-to-peak singled-ended swing is 1/2 of the differential swing.

## Timing Diagrams

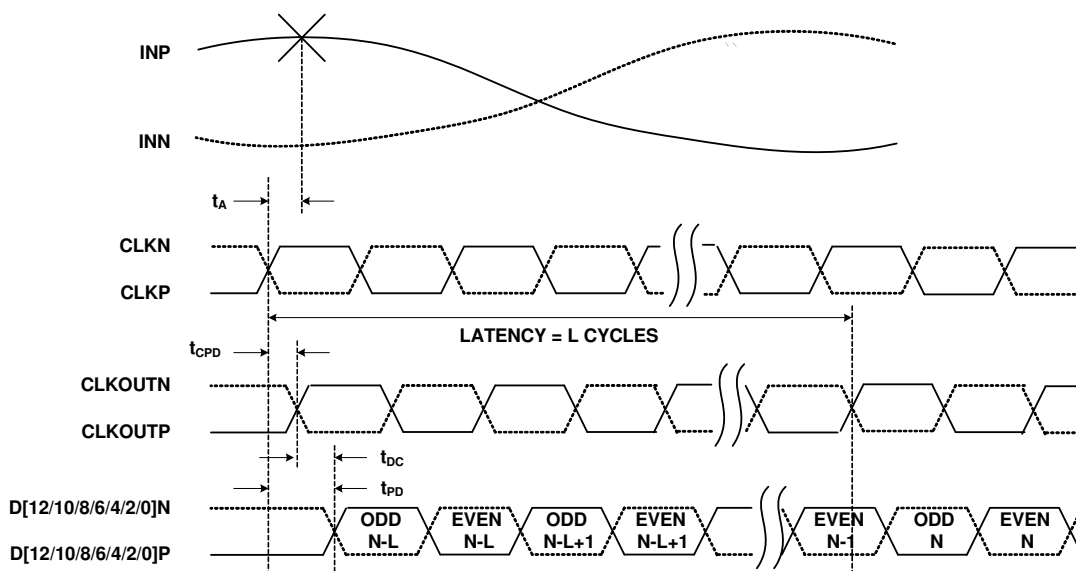


FIGURE 1A. LVDS DDR

## Timing Diagrams (Continued)

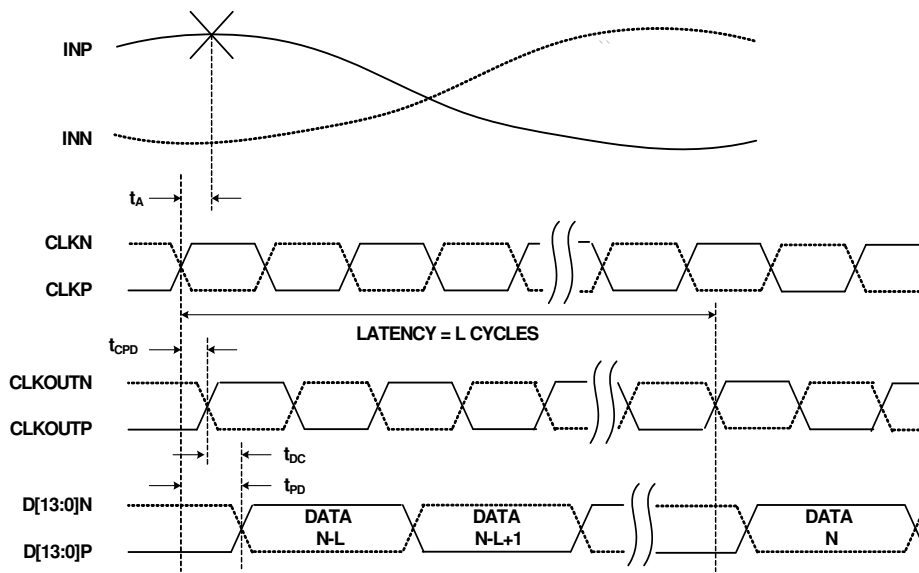


FIGURE 1B. LVDS SDR

FIGURE 1. LVDS TIMING DIAGRAMS

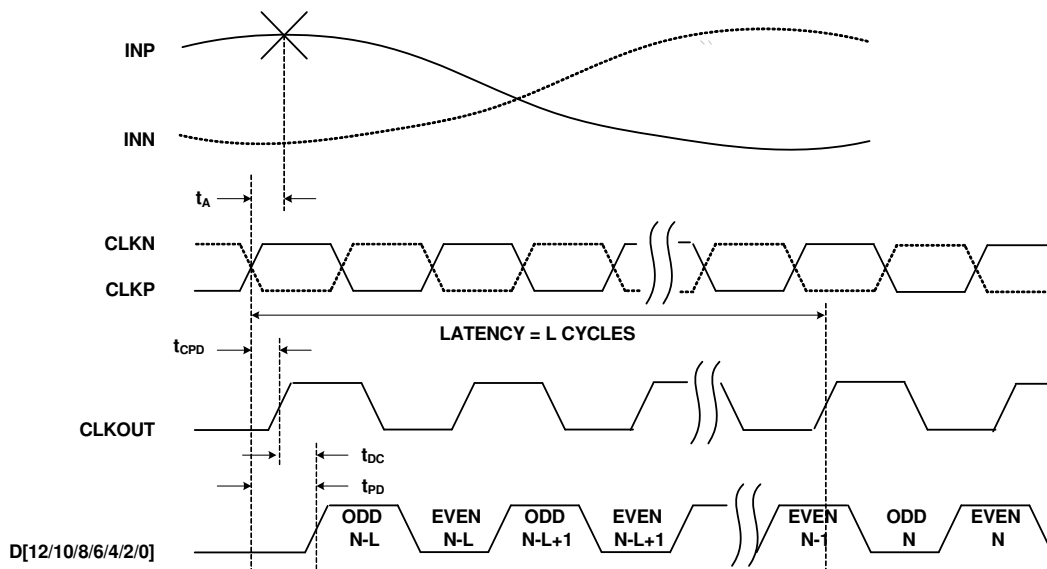
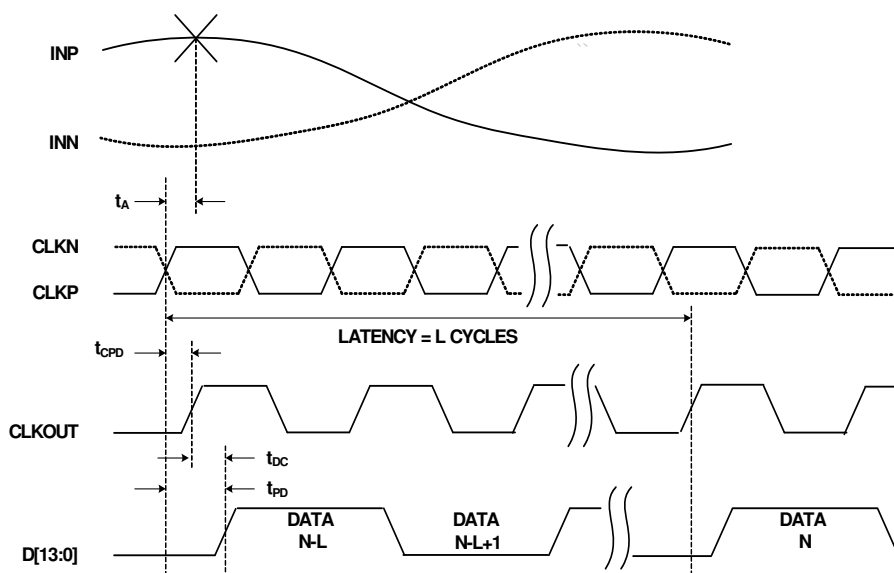


FIGURE 2A. CMOS DDR

## Timing Diagrams (Continued)



**FIGURE 2B. CMOS SDR**  
**FIGURE 2. CMOS TIMING DIAGRAMS**

## Switching Specifications **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	CONDITION	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
<b>ADC OUTPUT</b>						
Aperture Delay	$t_A$			114		ps
RMS Aperture Jitter	$j_A$			75		fs
Input Clock to Output Clock Propagation Delay	$t_{CPD}$	AVDD, OVDD = 1.7V to 1.9V, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	<b>1.65</b>	2.4	<b>3</b>	ns
		AVDD, OVDD = 1.8V, $T_A = +25^\circ\text{C}$	<b>1.9</b>	2.3	<b>2.75</b>	ns
Relative Input Clock to Output Clock Propagation Delay (Note 12)	$dt_{CPD}$	AVDD, OVDD = 1.7V to 1.9V, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	<b>-450</b>		<b>450</b>	ps
Input Clock to Data Propagation Delay	$t_{PD}$		<b>1.65</b>	2.4	<b>3.5</b>	ns
Output Clock to Data Propagation Delay, LVDS Mode	$t_{DC}$	Rising/Falling Edge	<b>-0.1</b>	0.16	<b>0.5</b>	ns
Output Clock to Data Propagation Delay, CMOS Mode	$t_{DC}$	Rising/Falling Edge	<b>-0.1</b>	0.2	<b>0.65</b>	ns
Synchronous Clock Divider Reset Setup Time (with respect to the positive edge of CLKP)	$t_{RSTS}$		<b>0.4</b>	0.06		ns
Synchronous Clock Divider Reset Hold Time (with respect to the positive edge of CLKP)	$t_{RSTH}$			0.02	<b>0.35</b>	ns
Synchronous Clock Divider Reset Recovery Time	$t_{RSTRT}$	DLL recovery time after Synchronous Reset		52		$\mu\text{s}$
Latency (Pipeline Delay)	L			10		cycles
Overvoltage Recovery	$t_{OVR}$			1		cycles

# ISLA214P

## Switching Specifications **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	CONDITION	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
<b>SPI INTERFACE (Notes 13, 14)</b>						
SCLK Period	$t_{CLK}$	Write Operation	<b>16</b>			cycles
	$t_{CLK}$	Read Operation	<b>16</b>			cycles
CSB↓ to SCLK↑ Setup Time	$t_S$	Read or Write	<b>28</b>			cycles
CSB↑ after SCLK↑ Hold Time	$t_H$	Write	<b>5</b>			cycles
CSB↑ after SCLK↓ Hold Time	$t_{HR}$	Read	<b>16</b>			cycles
Data Valid to SCLK↑ Setup Time	$t_{DS}$	Write	<b>6</b>			cycles
Data Valid after SCLK↑ Hold Time	$t_{DH}$	Read or Write			<b>4</b>	cycles
Data Valid after SCLK↓ Time	$t_{DVR}$	Read			<b>5</b>	cycles

### NOTES:

- The relative propagation delay is the difference in propagation time between any two devices that are matched in temperature and voltage, and is specified over the full operating temperature and voltage range.
- SPI Interface timing is directly proportional to the ADC sample period ( $t_S$ ). Values above reflect multiples of a 4ns sample period, and must be scaled proportionally for lower sample rates. ADC sample clock must be running for SPI communication.
- The SPI may operate asynchronously with respect to the ADC sample clock.

## Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V,  $T_A = +25^\circ\text{C}$ ,  $A_{IN} = -1\text{dBFS}$ ,  $f_{IN} = 105\text{MHz}$ ,  $f_{SAMPLE} = 250\text{MSPS}$ .

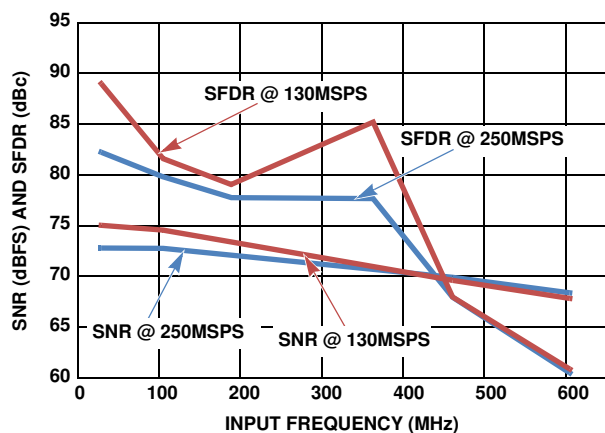


FIGURE 3. SNR AND SFDR vs  $f_{IN}$

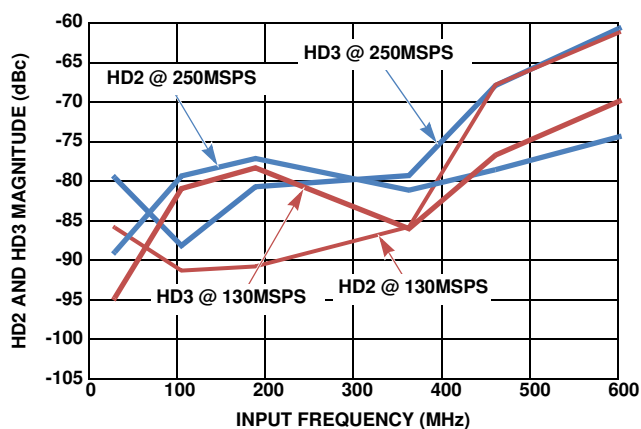


FIGURE 4. HD2 AND HD3 vs  $f_{IN}$

## Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T<sub>A</sub> = +25 °C, A<sub>IN</sub> = -1dBFS, f<sub>IN</sub> = 105MHz, f<sub>SAMPLE</sub> = 250MSPS. (Continued)

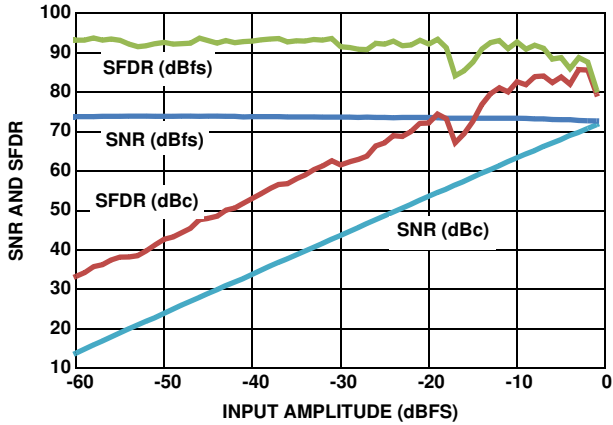


FIGURE 5. SNR AND SFDR vs A<sub>IN</sub>

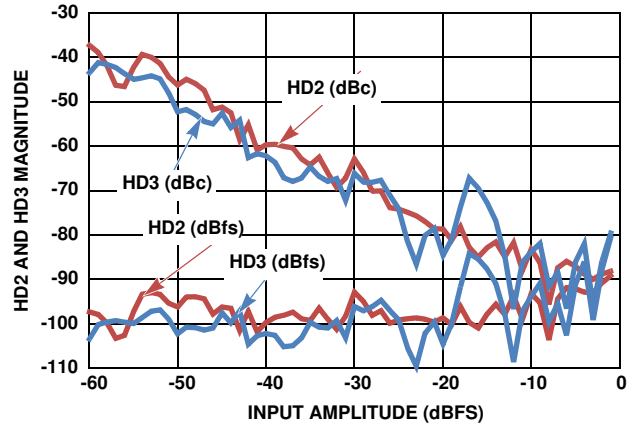


FIGURE 6. HD2 AND HD3 vs A<sub>IN</sub>

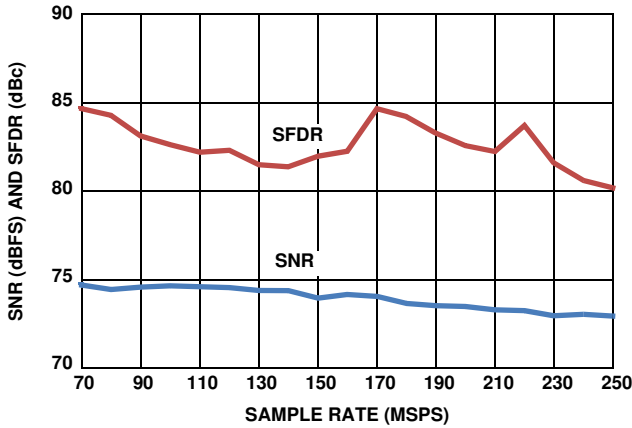


FIGURE 7. SNR AND SFDR vs f<sub>SAMPLE</sub>

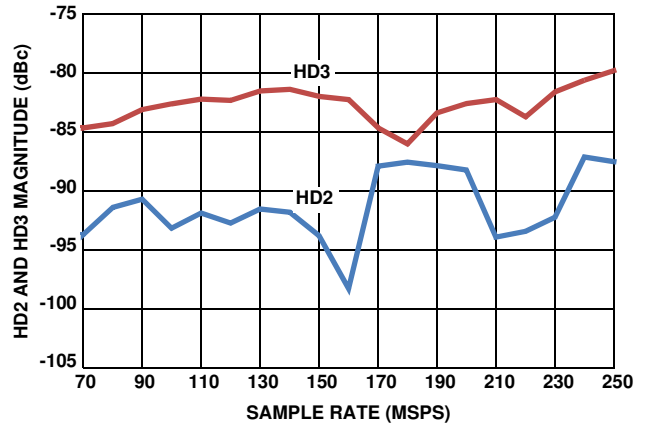


FIGURE 8. HD2 AND HD3 vs f<sub>SAMPLE</sub>

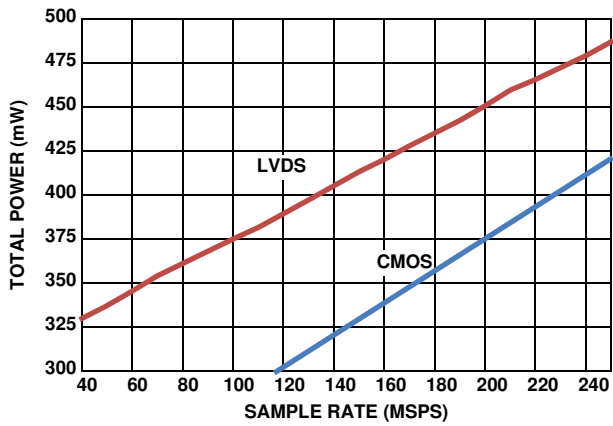


FIGURE 9. POWER vs f<sub>SAMPLE</sub> IN 3mA LVDS MODE (SDR) AND CMOS MODE (DDR)

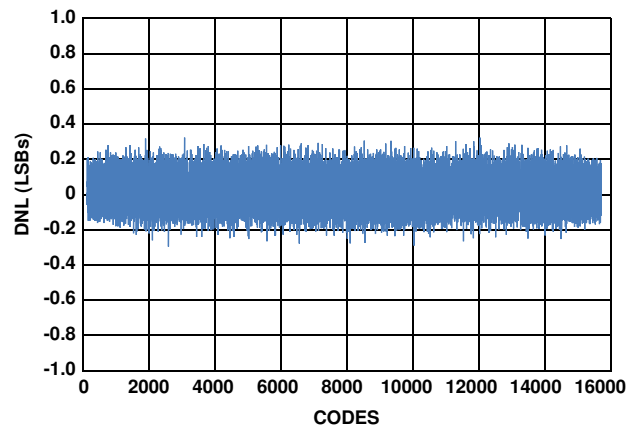


FIGURE 10. DIFFERENTIAL NONLINEARITY



## Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T<sub>A</sub> = +25 °C, A<sub>IN</sub> = -1dBFS, f<sub>IN</sub> = 105MHz, f<sub>SAMPLE</sub> = 250MSPS. (Continued)

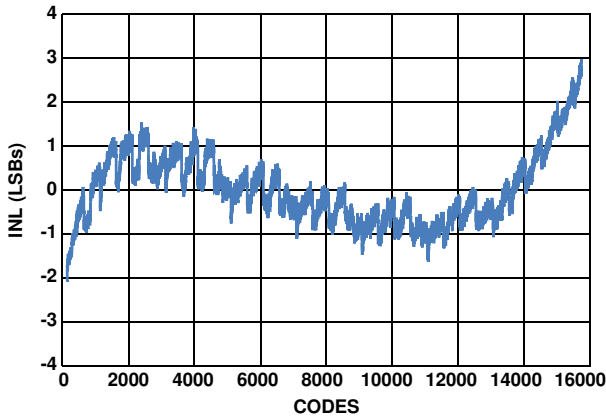


FIGURE 11. INTEGRAL NONLINEARITY

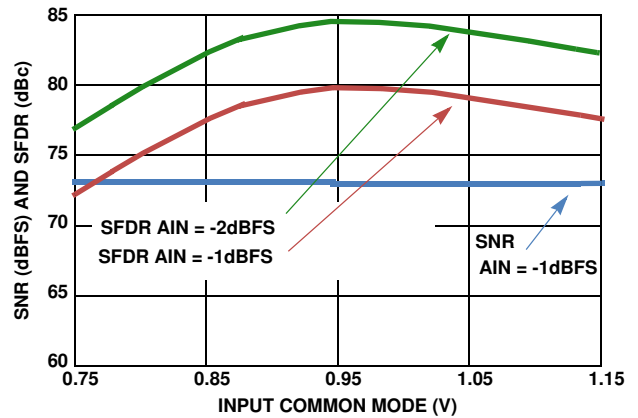


FIGURE 12. SNR AND SFDR vs VCM

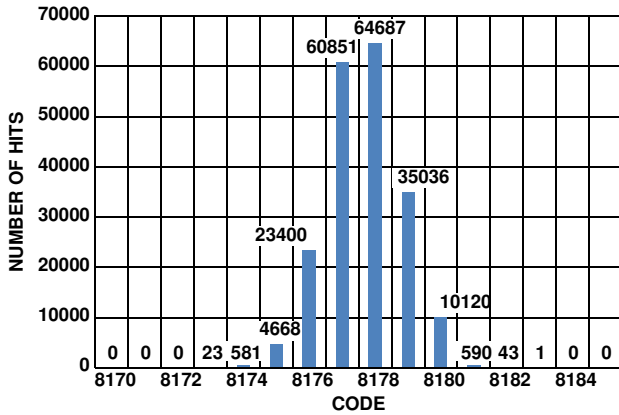


FIGURE 13. NOISE HISTOGRAM

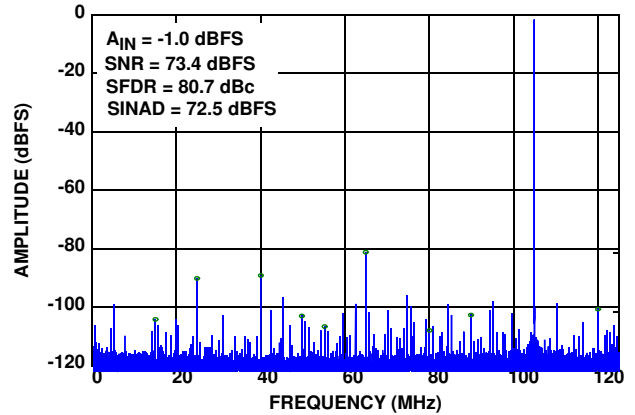


FIGURE 14. SINGLE-TONE SPECTRUM @ 105MHz

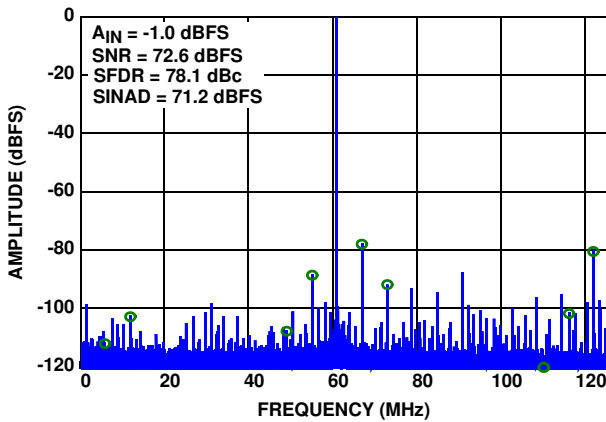


FIGURE 15. SINGLE-TONE SPECTRUM @ 190MHz

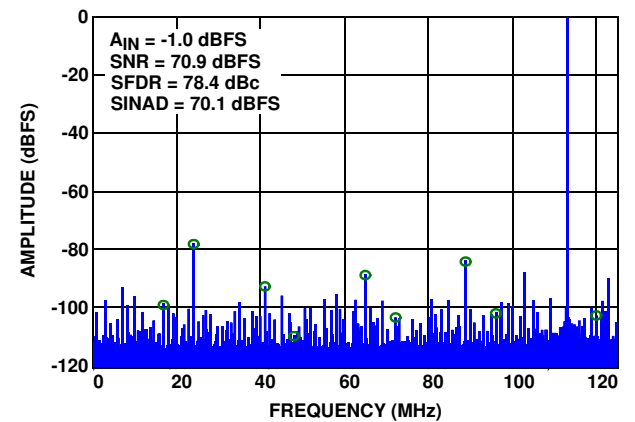


FIGURE 16. SINGLE-TONE SPECTRUM @ 363MHz

## Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T<sub>A</sub> = +25 °C, A<sub>IN</sub> = -1dBFS, f<sub>IN</sub> = 1.05MHz, f<sub>SAMPLE</sub> = 250MSPS. (Continued)

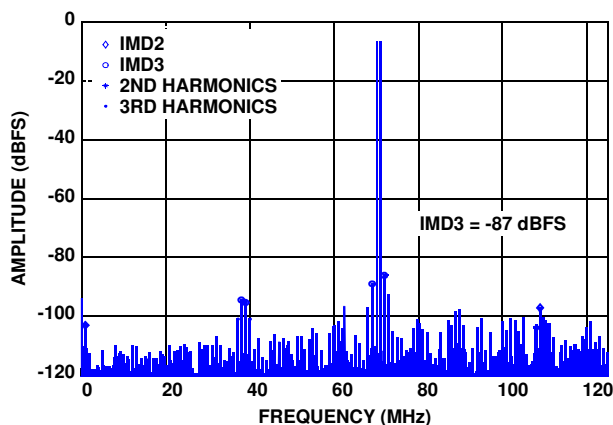


FIGURE 17. TWO-TONE SPECTRUM (F1 = 70MHz, F2 = 71MHz AT -7dBFS)

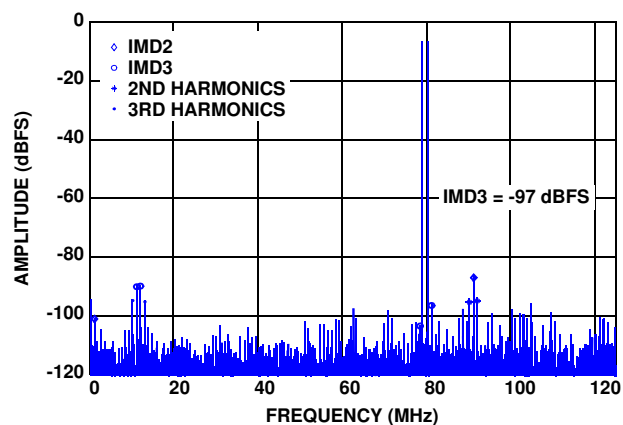


FIGURE 18. TWO-TONE SPECTRUM (F1 = 170MHz, F2 = 171MHz AT -7dBFS)

## Theory of Operation

### Functional Description

The ISLA214P is based on a 14-bit, 250MSPS A/D converter core that utilizes a pipelined successive approximation architecture (see Figure 19). The input voltage is captured by a Sample-Hold Amplifier (SHA) and converted to a unit of charge. Proprietary charge-domain techniques are used to successively compare the input to a series of reference charges. Decisions made during the successive approximation operations determine the digital code for each input value. Digital error correction is also applied, resulting in a total latency of 10 clock cycles. This is evident to the user as a latency between the start of a conversion and the data being available on the digital outputs.

### Power-On Calibration

As mentioned previously, the cores perform a self-calibration at start-up. An internal power-on-reset (POR) circuit detects the supply voltage ramps and initiates the calibration when the analog and digital supply voltages are above a threshold. The following conditions must be adhered to for the power-on calibration to execute successfully.

- A frequency-stable conversion clock must be applied to the CLKP/CLKN pins
- DNC pins must not be connected
- SDO has an internal pull-up and should not be driven externally
- RESETN is pulled low by the ADC internally during POR. External driving of RESETN is optional.
- SPI communications must not be attempted

A user-initiated reset can subsequently be invoked in the event that the above conditions cannot be met at power-up.

After the power supply has stabilized the internal POR releases RESETN and an internal pull-up pulls it high, which starts the calibration sequence. If a subsequent user-initiated reset is desired, the RESETN pin should be connected to an open-drain driver with an off-state/high impedance state leakage of less than 0.5mA to assure exit from the reset state so calibration can start.

The calibration sequence is initiated on the rising edge of RESETN, as shown in Figure 20. Calibration status can be determined by reading the cal\_status bit (LSB) at 0xB6. This bit is '0' during calibration and goes to a logic '1' when calibration is complete. The data outputs produce 0xCCCC during calibration; this can also be used to determine calibration status.

If the selectable clock divider is set to 1 (default), the output clock (CLKOUTP/CLKOUTN) will not be affected by the assertion of RESETN. If the selectable clock divider is set to 2 or 4, the output clock is set low while RESETN is asserted (low). Normal operation of the output clock resumes at the next input clock edge (CLKP/CLKN) after RESETN is de-asserted. At 250MSPS, the nominal calibration time is 200ms, while the maximum calibration time is 550ms.

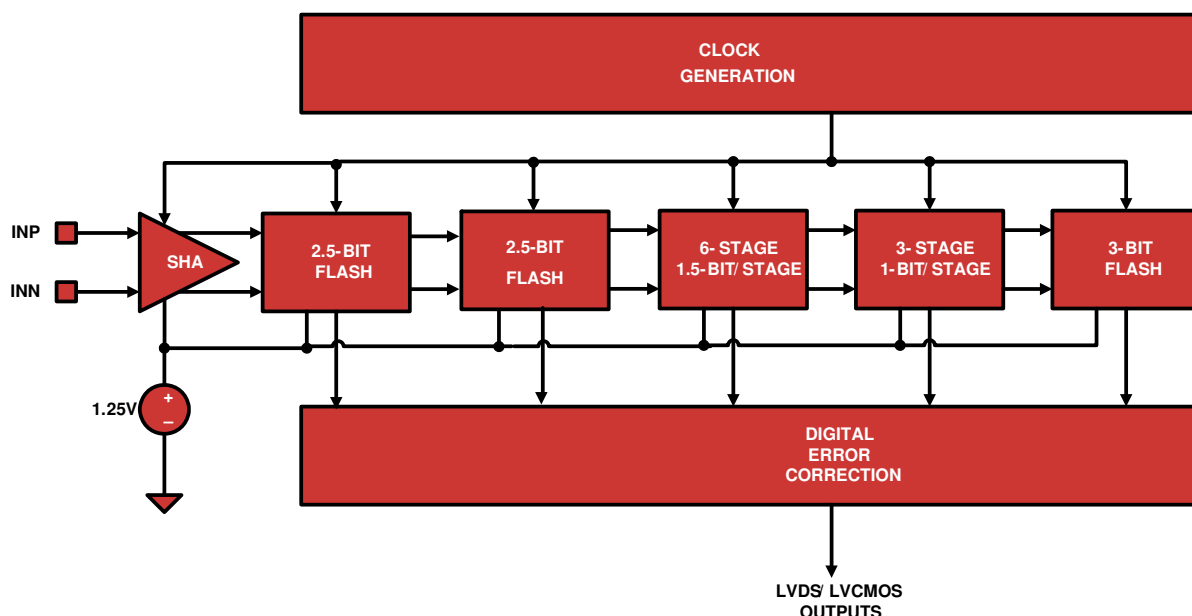


FIGURE 19. A/D CORE BLOCK DIAGRAM

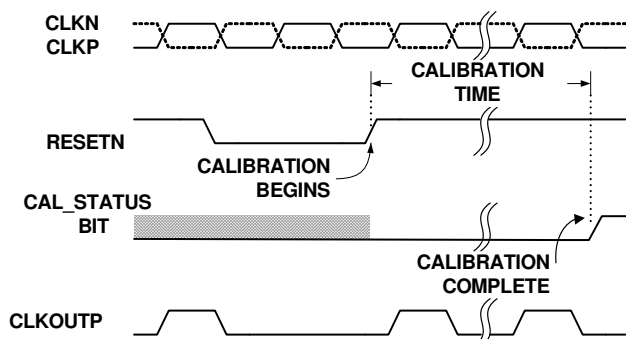


FIGURE 20. CALIBRATION TIMING

## User Initiated Reset

Recalibration of the A/D can be initiated at any time by driving the RESETN pin low for a minimum of one clock cycle. An open-drain driver with a drive strength in its high impedance state of less than 0.5mA is recommended, as RESETN has an internal high impedance pull-up to OVDD. As is the case during power-on reset, RESETN and DNC pins must be in the proper state for the calibration to successfully execute.

The performance of the ISLA214P changes with variations in temperature, supply voltage or sample rate. The extent of these changes may necessitate recalibration, depending on system performance requirements. Best performance will be achieved by recalibrating the A/D under the environmental conditions at which it will operate.

A supply voltage variation of <100mV will generally result in an SNR change of <0.5dBFS and SFDR change of <3dBc.

In situations where the sample rate is not constant, best results will be obtained if the device is calibrated at the highest sample rate. Reducing the sample rate by less than 80MSPS will typically result in an SNR change of <0.5dBFS and an SFDR change of <3dBc.

Figures 21 through 26 show the effect of temperature on SNR and SFDR performance with power on calibration performed at -40°C, +25°C, and +85°C. Each plot shows the variation of SNR/SFDR across temperature after a single power on calibration at -40°C, +25°C and +85°C. Best performance is typically achieved by a user-initiated power on calibration at the operating conditions, as stated earlier. However, it can be seen that performance drift with temperature is not a very strong function of the temperature at which the power on calibration is performed.

# Temperature Calibration

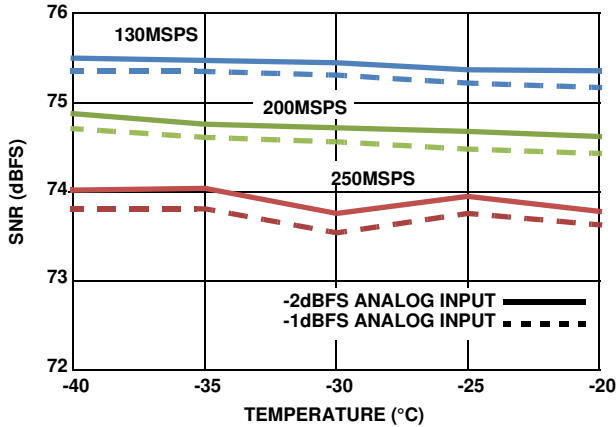


FIGURE 21. TYPICAL SNR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT -40 °C,  $f_{IN} = 105\text{MHz}$

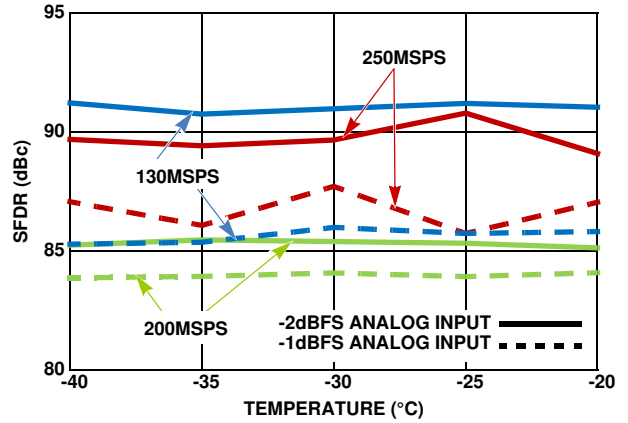


FIGURE 22. TYPICAL SFDR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT -40 °C,  $f_{IN} = 105\text{MHz}$

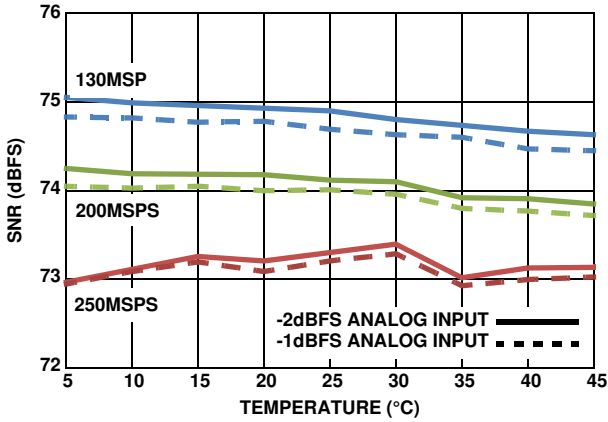


FIGURE 23. TYPICAL SNR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +25 °C,  $f_{IN} = 105\text{MHz}$

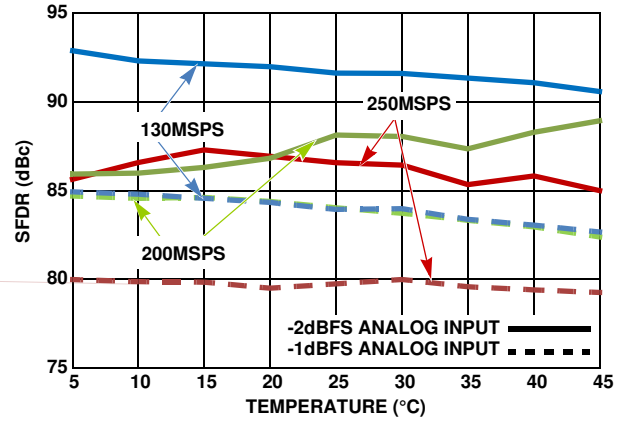


FIGURE 24. TYPICAL SFDR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +25 °C,  $f_{IN} = 105\text{MHz}$

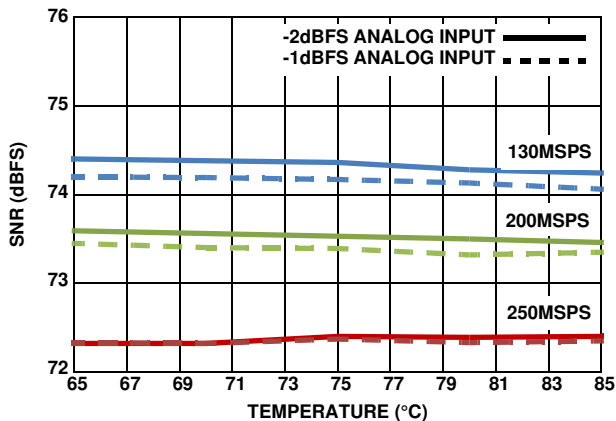


FIGURE 25. TYPICAL SNR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +85 °C,  $f_{IN} = 105\text{MHz}$

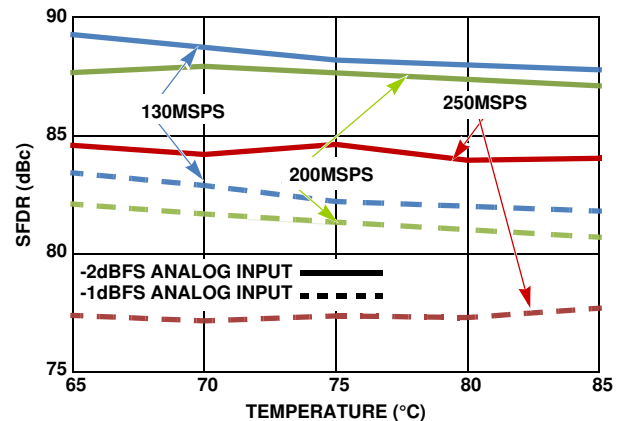


FIGURE 26. TYPICAL SFDR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +85 °C,  $f_{IN} = 105\text{MHz}$

## Analog Input

A single fully differential input (VINP/VINN) connects to the sample and hold amplifier (SHA) of each unit A/D. The ideal full-scale input voltage is 2.0V, centered at the VCM voltage of 0.94V as shown in Figure 27.

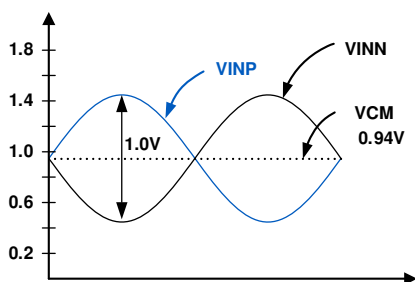


FIGURE 27. ANALOG INPUT RANGE

Best performance is obtained when the analog inputs are driven differentially. The common-mode output voltage, VCM, should be used to properly bias the inputs as shown in Figures 28 through 30. An RF transformer will give the best noise and distortion performance for wideband and/or high intermediate frequency (IF) inputs. Two different transformer input schemes are shown in Figures 28 and 29.

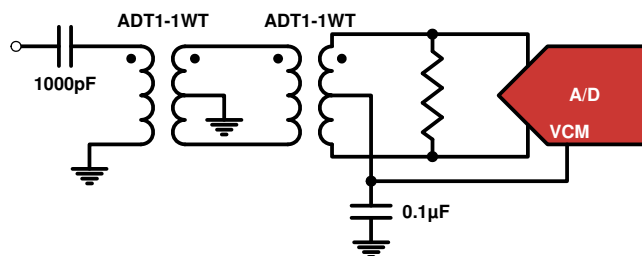


FIGURE 28. TRANSFORMER INPUT FOR GENERAL PURPOSE APPLICATIONS

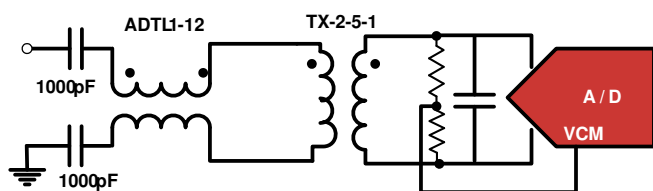


FIGURE 29. TRANSMISSION-LINE TRANSFORMER INPUT FOR HIGH IF APPLICATIONS

This dual transformer scheme is used to improve common-mode rejection, which keeps the common-mode level of the input matched to VCM. The value of the shunt resistor should be determined based on the desired load impedance. The differential input resistance of the ISLA214P is 600Ω.

The SHA design uses a switched capacitor input stage (see Figure 43), which creates current spikes when the sampling capacitance is reconnected to the input voltage. This causes a disturbance at the input which must settle before the next sampling point. Lower source impedance will result in faster settling and improved performance. Therefore a 2:1 or 1:1

transformer and low shunt resistance are recommended for optimal performance.

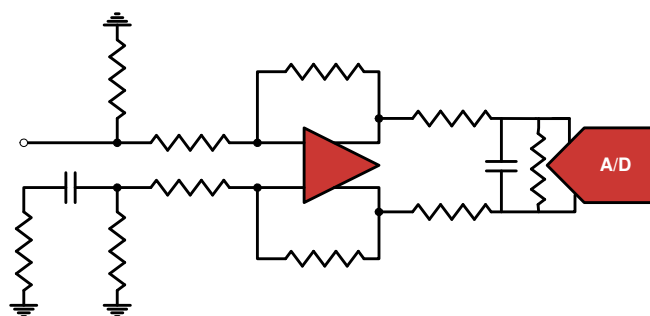


FIGURE 30. DIFFERENTIAL AMPLIFIER INPUT

A differential amplifier, as shown in the simplified block diagram in Figure 30, can be used in applications that require DC-coupling. In this configuration, the amplifier will typically dominate the achievable SNR and distortion performance. Intersil's new ISL552x differential amplifier family can also be used in certain AC applications with minimal performance degradation. Contact the factory for more information.

## Clock Input

The clock input circuit is a differential pair (see Figure 44). Driving these inputs with a high level (up to 1.8V<sub>p-p</sub> on each input) sine or square wave will provide the lowest jitter performance. A transformer with 4:1 impedance ratio will provide increased drive levels. The clock input is functional with AC-coupled LVDS, LVPECL, and CML drive levels. To maintain the lowest possible aperture jitter, it is recommended to have high slew rate at the zero crossing of the differential clock input signal.

The recommended drive circuit is shown in Figure 31. A duty range of 40% to 60% is acceptable. The clock can be driven single-ended, but this will reduce the edge rate and may impact SNR performance. The clock inputs are internally self-biased to AVDD/2 to facilitate AC coupling.

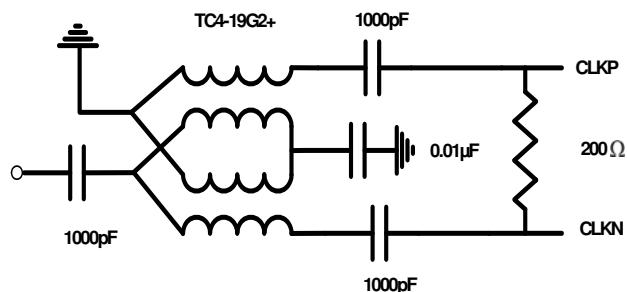


FIGURE 31. RECOMMENDED CLOCK DRIVE

A selectable 2x or 4x frequency divider is provided in series with the clock input. The divider can be used in the 2x mode with a sample clock equal to twice the desired sample rate or in 4x mode with a sample clock equal to four times the desired sample rate. This allows the use of the Phase Slip feature, which enables synchronization of multiple ADCs. The Phase Slip feature can be used as an alternative to using the CLKDIVRST pins to synchronize ADCs in a multiple ADC system.

**TABLE 1. CLKDIV PIN SETTINGS**

CLKDIV PIN	DIVIDE RATIO
AVSS	2
Float	1
AVDD	4

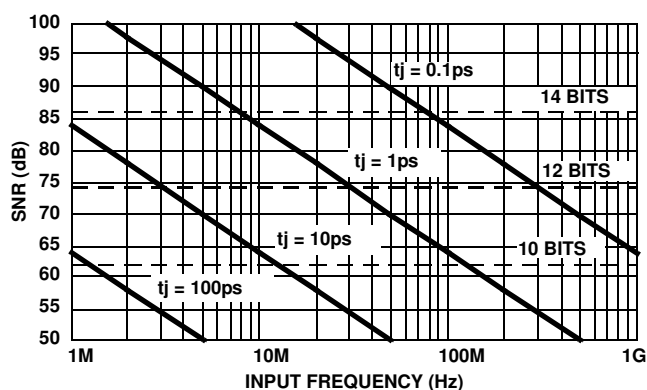
The clock divider can also be controlled through the SPI port, which overrides the CLKDIV pin setting. See “SPI Physical Interface” on page 25. A delay-locked loop (DLL) generates internal clock signals for various stages within the charge pipeline. If the frequency of the input clock changes, the DLL may take up to 52µs to regain lock at 250MSPS. The lock time is inversely proportional to the sample rate.

The DLL has two ranges of operation, slow and fast. The slow range can be used for sample rates between 40MSPS and 100MSPS, while the default fast range can be used from 80MSPS to the maximum specified sample rate.

## Jitter

In a sampled data system, clock jitter directly impacts the achievable SNR performance. The theoretical relationship between clock jitter ( $t_j$ ) and SNR is shown in Equation 1 and is illustrated in Figure 32.

$$SNR = 20 \log_{10} \left( \frac{1}{2\pi f_{IN} t_j} \right) \quad (EQ. 1)$$



**FIGURE 32. SNR vs CLOCK JITTER**

This relationship shows the SNR that would be achieved if clock jitter were the only non-ideal factor. In reality, achievable SNR is limited by internal factors such as linearity, aperture jitter and thermal noise. Internal aperture jitter is the uncertainty in the sampling instant shown in Figure 1A. The internal aperture jitter combines with the input clock jitter in a root-sum-square fashion, since they are not statistically correlated, and this determines the total jitter in the system. The total jitter, combined with other noise sources, then determines the achievable SNR.

## Voltage Reference

A temperature compensated internal voltage reference provides the reference charges used in the successive approximation operations. The full-scale range of each A/D is proportional to the reference voltage. The nominal value of the voltage reference is 1.25V.

## Digital Outputs

Output data is available as a parallel bus in LVDS-compatible(default) or CMOS modes. In either case, the data is presented in either double data rate (DDR) or single data rate (default) format. Figures 1A and 1B show the timing relationships for LVDS and CMOS modes, respectively.

Additionally, the drive current for LVDS mode can be set to a nominal 3mA(default) or a power-saving 2mA. The lower current setting can be used in designs where the receiver is in close physical proximity to the A/D. The applicability of this setting is dependent upon the PCB layout, therefore the user should experiment to determine if performance degradation is observed.

The output mode can be controlled through the SPI port, by writing to address 0x73, see “Serial Peripheral Interface” on page 25.

An external resistor creates the bias for the LVDS drivers. A 10kΩ, 1% resistor must be connected from the RLVDSP pin to OVSS.

## Power Dissipation

The power dissipated by the ISLA214P is primarily dependent on the sample rate and the output modes: LVDS vs CMOS and DDR vs SDR. There is a static bias in the analog supply, while the remaining power dissipation is linearly related to the sample rate. The output supply dissipation changes to a lesser degree in LVDS mode, but is more strongly related to the clock frequency in CMOS mode.

## Nap/Sleep

Portions of the device may be shut down to save power during times when operation of the A/D is not required. Two power saving modes are available: Nap, and Sleep. Nap mode reduces power dissipation to < 60mW while Sleep mode reduces power dissipation to 9mW typically.

All digital outputs (Data, CLKOUT and OR) are placed in a high impedance state during Nap or Sleep. The input clock should remain running and at a fixed frequency during Nap or Sleep, and CSB should be high. Recovery time from Nap mode will increase if the clock is stopped, since the internal DLL can take up to 52µs to regain lock at 250MSPS.

By default after the device is powered on, the operational state is controlled by the NAPSLP pin as shown in Table 2.

**TABLE 2. NAPSLP PIN SETTINGS**

NAPSLP PIN	MODE
AVSS	Normal
Float	Sleep
AVDD	Nap

The power-down mode can also be controlled through the SPI port, which overrides the NAPSLP pin setting. Details on this are contained in “Serial Peripheral Interface” on page 25.

## Data Format

Output data can be presented in three formats: two's complement (default), Gray code and offset binary. The data format can be controlled through the SPI port, by writing to address 0x73. Details on this are contained in "Serial Peripheral Interface" on page 25.

Offset binary coding maps the most negative input voltage to code 0x000 (all zeros) and the most positive input to 0xFF (all ones). Two's complement coding simply complements the MSB of the offset binary representation.

When calculating Gray code the MSB is unchanged. The remaining bits are computed as the XOR of the current bit position and the next most significant bit. Figure 33 shows this operation.

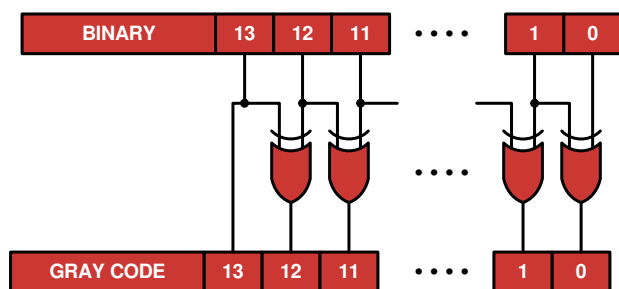


FIGURE 33. BINARY TO GRAY CODE CONVERSION

Converting back to offset binary from Gray code must be done recursively, using the result of each bit for the next lower bit as shown in Figure 34.

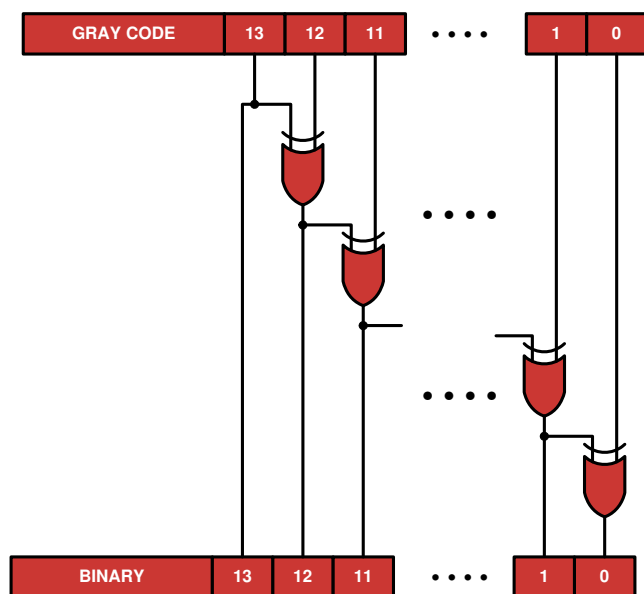


FIGURE 34. GRAY CODE TO BINARY CONVERSION

Mapping of the input voltage to the various data formats is shown in Table 3.

TABLE 3. INPUT VOLTAGE TO OUTPUT CODE MAPPING

INPUT VOLTAGE	OFFSET BINARY	TWO'S COMPLEMENT	GRAY CODE
-Full Scale	00 0000 0000 0000	10 0000 0000 0000	00 0000 0000 0000
-Full Scale + 1LSB	00 0000 0000 0001	10 0000 0000 0001	00 0000 0000 0001
Mid-Scale	10 0000 0000 0000	00 0000 0000 0000	11 0000 0000 0000
+Full Scale - 1LSB	11 1111 1111 1110	01 1111 1111 1110	10 0000 0000 0001
+Full Scale	11 1111 1111 1111	01 1111 1111 1111	10 0000 0000 0000

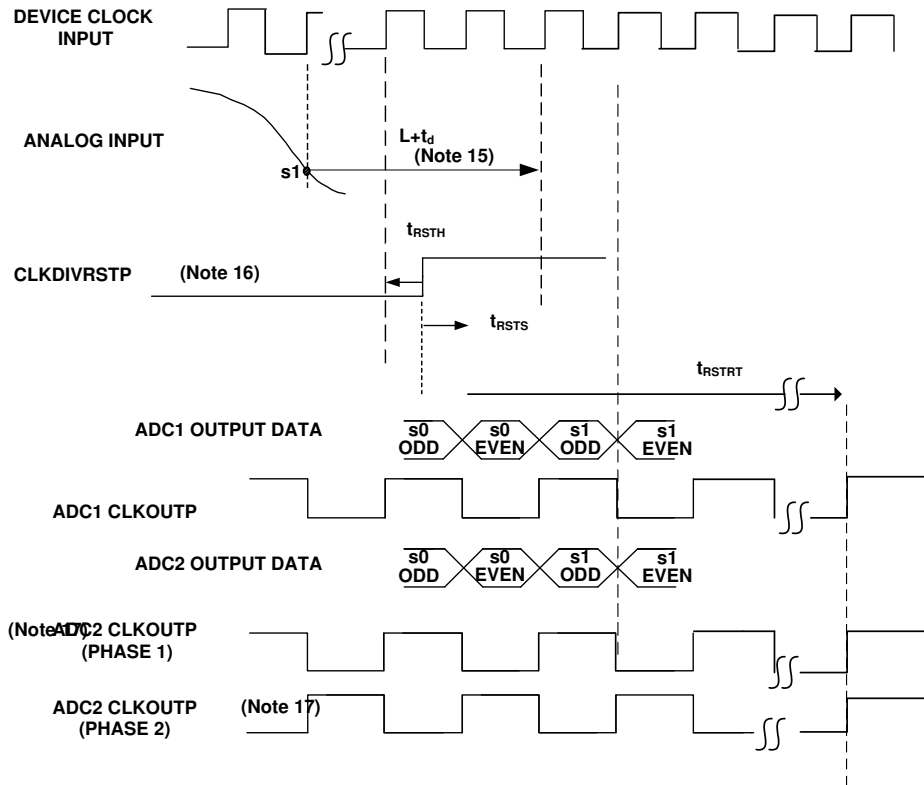
## Clock Divider Synchronous Reset

If the selectable clock divider is used, the ADC's internal sample clock will be at half the frequency (DIV = 2) or one quarter the frequency (DIV = 4) of the device clock. The phase relationship between the sample clock and the device clock is initially indeterminate. An output clock (CLKOUTP, CLKOUTN) is provided to facilitate latching of the sampled data and estimation of the internal sample clock's phase. The output clock has a fixed phase relationship to the sample clock. When the selectable clock divider is set to 2 or 4, the output clock's phase relationship to the sample clock remains fixed but is initially indeterminate with respect to the device clock. When the selectable clock divider is set to 2 or 4, the synchronous clock divider reset feature allows the phase of the internal sample clock and the output clock to be synchronized (refer to Figure 35) with respect to the device clock. This simplifies data capture in systems employing multiple A/Ds where sampling of the inputs is desired to be synchronous.

The reset signal must be well-timed with respect to the sample clock (See "Switching Specifications" on page 13).

A 100Ω differential termination resistor must be supplied between CLKDIVRSTP and CLKDIVRSTN, external to the ADC, (on the PCB) and should be located as close to the CLKDIVRSTP/N pins as possible.

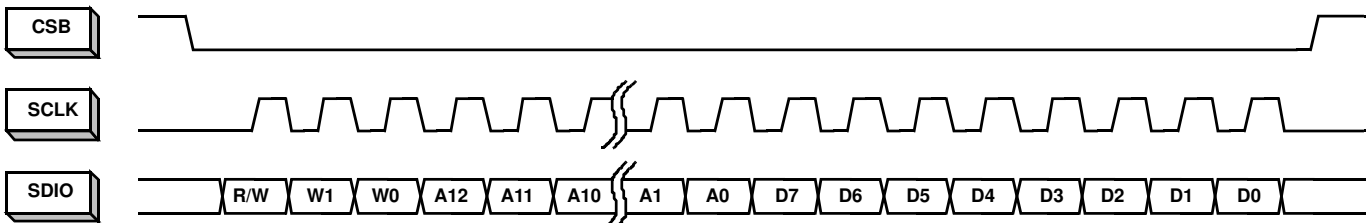
# ISLA214P



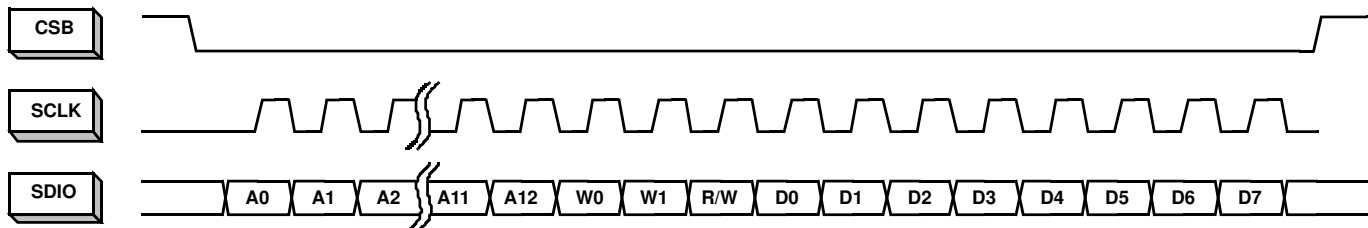
**NOTES:**

- 15. Delay equals fixed pipeline latency (L cycles of sample clock) plus fixed analog propagation delay, td.
- 16. CLKDIVRSTP setup and hold times are with respect to input sample clock rising edge.  
CLKDIVRSTN is not shown, but must be driven, and is the compliment of CLKDIVRSTP.
- 17. Either Output Clock Phase (phase 1 or phase 2 ) equally likely prior to synchronization.

**FIGURE 35. SYNCHRONOUS RESET OPERATION, CLOCK DIVIDE = 2, DDR-MODE**



**FIGURE 36. MSB-FIRST ADDRESSING**



**FIGURE 37. LSB-FIRST ADDRESSING**



# ISLA214P

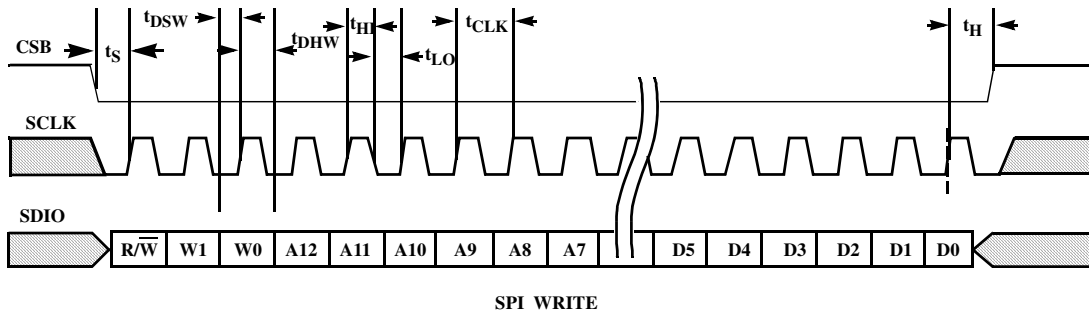


FIGURE 38. SPI WRITE

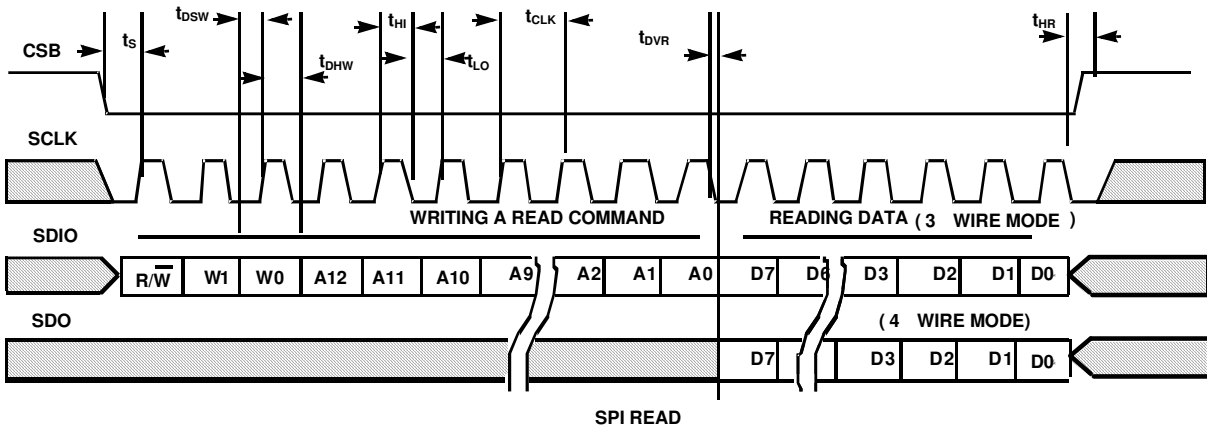


FIGURE 39. SPI READ

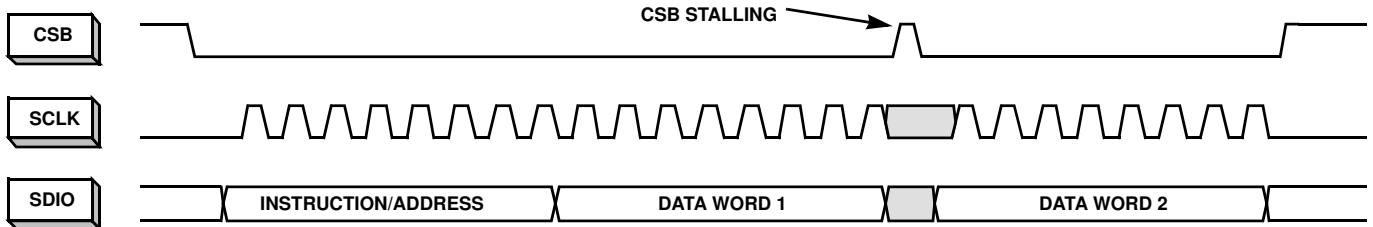


FIGURE 40. 2-BYTE TRANSFER

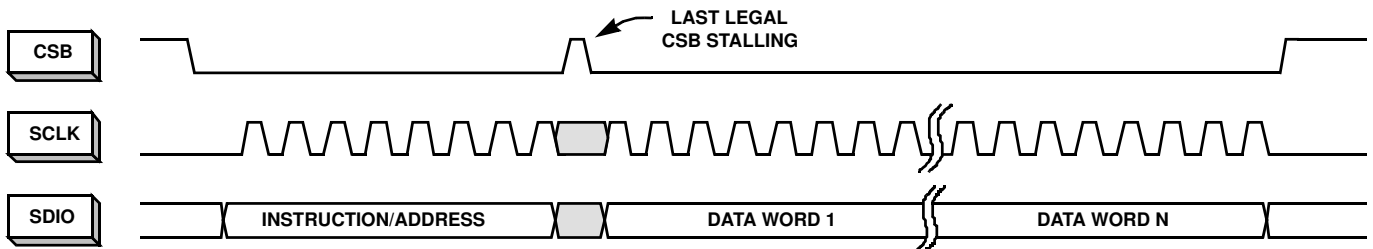


FIGURE 41. N-BYTE TRANSFER

## Serial Peripheral Interface

A serial peripheral interface (SPI) bus is used to facilitate configuration of the device and to optimize performance. The SPI bus consists of chip select (CSB), serial clock (SCLK) serial data output (SDO), and serial data input/output (SDIO). The maximum SCLK rate is equal to the A/D sample rate ( $f_{\text{SAMPLE}}$ ) divided by 16 for both write operations and read operations. At  $f_{\text{SAMPLE}} = 250\text{MHz}$ , maximum SCLK is 15.63MHz for writing and read operations. There is no minimum SCLK rate.

The following sections describe various registers that are used to configure the SPI or adjust performance or functional parameters. Many registers in the available address space (0x00 to 0xFF) are not defined in this document. Additionally, within a defined register there may be certain bits or bit combinations that are reserved. Undefined registers and undefined values within defined registers are reserved and should not be selected. Setting any reserved register or value may produce indeterminate results.

### SPI Physical Interface

The serial clock pin (SCLK) provides synchronization for the data transfer. By default, all data is presented on the serial data input/output (SDIO) pin in three-wire mode. The state of the SDIO pin is set automatically in the communication protocol (described in the following). A dedicated serial data output pin (SDO) can be activated by setting 0x00[7] high to allow operation in four-wire mode.

The SPI port operates in a half duplex master/slave configuration, with the ISLA214P functioning as a slave. Multiple slave devices can interface to a single master in three-wire mode only, since the SDO output of an unaddressed device is asserted in four wire mode.

The chip-select bar (CSB) pin determines when a slave device is being addressed. Multiple slave devices can be written to concurrently, but only one slave device can be read from at a given time (again, only in three-wire mode). If multiple slave devices are selected for reading at the same time, the results will be indeterminate.

The communication protocol begins with an instruction/address phase. The first rising SCLK edge following a high-to-low transition on CSB determines the beginning of the two-byte instruction/address command; SCLK must be static low before the CSB transition. Data can be presented in MSB-first order or LSB-first order. The default is MSB-first, but this can be changed by setting 0x00[6] high. Figures 36 and 37 show the appropriate bit ordering for the MSB-first and LSB-first modes, respectively. In MSB-first mode, the address is incremented for multi-byte transfers, while in LSB-first mode it's decremented.

In the default mode, the MSB is R/W, which determines if the data is to be read (active high) or written. The next two bits, W1 and W0, determine the number of data bytes to be read or written (see Table 4). The lower 13 bits contain the first address for the data transfer. This relationship is illustrated in Figure 38, and timing values are given in "Switching Specifications" on page 13.

After the instruction/address bytes have been read, the appropriate number of data bytes are written to or read from the

A/D (based on the R/W bit status). The data transfer will continue as long as CSB remains low and SCLK is active. Stalling of the CSB pin is allowed at any byte boundary (instruction/address or data) if the number of bytes being transferred is three or less. For transfers of four bytes or more, CSB is allowed to stall in the middle of the instruction/address bytes or before the first data byte. If CSB transitions to a high state after that point the state machine will reset and terminate the data transfer.

TABLE 4. BYTE TRANSFER SELECTION

[W1:W0]	BYTES TRANSFERRED
00	1
01	2
10	3
11	4 or more

Figures 40 and 41 on page 24 illustrate the timing relationships for 2-byte and N-byte transfers, respectively. The operation for a 3-byte transfer can be inferred from these diagrams.

### SPI Configuration

#### ADDRESS 0X00: CHIP\_PORT\_CONFIG

Bit ordering and SPI reset are controlled by this register. Bit order can be selected as MSB to LSB (MSB first) or LSB to MSB (LSB first) to accommodate various micro controllers.

#### Bit 7 SDO Active

#### Bit 6 LSB First

Setting this bit high configures the SPI to interpret serial data as arriving in LSB to MSB order.

#### Bit 5 Soft Reset

Setting this bit high resets all SPI registers to default values.

#### Bit 4 Reserved

This bit should always be set high.

**Bits 3:0** These bits should always mirror bits 4:7 to avoid ambiguity in bit ordering.

#### ADDRESS 0X02: BURST\_END

If a series of sequential registers are to be set, burst mode can improve throughput by eliminating redundant addressing. The burst is ended by pulling the CSB pin high. Setting the burst\_end address determines the end of the transfer; during a write operation, the user must be cautious to transmit the correct number of bytes based on the starting and ending addresses.

#### Bits 7:0 Burst End Address

This register value determines the ending address of the burst data.