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14-Bit, 500MSPS ADC

ISLA214P50

The ISLA214P50 is a 14-bit, 500MSPS analog-to-digital converter designed with Intersil's proprietary FemtoCharge™ technology on a standard CMOS process. The ISLA214P50 is part of a pin-compatible portfolio of 12 to 16-bit A/Ds with maximum sample rates ranging from 130MSPS to 500MSPS.

The device utilizes two time-interleaved 250MSPS unit ADCs to achieve the ultimate sample rate of 500MSPS. A single 500MHz conversion clock is presented to the converter, and all interleave clocking is managed internally. The proprietary Intersil Interleave Engine (I2E) performs automatic correction of offset, gain, and sample time mismatches between the unit ADCs to optimize performance.

A serial peripheral interface (SPI) port allows for extensive configurability of the A/D. The SPI also controls the interleave correction circuitry, allowing the system to issue offline and continuous calibration commands as well as configure many dynamic parameters.

Digital output data is presented in selectable LVDS or CMOS formats. The ISLA214P50 is available in a 72 Ld QFN package with an exposed paddle. Operating from a 1.8V supply, performance is specified over the full industrial temperature range (-40°C to +85°C).

Key Specifications

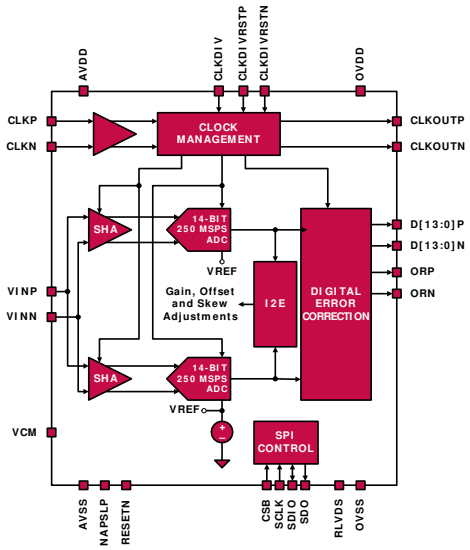
- SNR @ 500MSPS
  - = 72.7dBFS f_{IN} = 30MHz
  - = 70.6dBFS f_{IN} = 363MHz
- SFDR @ 500MSPS
  - = 84dBc f_{IN} = 30MHz
  - = 76dBc f_{IN} = 363MHz
- Total Power Consumption = 835mW @ 500MSPS

Features

- Automatic fine interleave correction calibration
- Single supply 1.8V operation
- Clock duty cycle stabilizer
- 75fs clock jitter
- 700MHz bandwidth
- Programmable built-in test patterns
- Multi-ADC support
  - SPI programmable fine gain and offset control
  - Support for multiple adc synchronization
  - Optimized output timing
- Nap and sleep modes
  - 200µs sleep wake-up time
- Data output clock
- DDR LVDS-compatible or LVCMOS outputs
- Selectable clock divider

Applications

- Radar array processing
- Software defined radios
- Broadband communications
- High-performance data acquisition
- Communications test equipment

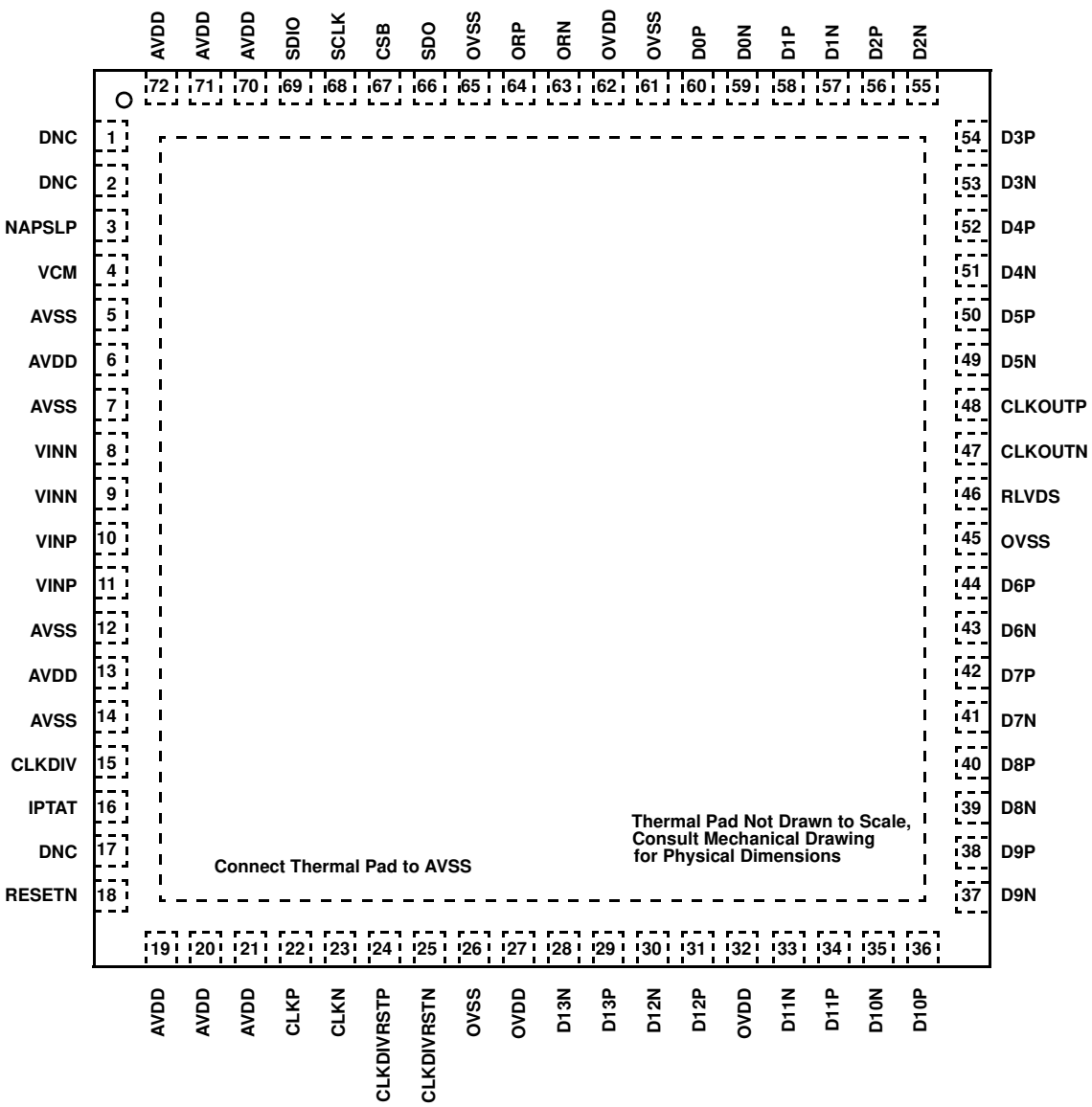


Pin-Compatible Family

MODEL	RESOLUTION	SPEED (MSPS)
ISLA216P25	16	250
ISLA216P20	16	200
ISLA216P13	16	130
ISLA214P50	14	500
ISLA214P25	14	250
ISLA214P20	14	200
ISLA214P13	14	130
ISLA212P50	12	500
ISLA212P25	12	250
ISLA212P20	12	200
ISLA212P13	12	130

Pin Configuration - LVDS MODE

ISLA214P50
(72 LD QFN)
TOP VIEW



Pin Descriptions - 72 Ld QFN, LVDS Mode

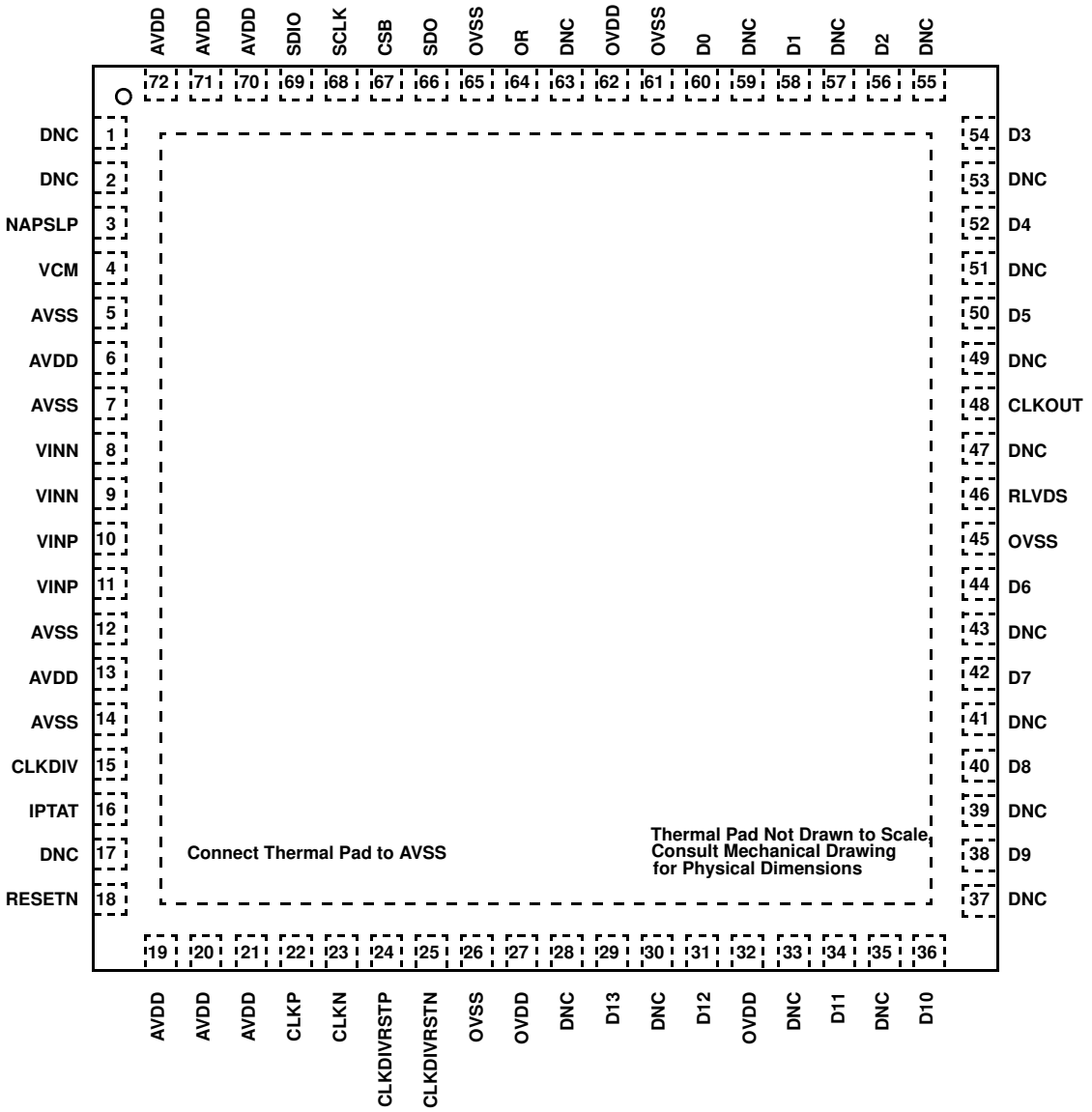
PIN NUMBER	LVDS PIN NAME	LVDS PIN FUNCTION
1, 2, 17	DNC	Do Not Connect
6, 13, 19, 20, 21, 70, 71, 72	AVDD	1.8V Analog Supply
5, 7, 12, 14	AVSS	Analog Ground
27, 32, 62	OVDD	1.8V Output Supply
26, 45, 61, 65	OVSS	Output Ground
3	NAPSLP	Tri-Level Power Control (Nap, Sleep modes)
4	VCM	Common Mode Output
8, 9	VINN	Analog Input Negative

Pin Descriptions - 72 Ld QFN, LVDS Mode (Continued)

PIN NUMBER	LVDS PIN NAME	LVDS PIN FUNCTION
10, 11	VINP	Analog Input Positive
15	CLKDIV	Tri-Level Clock Divider Control
16	IPTAT	Temperature Monitor (Output current proportional to absolute temperature)
18	RESETN	Power On Reset (Active Low)
22, 23	CLKP, CLKN	Clock Input True, Complement
24, 25	CLKDIVRSTP, CLKDIVRSTN	Synchronous Clock Divider Reset True, Complement
28, 29	D13N, D13P	LVDS Bit 13 (MSB) Output Complement, True
30, 31	D12N, D12P	LVDS Bit 12 Output Complement, True
33, 34	D11N, D11P	LVDS Bit 11 Output Complement, True
35, 36	D10N, D10P	LVDS Bit 10 Output Complement, True
37, 38	D9N, D9P	LVDS Bit 9 Output Complement, True
39, 40	D8N, D8P	LVDS Bit 8 Output Complement, True
41, 42	D7N, D7P	LVDS Bit 7 Output Complement, True
43, 44	D6N, D6P	LVDS Bit 6 Output Complement, True
46	RLVDS	LVDS Bias Resistor (connect to OVSS with 1%10kW)
47, 48	CLKOUTN, CLKOUTP	LVDS Clock Output Complement, True
49, 50	D5N, D5P	LVDS Bit 5 Output Complement, True
51, 52	D4N, D4P	LVDS Bit 4 Output Complement, True
53, 54	D3N, D3P	LVDS Bit 3 Output Complement, True
55, 56	D2N, D2P	LVDS Bit 2 Output Complement, True
57, 58	D1N, D1P	LVDS Bit 1 Output Complement, True
59, 60	D0N, D0P	LVDS Bit 0 (LSB) Output Complement, True
63, 64	ORN, ORP	LVDS Over Range Complement, True
66	SDO	SPI Serial Data Output
67	CSB	SPI Chip Select (active low)
68	SCLK	SPI Clock
69	SDIO	SPI Serial Data Input/Output
Exposed Paddle	AVSS	Analog Ground

Pin Configuration - CMOS MODE

ISLA214P50
(72 LD QFN)
TOP VIEW



Pin Descriptions - 72 Ld QFN, CMOS Mode

PIN NUMBER	CMOS PIN NAME	CMOS PIN FUNCTION
1, 2, 17, 28, 30, 33, 35, 37, 39, 41, 43, 47, 49, 51, 53, 55, 57, 59, 63	DNC	Do Not Connect
6, 13, 19, 20, 21, 70, 71, 72	AVDD	1.8V Analog Supply
5, 7, 12, 14	AVSS	Analog Ground
27, 32, 62	OVDD	1.8V Output Supply
26, 45, 61, 65	OVSS	Output Ground
3	NAPSLP	Tri-Level Power Control (Nap, Sleep modes)
4	VCM	Common Mode Output

Pin Descriptions - 72 Ld QFN, CMOS Mode (Continued)

PIN NUMBER	CMOS PIN NAME	CMOS PIN FUNCTION
8, 9	VINN	Analog Input Negative
10, 11	VINP	Analog Input Positive
15	CLKDIV	Tri-Level Clock Divider Control
16	IPTAT	Temperature Monitor (Output current proportional to absolute temperature)
18	RESETN	Power On Reset (Active Low)
22, 23	CLKP, CLKN	Clock Input True, Complement
24, 25	CLKDIVRSTP, CLKDIVRSTN	Synchronous Clock Divider Reset True, Complement
29	D13	CMOS Bit 13 (MSB) Output
31	D12	CMOS Bit 12 Output
34	D11	CMOS Bit 11 Output
36	D10	CMOS Bit 10 Output
38	D9	CMOS Bit 9 Output
40	D8	CMOS Bit 8 Output
42	D7	CMOS Bit 7 Output
44	D6	CMOS Bit 6 Output
46	RLVDS	LVDS Bias Resistor (connect to OVSS with 1%10kW)
48	CLKOUT	CMOS Clock Output
50	D5	CMOS Bit 5 Output
52	D4	CMOS Bit 4 Output
54	D3	CMOS Bit 3 Output
56	D2	CMOS Bit 2 Output
58	D1	CMOS Bit 1 Output
60	D0	CMOS Bit 0 (LSB) Output
64	OR	CMOS Over Range
66	SDO	SPI Serial Data Output
67	CSB	SPI Chip Select (active low)
68	SCLK	SPI Clock
69	SDIO	SPI Serial Data Input/Output
Exposed Paddle	AVSS	Analog Ground

Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISLA214P50IRZ	ISLA214P50 IRZ	-40 to +85	72 Ld QFN	L72.10x10E
ISLA214P50IR72EV1Z	Evaluation Board			

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate–e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), please see device information page for ISLA214P50. For more information on MSL please see techbrief TB363.

Table of Contents

Absolute Maximum Ratings

AVDD to AVSS . . . . . -0.4V to 2.1V
OVDD to OVSS . . . . . -0.4V to 2.1V
AVSS to OVSS . . . . . -0.3V to 0.3V
Analog Inputs to AVSS . . . . . -0.4V to AVDD + 0.3V
Clock Inputs to AVSS . . . . . -0.4V to AVDD + 0.3V
Logic Input to AVSS . . . . . -0.4V to OVDD + 0.3V
Logic Inputs to OVSS . . . . . -0.4V to OVDD + 0.3V
Latchup (Tested per JESD-78C;Class 2,Level A 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
72 Ld QFN (Notes 3, 4)	23	0.9

Operating Temperature . . . . . -40°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
4. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T_A = -40°C to +85°C (typical specifications at +25°C), A_{IN} = -1dBFS, f_{SAMPLE} = 500MSPS. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	CONDITIONS	ISLA214P50			UNITS
			MIN (Note 5)	TYP	MAX (Note 5)	
DC SPECIFICATIONS (Note 6)						
Analog Input						
Full-Scale Analog Input Range	V_{FS}	Differential	**1.95**	2.0	**2.15**	V_{P-P}
Input Resistance	R_{IN}	Differential		300		Ω
Input Capacitance	C_{IN}	Differential		9		pF
Full Scale Range Temp. Drift	A_{VTC}	Full Temp		160		ppm/°C
Input Offset Voltage	V_{OS}		**-5.0**	-1.3	**5.0**	mV
Common-Mode Output Voltage	V_{CM}			0.94		V
Common-Mode Input Current (per pin)	I_{CM}			2.6		µA/MSPS
Clock Inputs						
Inputs Common Mode Voltage				0.9		V
CLKP, CLKN Input Swing				1.8		V
Power Requirements						
1.8V Analog Supply Voltage	AVDD		**1.7**	1.8	**1.9**	**V**
1.8V Digital Supply Voltage	OVDD		**1.7**	1.8	**1.9**	**V**
1.8V Analog Supply Current	I_{AVDD}			374	**391**	mA
1.8V Digital Supply Current (Note 6)	I_{OVDD}	3mA LVDS, (I2E powered down, Fs/4 Filter powered down)		90	**104**	mA
Power Supply Rejection Ratio	PSRR	30MHz, 45mVP-P signal on AVDD		60		dB

Electrical Specifications All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T_A = -40°C to +85°C (typical specifications at +25°C), A_{IN} = -1dBFS, f_{SAMPLE} = 500MSPS. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	CONDITIONS	ISLA214P50			UNITS
			MIN (Note 5)	TYP	MAX (Note 5)	
Total Power Dissipation						
Normal Mode	P_D	2mA LVDS, (I2E powered down, Fs/4 Filter powered down)		809		mW
		3mA LVDS, (I2E powered down, Fs/4 Filter powered down)		835	**891**	mW
		3mA LVDS, (I2E on, Fs/4 Filter off)		867		mW
		3mA LVDS, (I2E on, Fs/4 Filter on)		900	**958**	mW
Nap Mode	P_D			89	**104**	mW
Sleep Mode	P_D	CSB at logic high		7	**19**	mW
Nap/Sleep Mode Wakeup Time		Sample Clock Running		200		µs
AC SPECIFICATIONS						
Differential Nonlinearity	DNL	f_{IN} = 105MHz **No Missing Codes**	**-0.99**	±0.5	**1.4**	LSB
Integral Nonlinearity	INL	fin = 105MHz		±2.5		LSB
Minimum Conversion Rate (Note 7)	f_S MIN				**80**	**MSPS**
Maximum Conversion Rate	f_S MAX		**500**			MSPS
Signal-to-Noise Ratio (Note 8)	SNR	f_{IN} = 30MHz		72.7		dBFS
		f_{IN} = 105MHz	69.0	72.6		dBFS
		f_{IN} = 190MHz		71.9		dBFS
		f_{IN} = 363MHz		70.6		dBFS
		f_{IN} = 461MHz		70.0		dBFS
		f_{IN} = 605MHz		68.3		dBFS
Signal-to-Noise and Distortion (Note 8)	SINAD	f_{IN} = 30MHz		72.2		dBFS
		f_{IN} = 105MHz	68.5	71.7		dBFS
		f_{IN} = 190MHz		70.7		dBFS
		f_{IN} = 363MHz		69.3		dBFS
		f_{IN} = 461MHz		64.7		dBFS
		f_{IN} = 605MHz		60.7		dBFS
Effective Number of Bits (Note 8)	ENOB	f_{IN} = 30MHz		11.70		Bits
		f_{IN} = 105MHz	11.09	11.62		Bits
		f_{IN} = 190MHz		11.44		Bits
		f_{IN} = 363MHz		11.22		Bits
		f_{IN} = 461MHz		10.45		Bits
		f_{IN} = 605MHz		9.79		Bits

Electrical Specifications

All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T_A = -40°C to +85°C (typical specifications at +25°C), A_{IN} = -1dBFS, f_{SAMPLE} = 500MSPS. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	CONDITIONS	ISLA214P50			UNITS
			MIN (Note 5)	TYP	MAX (Note 5)	
Spurious-Free Dynamic Range (Note 8)	SFDR	f_{IN} = 30MHz		84		dBc
		f_{IN} = 105MHz	72	82		dBc
		f_{IN} = 190MHz		78		dBc
		f_{IN} = 363MHz		76		dBc
		f_{IN} = 461MHz		66		dBc
		f_{IN} = 605MHz		61		dBc
Spurious-Free Dynamic Range Excluding H2,H3 (Note 8)	SFDRX23	f_{IN} = 30MHz		88		dBc
		f_{IN} = 105MHz		89		dBc
		f_{IN} = 190MHz		88		dBc
		f_{IN} = 363MHz		83		dBc
		f_{IN} = 461MHz		84		dBc
		f_{IN} = 605MHz		77		dBc
Intermodulation Distortion	IMD	f_{IN} = 70MHz		88		dBFS
		f_{IN} = 170MHz		96		dBFS
Word Error Rate	WER			10^{-12}		
Full Power Bandwidth	FPBW			700		MHz

NOTES:

5. Compliance to datasheet limits is assured by one of the following methods: production test, characterization and/or design.
6. Digital Supply Current is dependent upon the capacitive loading of the digital outputs. I_{OVDD} specifications apply for 10pF load on each digital output.
7. The DLL Range setting must be changed for low speed operation.
8. Minimum specification guaranteed when calibrated at +85°C.

Digital Specifications

Boldface limits apply over the operating temperature range, -40°C to +85°C.

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
INPUTS (Note 9)						
Input Current High (RESETN)	I_{IH}	V_{IN} = 1.8V	**0**	1	**10**	µA
Input Current Low (RESETN)	I_{IL}	V_{IN} = 0V	**-25**	-12	**-8**	µA
Input Current High (SDIO)	I_{IH}	V_{IN} = 1.8V		4	**12**	µA
Input Current Low (SDIO)	I_{IL}	V_{IN} = 0V	**-600**	-415	**-300**	µA
Input Current High (CSB)	I_{IH}	V_{IN} = 1.8V	**40**	58	**75**	µA
Input Current Low (CSB)	I_{IL}	V_{IN} = 0V		5	**10**	µA
Input Current High (CLKDIV)	I_{IH}		**16**	25	**34**	µA
Input Current Low (CLKDIV)	I_{IL}		**-34**	-25	**-16**	µA
Input Voltage High (SDIO, RESETN)	V_{IH}		**1.17**			V
Input Voltage Low (SDIO, RESETN)	V_{IL}				**.63**	V
Input Capacitance	C_{DI}			4		pF
LVDS INPUTS (CLKRSTP,CLKRSTN)						
Input Common Mode Range	V_{ICM}		**825**		**1575**	mV
Input Differential Swing (peak to peak, single-ended)	V_{ID}		**250**		**450**	mV

Digital Specifications Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
CLKDIVRSTP Input Pull-down Resistance	R_{Ipd}			100		kΩ
CLKDIVRSTN Input Pull-up Resistance	R_{Ipu}			100		kΩ
LVDS OUTPUTS						
Differential Output Voltage (Note 10)	V_T	3mA Mode		612		mV_{P-P}
Output Offset Voltage	V_{OS}	3mA Mode	**1120**	1150	**1200**	mV
Output Rise Time	t_R			240		ps
Output Fall Time	t_F			240		ps
CMOS OUTPUTS						
Voltage Output High	V_{OH}	I_{OH} = -500µA	**OVDD - 0.3**	OVDD - 0.1		V
Voltage Output Low	V_{OL}	I_{OL} = 1mA		0.1	**0.3**	V
Output Rise Time	t_R			1.8		ns
Output Fall Time	t_F			1.4		ns

NOTES:

9. The Tri-Level Inputs internal switching thresholds are approximately. 0.43V and 1.34V. It is advised to float the inputs, tie to ground or AVDD depending on desired function.

10. The voltage is expressed in peak-to-peak differential swing. The peak-to-peak singled-ended swing is 1/2 of the differential swing.

I2E Specifications Boldface limits apply over the operating temperature range, -40°C to +85°C.

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
Offset Mismatch-induced Spurious Power		No I2E Calibration performed		-65		dBFS
		Active Run state enabled		-70		dBFS
I2E Settling Times	I2Epost_t	Calibration settling time for Active Run state			**1000**	ms
Minimum Duration of Valid Analog Input	t_{TE}	Allow one I2E iteration of Offset, Gain and Phase correction			**100**	µs
Largest Interleave Spur		f_{IN} = 10MHz to 240MHz, Active Run State enabled, in Track Mode		-99		dBc
		f_{IN} = 10MHz to 240MHz, Active Run State enabled and previously settled, in Hold Mode	**-75**	-80		dBc
		f_{IN} = 260MHz to 490MHz, Active Run State enabled, in Track Mode		-99		dBc
		f_{IN} = 260MHz to 490MHz, Active Run State enabled and previously settled, in Hold Mode		-75		dBc
Total Interleave Spurious Power		Active Run State enabled, in Track Mode, f_{IN} is a broadband signal in the 1st Nyquist zone		-85		dBc
		Active Run State enabled, in Track Mode, f_{IN} is a broadband signal in the 2nd Nyquist zone		-75		dBc
Sample Time Mismatch Between Unit ADCs		Active Run State enabled, in Track Mode		25		fs
Gain Mismatch Between Unit ADCs				0.01		%FS
Offset Mismatch Between Unit ADCs				1		mV

Timing Diagrams

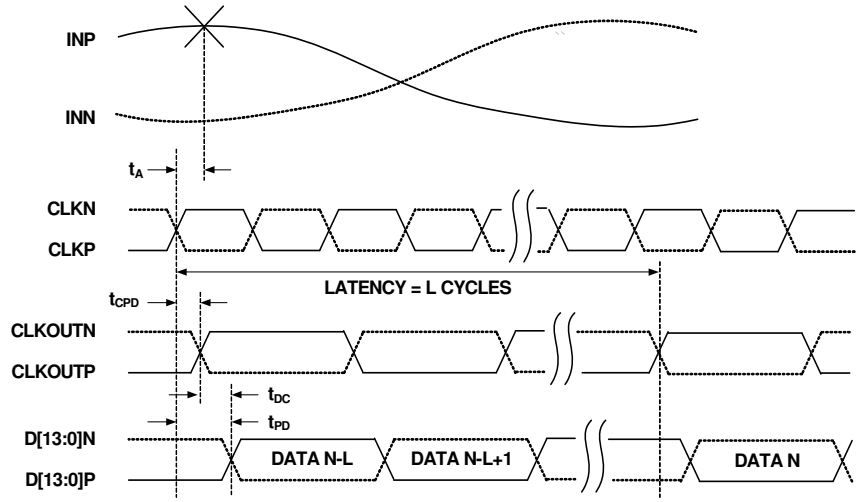


FIGURE 1A. LVDS

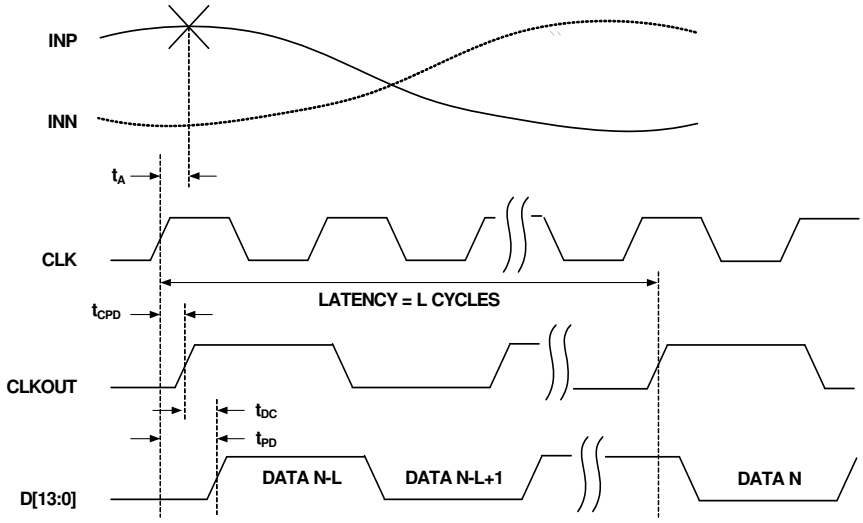


FIGURE 1B. CMOS

FIGURE 1. TIMING DIAGRAMS

Switching Specifications

Boldface limits apply over the operating temperature range, -40°C to +85°C.

PARAMETER	CONDITION	SYMBOL	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
ADC OUTPUT						
Aperture Delay		t_A		114		ps
RMS Aperture Jitter		j_A		75		fs
Input Clock to Output Clock Propagation Delay	AVDD, OVDD = 1.7V to 1.9V, T_A = -40°C to +85°C	t_{CPD}	**1.65**	2.4	**3**	ns
	AVDD, OVDD = 1.8V, T_A = +25°C	t_{CPD}	1.9	2.3	2.75	ns
Relative Input Clock to Output Clock Propagation Delay (Note 13)	AVDD, OVDD = 1.7V to 1.9V, T_A = -40°C to +85°C	dt_{CPD}	**-450**		**450**	ps
Input Clock to Data Propagation Delay		t_{PD}	**1.65**	2.4	**3.5**	ns
Output Clock to Data Propagation Delay, LVDS Mode	Rising/Falling Edge	t_{DC}	**-0.1**	0.16	**0.5**	ns
Output Clock to Data Propagation Delay, CMOS Mode	Rising/Falling Edge	t_{DC}	**-0.1**	0.2	**0.65**	ns
Synchronous Clock Divider Reset Setup Time (with respect to the positive edge of CLKP)		t_{RSTS}	**0.4**	0.06		ns
Synchronous Clock Divider Reset Hold Time (with respect to the positive edge of CLKP)		t_{RSTH}		0.02	**0.35**	ns
Synchronous Clock Divider Reset Recovery Time	DLL recovery time after Synchronous Reset	t_{RSTRT}		52		µs
Latency (Pipeline Delay)		L		20		cycles
Overvoltage Recovery		t_{OVR}		2		cycles
SPI INTERFACE (Notes 11, 12)						
SCLK Period	Write Operation	t_{CLK}	**32**			cycles
	Read Operation	t_{CLK}	**32**			cycles
CSB↓ to SCLK↑ Setup Time	Read or Write	t_S	**56**			cycles
CSB↑ after SCLK↑ Hold Time	Write	t_H	**10**			cycles
Data Valid to SCLK↑ Setup Time	Write	t_{DS}	**12**			cycles
Data Valid after SCLK↑ Hold Time	Read or Write	t_{DH}			**8**	cycles
Data Valid after SCLK↓ Time	Read	t_{DVR}			**10**	cycles

NOTES:

11. SPI Interface timing is directly proportional to the ADC sample period (t_S). Values above reflect multiples of a 4ns sample period, and must be scaled proportionally for lower sample rates. ADC sample clock must be running for SPI communication.
12. The SPI may operate asynchronously with respect to the ADC sample clock.
13. The relative propagation delay is the difference in propagation time between any two devices that are matched in temperature and voltage, and is specified over the full operating temperature and voltage range.

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -1dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 500MSPS.

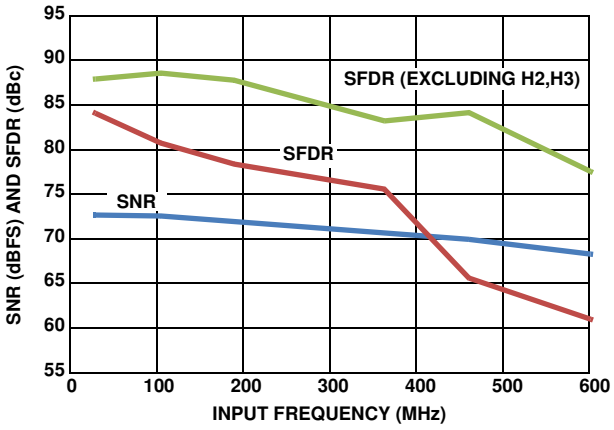


FIGURE 2. SNR AND SFDR vs f_{IN}

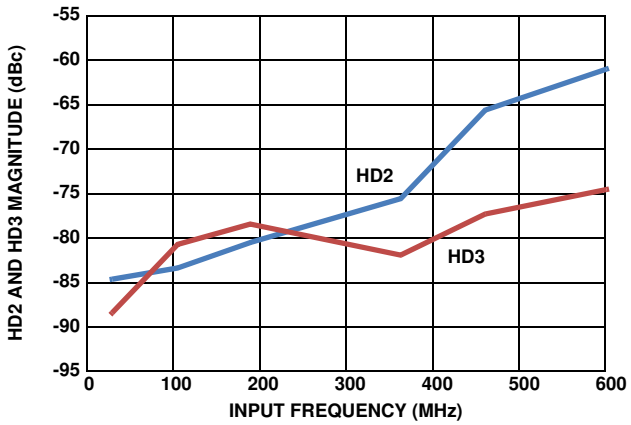


FIGURE 3. HD2 AND HD3 vs f_{IN}

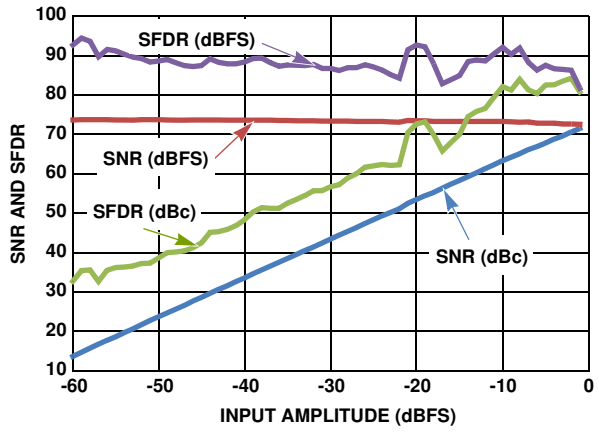


FIGURE 4. SNR AND SFDR vs A_{IN}

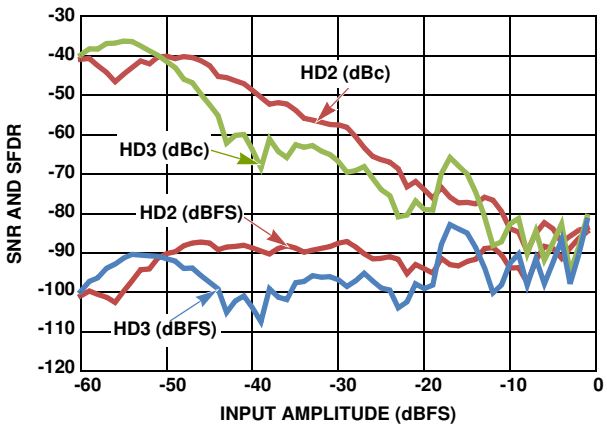


FIGURE 5. HD2 AND HD3 vs A_{IN}

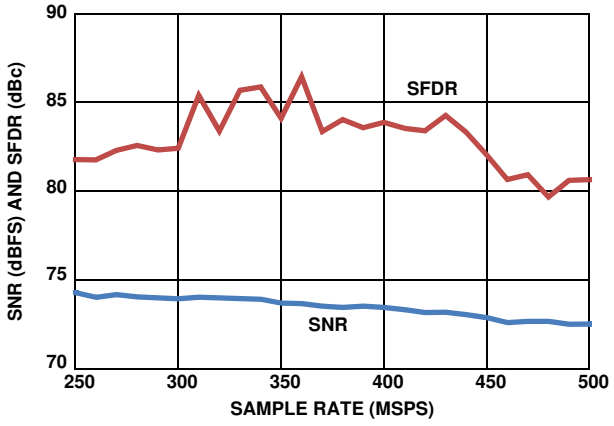


FIGURE 6. SNR AND SFDR vs f_{SAMPLE}

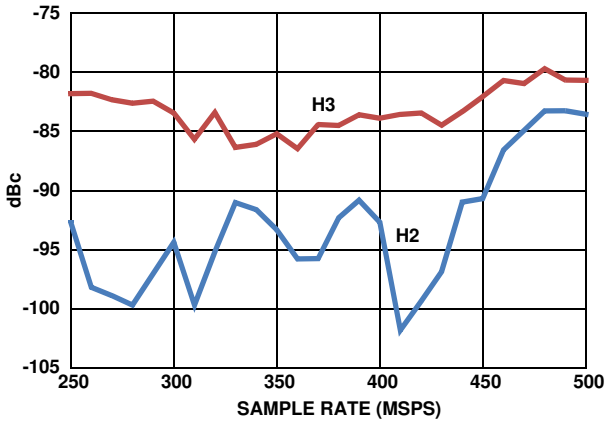


FIGURE 7. HD2 AND HD3 vs f_{SAMPLE}

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -1dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 500MSPS. **(Continued)**

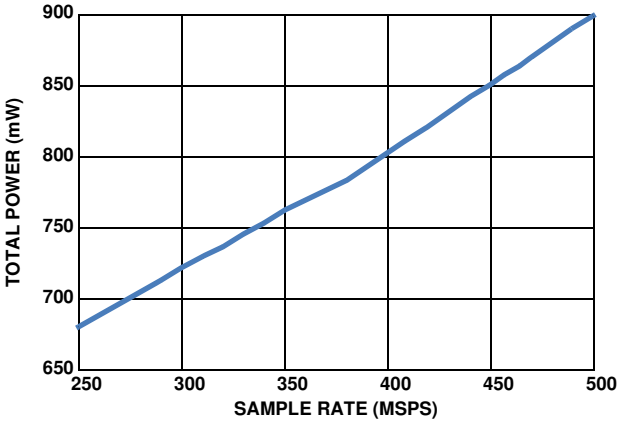


FIGURE 8. POWER vs f_{SAMPLE} IN 3mA LVDS MODE

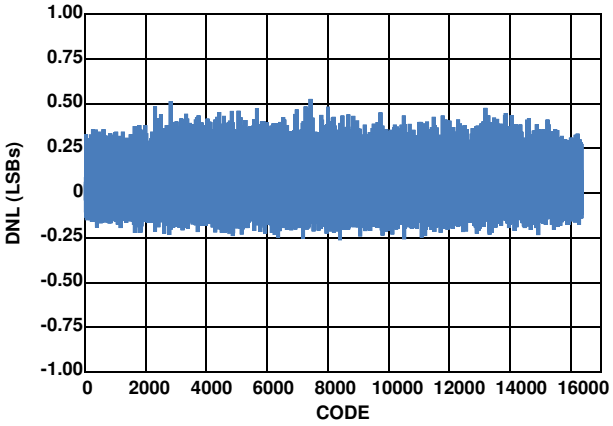


FIGURE 9. DIFFERENTIAL NONLINEARITY

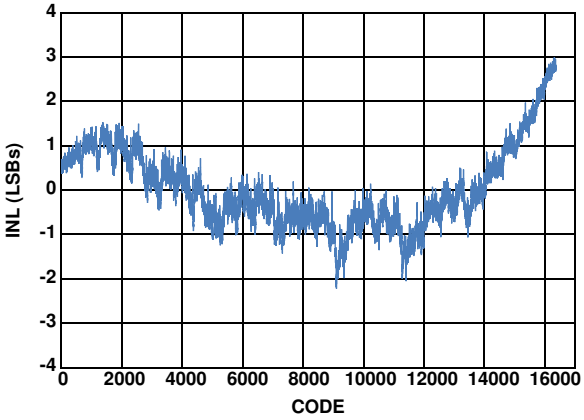


FIGURE 10. INTEGRAL NONLINEARITY

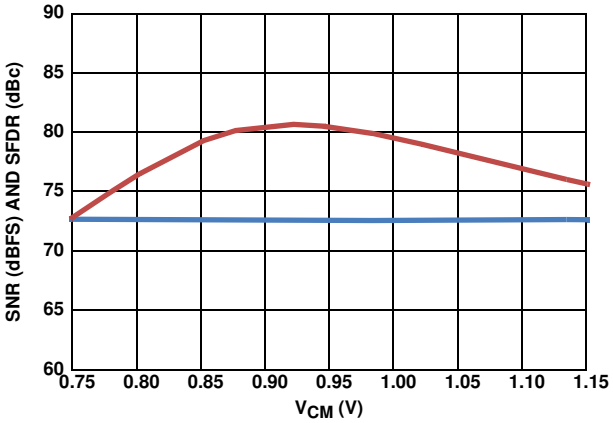


FIGURE 11. SNR AND SFDR vs V_{CM}

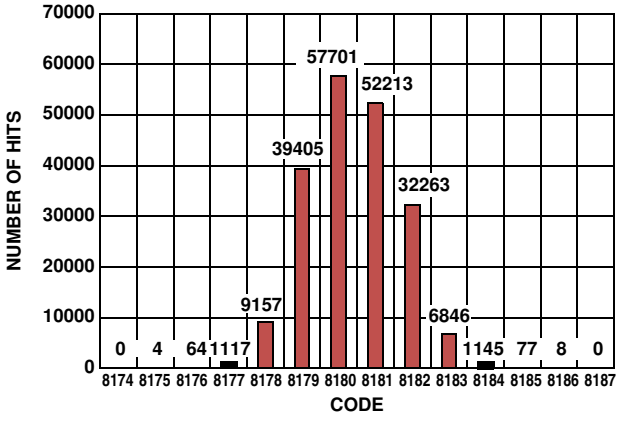


FIGURE 12. NOISE HISTOGRAM

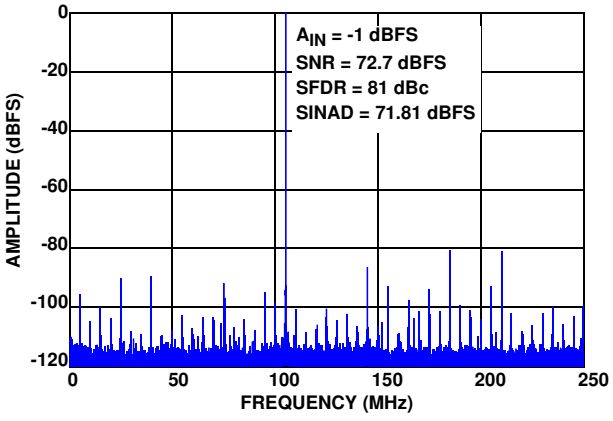


FIGURE 13. SINGLE-TONE SPECTRUM @ 105MHz

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -1dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 500MSPS. **(Continued)**

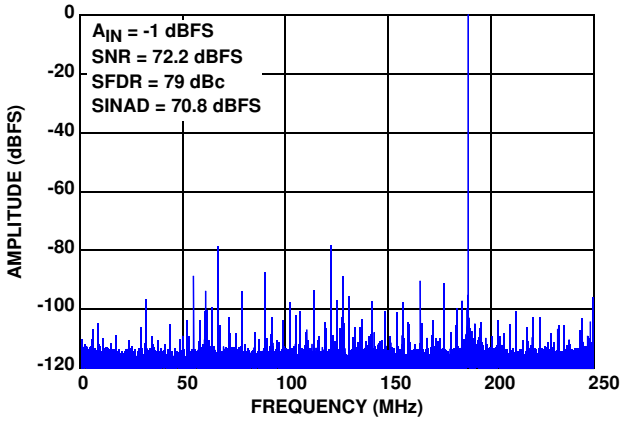


FIGURE 14. SINGLE-TONE SPECTRUM @ 190MHz

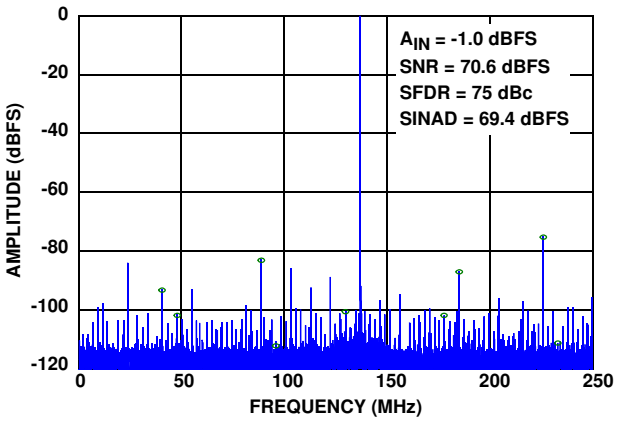


FIGURE 15. SINGLE-TONE SPECTRUM @ 363MHz

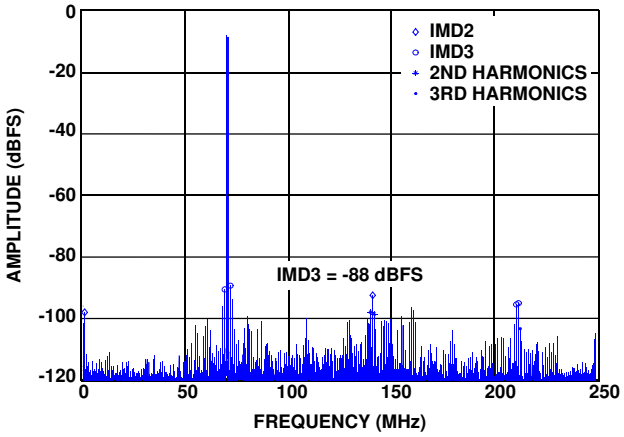


FIGURE 16. TWO-TONE SPECTRUM (F1 = 70MHz, F2 = 71MHz -7dBFS)

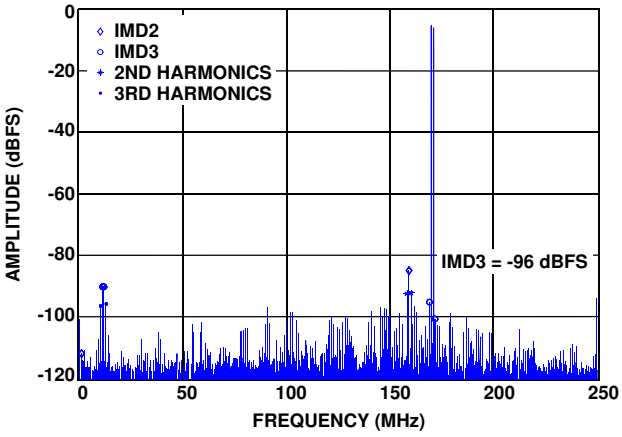


FIGURE 17. TWO-TONE SPECTRUM (F1 = 170MHz, F2 = 171MHz -7dBFS)

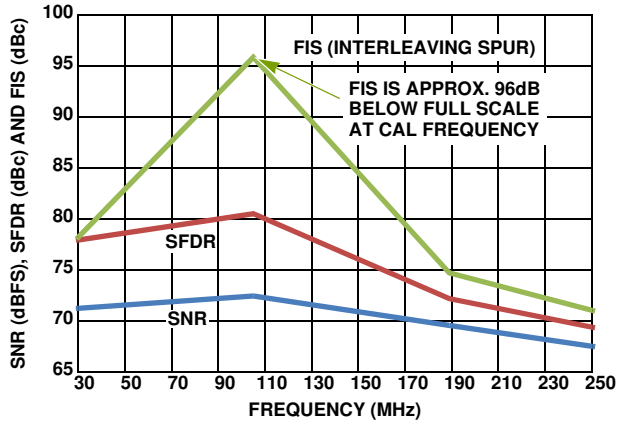


FIGURE 18. INPUT FREQUENCY SWEEP WITH I2E FROZEN, I2E PREVIOUSLY CALIBRATED AT 105MHZ

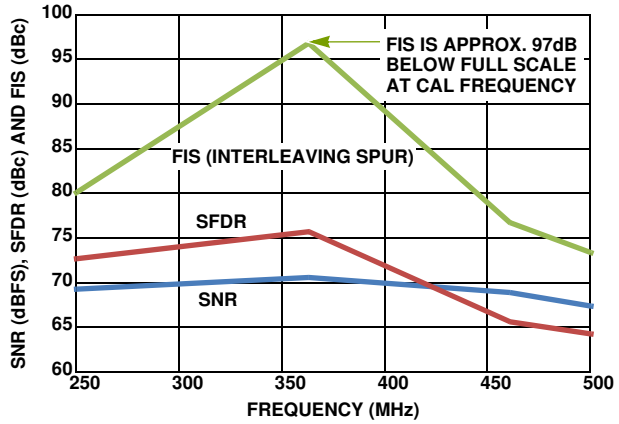


FIGURE 19. INPUT FREQUENCY SWEEP WITH I2E FROZEN, I2E PREVIOUSLY CALIBRATED AT 363MHZ

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -1dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 500MSPS. **(Continued)**

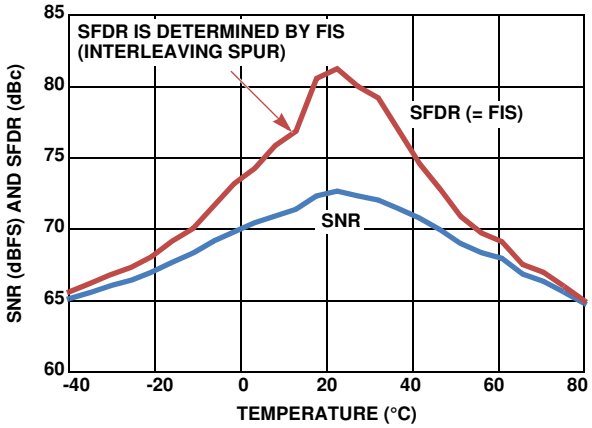


FIGURE 20. TEMPERATURE SWEEP WITH I2E FROZEN, I2E PREVIOUSLY CALIBRATED AT +25°C, F_{IN} = 105MHZ

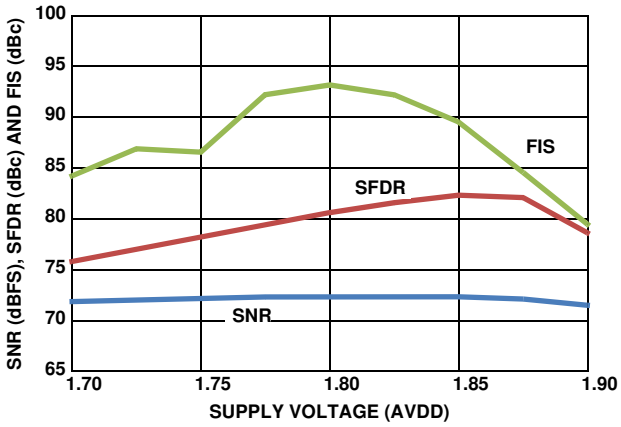


FIGURE 21. ANALOG SUPPLY VOLTAGE SWEEP WITH I2E FROZEN, I2E PREVIOUSLY CALIBRATED AT 1.8V, F_{IN} = 105MHZ

Theory of Operation

Functional Description

The ISLA214P50 is based upon a 14-bit, 250MSPS A/D converter core that utilizes a pipelined successive approximation architecture (Figure 22). The input voltage is captured by a Sample-Hold Amplifier (SHA) and converted to a unit of charge. Proprietary charge-domain techniques are used to successively compare the input to a series of reference charges. Decisions made during the successive approximation operations determine the digital code for each input value. Digital error correction is also applied, resulting in a total latency of 20 clock cycles. This is evident to the user as a latency between the start of a conversion and the data being available on the digital outputs.

The device contains two core A/D converters with carefully matched transfer characteristics. The cores are clocked on alternate clock edges, resulting in a doubling of the sample rate.

Time–interleaved A/D systems can exhibit non–ideal artifacts in the frequency domain if the individual core A/D characteristics are not well matched. Gain, offset and timing skew mismatches are of primary concern.

The Intersil Interleave Engine (I2E) performs automatic interleave calibration for the offset, gain, and sample time skew mismatch between the core A/Ds. The I2E circuitry also adjusts in real-time for temperature and voltage variations.

Residual gain and sample time skew mismatch result in fundamental image spurs at $f_{NYQUIST} \pm f_{IN}$. Offset mismatches create spurs at DC and multiples of $f_{NYQUIST}$.

Power-On Calibration

As mentioned previously, the cores perform a self-calibration at start-up. An internal power-on-reset (POR) circuit detects the supply voltage ramps and initiates the calibration when the analog and digital supply voltages are above a threshold. The following conditions must be adhered to for the power-on calibration to execute successfully:

- A frequency-stable conversion clock must be applied to the CLKP/CLKN pins
- DNC pins must not be connected
- SDO has an internal pull-up and should not be driven externally
- RESETN is pulled low by the ADC internally during POR. External driving of RESETN is optional.
- SPI communications must not be attempted

A user-initiated reset can subsequently be invoked in the event that the above conditions cannot be met at power-up.

After the power supply has stabilized the internal POR releases RESETN and an internal pull-up pulls it high, which starts the calibration sequence. If a subsequent user-initiated reset is desired, the RESETN pin should be connected to an open-drain driver with an off-state/high impedance state leakage of less than 0.5mA to assure exit from the reset state so calibration can start.

The calibration sequence is initiated on the rising edge of RESETN, as shown in Figure 23. Calibration status can be determined by reading the cal_status bit (LSB) at 0xB6. This bit is ‘0’ during calibration and goes to a logic ‘1’ when calibration is complete. The data outputs output 0xCCCC during calibration; this can also be used to determine calibration status.

While RESETN is low, the output clock (CLKOUTP/CLKOUTN) is set low. Normal operation of the output clock resumes at the next input clock edge (CLKP/CLKN) after RESETN is de-asserted. At 250MSPS the nominal calibration time is 200ms, while the maximum calibration time is 550ms.

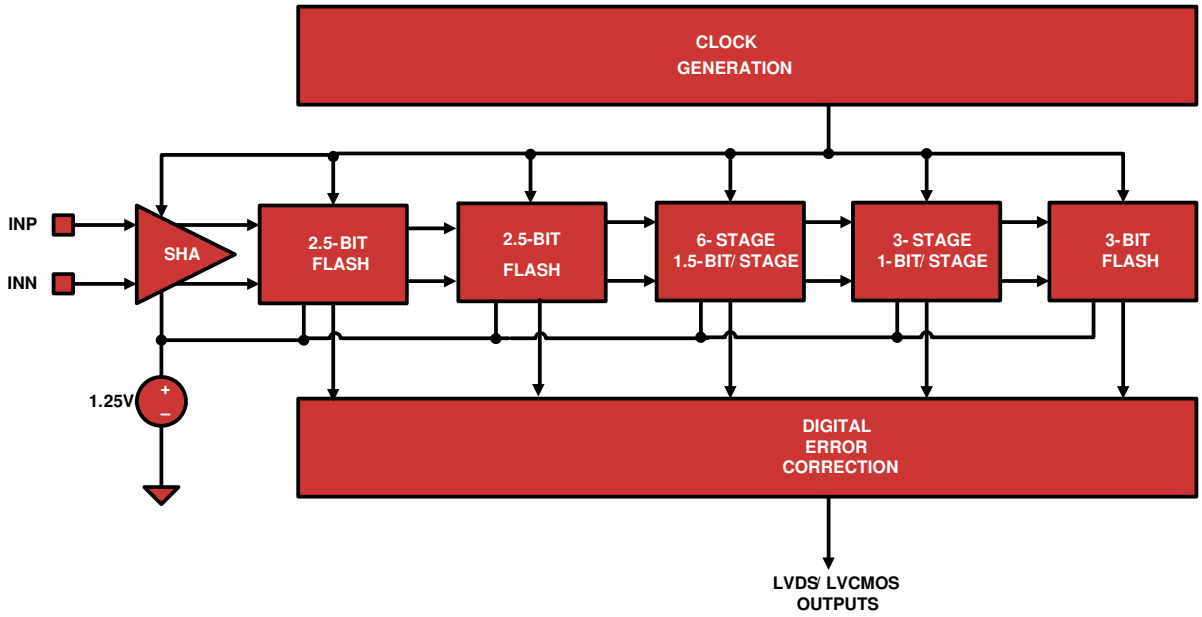


FIGURE 22. A/D CORE BLOCK DIAGRAM

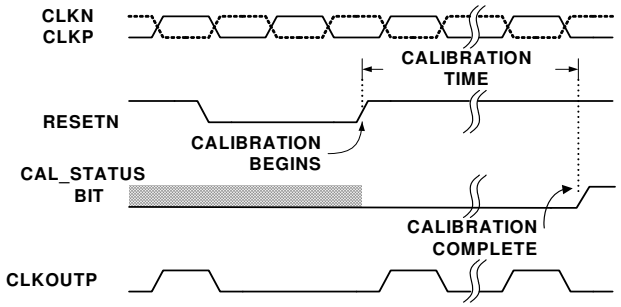


FIGURE 23. CALIBRATION TIMING

User Initiated Reset

Recalibration of the A/D can be initiated at any time by driving the RESETN pin low for a minimum of one clock cycle. An open-drain driver with a drive strength in its high impedance state of less than 0.5mA is recommended, as RESETN has an internal high impedance pull-up to OVDD. As is the case during power-on reset, RESETN and DNC pins must be in the proper state for the calibration to successfully execute.

The performance of the ISLA214P50 changes with variations in temperature, supply voltage or sample rate. The extent of these changes may necessitate recalibration, depending on system performance requirements. Best performance will be achieved by recalibrating the A/D under the environmental conditions at which it will operate.

A supply voltage variation of less than 100mV will generally result in an SNR change of less than 0.5dBFS and SFDR change of less than 3dBc.

In situations where the sample rate is not constant, best results will be obtained if the device is calibrated at the highest sample rate. Reducing the sample rate by less than 80MSPS will typically result in an SNR change of less than 0.5dBFS and an SFDR change of less than 3dBc.

Figures 24 through 26 show the effect of temperature on SNR and SFDR performance with power on calibration performed at -40°C, +25°C, and +85°C. Each plot shows the variation of SNR/SFDR across temperature after a single power on calibration at -40°C, +25°C and +85°C. Best performance is typically achieved by a user-initiated power on calibration at the operating conditions, as stated earlier. Applications working across the full temperature range can use the on-chip calibration feature to maximize performance when large temperature variations are expected.

Temperature Calibration

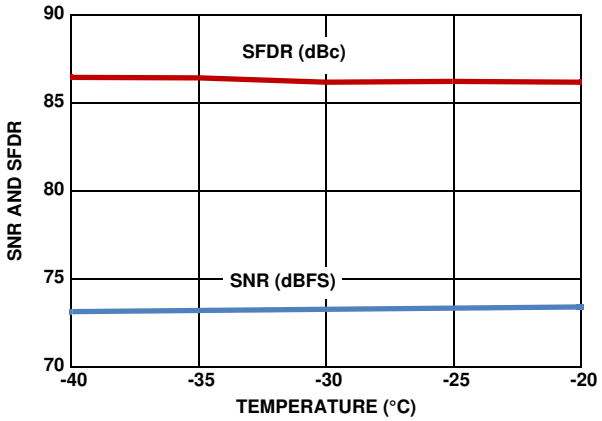


FIGURE 24. TYPICAL SNR, SFDR PERFORMANCE vs TEMPERATURE,DEVICE CALIBRATED AT -40°C, 500MSPS OPERATION, f_{IN} = 105MHz

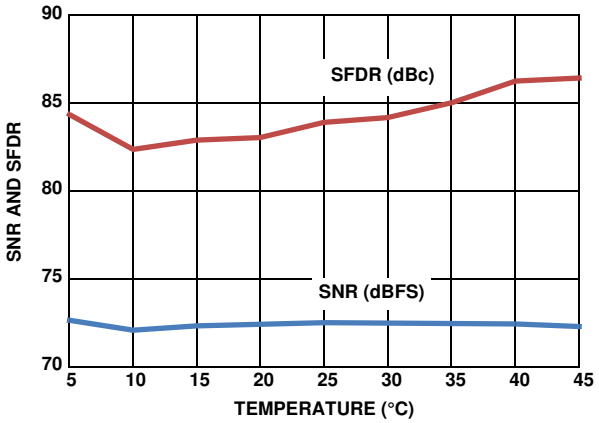


FIGURE 25. TYPICAL SNR, SFDR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +25°C, 500MSPS OPERATION, f_{IN} = 105MHz

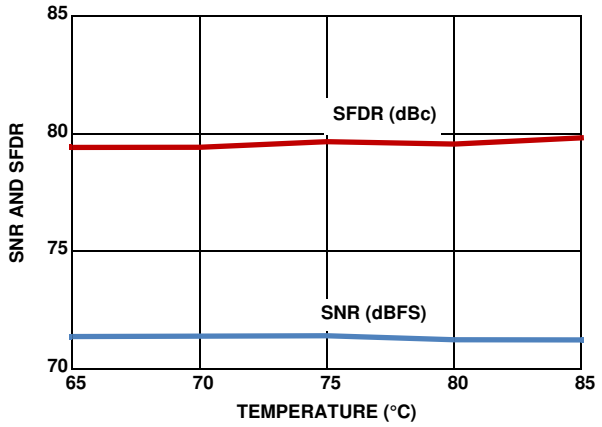


FIGURE 26. TYPICAL SNR, SFDR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +85°C, 500MSPS OPERATION, f_{IN} = 105MHz

Analog Input

A single fully differential input (VINP/VINN) connects to the sample and hold amplifier (SHA) of each unit A/D. The ideal full-scale input voltage is 2.0V, centered at the VCM voltage of 0.94V as shown in Figure 27.

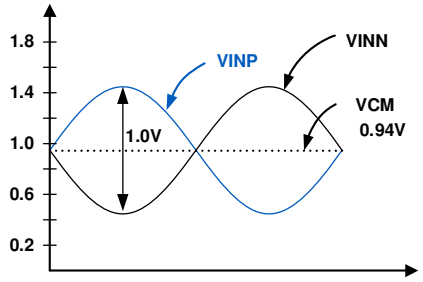


FIGURE 27. ANALOG INPUT RANGE

Best performance is obtained when the analog inputs are driven differentially. The common-mode output voltage, VCM, should be used to properly bias the inputs as shown in Figures 28 through 30. An RF transformer will give the best noise and distortion performance for wideband and/or high intermediate frequency (IF) inputs. Two different transformer input schemes are shown in Figures 28 and 29.

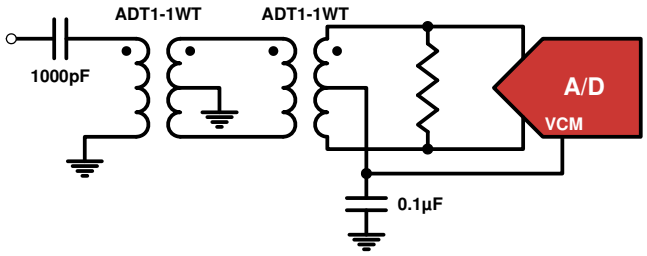


FIGURE 28. TRANSFORMER INPUT FOR GENERAL PURPOSE APPLICATIONS

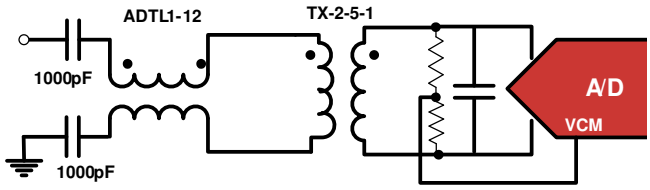


FIGURE 29. TRANSMISSION-LINE TRANSFORMER INPUT FOR HIGH IF APPLICATIONS

This dual transformer scheme is used to improve common-mode rejection, which keeps the common-mode level of the input matched to VCM. The value of the shunt resistor should be determined based on the desired load impedance. The differential input resistance of the ISLA214P50 is 300Ω.

The SHA design uses a switched capacitor input stage (see Figure 43 on page 35), which creates current spikes when the sampling capacitance is reconnected to the input voltage. This causes a disturbance at the input which must settle before the

next sampling point. Lower source impedance will result in faster settling and improved performance. Therefore a 1:1 transformer and low shunt resistance are recommended for optimal performance.

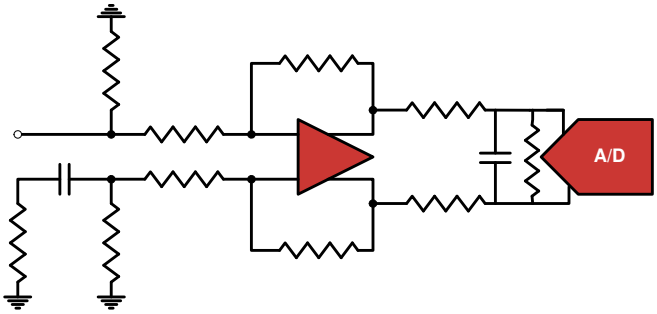


FIGURE 30. DIFFERENTIAL AMPLIFIER INPUT

A differential amplifier, as shown in the simplified block diagram in Figure 30, can be used in applications that require DC-coupling. In this configuration, the amplifier will typically dominate the achievable SNR and distortion performance. Intersil's new ISL552xx differential amplifier family can also be used in certain AC applications with minimal performance degradation. Contact the factory for more information.

Clock Input

The clock input circuit is a differential pair (see Figure 44). Driving these inputs with a high level (up to $1.8V_{P-P}$ on each input) sine or square wave will provide the lowest jitter performance. A transformer with 4:1 impedance ratio will provide increased drive levels. The clock input is functional with AC-coupled LVDS, LVPECL, and CML drive levels. To maintain the lowest possible aperture jitter, it is recommended to have high slew rate at the zero crossing of the differential clock input signal.

The recommended drive circuit is shown in Figure 31. A duty range of 40% to 60% is acceptable. The clock can be driven single-ended, but this will reduce the edge rate and may impact SNR performance. The clock inputs are internally self-biased to AVDD/2 to facilitate AC coupling.

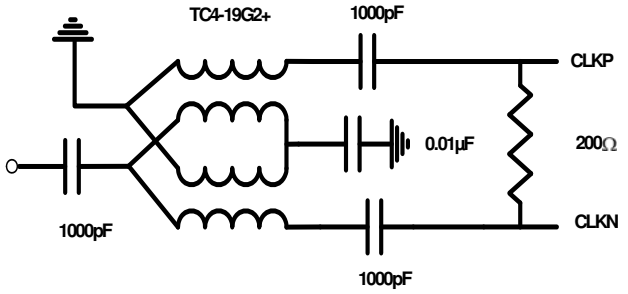


FIGURE 31. RECOMMENDED CLOCK DRIVE

A selectable 2x frequency divider is provided in series with the clock input. The divider can be used in the 2x mode with a sample clock equal to twice the desired sample rate. This allows the use of the Phase Slip feature, which enables synchronization of multiple ADCs. The Phase Slip feature can be used as an alternative to using the CLKDIVRST pins to synchronize ADCs in a multiple ADC system.

TABLE 1. CLKDIV PIN SETTINGS

CLKDIV PIN	DIVIDE RATIO
AVSS	2
Float	1
AVDD	Not Allowed

Jitter

In a sampled data system, clock jitter directly impacts the achievable SNR performance. The theoretical relationship between clock jitter (t_J) and SNR is shown in Equation 1 and is illustrated in Figure 32.

$$SNR = 20 \log_{10}\left(\frac{1}{2\pi f_{IN} t_J}\right) \quad \text{(EQ. 1)}$$

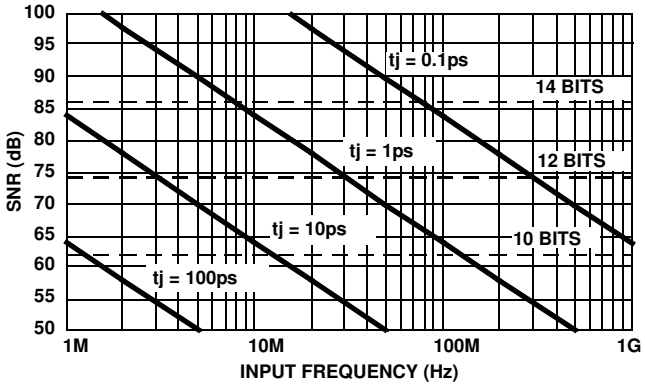


FIGURE 32. SNR vs CLOCK JITTER

This relationship shows the SNR that would be achieved if clock jitter were the only non-ideal factor. In reality, achievable SNR is limited by internal factors such as linearity, aperture jitter and thermal noise. Internal aperture jitter is the uncertainty in the sampling instant shown in Figure1A. The internal aperture jitter combines with the input clock jitter in a root-sum-square fashion, since they are not statistically correlated, and this determines the total jitter in the system. The total jitter, combined with other noise sources, then determines the achievable SNR.

Voltage Reference

A temperature compensated internal voltage reference provides the reference charges used in the successive approximation operations. The full-scale range of each A/D is proportional to the reference voltage. The nominal value of the voltage reference is 1.25V.

Digital Outputs

Output data is available as a parallel bus in LVDS-compatible(default) or CMOS modes. In either case, the data is presented in double data rate (DDR) format. Figures 1A and 1B show the timing relationships for LVDS and CMOS modes, respectively.

Additionally, the drive current for LVDS mode can be set to a nominal 3mA(default) or a power-saving 2mA. The lower current setting can be used in designs where the receiver is in close physical proximity to the A/D. The applicability of this setting is dependent upon the PCB layout, therefore the user should

experiment to determine if performance degradation is observed.

The output mode can be controlled through the SPI port, by writing to address 0x73, see “Serial Peripheral Interface” on page 25.

An external resistor creates the bias for the LVDS drivers. A 10kΩ, 1% resistor must be connected from the RLVDS pin to OVSS.

Power Dissipation

The power dissipated by the ISLA214P50 is primarily dependent on the sample rate and the output modes: LVDS vs CMOS and DDR vs SDR. There is a static bias in the analog supply, while the remaining power dissipation is linearly related to the sample rate. The output supply dissipation changes to a lesser degree in LVDS mode, but is more strongly related to the clock frequency in CMOS mode.

Nap/Sleep

Portions of the device may be shut down to save power during times when operation of the A/D is not required. Two power saving modes are available: Nap, and Sleep. Nap mode reduces power dissipation to less than 104mW while Sleep mode reduces power dissipation to less than 19mW.

All digital outputs (Data, CLKOUT and OR) are placed in a high impedance state during Nap or Sleep. The input clock should remain running and at a fixed frequency during Nap or Sleep, and CSB should be high. Recovery time from Nap mode will increase if the clock is stopped, since the internal DLL can take up to 52µs to regain lock at 500MSPS.

By default after the device is powered on, the operational state is controlled by the NAPSLP pin as shown in Table 2.

TABLE 2. NAPSLP PIN SETTINGS

NAPSLP PIN	MODE
AVSS	Normal
Float	Sleep
AVDD	Nap

The power-down mode can also be controlled through the SPI port, which overrides the NAPSLP pin setting. Details on this are contained in “Serial Peripheral Interface” on page 25.

Data Format

Output data can be presented in three formats: two’s complement (default), Gray code and offset binary. The data format can also be controlled through the SPI port, by writing to address 0x73. Details on this are contained in “Serial Peripheral Interface” on page 25.

Offset binary coding maps the most negative input voltage to code 0x000 (all zeros) and the most positive input to 0xFFF (all ones). Two’s complement coding simply complements the MSB of the offset binary representation.

When calculating Gray code the MSB is unchanged. The remaining bits are computed as the XOR of the current bit position and the next most significant bit. Figure 33 shows this operation.

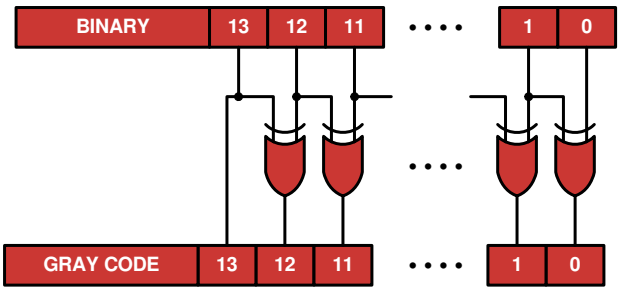
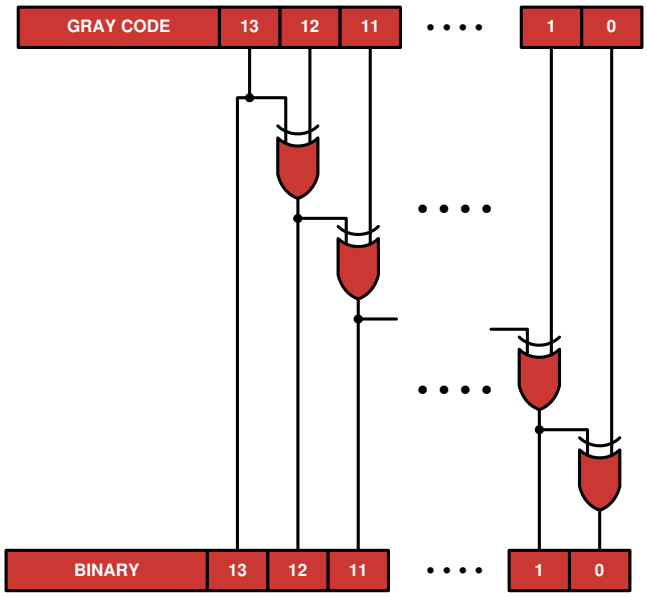


FIGURE 33. BINARY TO GRAY CODE CONVERSION

Converting back to offset binary from Gray code must be done recursively, using the result of each bit for the next lower bit as shown in Figure 34.



Mapping of the input voltage to the various data formats is shown in Table 3.

TABLE 3. INPUT VOLTAGE TO OUTPUT CODE MAPPING

INPUT VOLTAGE	OFFSET BINARY	TWO’S COMPLEMENT	GRAY CODE
–Full Scale	00 0000 0000 0000	10 0000 0000 0000	00 0000 0000 0000
–Full Scale + 1LSB	00 0000 0000 0001	10 0000 0000 0001	00 0000 0000 0001
Mid–Scale	10 0000 0000 0000	00 0000 0000 0000	11 0000 0000 0000
+Full Scale – 1LSB	11 1111 1111 1110	01 1111 1111 1110	10 0000 0000 0001
+Full Scale	11 1111 1111 1111	01 1111 1111 1111	10 0000 0000 0000

I2E Requirements and Restrictions

Overview

I2E is a blind and background capable algorithm, designed to transparently eliminate interleaving artifacts. This circuitry eliminates interleave artifacts due to offset, gain, and sample time mismatches between unit A/Ds, and across supply voltage and temperature variations in real-time.

Differences in the offset, gain, and sample times of time-interleaved A/Ds create artifacts in the digital outputs. Each of these artifacts creates a unique signature that may be detectable in the captured samples. The I2E algorithm optimizes performance by detecting error signatures and adjusting each unit A/D using minimal additional power.

I2E calibration is off by default at power-up. The I2E algorithm can be put in Active Run state via SPI. When the I2E algorithm is in Active Run state, it detects and corrects for offset, gain, and sample time mismatches in real time (see Track Mode description under “Active Run State” on page 22). However, certain analog input characteristics can obscure the estimation of these mismatches. The I2E algorithm is capable of detecting these obscuring analog input characteristics, and as long as they are present I2E will stop updating the correction in real time. Effectively, this freezes the current correction circuitry to the last known-good state (see Hold Mode description under “Active Run State” on page 22). Once the analog input signal stops obscuring the interleaved artifacts, the I2E algorithm will automatically start correcting for mismatch in real time again.

Active Run State

During the Active Run state the I2E algorithm actively suppresses artifacts due to interleaving based on statistics in the digitized data. I2E has two modes of operation in this state (described in the following), dynamically chosen in real-time by the algorithm based on the statistics of the analog input signal.

1. Track Mode refers to the default state of the algorithm, when all artifacts due to interleaving are actively being eliminated. To be in Track Mode the analog input signal to the device must adhere to the following requirements:

- Possess total power greater than -20dBFS, integrated from 1MHz to Nyquist but excluding signal energy in a 100kHz band centered at $f_S/4$

The criteria above assumes 500MSPS operation; the frequency bands should be scaled proportionally for lower sample rates. Note that the effect of excluding energy in the 100kHz band around of $f_S/4$ exists in every Nyquist zone. This band generalizes to the form ($N*f_S/4$ - 50kHz) to ($N*f_S/4$ + 50kHz), where N is any odd integer. An input signal that violates these criteria briefly (approximately 10µs), before and after which it meets this criteria, will not impact system performance.

The algorithm must be in Track Mode for approximately one second (defined as I2Epost_t on “I2E Specifications” on page 11) after power-up before the specifications apply. Once this requirement has been met, the specifications of the device will continue to be met while I2E remains in Track Mode, even in the presence of temperature and supply voltage changes.

2. Hold Mode refers to the state of the I2E algorithm when the analog input signal does not meet the requirements specified above. If the algorithm detects that the signal no longer meets the criteria, it automatically enters Hold Mode. In Hold Mode, the I2E circuitry freezes the adjustment values based on the most recent set of valid input conditions. However, in Hold Mode, the I2E circuitry will not correct for new changes in interleave artifacts induced by supply voltage and temperature changes. The I2E circuitry will remain in Hold Mode until such time as the analog input signal meets the requirements for Track Mode.

Power Meter

The power meter calculates the average power of the analog input, and determines if it’s within range to allow operation in Track Mode. Both AC RMS and total RMS power are calculated, and there are separate SPI programmable thresholds and hysteresis values for each.

FS/4 Filter

A digital filter removes the signal energy in a 100kHz band around $f_S/4$ before the I2E circuitry uses these samples for estimating offset, gain, and sample time mismatches (data samples produced by the A/D are unaffected by this filtering). This allows the I2E algorithm to continue in Active Run state while in the presence of a large amount of input energy near the $f_S/4$ frequency. This filter can be powered down if it’s known that the signal characteristics won’t violate the restrictions. Powering down the FS/4 filter will reduce power consumption by approximately 30mW.

Nyquist Zones

The I2E circuitry allows the use of any one Nyquist zone without configuration, but requires the use of only one Nyquist zone. Inputs that switch dynamically between Nyquist zones will cause poor performance for the I2E circuitry. For example, I2E will function properly for a particular application that has f_S = 500MSPS and uses the 1^{st} Nyquist zone (0MHz to 250MHz). I2E will also function properly for an application that uses f_S = 500MSPS and the 2^{nd} Nyquist zone (250MHz to 500MHz). I2E will not function properly for an application that uses f_S = 500MSPS, and input frequency bands from 150MHz to 210MHz and 250MHz to 290MHz simultaneously. There is no need to configure the I2E algorithm to use a particular Nyquist zone, but no dynamic switching between Nyquist zones is permitted while I2E is running.

Configurability and Communication

I2E can respond to status queries, be turned on and turned off, and generally configured via SPI programmable registers. Configuring of I2E is generally unnecessary unless the application cannot meet the requirements of Track Mode on or after power up. Parameters that can be adjusted and read back include FS/4 filter threshold and status, Power Meter threshold and status, and initial values for the offset, gain, and sample time values to use when I2E starts.

Clock Divider Synchronous Reset

An output clock (CLKOUTP, CLKOUTN) is provided to facilitate latching of the sampled data. This clock is at half the frequency of the sample clock, and the absolute phase of the output clocks for multiple A/Ds is indeterminate. This feature allows the phase of multiple A/Ds to be synchronized (refer to Figure 35), which greatly simplifies data capture in systems employing multiple A/Ds.

The reset signal must be well-timed with respect to the sample clock (see “Switching Specifications” Table on page 13).

A 100Ω differential termination resistor must be supplied between CLKDIVRSTP and CLKDIVRSTN, external to the ADC, (on the PCB) and should be located as close to the CLKDIVRSTP/N pins as possible.

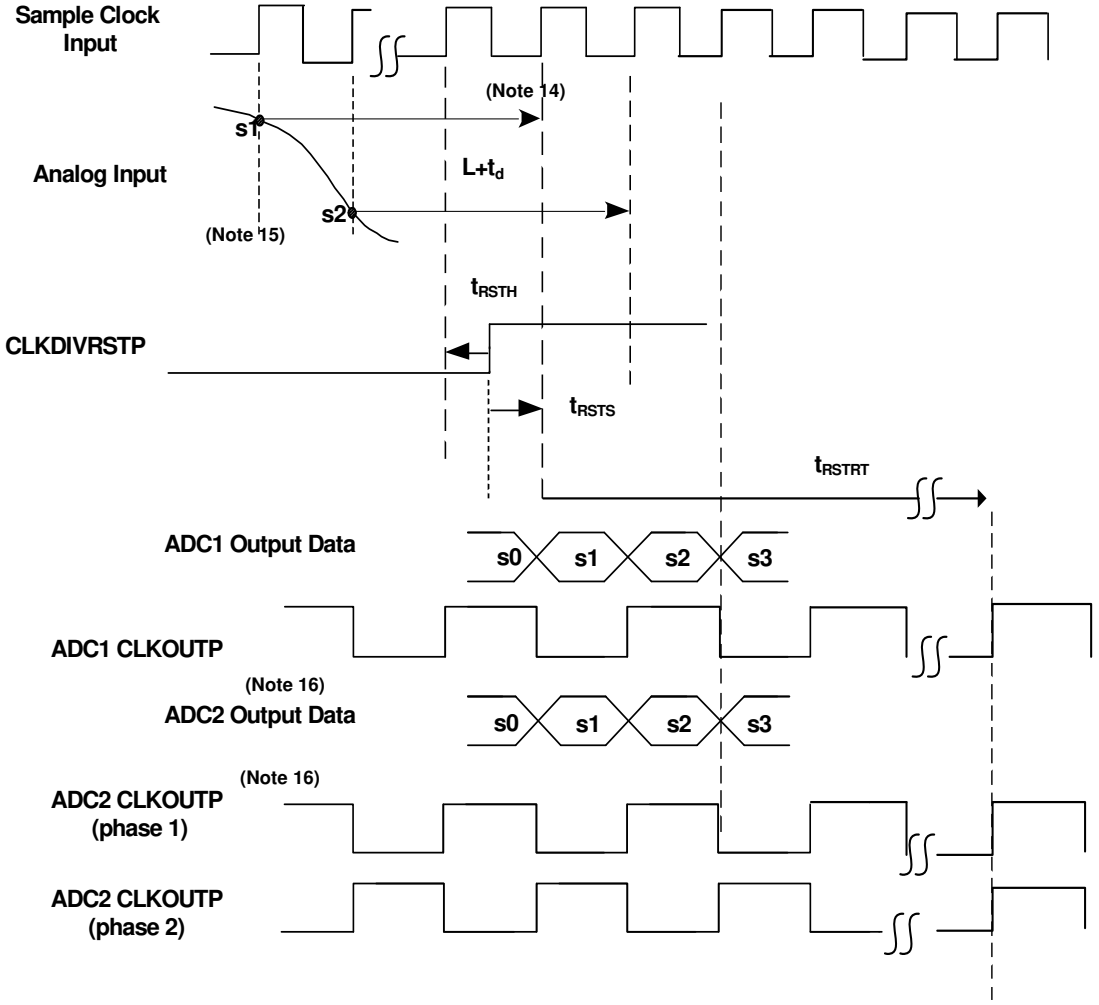


FIGURE 35. SYNCHRONOUS RESET OPERATION

NOTES:

14. Delay equals fixed pipeline latency (L cycles) plus fixed analog propagation delay t_d
15. CLKDIVRSTP setup and hold times are with respect to input sample clock rising edge. CLKDIVRSTN is not shown, but must be driven, and is the compliment of CLKDIVRSTP
16. Either Output Clock Phase (phase 1 or phase 2) equally likely prior to synchronization.

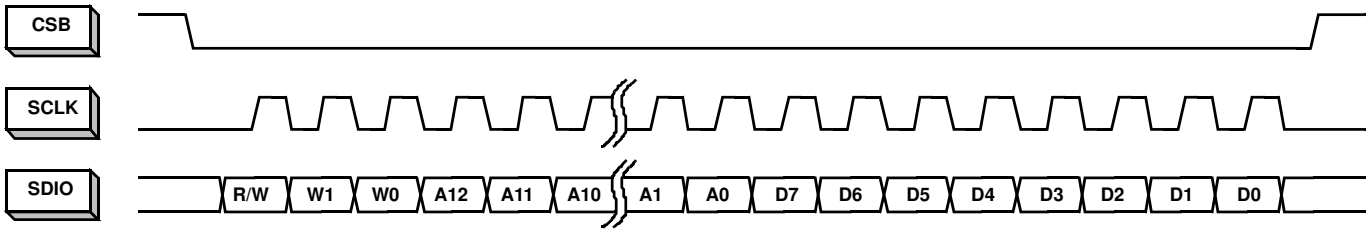


FIGURE 36. MSB-FIRST ADDRESSING

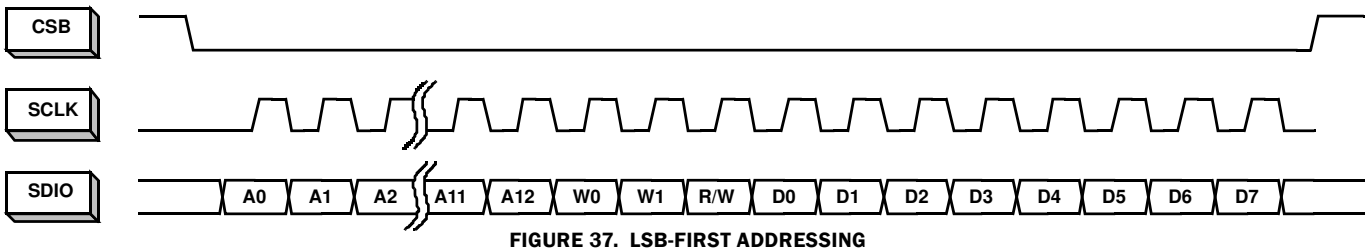
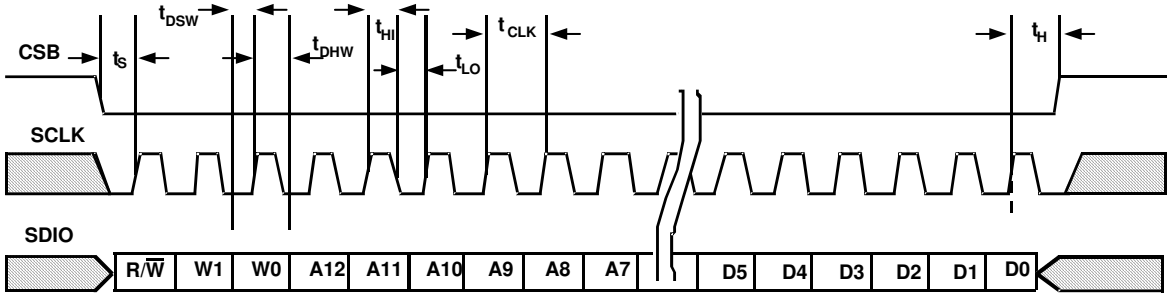


FIGURE 37. LSB-FIRST ADDRESSING



SPI WRITE

FIGURE 38. SPI WRITE

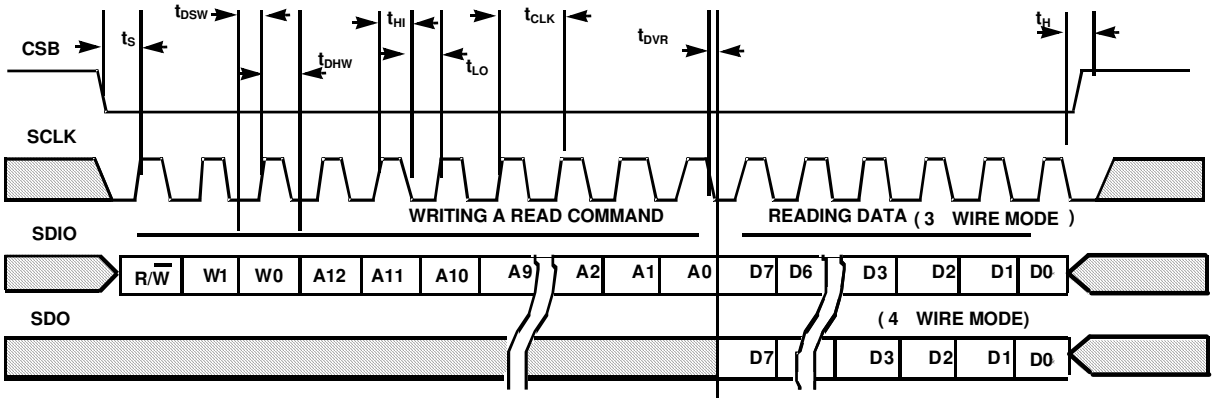


FIGURE 39. SPI READ

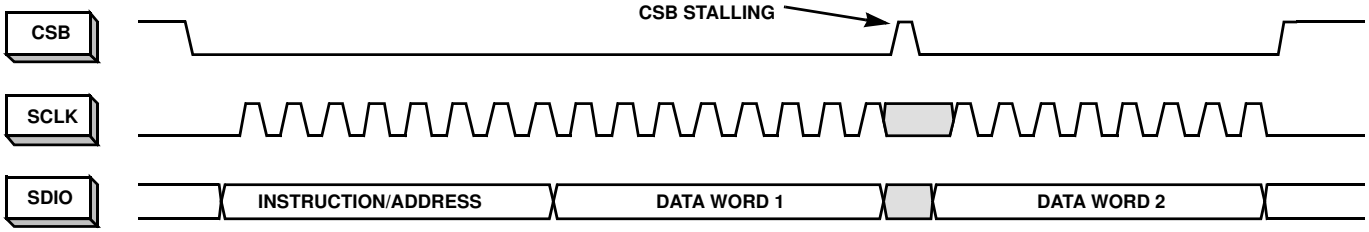


FIGURE 40. 2-BYTE TRANSFER

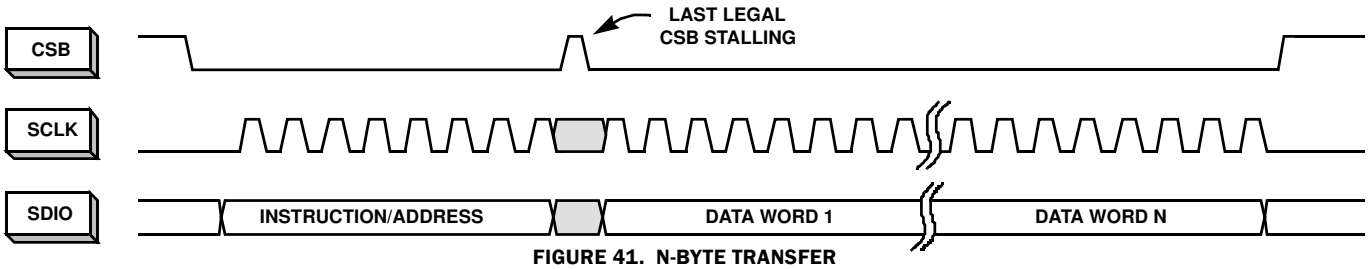


FIGURE 41. N-BYTE TRANSFER

Serial Peripheral Interface

A serial peripheral interface (SPI) bus is used to facilitate configuration of the device and to optimize performance. The SPI bus consists of chip select (CSB), serial clock (SCLK) serial data output (SDO), and serial data input/output (SDIO). The maximum SCLK rate is equal to the A/D sample rate (f_{SAMPLE}) divided by 32 for both write operations and read operations. At f_{SAMPLE} = 500MHz, maximum SCLK is 15.63MHz for writing and read operations. There is no minimum SCLK rate.

The following sections describe various registers that are used to configure the SPI or adjust performance or functional parameters. Many registers in the available address space (0x00 to 0xFF) are not defined in this document. Additionally, within a defined register there may be certain bits or bit combinations that are reserved. Undefined registers and undefined values within defined registers are reserved and should not be selected. Setting any reserved register or value may produce indeterminate results.

SPI Physical Interface

The serial clock pin (SCLK) provides synchronization for the data transfer. By default, all data is presented on the serial data input/output (SDIO) pin in three-wire mode. The state of the SDIO pin is set automatically in the communication protocol (described in the following). A dedicated serial data output pin (SDO) can be activated by setting 0x00[7] high to allow operation in four-wire mode.

The SPI port operates in a half duplex master/slave configuration, with the ISLA214P50 functioning as a slave. Multiple slave devices can interface to a single master in three-wire mode only, since the SDO output of an unaddressed device is asserted in four wire mode.

The chip-select bar (CSB) pin determines when a slave device is being addressed. Multiple slave devices can be written to concurrently, but only one slave device can be read from at a given time (again, only in three-wire mode). If multiple slave devices are selected for reading at the same time, the results will be indeterminate.

The communication protocol begins with an instruction/address phase. The first rising SCLK edge following a high to low transition on CSB determines the beginning of the two-byte instruction/address command; SCLK must be static low before the CSB transition. Data can be presented in MSB-first order or LSB-first order. The default is MSB-first, but this can be changed by setting 0x00[6] high. Figures 36 and 37 show the appropriate bit ordering for the MSB-first and LSB-first modes, respectively. In MSB-first mode, the address is incremented for multi-byte transfers, while in LSB-first mode it's decremented.

In the default mode, the MSB is R/W, which determines if the data is to be read (active high) or written. The next two bits, W1 and W0, determine the number of data bytes to be read or written (see Table 4). The lower 13 bits contain the first address for the data transfer. This relationship is illustrated in Figure 38, and timing values are given in "Switching Specifications Boldface limits apply over the operating temperature range, -40°C to +85°C." on page 13.

After the instruction/address bytes have been read, the appropriate number of data bytes are written to or read from the A/D (based on the R/W bit status). The data transfer will continue as long as CSB remains low and SCLK is active. Stalling of the CSB pin is allowed at any byte boundary (instruction/address or data) if the number of bytes being transferred is three or less. For transfers of four bytes or more, CSB is allowed to stall in the middle of the instruction/address bytes or before the first data byte. If CSB transitions to a high state after that point the state machine will reset and terminate the data transfer.

TABLE 4. BYTE TRANSFER SELECTION

[W1:W0]	BYTES TRANSFERRED
00	1
01	2
10	3
11	4 or more

Figures 40 and 41 illustrate the timing relationships for 2-byte and N-byte transfers, respectively. The operation for a 3-byte transfer can be inferred from these diagrams.

SPI Configuration

ADDRESS 0X00: CHIP_PORT_CONFIG

Bit ordering and SPI reset are controlled by this register. Bit order can be selected as MSB to LSB (MSB first) or LSB to MSB (LSB first) to accommodate various micro controllers.

Bit 7 SDO Active

Bit 6 LSB First

Setting this bit high configures the SPI to interpret serial data as arriving in LSB to MSB order.

Bit 5 Soft Reset

Setting this bit high resets all SPI registers to default values.

Bit 4 Reserved

This bit should always be set high.