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16-Bit, 250MSPS/200MSPS/130MSPS ADC

ISLA216P

The ISLA216P is a family of low power, high performance 16-bit analog-to-digital converters. Designed with Intersil's proprietary FemtoCharge™ technology on a standard CMOS process, the family supports sampling rates of up to 250MSPS. The ISLA216P is part of a pin-compatible portfolio of 12 to 16-bit A/Ds with maximum sample rates ranging from 130MSPS to 500MSPS.

A serial peripheral interface (SPI) port allows for extensive configurability, as well as fine control of various parameters such as gain and offset.

Digital output data is presented in selectable LVDS or CMOS formats. The ISLA216P is available in a 72-contact QFN package with an exposed paddle. Operating from a 1.8V supply, performance is specified over the full industrial temperature range (-40°C to +85°C).

Key Specifications

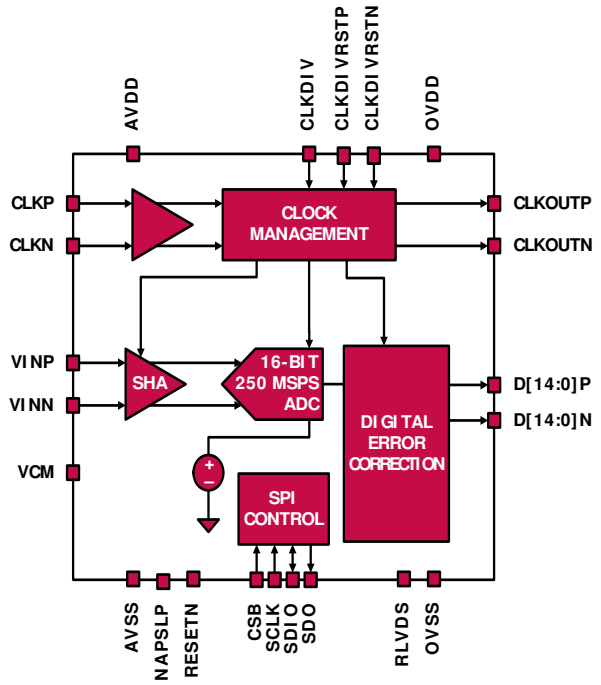
- SNR @ 250/200/130MSPS
  - 75.0/76.6/77.5dBFS f_{IN} = 30MHz
  - 72.1/72.6/72.4dBFS f_{IN} = 363MHz
- SFDR @ 250/200/130MSPS
  - 87/91/96dBc f_{IN} = 30MHz
  - 81/80/82dBc f_{IN} = 363MHz
- Total Power Consumption = 786mW @ 250MSPS

Features

- Single supply 1.8V operation
- Clock duty cycle stabilizer
- 75fs Clock jitter
- 700MHz Bandwidth
- Programmable built-in test patterns
- Multi-ADC support
  - SPI Programmable fine gain and offset control
  - Support for multiple ADC synchronization
  - Optimized output timing
- Nap and sleep modes
  - 200µs Sleep wake-up time
- Data output clock
- DDR LVDS-compatible or LVCMOS outputs
- Selectable Clock Divider

Applications

- Radar array processing
- Software defined radios
- Broadband communications
- High-performance data acquisition
- Communications test equipment

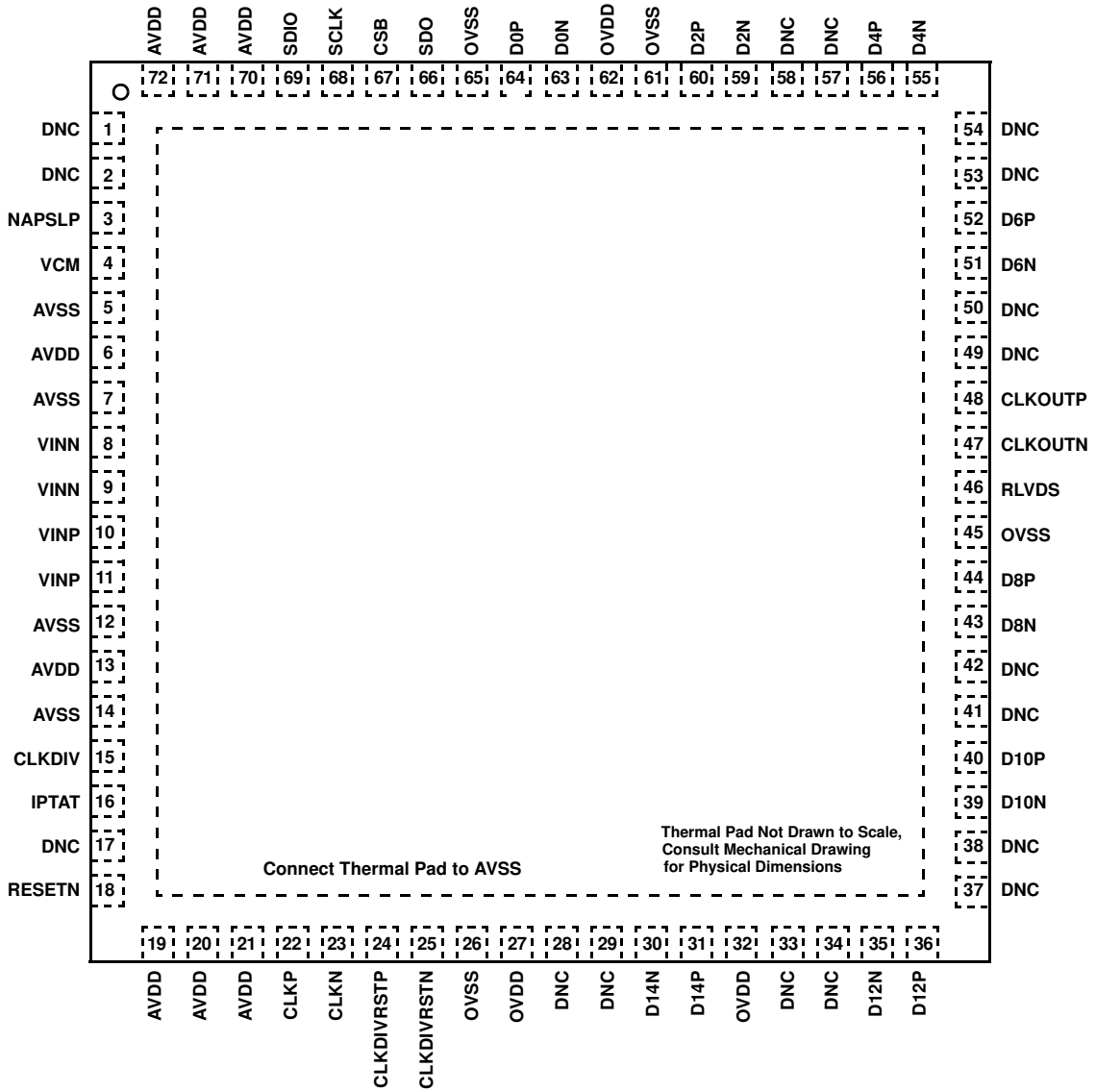


Pin-Compatible Family

MODEL	RESOLUTION	SPEED (MSPS)
ISLA216P25	16	250
ISLA216P20	16	200
ISLA216P13	16	130
ISLA214P50	14	500
ISLA214P25	14	250
ISLA214P20	14	200
ISLA214P13	14	130
ISLA212P50	12	500
ISLA212P25	12	250
ISLA212P20	12	200
ISLA212P13	12	130

Pin Configuration - LVDS MODE

ISLA216P
(72 LD QFN)
TOP VIEW



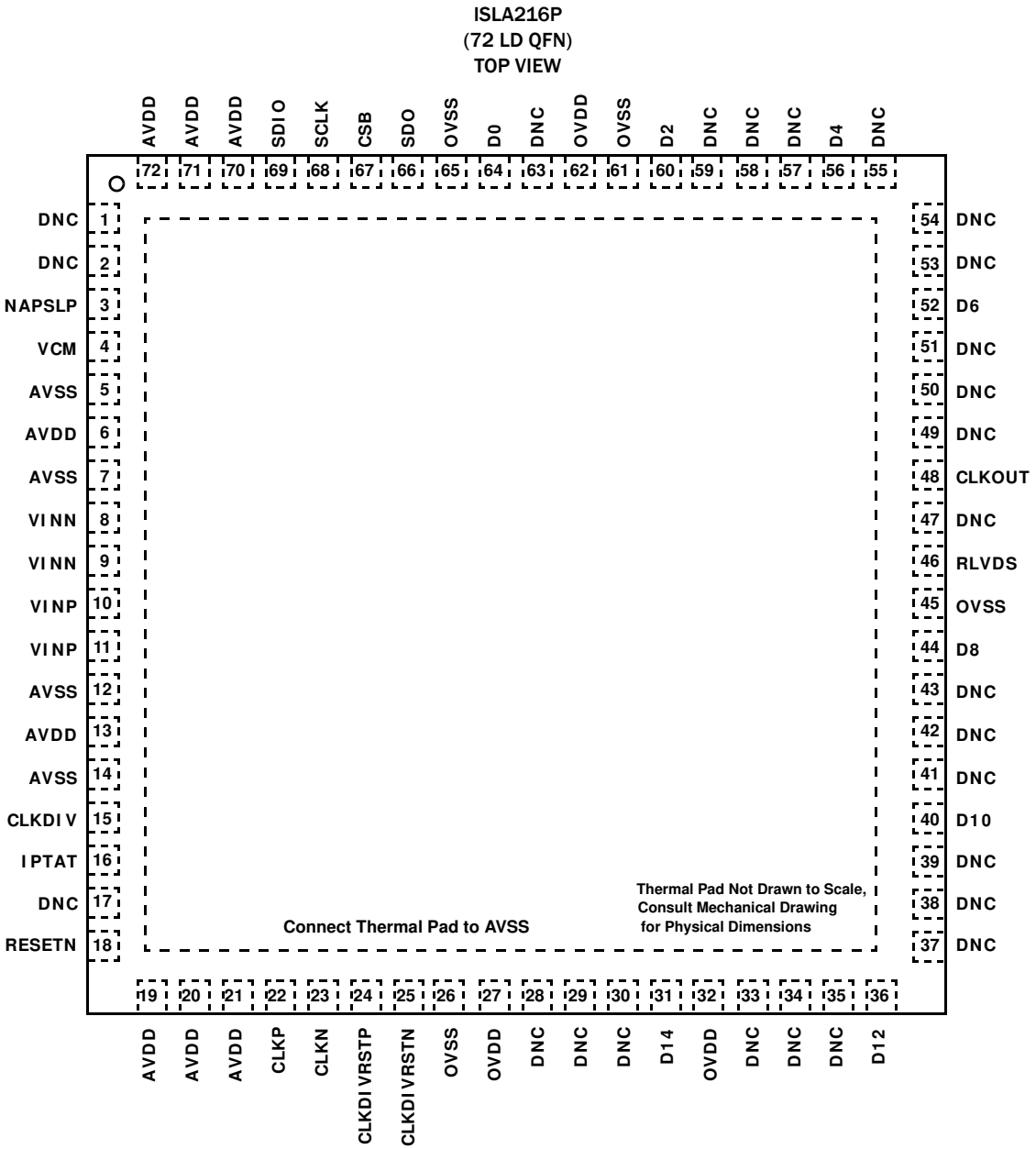
Pin Descriptions - 72 Ld QFN, LVDS Mode

PIN NUMBER	LVDS PIN NAME	LVDS PIN FUNCTION
1, 2, 17, 28, 29, 33, 34, 37, 38, 41, 42, 49, 50, 53, 54, 57, 58	DNC	Do Not Connect
6, 13, 19, 20, 21, 70, 71, 72	AVDD	1.8V Analog Supply
5, 7, 12, 14	AVSS	Analog Ground
27, 32, 62	OVDD	1.8V Output Supply
26, 45, 61, 65	OVSS	Output Ground
3	NAPSLP	Tri-Level Power Control (Nap, Sleep modes)

Pin Descriptions - 72 Ld QFN, LVDS Mode (Continued)

PIN NUMBER	LVDS PIN NAME	LVDS PIN FUNCTION
4	VCM	Common Mode Output
8, 9	VINN	Analog Input Negative
10, 11	VINP	Analog Input Positive
15	CLKDIV	Tri-Level Clock Divider Control
16	IPTAT	Temperature Monitor (Output current proportional to absolute temperature)
18	RESETN	Power On Reset (Active Low)
22, 23	CLKP, CLKN	Clock Input True, Complement
24, 25	CLKDIVRSTP, CLKDIVRSTN	Synchronous Clock Divider Reset True, Complement
30	D14N	DDR Logical Bits 14, 15 Complement
31	D14P	DDR Logical Bits 14, 15 True
35	D12N	DDR Logical Bits 12, 13 Complement
36	D12P	DDR Logical Bits 12, 13 True
39	D10N	DDR Logical Bits 10, 11 Complement
40	D10P	DDR Logical Bits 10, 11 True
43	D8N	DDR Logical Bits 8, 9 Complement
44	D8P	DDR Logical Bits 8, 9 True
46	RLVDS	LVDS Bias Resistor (Connect to OVSS with 1%10kΩ)
47, 48	CLKOUTN, CLKOUTP	LVDS Clock Output Complement, True
51	D6N	DDR Logical Bits 6, 7 Complement
52	D6P	DDR Logical Bits 6, 7 True
55	D4N	DDR Logical Bits 4, 5 Complement
56	D4P	DDR Logical Bits 4, 5 True
59	D2N	DDR Logical Bits 2, 3 Complement
60	D2P	DDR Logical Bits 2, 3 True
63	D0N	DDR Logical Bits 0, 1 Complement
64	D0P	DDR Logical Bits 0, 1 True
66	SDO	SPI Serial Data Output
67	CSB	SPI Chip Select (active low)
68	SCLK	SPI Clock
69	SDIO	SPI Serial Data Input/Output
Exposed Paddle	AVSS	Analog Ground

Pin Configuration - CMOS MODE



Pin Descriptions - 72 Ld QFN, CMOS Mode

PIN NUMBER	CMOS PIN NAME	CMOS PIN FUNCTION
1, 2, 17, 28, 29, 30, 33, 34, 35, 37, 38, 39, 41, 42, 43, 47, 49, 50, 51, 53, 54, 55, 57, 58, 59, 63	DNC	Do Not Connect
6, 13, 19, 20, 21, 70, 71, 72	AVDD	1.8V Analog Supply
5, 7, 12, 14	AVSS	Analog Ground
27, 32, 62	OVDD	1.8V Output Supply
26, 45, 61, 65	OVSS	Output Ground
3	NAPSLP	Tri-Level Power Control (Nap, Sleep modes)

Pin Descriptions - 72 Ld QFN, CMOS Mode (Continued)

PIN NUMBER	CMOS PIN NAME	CMOS PIN FUNCTION
4	VCM	Common Mode Output
8, 9	VINN	Analog Input Negative
10, 11	VINP	Analog Input Positive
15	CLKDIV	Tri-Level Clock Divider Control
16	IPTAT	Temperature Monitor (Output current proportional to absolute temperature)
18	RESETN	Power On Reset (Active Low)
22, 23	CLKP, CLKN	Clock Input True, Complement
24, 25	CLKDIVRSTP, CLKDIVRSTN	Synchronous Clock Divider Reset True, Complement
31	D14	DDR Logical Bits 14, 15
36	D12	DDR Logical Bits 12, 13
40	D10	DDR Logical Bits 10, 11
44	D8	DDR Logical Bits 8, 9
46	RLVDS	LVDS Bias Resistor (Connect to OVSS with 1%10kΩ)
48	CLKOUT	CMOS Clock Output
52	D6	DDR Logical Bits 6, 7
56	D4	DDR Logical Bits 4, 5
60	D2	DDR Logical Bits 2, 3
64	D0	DDR Logical Bits 0, 1
66	SDO	SPI Serial Data Output
67	CSB	SPI Chip Select (active low)
68	SCLK	SPI Clock
69	SDIO	SPI Serial Data Input/Output
Exposed Paddle	AVSS	Analog Ground

Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISLA216P13IRZ	ISLA216P13 IRZ	-40°C to +85°C	72 Ld QFN	L72.10x10E
ISLA216P20IRZ	ISLA216P20 IRZ	-40°C to +85°C	72 Ld QFN	L72.10x10E
ISLA216P25IRZ	ISLA216P25 IRZ	-40°C to +85°C	72 Ld QFN	L72.10x10E
Coming Soon ISLA216P13IR1Z	ISLA216P13 IR1Z	-40°C to +85°C	48 Ld QFN	TBD
Coming Soon ISLA216P20IR1Z	ISLA216P20 IR1Z	-40°C to +85°C	48 Ld QFN	TBD
Coming Soon ISLA216P25IR1Z	ISLA216P25 IR1Z	-40°C to +85°C	48 Ld QFN	TBD
ISLA216IR72EV1Z	Evaluation Board (72 pin QFN ADC)			

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), please see device information page for ISLA216P. For more information on MSL please see techbrief TB363.

Table of Contents

Absolute Maximum Ratings

AVDD to AVSS . . . . . -0.4V to 2.1V
OVDD to OVSS . . . . . -0.4V to 2.1V
AVSS to OVSS . . . . . -0.3V to 0.3V
Analog Inputs to AVSS . . . . . -0.4V to AVDD + 0.3V
Clock Inputs to AVSS . . . . . -0.4V to AVDD + 0.3V
Logic Input to AVSS . . . . . -0.4V to OVDD + 0.3V
Logic Inputs to OVSS . . . . . -0.4V to OVDD + 0.3V
Latchup (Tested per JESD-78C;Class 2,Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
72 Ld QFN (Notes 3, 4)	23	0.9
48 Ld QFN (Notes 3, 4)	24	1.0

Operating Temperature . . . . . -40°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
4. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T_A = -40°C to +85°C (typical specifications at +25°C), A_{IN} = -2dBFS, f_{SAMPLE} = Maximum Conversion Rate (per speed grade). **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	CONDITIONS	ISLA216P25			ISLA216P20			ISLA216P13			UNITS
			MIN (Note 5)	TYP	MAX (Note 5)	MIN (Note 5)	TYP	MAX (Note 5)	MIN (Note 5)	TYP	MAX (Note 5)	
DC SPECIFICATIONS (Note 6)												
Analog Input												
Full-Scale Analog Input Range	V_{FS}	Differential	**1.95**	2.0	**2.2**	**1.95**	2.0	**2.2**	**1.95**	2.0	**2.2**	V_{P-P}
Input Resistance	R_{IN}	Differential		300			300			300		Ω
Input Capacitance	C_{IN}	Differential		9			9			9		pF
Full Scale Range Temp. Drift	A_{VTC}	Full Temp		180			180			180		ppm/°C
Input Offset Voltage	V_{OS}		**-5.0**	-1.7	**5.0**	**-5.0**	-1.7	**5.0**	**-5.0**	-1.7	**5.0**	mV
Common-Mode Output Voltage	V_{CM}			0.94			0.94			0.94		V
Common-Mode Input Current (per pin)	I_{CM}			5.2			5.2			5.2		µA/MSPS
Clock Inputs												
Inputs Common Mode Voltage				0.9			0.9			0.9		V
CLKP,CLKN Input Swing				1.8			1.8			1.8		V
Power Requirements												
1.8V Analog Supply Voltage	AVDD		**1.7**	1.8	**1.9**	**1.7**	1.8	**1.9**	**1.7**	1.8	**1.9**	V
1.8V Digital Supply Voltage	OVDD		**1.7**	1.8	**1.9**	**1.7**	1.8	**1.9**	**1.7**	1.8	**1.9**	V
1.8V Analog Supply Current	I_{AVDD}			372	**397**		342	**360**		293	**310**	mA
1.8V Digital Supply Current (Note 6)	I_{OVDD}	3mA LVDS		64	**73**		58	**68**		50	**58**	mA
Power Supply Rejection Ratio	PSRR	30MHz, 50mVP-P signal on AVDD		-65			-65			-65		dB

Electrical Specifications All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T_A = -40°C to +85°C (typical specifications at +25°C), A_{IN} = -2dBFS, f_{SAMPLE} = Maximum Conversion Rate (per speed grade). **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	CONDITIONS	ISLA216P25			ISLA216P20			ISLA216P13			UNITS
			MIN (Note 5)	TYP	MAX (Note 5)	MIN (Note 5)	TYP	MAX (Note 5)	MIN (Note 5)	TYP	MAX (Note 5)	
Total Power Dissipation												
Normal Mode	P_D	2mA LVDS		771			706			603		mW
		3mA LVDS		786	**846**		720	**770**		616	**662**	mW
		CMOS		760			685			580		mW
Nap Mode	P_D			88	**103**		83	**99**		77	**94**	mW
Sleep Mode	P_D	CSB at logic high		7	**19**		7	**19**		7	**19**	mW
Nap/Sleep Mode Wakeup Time		Sample Clock Running		200			400			630		µs
AC SPECIFICATIONS												
Differential Nonlinearity	DNL	f_{IN} = 30MHz **No Missing Codes**	**-0.99**	±0.35		**-0.99**	±0.25		**-0.99**	±0.25		LSB
Integral Nonlinearity	INL	f_{IN} = 30MHz		±10			±6			±5		LSB
Minimum Conversion Rate (Note 7)	f_S MIN				**40**			**40**			**40**	MSPS
Maximum Conversion Rate	f_S MAX		**250**			**200**			**130**			MSPS
Signal-to-Noise Ratio (Note 8)	SNR	f_{IN} = 30MHz		75.0			76.6			77.5		dBFS
		f_{IN} = 105MHz	71.7	74.9		74.8	76.4		75.5	76.9		dBFS
		f_{IN} = 190MHz		74.2			75.3			75.3		dBFS
		f_{IN} = 363MHz		72.1			72.6			72.4		dBFS
		f_{IN} = 461MHz		71.1			71.1			70.8		dBFS
		f_{IN} = 605MHz		69.2			69.2			68.9		dBFS
Signal-to-Noise and Distortion (Note 8)	SINAD	f_{IN} = 30MHz		74.7			76.5			77.4		dBFS
		f_{IN} = 105MHz	70.0	74.1		73.2	76.1		72.6	76.1		dBFS
		f_{IN} = 190MHz		73.1			74.7			74.6		dBFS
		f_{IN} = 363MHz		71.6			71.7			71.9		dBFS
		f_{IN} = 461MHz		69.2			68.6			67.9		dBFS
		f_{IN} = 605MHz		65.7			64.9			66.3		dBFS
Effective Number of Bits (Note 8)	ENOB	f_{IN} = 30MHz		12.12			12.42			12.56		Bits
		f_{IN} = 105MHz	11.34	12.02		11.87	12.35		11.77	12.35		Bits
		f_{IN} = 190MHz		11.85			12.12			12.10		Bits
		f_{IN} = 363MHz		11.60			11.62			11.65		Bits
		f_{IN} = 461MHz		11.20			11.10			10.99		Bits
		f_{IN} = 605MHz		10.62			10.49			10.72		Bits

Electrical Specifications

All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T_A = -40°C to +85°C (typical specifications at +25°C), A_{IN} = -2dBFS, f_{SAMPLE} = Maximum Conversion Rate (per speed grade). **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	CONDITIONS	ISLA216P25			ISLA216P20			ISLA216P13			UNITS
			MIN (Note 5)	TYP	MAX (Note 5)	MIN (Note 5)	TYP	MAX (Note 5)	MIN (Note 5)	TYP	MAX (Note 5)	
Spurious-Free Dynamic Range (Note 8)	SFDR	f_{IN} = 30MHz		87			91			96		dBc
		f_{IN} = 105MHz	74	83		74	89		72	83		dBc
		f_{IN} = 190MHz		81			84			83		dBc
		f_{IN} = 363MHz		81			80			82		dBc
		f_{IN} = 461MHz		73			72			70		dBc
		f_{IN} = 605MHz		67			67			67		dBc
Spurious-Free Dynamic Range Excluding H2, H3 (Note 8)	SFDRX23	f_{IN} = 30MHz		89			91			99		dBc
		f_{IN} = 105MHz	80	92		82	93		82	96		dBc
		f_{IN} = 190MHz		88			92			96		dBc
		f_{IN} = 363MHz		83			87			94		dBc
		f_{IN} = 461MHz		82			85			91		dBc
		f_{IN} = 605MHz		79			82			89		dBc
Intermodulation Distortion	IMD	f_{IN} = 70MHz		94			92			88		dBFS
		f_{IN} = 170MHz		87			87			87		dBFS
Word Error Rate	WER			10^{-12}			10^{-12}			10^{-12}		
Full Power Bandwidth	FPBW			700			700			700		MHz

NOTES:

5. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
6. Digital Supply Current is dependent upon the capacitive loading of the digital outputs. I_{OVDD} specifications apply for 10pF load on each digital output.
7. The DLL Range setting must be changed for low-speed operation.
8. Minimum specification guaranteed when calibrated at +85°C.

Digital Specifications

Boldface limits apply over the operating temperature range, -40°C to +85°C.

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
INPUTS						
Input Current High (RESETN)	I_{IH}	V_{IN} = 1.8V	**0**	1	**10**	µA
Input Current Low (RESETN)	I_{IL}	V_{IN} = 0V	**-25**	-12	**-7**	µA
Input Current High (SDIO)	I_{IH}	V_{IN} = 1.8V		4	**12**	µA
Input Current Low (SDIO)	I_{IL}	V_{IN} = 0V	**-600**	-415	**-300**	µA
Input Current High (CSB)	I_{IH}	V_{IN} = 1.8V	**40**	58	**75**	µA
Input Current Low (CSB)	I_{IL}	V_{IN} = 0V		5	**10**	µA
Input Voltage High (SDIO, RESETN)	V_{IH}		**1.17**			V
Input Voltage Low (SDIO, RESETN)	V_{IL}				**0.63**	V
Input Current High (CLKDIV) (Note 9)	I_{IH}		**16**	25	**34**	µA
Input Current Low (CLKDIV)	I_{IL}		**-34**	-25	**-16**	µA
Input Capacitance	C_{DI}			4		pF

Digital Specifications Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
LVDS INPUTS (CLKDIVRSTP,CLKDIVRSTN)						
Input Common Mode Range	V_{ICM}		**825**		**1575**	mV
Input Differential Swing (peak to peak, single-ended)	V_{ID}		**250**		**450**	mV
CLKDIVRSTP Input Pull-down Resistance	R_{Ipd}			100		kΩ
CLKDIVRSTN Input Pull-up Resistance	R_{Ipu}			100		kΩ
LVDS OUTPUTS						
Differential Output Voltage (Note 10)	V_T	3mA Mode		612		mV_{P-P}
Output Offset Voltage	V_{OS}	3mA Mode	**1120**	1150	**1200**	mV
Output Rise Time	t_R			240		ps
Output Fall Time	t_F			240		ps
CMOS OUTPUTS						
Voltage Output High	V_{OH}	I_{OH} = -500µA	**OVDD - 0.3**	OVDD - 0.1		V
Voltage Output Low	V_{OL}	I_{OL} = 1mA		0.1	**0.3**	V
Output Rise Time	t_R			1.8		ns
Output Fall Time	t_F			1.4		ns

NOTES:

9. The Tri-Level Inputs internal switching thresholds are approximately. 0.43V and 1.34V. It is advised to float the inputs, tie to ground or AVDD depending on desired function.
10. The voltage is expressed in peak-to-peak differential swing. The peak-to-peak singled-ended swing is 1/2 of the differential swing.

Timing Diagrams

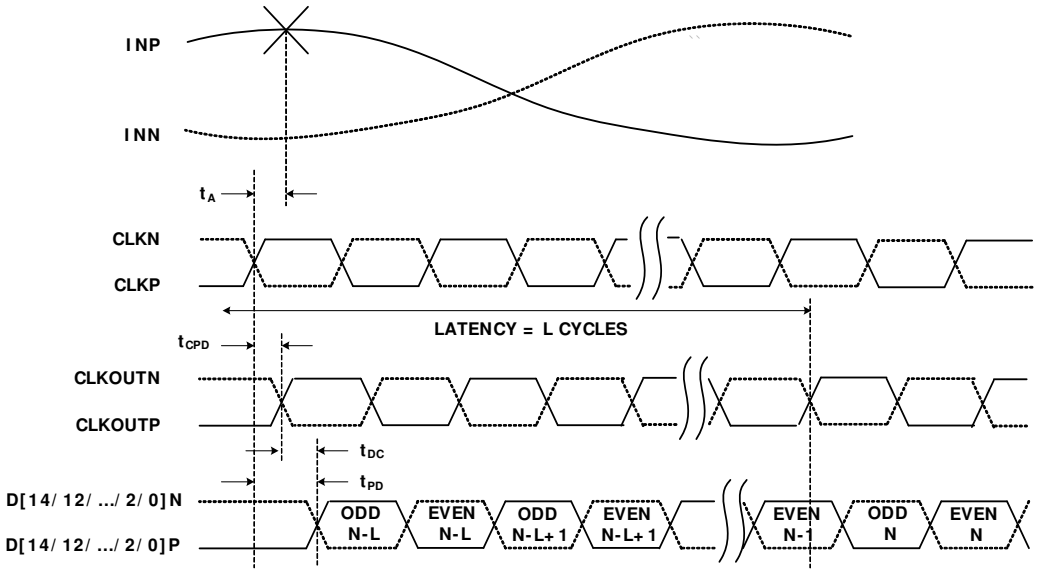


FIGURE 1A. LVDS

Timing Diagrams

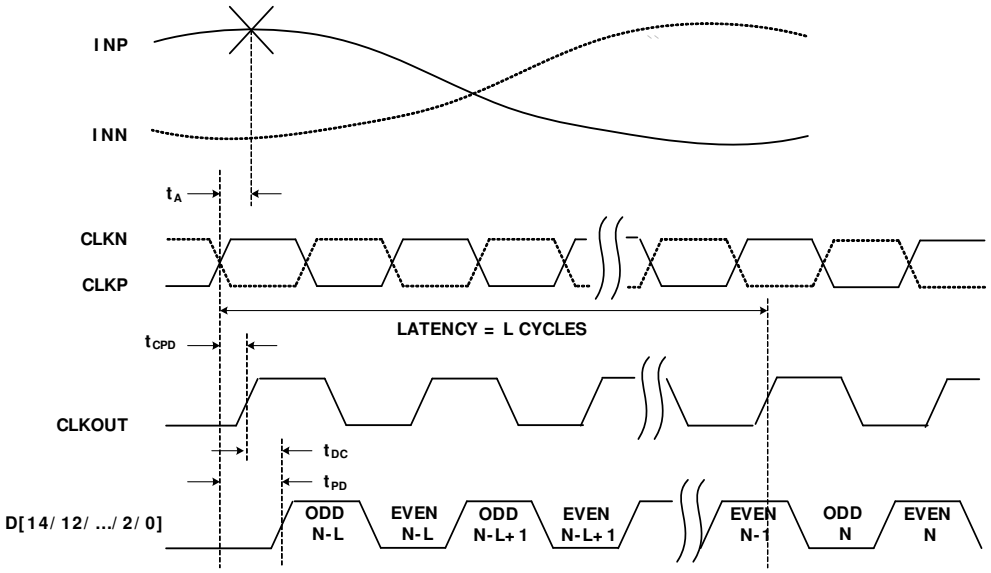


FIGURE 1B. CMOS

FIGURE 1. TIMING DIAGRAMS

Switching Specifications

Boldface limits apply over the operating temperature range, -40°C to +85°C.

PARAMETER	SYMBOL	CONDITION	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
ADC OUTPUT						
Aperture Delay	t_A			114		ps
RMS Aperture Jitter	j_A			75		fs
Input Clock to Output Clock Propagation Delay	t_{CPD}	AVDD, OVDD = 1.7V to 1.9V, T_A = -40°C to +85°C	**1.65**	2.4	**3**	ns
	t_{CPD}	AVDD, OVDD = 1.8V, T_A = +25°C	**1.9**	2.3	**2.75**	ns
Relative Input Clock to Output Clock Propagation Delay (Note 13)	dt_{CPD}	AVDD, OVDD = 1.7V to 1.9V, T_A = -40°C to +85°C	**-450**		**450**	ps
Input Clock to Data Propagation Delay	t_{PD}		**1.65**	2.4	**3.5**	ns
Output Clock to Data Propagation Delay, LVDS Mode	t_{DC}	Rising/Falling Edge	**-0.1**	0.16	**0.5**	ns
Output Clock to Data Propagation Delay, CMOS Mode	t_{DC}	Rising/Falling Edge	**-0.1**	0.2	**0.65**	ns
Synchronous Clock Divider Reset Setup Time (with respect to the positive edge of CLKP)	t_{RSTS}		**0.4**	0.06		ns
Synchronous Clock Divider Reset Hold Time (with respect to the positive edge of CLKP)	t_{RSTH}			0.02	**0.35**	ns
Synchronous Clock Divider Reset Recovery Time	t_{RSTRT}	DLL recovery time after Synchronous Reset		52		µs
Latency (Pipeline Delay)	L			10		cycles

Switching Specifications

Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)

PARAMETER	SYMBOL	CONDITION	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
Overvoltage Recovery	t_{OVR}			1		cycles
SPI INTERFACE (Notes 11, 12)						
SCLK Period	t_{CLK}	Write Operation	**16**			cycles
	t_{CLK}	Read Operation	**16**			cycles
CSB↓ to SCLK↑ Setup Time	t_S	Read or Write	**28**			cycles
CSB↑ after SCLK↑ Hold Time	t_H	Write	**5**			cycles
Data Valid to SCLK↑ Setup Time	t_{DS}	Write	**6**			cycles
Data Valid after SCLK↑ Hold Time	t_{DH}	Read or Write			**4**	cycles
Data Valid after SCLK↓ Time	t_{DVR}	Read			**5**	cycles

NOTES:

11. SPI Interface timing is directly proportional to the ADC sample period (t_S). Values above reflect multiples of a 4ns sample period, and must be scaled proportionally for lower sample rates. ADC sample clock must be running for SPI communication.
12. The SPI may operate asynchronously with respect to the ADC sample clock.
13. The relative propagation delay is the difference in propagation time between any two devices that are matched in temperature and voltage, and is specified over the full operating temperature and voltage range.

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -2dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 250MSPS.

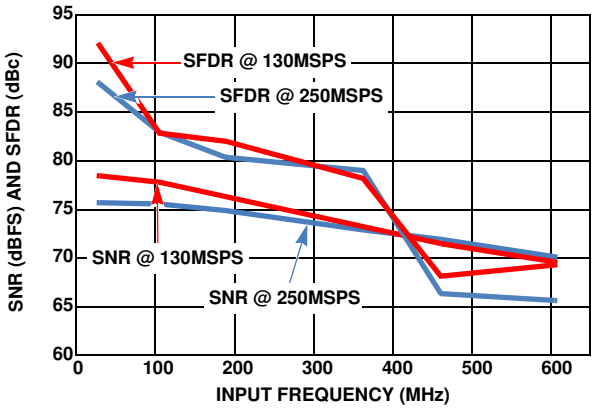


FIGURE 2. SNR AND SFDR vs f_{IN}

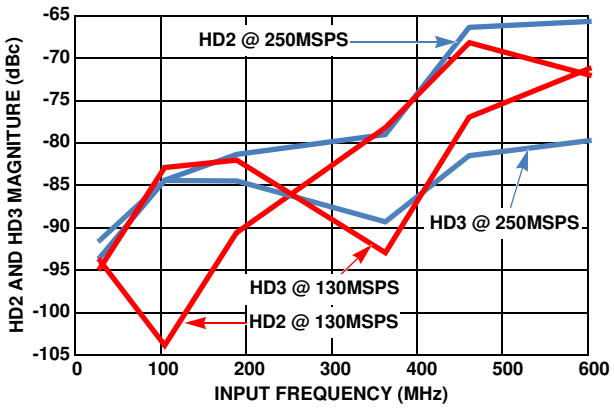


FIGURE 3. HD2 AND HD3 vs f_{IN}

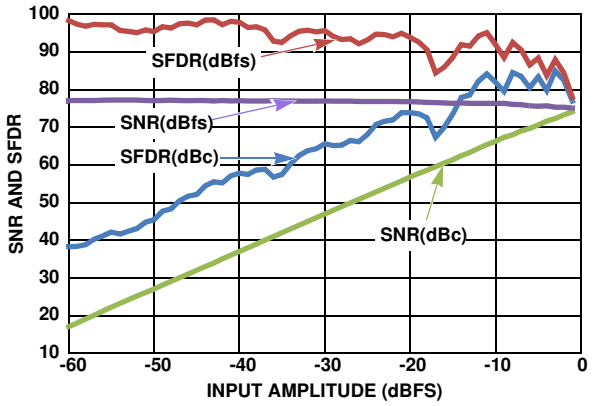


FIGURE 4. SNR AND SFDR vs A_{IN}

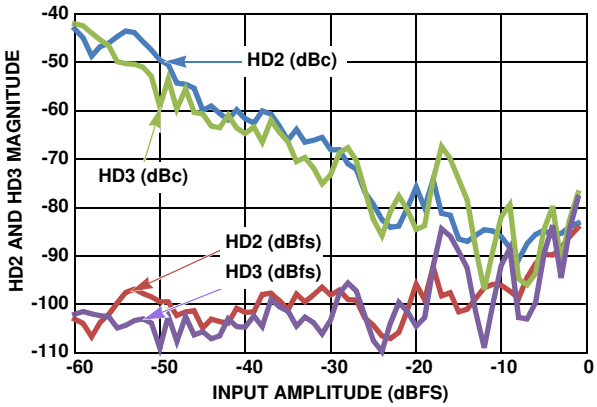


FIGURE 5. HD2 AND HD3 vs A_{IN}

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -2dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 250MSPS. **(Continued)**

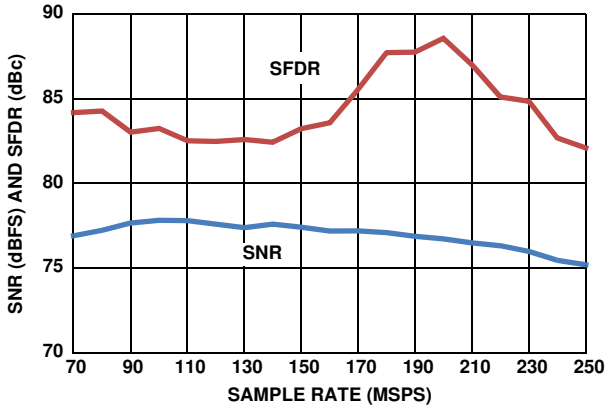


FIGURE 6. SNR AND SFDR vs f_{SAMPLE}

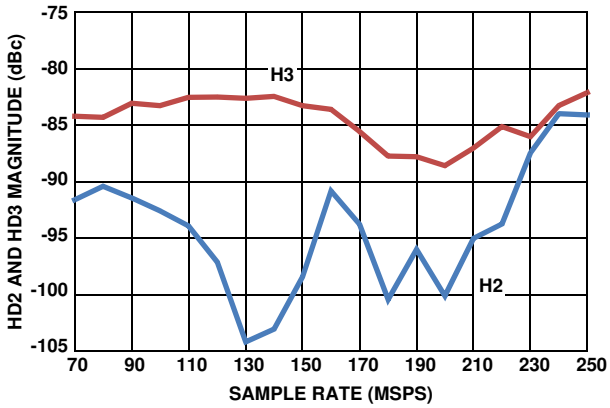


FIGURE 7. HD2 AND HD3 vs f_{SAMPLE}

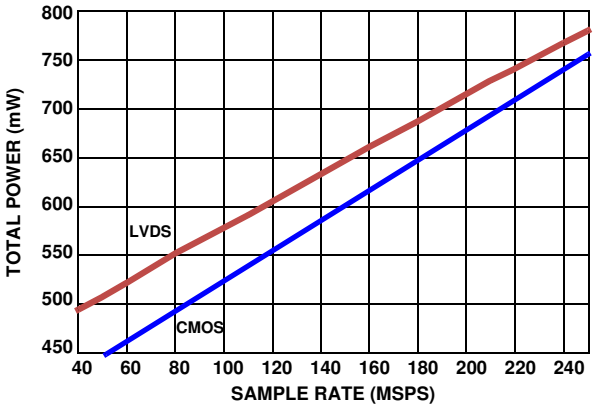


FIGURE 8. POWER vs f_{SAMPLE} IN 3mA LVDS MODE

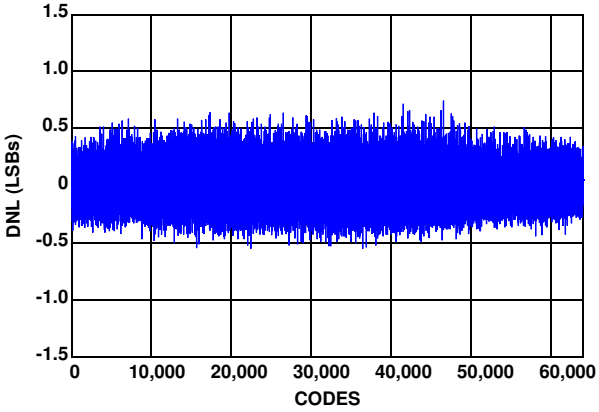


FIGURE 9. DIFFERENTIAL NONLINEARITY

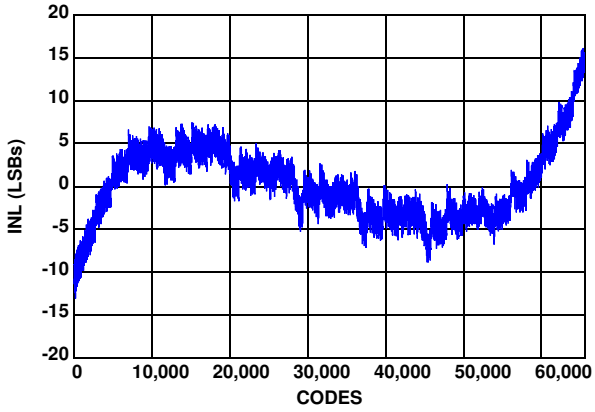


FIGURE 10. INTEGRAL NONLINEARITY

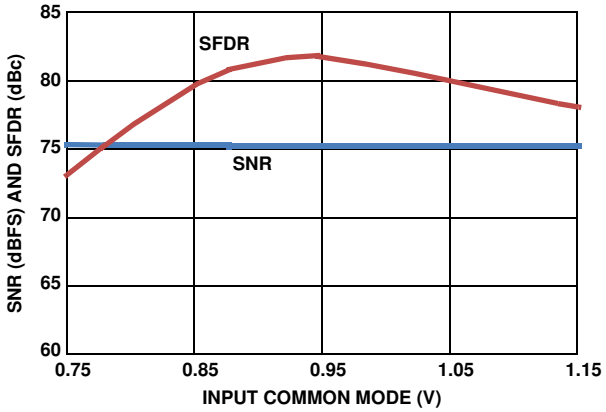


FIGURE 11. SNR AND SFDR vs VCM

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -2dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 250MSPS. **(Continued)**

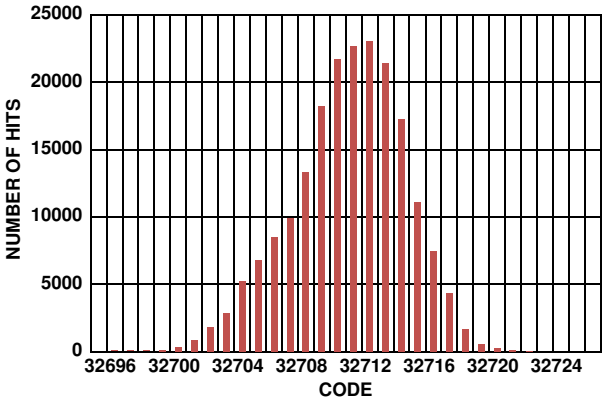


FIGURE 12. NOISE HISTOGRAM

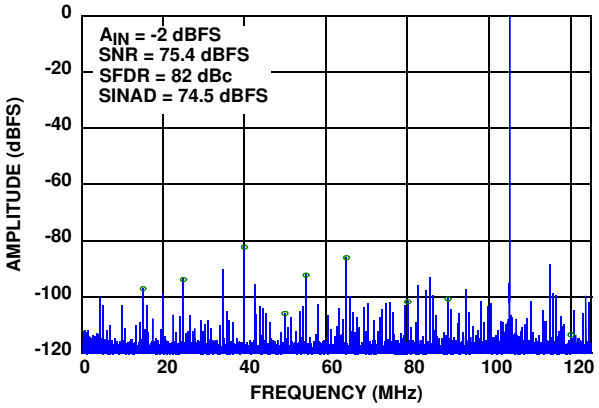


FIGURE 13. SINGLE-TONE SPECTRUM @ 105MHz

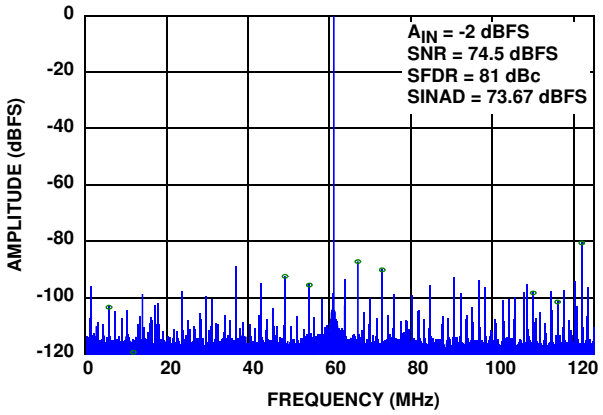


FIGURE 14. SINGLE-TONE SPECTRUM @ 190MHz

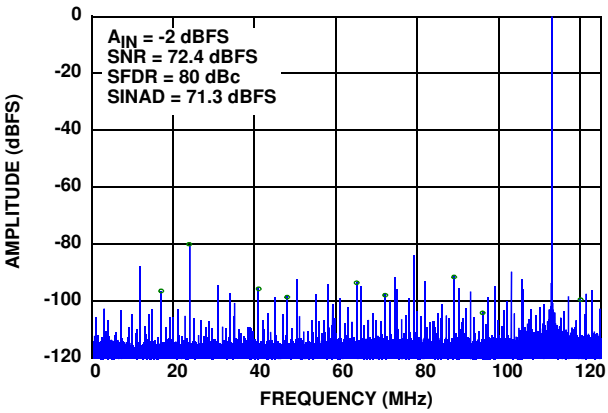


FIGURE 15. SINGLE-TONE SPECTRUM @ 363MHz

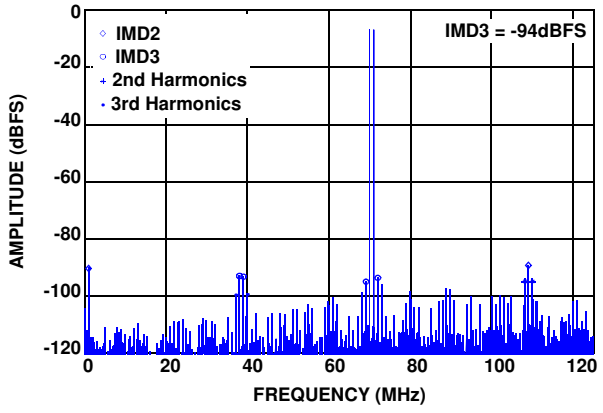


FIGURE 16. TWO-TONE SPECTRUM
(F1 = 70MHz, F2 = 71MHz AT -7dBFS)

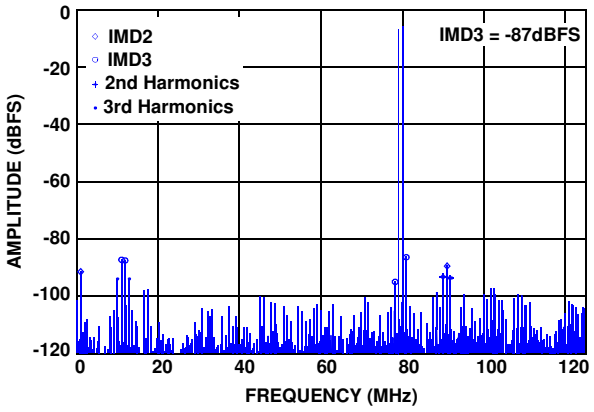


FIGURE 17. TWO-TONE SPECTRUM
(F1 = 170MHz, F2 = 171MHz AT -7dBFS)

Theory of Operation

Functional Description

The ISLA216P is based upon a 16-bit, 250MSPS A/D converter core that utilizes a pipelined successive approximation architecture (Figure 18). The input voltage is captured by a Sample-Hold Amplifier (SHA) and converted to a unit of charge. Proprietary charge-domain techniques are used to successively compare the input to a series of reference charges. Decisions made during the successive approximation operations determine the digital code for each input value. Digital error correction is also applied, resulting in a total latency of 10 clock cycles. This is evident to the user as a latency between the start of a conversion and the data being available on the digital outputs.

The ISLA216P family operates by simultaneously sampling the input signal with two ADC cores in parallel and summing the digital result. Since the input signal is correlated between the two cores and noise is not, an increase in SNR is achieved. As a result, the offset, gain, or operational mode of both cores should be adjusted when a change to the ADC's offset, gain, or operational mode is desired.

Power-On Calibration

As mentioned previously, the cores perform a self-calibration at start-up. An internal power-on-reset (POR) circuit detects the supply voltage ramps and initiates the calibration when the analog and digital supply voltages are above a threshold. The following conditions must be adhered to for the power-on calibration to execute successfully:

- A frequency-stable conversion clock must be applied to the CLKP/CLKN pins
- DNC pins must not be connected
- SDO has an internal pull-up and should not be driven externally
- RESETN is pulled low by the ADC internally during POR. External driving of RESETN is optional.
- SPI communications must not be attempted

A user-initiated reset can subsequently be invoked in the event that the above conditions cannot be met at power-up.

After the power supply has stabilized the internal POR releases RESETN and an internal pull-up pulls it high, which starts the calibration sequence. If a subsequent user-initiated reset is desired, the RESETN pin should be connected to an open-drain driver with an off-state/high impedance state leakage of less than 0.5mA to assure exit from the reset state so calibration can start.

The calibration sequence is initiated on the rising edge of RESETN, as shown in Figure 19. Calibration status can be determined by reading the cal_status bit (LSB) at 0xB6. This bit is '0' during calibration and goes to a logic '1' when calibration is complete. The data outputs produce 0xCCCC during calibration; this can also be used to determine calibration status.

If the selectable clock divider is set to 1 (default), the output clock (CLKOUTP/CLKOUTN) will not be affected by the assertion of RESETN. If the selectable clock divider is set to 2 or 4, the output clock is set low while RESETN is asserted (low). Normal operation of the output clock resumes at the next input clock edge (CLKP/CLKN) after RESETN is de-asserted. At 250MSPS the nominal calibration time is 200ms, while the maximum calibration time is 550ms.

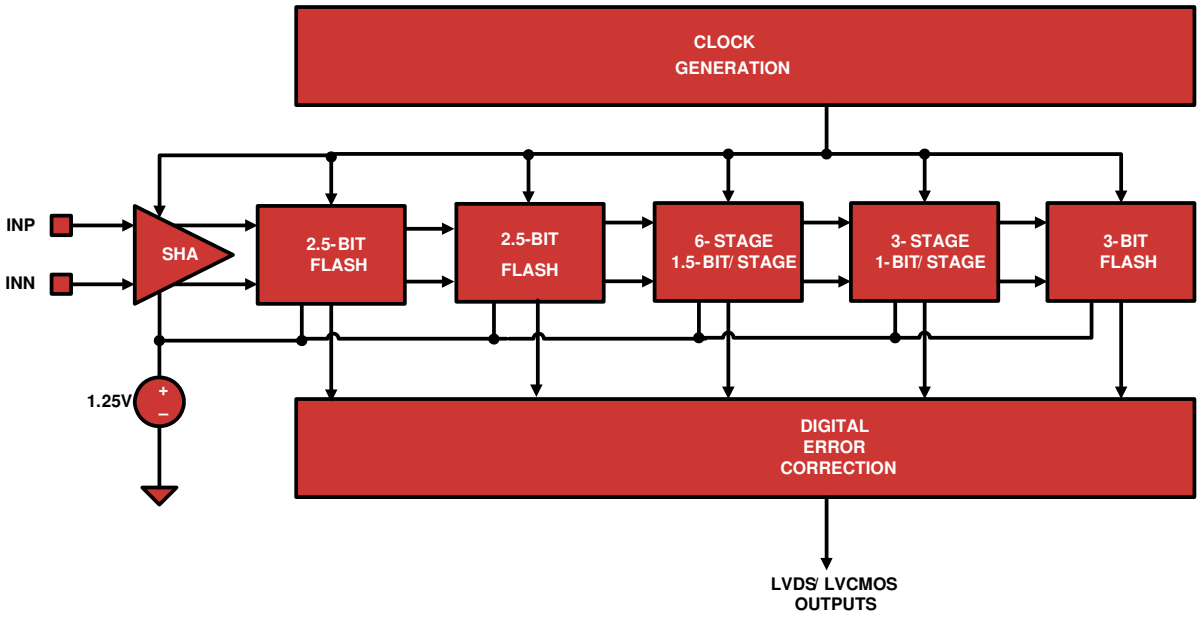


FIGURE 18. A/D CORE BLOCK DIAGRAM

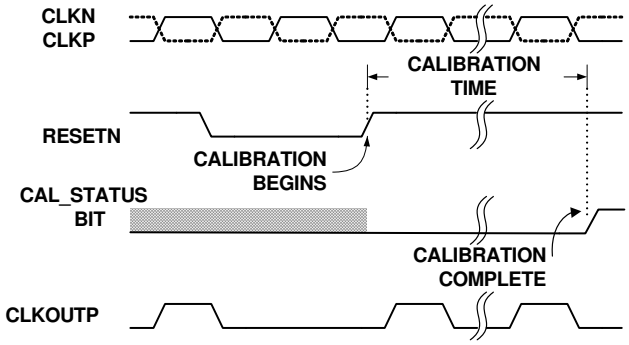


FIGURE 19. CALIBRATION TIMING

User Initiated Reset

Recalibration of the A/D can be initiated at any time by driving the RESETN pin low for a minimum of one clock cycle. An open-drain driver with a drive strength in its high impedance state of less than 0.5mA is recommended, as RESETN has an internal high impedance pull-up to OVDD. As is the case during power-on reset, RESETN and DNC pins must be in the proper state for the calibration to successfully execute.

The performance of the ISLA216P25 changes with variations in temperature, supply voltage or sample rate. The extent of these changes may necessitate recalibration, depending on system performance requirements. Best performance will be achieved by recalibrating the A/D under the environmental conditions at which it will operate.

A supply voltage variation of <100mV will generally result in an SNR change of <0.5dBFS and SFDR change of <3dBc.

In situations where the sample rate is not constant, best results will be obtained if the device is calibrated at the highest sample rate. Reducing the sample rate by less than 80MSPS will typically result in an SNR change of <0.5dBFS and an SFDR change of <3dBc.

Figures 20 through 25 show the effect of temperature on SNR and SFDR performance with power on calibration performed at -40°C, +25°C, and +85°C. Each plot shows the variation of SNR/SFDR across temperature after a single power on calibration at -40°C, +25°C and +85°C. Best performance is typically achieved by a user-initiated power on calibration at the operating conditions, as stated earlier. However, it can be seen that performance drift with temperature is not a very strong function of the temperature at which the power on calibration is performed; also note that SFDR performance typically improves as the analog input level moves away from full-scale as Figure 4 shows.

Temperature Calibration

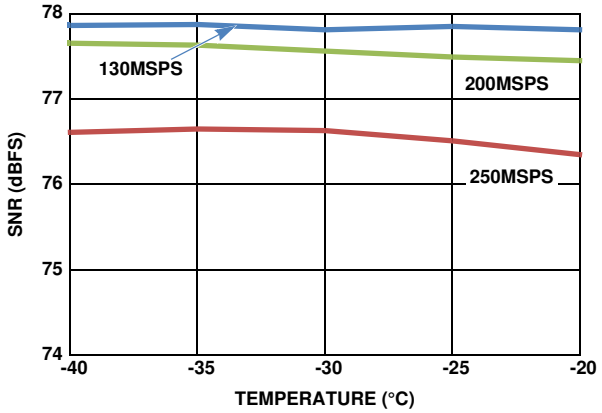


FIGURE 20. TYPICAL SNR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT -40°C, f_{IN} = 105MHz, -2dBFS

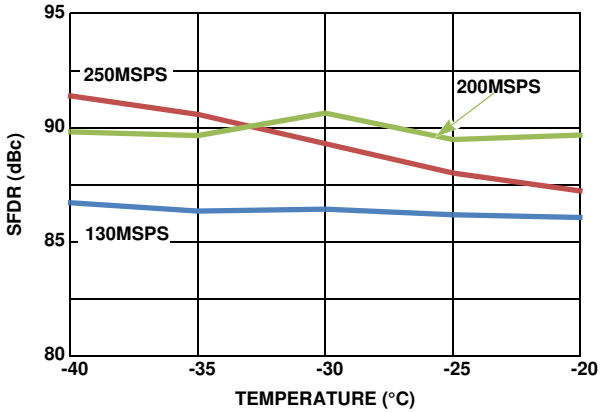


FIGURE 21. TYPICAL SFDR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT -40°C, f_{IN} = 105MHz, -2dBFS

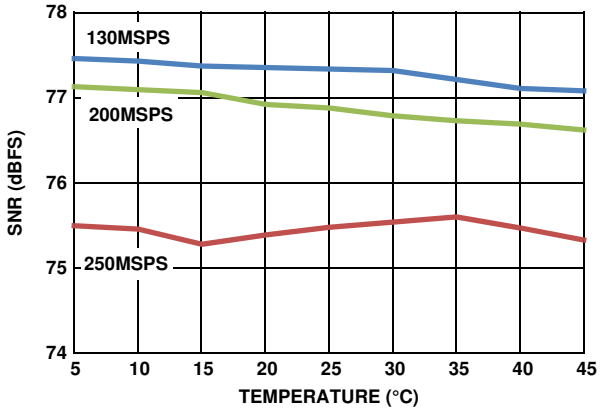


FIGURE 22. TYPICAL SNR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +25°C, f_{IN} = 105MHz, -2dBFS

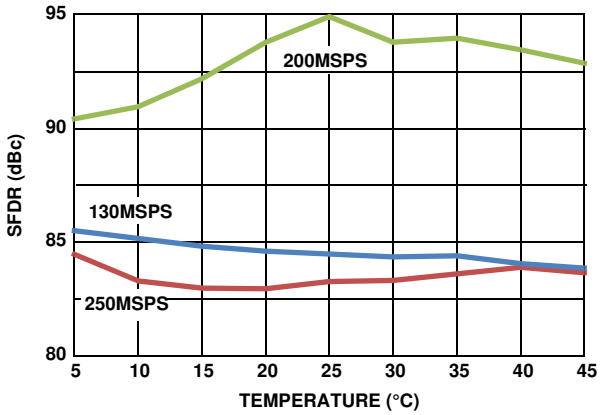


FIGURE 23. TYPICAL SFDR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +25°C, f_{IN} = 105MHz, -2dBFS

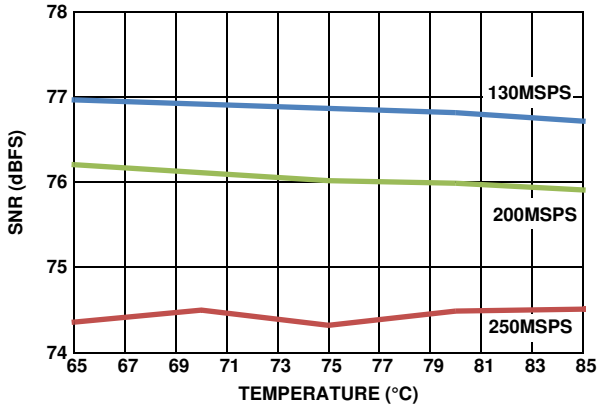


FIGURE 24. TYPICAL SNR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +85°C, f_{IN} = 105MHz, -2dBF

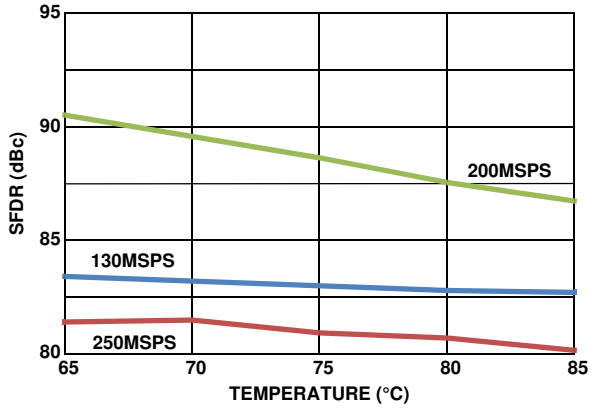


FIGURE 25. TYPICAL SFDR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +85°C, f_{IN} = 105MHz, -2dBFS

Analog Input

A single fully differential input (VINP/VINN) connects to the sample and hold amplifier (SHA) of each unit A/D. The ideal full-scale input voltage is 2.0V, centered at the VCM voltage of

0.94V as shown in Figure 26.

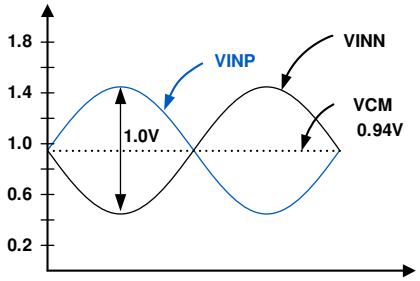


FIGURE 26. ANALOG INPUT RANGE

Best performance is obtained when the analog inputs are driven differentially. The common-mode output voltage, VCM, should be used to properly bias the inputs as shown in Figures 27 through 29. An RF transformer will give the best noise and distortion performance for wideband and/or high intermediate frequency (IF) inputs. Two different transformer input schemes are shown in Figures 27 and 28.

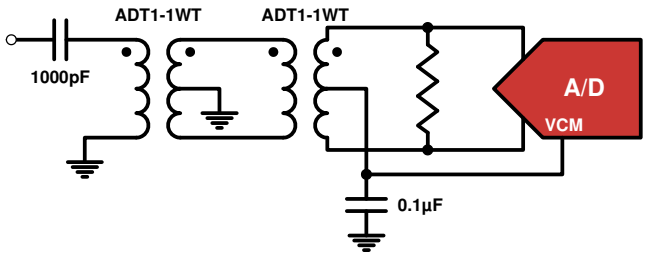


FIGURE 27. TRANSFORMER INPUT FOR GENERAL PURPOSE APPLICATIONS

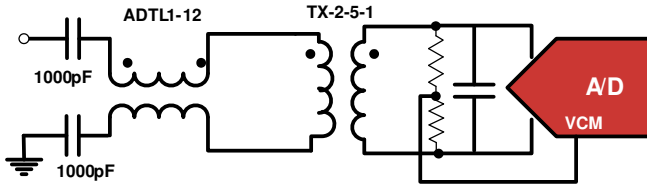


FIGURE 28. TRANSMISSION-LINE TRANSFORMER INPUT FOR HIGH IF APPLICATIONS

This dual transformer scheme is used to improve common-mode rejection, which keeps the common-mode level of the input matched to VCM. The value of the shunt resistor should be determined based on the desired load impedance. The differential input resistance of the ISLA216P25 is 300Ω.

The SHA design uses a switched capacitor input stage (see Figure 42), which creates current spikes when the sampling capacitance is reconnected to the input voltage. This causes a disturbance at the input which must settle before the next sampling point. Lower source impedance will result in faster settling and improved performance. Therefore a 2:1 or 1:1 transformer and low shunt resistance are recommended for optimal performance.

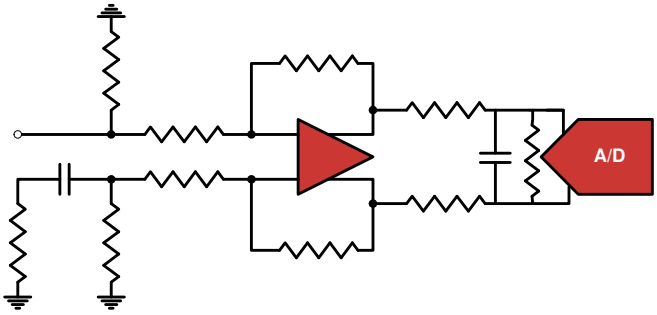


FIGURE 29. DIFFERENTIAL AMPLIFIER INPUT

A differential amplifier, as shown in the simplified block diagram in Figure 29, can be used in applications that require DC-coupling. In this configuration, the amplifier will typically dominate the achievable SNR and distortion performance. Intersil's new ISL552xx differential amplifier family can also be used in certain AC applications with minimal performance degradation. Contact the factory for more information.

Clock Input

The clock input circuit is a differential pair (see Figure 43). Driving these inputs with a high level (up to $1.8V_{P-P}$ on each input) sine or square wave will provide the lowest jitter performance. A transformer with 4:1 impedance ratio will provide increased drive levels. The clock input is functional with AC-coupled LVDS, LVPECL, and CML drive levels. To maintain the lowest possible aperture jitter, it is recommended to have high slew rate at the zero crossing of the differential clock input signal.

The recommended drive circuit is shown in Figure 30. A duty range of 40% to 60% is acceptable. The clock can be driven single-ended, but this will reduce the edge rate and may impact SNR performance. The clock inputs are internally self-biased to AVDD/2 to facilitate AC coupling.

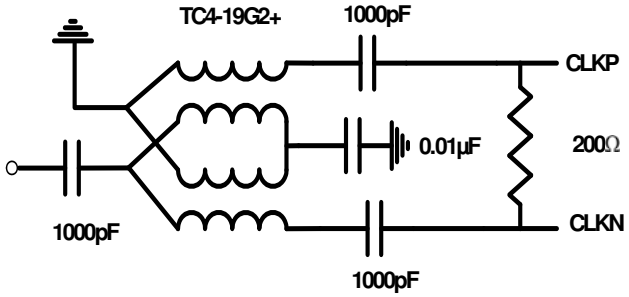


FIGURE 30. RECOMMENDED CLOCK DRIVE

A selectable 2x or 4x frequency divider is provided in series with the clock input. The divider can be used in the 2x mode with a sample clock equal to twice the desired sample rate or in 4x mode with a sample clock equal to four times the desired sample rate. This allows the use of the Phase Slip feature, which enables synchronization of multiple ADCs. The Phase Slip feature can be used as an alternative to using the CLKDIVRST pins to synchronize ADCs in a multiple ADC system.

TABLE 1. CLKDIV PIN SETTINGS

CLKDIV PIN	DIVIDE RATIO
AVSS	2
Float	1
AVDD	4

The clock divider can also be controlled through the SPI port, which overrides the CLKDIV pin setting. See "SPI Physical Interface" on page 24. A delay-locked loop (DLL) generates internal clock signals for various stages within the charge pipeline. If the frequency of the input clock changes, the DLL may take up to 52µs to regain lock at 250MSPS. The lock time is inversely proportional to the sample rate.

The DLL has two ranges of operation, slow and fast. The slow range can be used for sample rates between 40MSPS and 100MSPS, while the default fast range can be used from 80MSPS to the maximum specified sample rate.

Jitter

In a sampled data system, clock jitter directly impacts the achievable SNR performance. The theoretical relationship between clock jitter (t_J) and SNR is shown in Equation 1 and is illustrated in Figure 31.

$$SNR = 20 \log_{10}\left(\frac{1}{2\pi f_{IN} t_J}\right) \quad \text{(EQ. 1)}$$

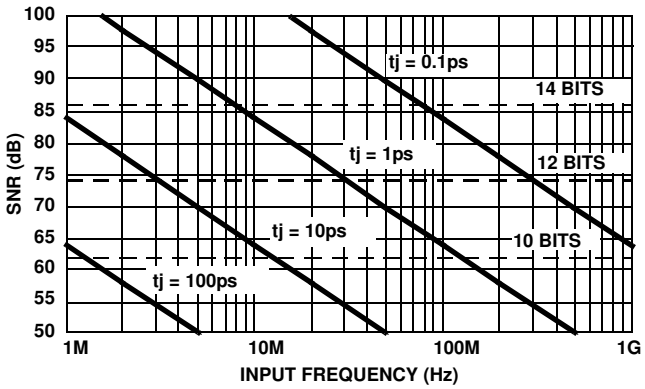


FIGURE 31. SNR vs CLOCK JITTER

This relationship shows the SNR that would be achieved if clock jitter were the only non-ideal factor. In reality, achievable SNR is limited by internal factors such as linearity, aperture jitter and thermal noise. Internal aperture jitter is the uncertainty in the sampling instant shown in Figure1A. The internal aperture jitter combines with the input clock jitter in a root-sum-square fashion, since they are not statistically correlated, and this determines the total jitter in the system. The total jitter, combined with other noise sources, then determines the achievable SNR.

Voltage Reference

A temperature compensated internal voltage reference provides the reference charges used in the successive approximation operations. The full-scale range of each A/D is proportional to the reference voltage. The nominal value of the voltage reference is 1.25V.

Digital Outputs

Output data is available as a parallel bus in LVDS-compatible (default) or CMOS modes. In either case, the data is presented in double data rate (DDR) format. Figures 1A and 1B show the timing relationships for LVDS and CMOS modes, respectively.

Additionally, the drive current for LVDS mode can be set to a nominal 3mA(default) or a power-saving 2mA. The lower current setting can be used in designs where the receiver is in close physical proximity to the A/D. The applicability of this setting is dependent upon the PCB layout, therefore the user should experiment to determine if performance degradation is observed.

The output mode can be controlled through the SPI port, by writing to address 0x73, see “Serial Peripheral Interface” on page 24.

An external resistor creates the bias for the LVDS drivers. A 10kΩ, 1% resistor must be connected from the RLVDS pin to OVSS.

Power Dissipation

The power dissipated by the ISLA216P25 is primarily dependent on the sample rate and the output modes: LVDS vs CMOS and DDR vs SDR. There is a static bias in the analog supply, while the remaining power dissipation is linearly related to the sample rate. The output supply dissipation changes to a lesser degree in LVDS mode, but is more strongly related to the clock frequency in CMOS mode.

Nap/Sleep

Portions of the device may be shut down to save power during times when operation of the A/D is not required. Two power saving modes are available: Nap, and Sleep. Nap mode reduces power dissipation to <103mW while Sleep mode reduces power dissipation to <19mW.

All digital outputs (Data, CLKOUT and OR) are placed in a high impedance state during Nap or Sleep. The input clock should remain running and at a fixed frequency during Nap or Sleep, and CSB should be high. Recovery time from Nap mode will increase if the clock is stopped, since the internal DLL can take up to 52µs to regain lock at 250MSPS.

By default after the device is powered on, the operational state is controlled by the NAPSLP pin as shown in Table 2.

TABLE 2. NAPSLP PIN SETTINGS

NAPSLP PIN	MODE
AVSS	Normal
Float	Sleep
AVDD	Nap

The power-down mode can also be controlled through the SPI port, which overrides the NAPSLP pin setting. Details on this are contained in “Serial Peripheral Interface” on page 24.

Data Format

Output data can be presented in three formats: two’s complement (default), Gray code and offset binary. The data format can also be controlled through the SPI port, by writing to address 0x73. Details on this are contained in “Serial Peripheral Interface” on page 24.

Offset binary coding maps the most negative input voltage to code 0x000 (all zeros) and the most positive input to 0xFFF (all ones). Two’s complement coding simply complements the MSB of the offset binary representation.

When calculating Gray code the MSB is unchanged. The remaining bits are computed as the XOR of the current bit position and the next most significant bit. Figure 32 shows this operation.

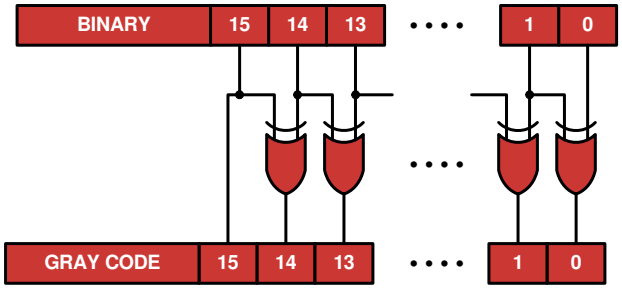


FIGURE 32. BINARY TO GRAY CODE CONVERSION

Converting back to offset binary from Gray code must be done recursively, using the result of each bit for the next lower bit as shown in Figure 33.

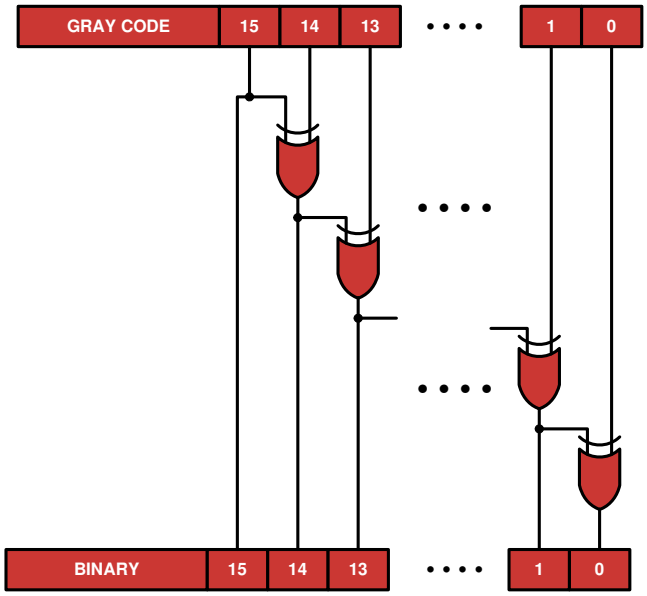


FIGURE 33. GRAY CODE TO BINARY CONVERSION

Mapping of the input voltage to the various data formats is shown in Table 3.

TABLE 3. INPUT VOLTAGE TO OUTPUT CODE MAPPING

INPUT VOLTAGE	OFFSET BINARY	TWO'S COMPLEMENT	GRAY CODE
–Full Scale	0000 0000 0000 0000	1000 0000 0000 0000	0000 0000 0000 0000
–Full Scale + 1LSB	0000 0000 0000 0001	1000 0000 0000 0001	0000 0000 0000 0001
Mid–Scale	1000 0000 0000 0000	0000 0000 0000 0000	1100 0000 0000 0000
+Full Scale – 1LSB	1111 1111 1111 1110	0111 1111 1111 1110	1000 0000 0000 0001
+Full Scale	1111 1111 1111 1111	0111 1111 1111 1111	1000 0000 0000 0000

Clock Divider Synchronous Reset

If the selectable clock divider is used, the ADC's internal sample clock will be at half the frequency (DIV=2) or one quarter the frequency (DIV=4) of the device clock. The phase relationship between the sample clock and the device clock is initially indeterminate. An output clock (CLKOUTP, CLKOUTN) is provided to facilitate latching of the sampled data and estimation of the internal sample clock's phase. The output clock has a fixed phase relationship to the sample clock. When the selectable clock divider is set to 2 or 4, the output clock's phase relationship to the sample clock remains fixed but is initially indeterminate with respect to the device clock. When the selectable clock divider is set to 2 or 4, the synchronous clock divider reset feature allows the phase of the internal sample clock and the output clock to be synchronized (refer to Figure 34) with respect to the device clock. This simplifies data capture in systems employing multiple A/Ds where sampling of the inputs is desired to be synchronous.

The reset signal must be well-timed with respect to the sample clock (See “Switching Specifications” on page 11).

A 100Ω differential termination resistor must be supplied between CLKDIVRSTP and CLKDIVRSTN, external to the ADC, (on the PCB) and should be located as close to the CLKDIVRSTP/N pins as possible.

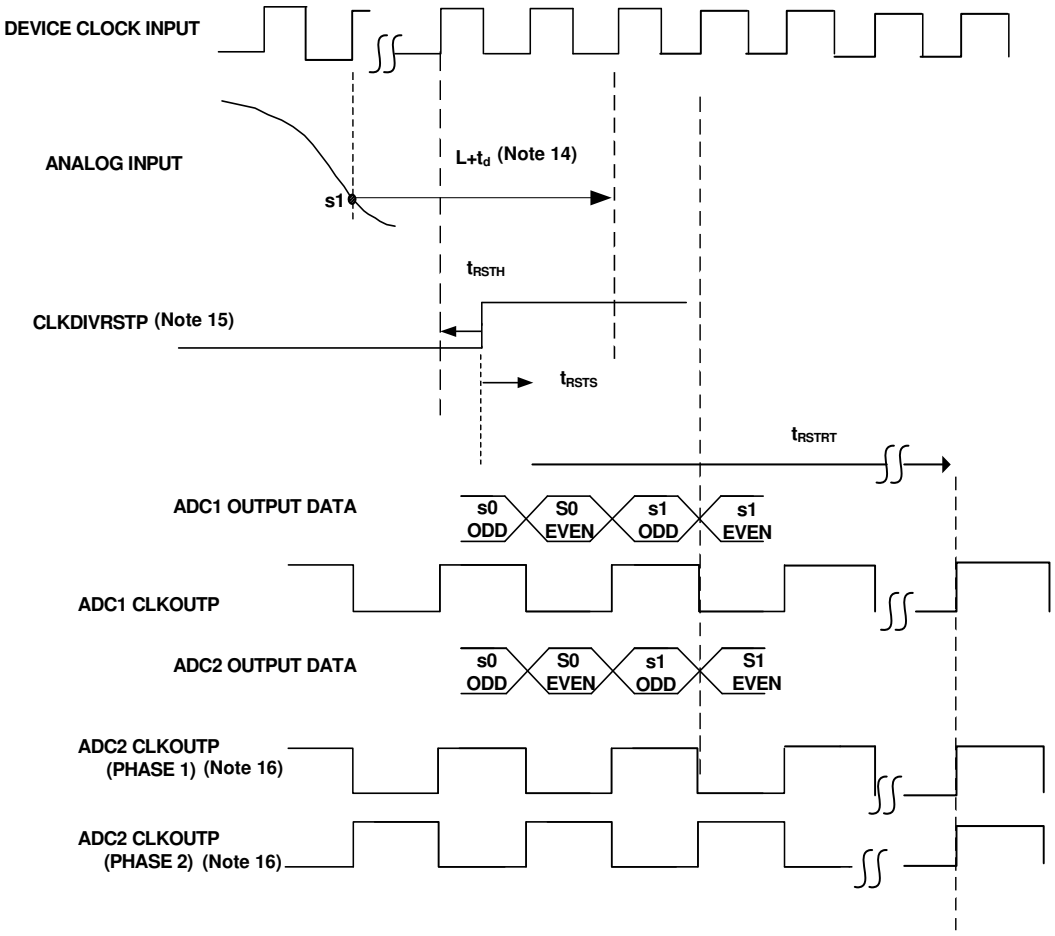


FIGURE 34. SYNCHRONOUS RESET OPERATION, CLOCK DIVIDE = 2

NOTES:

14. Delay equals fixed pipeline latency (L cycles of sample clock) plus fixed analog propagation delay, td.
15. CLKDIVRSTP setup and hold times are with respect to input sample clock rising edge.CLKDIVRSTN is not shown, but must be driven, and is the compliment of CLKDIVRSTP.
16. Either Output Clock Phase (phase 1 or phase 2) equally likely prior to synchronization.

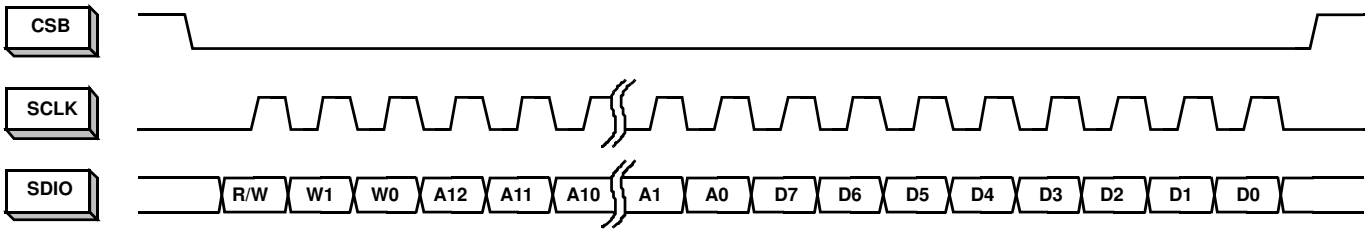


FIGURE 35. MSB-FIRST ADDRESSING

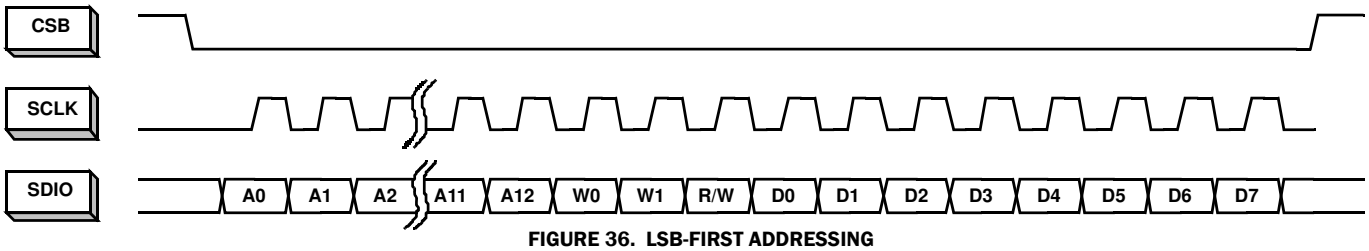
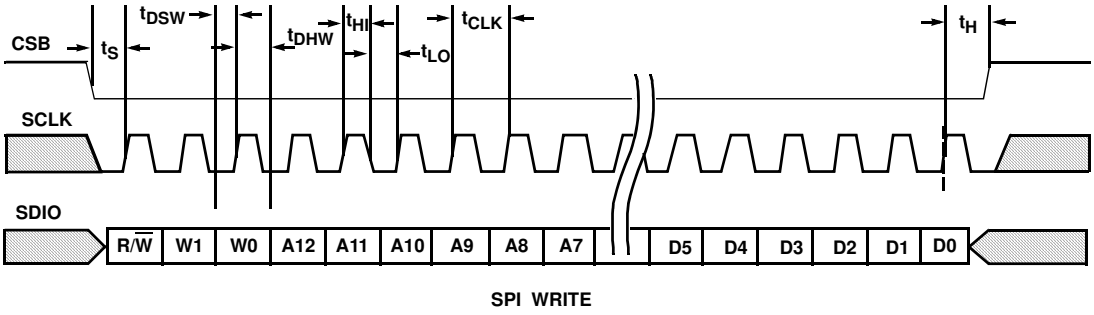
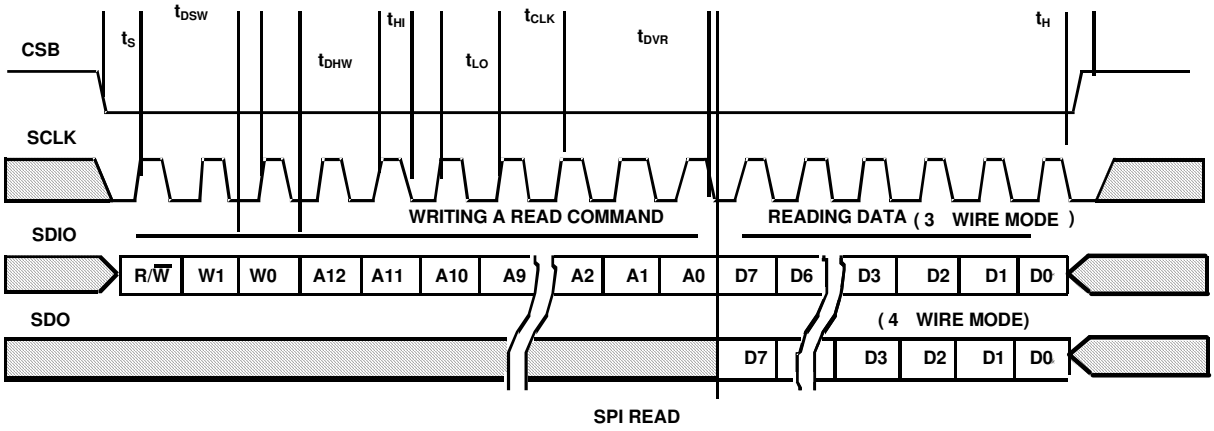


FIGURE 36. LSB-FIRST ADDRESSING



SPI WRITE

FIGURE 37. SPI WRITE



SPI READ

FIGURE 38. SPI READ

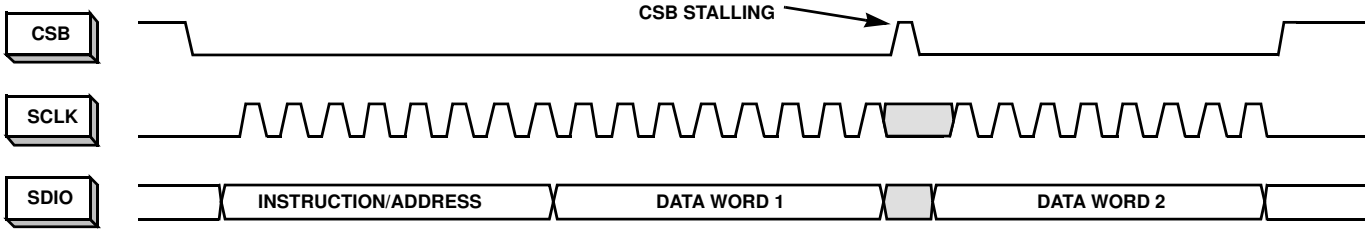


FIGURE 39. 2-BYTE TRANSFER

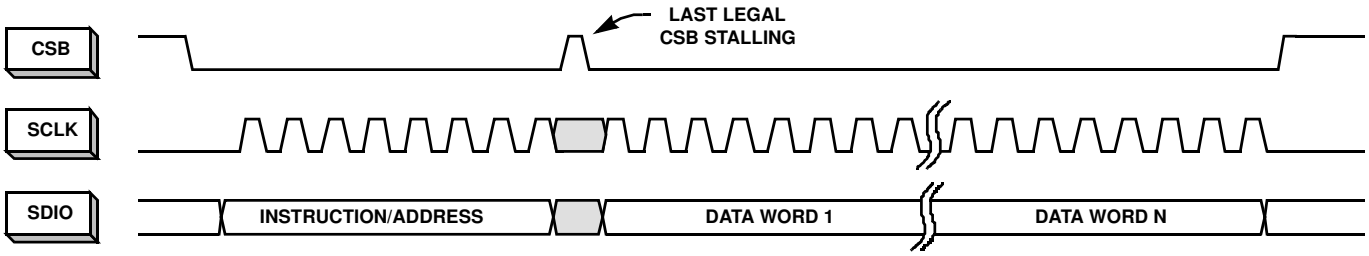


FIGURE 40. N-BYTE TRANSFER

Serial Peripheral Interface

A serial peripheral interface (SPI) bus is used to facilitate configuration of the device and to optimize performance. The SPI bus consists of chip select (CSB), serial clock (SCLK) serial data output (SDO), and serial data input/output (SDIO). The maximum SCLK rate is equal to the A/D sample rate (f_{SAMPLE}) divided by 16 for both write operations and read operations. At f_{SAMPLE} = 250MHz, maximum SCLK is 15.63MHz for writing and read operations. There is no minimum SCLK rate.

The following sections describe various registers that are used to configure the SPI or adjust performance or functional parameters. Many registers in the available address space (0x00 to 0xFF) are not defined in this document. Additionally, within a defined register there may be certain bits or bit combinations that are reserved. Undefined registers and undefined values within defined registers are reserved and should not be selected. Setting any reserved register or value may produce indeterminate results.

SPI Physical Interface

The serial clock pin (SCLK) provides synchronization for the data transfer. By default, all data is presented on the serial data input/output (SDIO) pin in three-wire mode. The state of the SDIO pin is set automatically in the communication protocol (described in the following). A dedicated serial data output pin (SDO) can be activated by setting 0x00[7] high to allow operation in four-wire mode.

The SPI port operates in a half duplex master/slave configuration, with the ISLA216P25 functioning as a slave. Multiple slave devices can interface to a single master in three-wire mode only, since the SDO output of an unaddressed device is asserted in four wire mode.

The chip-select bar (CSB) pin determines when a slave device is being addressed. Multiple slave devices can be written to concurrently, but only one slave device can be read from at a given time (again, only in three-wire mode). If multiple slave devices are selected for reading at the same time, the results will be indeterminate.

The communication protocol begins with an instruction/address phase. The first rising SCLK edge following a high-to-low transition on CSB determines the beginning of the two-byte instruction/address command; SCLK must be static low before the CSB transition. Data can be presented in MSB-first order or LSB-first order. The default is MSB-first, but this can be changed by setting 0x00[6] high. Figures 35 and 36 show the appropriate bit ordering for the MSB-first and LSB-first modes, respectively. In MSB-first mode, the address is incremented for multi-byte transfers, while in LSB-first mode it's decremented.

In the default mode, the MSB is R/W, which determines if the data is to be read (active high) or written. The next two bits, W1 and W0, determine the number of data bytes to be read or written (see Table 4). The lower 13 bits contain the first address for the data transfer. This relationship is illustrated in Figure 37, and timing values are given in "Switching Specifications Boldface limits apply over the operating temperature range, -40°C to +85°C." on page 11.

After the instruction/address bytes have been read, the appropriate number of data bytes are written to or read from the A/D (based on the R/W bit status). The data transfer will continue as long as CSB remains low and SCLK is active. Stalling of the CSB pin is allowed at any byte boundary (instruction/address or data) if the number of bytes being transferred is three or less. For transfers of four bytes or more, CSB is allowed to stall in the middle of the instruction/address bytes or before the first data byte. If CSB transitions to a high state after that point the state machine will reset and terminate the data transfer.

TABLE 4. BYTE TRANSFER SELECTION

[W1:W0]	BYTES TRANSFERRED
00	1
01	2
10	3
11	4 or more

Figures 39 and 40 illustrate the timing relationships for 2-byte and N-byte transfers, respectively. The operation for a 3-byte transfer can be inferred from these diagrams.

SPI Configuration

ADDRESS 0X00: CHIP_PORT_CONFIG

Bit ordering and SPI reset are controlled by this register. Bit order can be selected as MSB to LSB (MSB first) or LSB to MSB (LSB first) to accommodate various micro controllers.

Bit 7 SDO Active

Bit 6 LSB First

Setting this bit high configures the SPI to interpret serial data as arriving in LSB to MSB order.

Bit 5 Soft Reset

Setting this bit high resets all SPI registers to default values.

Bit 4 Reserved

This bit should always be set high.

Bits 3:0 These bits should always mirror bits 4:7 to avoid ambiguity in bit ordering.

ADDRESS 0X02: BURST_END

If a series of sequential registers are to be set, burst mode can improve throughput by eliminating redundant addressing. The burst is ended by pulling the CSB pin high. Setting the burst_end address determines the end of the transfer. During a write operation, the user must be cautious to transmit the correct number of bytes based on the starting and ending addresses.

Bits 7:0 Burst End Address

This register value determines the ending address of the burst data.

Device Information

ADDRESS 0X08: CHIP_ID

ADDRESS 0X09: CHIP_VERSION

The generic die identifier and a revision number, respectively, can be read from these two registers.

Device Configuration/Control

A common SPI map, which can accommodate single-channel or multi-channel devices, is used for all Intersil A/D products.

ADDRESS 0X20: OFFSET_COARSE_ADC0

ADDRESS 0X21: OFFSET_FINE_ADC0

The input offset of the A/D core can be adjusted in fine and coarse steps. Both adjustments are made via an 8-bit word as detailed in Table 5. The data format is twos complement.

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register. Bit 0 in register 0xFE must be set high to enable updates written to 0x20 and 0x21 to be used by the ADC (see description for 0xFE).

TABLE 5. OFFSET ADJUSTMENTS

PARAMETER	0x20[7:0] COARSE OFFSET	0x21[7:0] FINE OFFSET
Steps	255	255
–Full Scale (0x00)	-133LSB (-47mV)	-5LSB (-1.75mV)
Mid–Scale (0x80)	0.0LSB (0.0mV)	0.0LSB
+Full Scale (0xFF)	+133LSB (+47mV)	+5LSB (+1.75mV)
Nominal Step Size	1.04LSB (0.37mV)	0.04LSB (0.014mV)

ADDRESS 0X22: GAIN_COARSE_ADC0

ADDRESS 0X23: GAIN_MEDIUM_ADC0

ADDRESS 0X24: GAIN_FINE_ADC0

Gain of the A/D core can be adjusted in coarse, medium and fine steps. Coarse gain is a 4-bit adjustment while medium and fine are 8-bit. Multiple Coarse Gain Bits can be set for a total adjustment range of ±4.2%. (‘0011’ ≅ -4.2% and ‘1100’ ≅ +4.2%) It is recommended to use one of the coarse gain settings (-4.2%, -2.8%, -1.4%, 0, 1.4%, 2.8%, 4.2%) and fine-tune the gain using the registers at 0x0023 and 0x24.

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register. Bit 0 in register 0xFE must be set high to enable updates written to 0x23 and 0x24 to be used by the ADC (see description for 0xFE).

TABLE 6. COARSE GAIN ADJUSTMENT

0x22[3:0] core 0 0x26[3:0] core 1	NOMINAL COARSE GAIN ADJUST (%)
Bit3	+2.8
Bit2	+1.4
Bit1	-2.8
Bit0	-1.4

TABLE 7. MEDIUM AND FINE GAIN ADJUSTMENTS

PARAMETER	0x23[7:0] MEDIUM GAIN	0x24[7:0] FINE GAIN
Steps	256	256
–Full Scale (0x00)	-2%	-0.20%
Mid–Scale (0x80)	0.00%	0.00%
+Full Scale (0xFF)	+2%	+0.2%
Nominal Step Size	0.016%	0.0016%

ADDRESS 0X25: MODES

Two distinct reduced power modes can be selected. By default, the tri-level NAPSLP pin can select normal operation, nap or sleep modes (refer to“Nap/Sleep” on page 20). This functionality can be overridden and controlled through the SPI. This is an indexed function when controlled from the SPI, but a global function when driven from the pin. This register is not changed by a Soft Reset.

TABLE 8. POWER-DOWN CONTROL

VALUE	0x25[2:0] POWER DOWN MODE
000	Pin Control
001	Normal Operation
010	Nap Mode
100	Sleep Mode