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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

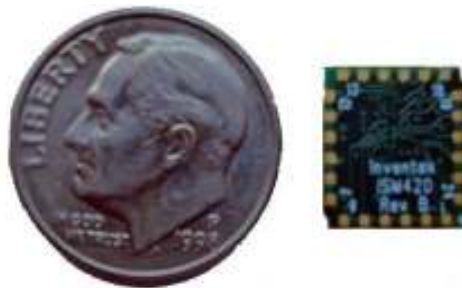




# **Inventek Systems**

## **User Manuel OEM GPS Module Interposer**

**Part No. ISM420-INT – Rev A**



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## 1 GENERAL DESCRIPTION

This specification is a description of the Interposer board for the ISM420 SiRF IV ROM based GPS module. This board was designed specifically for a simple and low cost method to evaluate the RF performance of the ISM420 and become familiar with the various interfaces and how to control the GPS module.

For detailed specifications on the ISM420 please see the functional specification on the [www.inventeksys.com](http://www.inventeksys.com)

The [Inventek](#) ISM420 is a 48 channel global positioning system (GPS) receiver in a very compact Surface Mount Device (SMD) GPS module with high sensitivity, high gain, and low power. The small form factor GP receiver is designed for a broad spectrum of OEM applications and is based on the fast and deep GPS signal search capabilities of CSR , SiRFstarIV™ architecture.

Several key features about this interposer are:

- ✚ 20 pin DIP socket – 100 mil on center
- ✚ 1.8 Volts
- ✚ Ipex or Hiroshi U.FL connector for an external antenna.
- ✚ No external EE on board
- ✚ Setup to be defaulted in NMEA-0182, 4800 baud, 1, N

## 2 PART NUMBER DETAIL DESCRIPTION

### Ordering Information

Device	Description	Ordering Number
ISM420INT	Interposer Board, DIP, UART, ISM420	ISM420R-INT

### **3 GENERAL FEATURES**

- Based on the high performance features of the SiRFstar IV, GSD4e ROM processor.
- High sensitivity navigation engine (PVT) tracks as low as -163dBm
- 48 track verification channels
- NMEA-0183, or OSP SiRF binary output
- Integrated LNA, SAW Filter, TCXO and RTC
- Inputs (only) +3.3 V tolerant
- Single power supply voltage 1.8V.
- Lead Free Design which is compliant with ROHS requirements
- 50 Ohm antenna input

#### 3.1 Flexible Power Control

For embedded applications that will be using NMEA OR SiRF protocol, it is possible to control the state of ISM420 by simply toggling the ON/OFF pin (4). This permits the user to save considerable battery energy by keeping the module in the lowest possible energy state where it consumes less than 10uA. When a satellite fix is required simply toggling the ON/OFF pin (4) puts the module back into full power. If the last fix was less than 2 hours ago, the ISM420 will do a hot fix and be able to get a fix in one second in open sky environment. Then the users circuit can toggle the ON/OFF pin (4) again to put the module into the hibernate state. No external battery backup circuits required. An application requiring location information every minute will save over 98% on the power consumption depending upon frequency of updates. For portable applications, such as in a laptop, that do not have easy access to the actual module pins, the same can be accomplished by send a command via the SiRF binary port to either wake up the module or put the module into hibernate state.

### **4 COMPLIMENTARY DOCUMENTATION**

#### ***4.1 Inventek Systems***

SiRF Binary Protocol Reference Manual

OSP Reference Manual

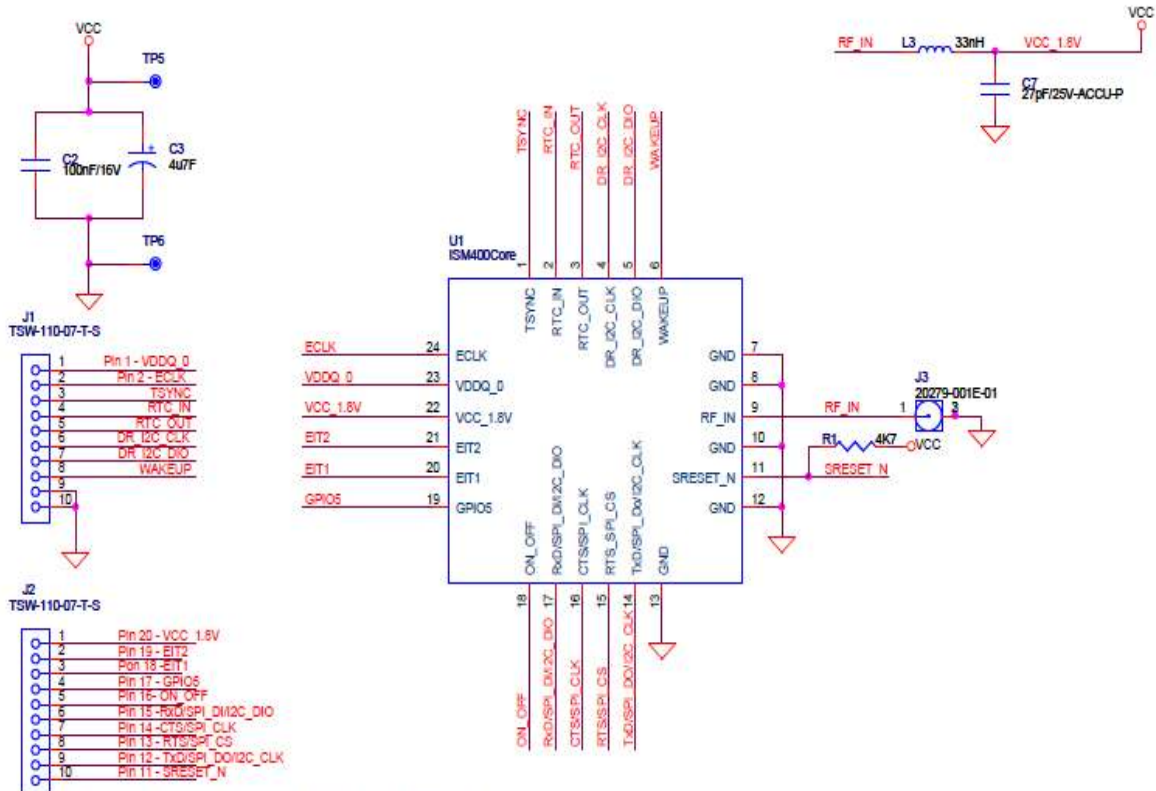
NMEA Reference Manual

SiRF Live Demo Software

## 5 Schematic

### 5.1 Module Architecture

Figure 1 Inventek's ISM420-INT General Block Diagram



The ISM420-INT default state is UART-4800 baud. The I/O's are 3.3 v tolerant, however the output is only 1.8V. You may need a level translator for 3.0 v on the I/O's. It is also critical that you have min. ripple on your 1.8 volt supply. To setup a quick test, you need to connect the following:  
 J1 - Pin 9/10 - Ground  
 J2- Pin 20 - 1.8 V  
 J2 - Pin 16 - to a momentary switch connect to 1.8V  
 J2 - Pin 15 - RX  
 J2- Pin 12 - TX

		<b>Inventek Systems</b> Copyright 2009. All Rights Reserved Confidential Information
Title: ISM42-INT Breakout		
Size: A	Doc.: IOM-420-INT Rev A (UART ONLY MODE) Schematic - D72103	Rev.: A
Date: Friday, April 30, 2010		Sheet: 1 of 1

## 5.2 Hardware Features

The ISM420-INT is a complete navigation GPS processor built on a low power SiRF IV GSD4e processor. The module has an ARM7 processor and RF front end with integrated LAN and SAW to complete a standalone or Aided-GPS engine.

The user is only able to select the output to the host to be UART for the Rev A board, future designs will support I2C or SPI. You will be able to boot strap the device to come in any of the above modes. The default output is a UART outputting, NMEA-0183 at 4800 baud.

It is recommended you connect an external Flash memory to the ISM420 to allow for both ROM patch space for any future ROM fixes and also this is where the ISM420 will store client generated extended ephemeris. The client generated extended ephemeris allows for quick TTFF and can save significant battery power as well as allow for smaller GPS antenna designs.

ROM based Autonomous by simply toggling the ON/OFF pin (4). This permits the user to save considerable battery energy by keeping the module in the lowest

## 5.3 Recommended Antenna Specifications

ISM420R1-CX module is designed for use with an active or passive antenna.

# 6 HARDWARE ELECTRICAL SPECIFICATIONS

## 6.1 Power Supply Maximum Ratings

Parameter	ISM420 Module
Input voltage	1.8 VDC
Current (avg) at full power (1.8V)	45 mA

### 6.1.1 Detailed Pin Description

**J1 – Pin 9,10 – Connect to Ground**

**J2 - Pin 20 – Connect to 1.8 V RTC in: Do not connect.**

**J2 – Pin 16 – to a momentary switch to 1.8V to turn on GPS**

**J2- Pin 15 – Rx- UART\_RX UART data receive**

**J2 – Pin 12 – Tx - UART\_TX UART data transmit**

**Wakeup:** This is an output that indicates the state of the GPS.  
Low is hibernate and high is active. Wake up can be used to control / enable external devices.

**RF-in**  
RF IN from antenna

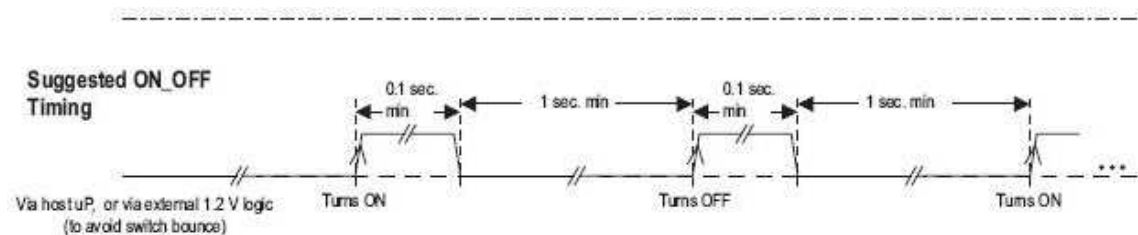
If you want to have your own external RF Connector uses the following guidelines.  
\* Make sure to use a standard 50 ohm SMA or similar connection.

Please note – care should be taken when laying out the RF IN on your PCB as it is a 50 ohm transmission line. This will match the impedance of the connector pin for minimal transmission loss. Care should be taken to not place switching circuits in close proximity to this trace.

**Reset** - Do not connect

**Pin 18 ON\_OFF** (input)

The input level is 1.8V level direct hardware connection to the internal Finite State Machine. The RTC clock must be on and standby for this control to be functional. Minimum on pulse duration is two RTC ticks, about 63us. Minimum inter-pulse interval is one second. Minimum off duration is two RTC ticks, about 63us. See Figure below give a guideline for pulse waveform. A critical item to avoid is contact bounce if mechanical switch are used.



**EIT** Do not connect

**EIT** Pull to ground

**V In** Input Voltage, 1.8 V and add minimize ripple

**VDDQ\_0** Pull down if not used



**ECLK** – Do not connect

## 7 BASIC OPERATION (SPI/UART or I<sup>2</sup>C)

The ISM420 has three outputs to the host, SPI, I<sup>2</sup>C and UART. All ports are multiplexed on a shared set of pins. At system reset, the host port pins are disabled, so no conflict occurs.

At system reset, you can boot strap the device as follows:

Port Type	Pin 16	Pin 15
UART	1( External pull-up)	1(internal pull-up)
SPI (Default)	0 (internal pull-down)	1 (internal pull-up)
I2C	0 (Add a pull down)	0 ( Add a pull-down)

The host ports are configured based on these straps. The software sets up the port pins requirements during low power modes.

### UART Mode

Port Type	16	15
UART Mode	1( External Pull up)	Do no connect

The ISM420 will output NMEA-0183, 4800 baud, 8-N-1. The transmit and receive channel contain a 64B FIFO.

- TX is GPS output
- RX used for GPS control
- nCTS and nRTS are optionally used for hardware flow control.

Through this UART connection, your host microcontroller can change the baud rate, change the output to OSP ( SiRF Binary) or enable or disable many features of the ISM420. Outputs are LVCMOS 1.8V compatible.

### SPI Mode

Port Type	Pin 16	Pin 15
SPI Mode	Do no connect	Do no connect

The host interface SPI is a slave mode SPI.

- MOSI,MISO,nCS and SCLK
- Transmit and Receive have independent 1024B FIFO buffers.
- An interrupt is provided when the transmit FIFO and output serial register are both empty.

- The transmit and receive have individual software defined 2-byte idle patterns of 0xa7 0xb4.
- Max clock of 6.8Mhz

### I<sup>2</sup>C Mode

Port Type	Pin 16	Pin 15
SPI Mode	0 (Add a pull down)	0 (Add a pull down)

The host interface I<sup>2</sup>C mode.

- Operation up to 400kbps.
- Transmit and Receive have independent FIFO length of 64 bytes.
- The default address is
  - RC: 0x60
  - TX: 0x62
- Multi-master I<sup>2</sup>C mode is default mode

## 8 SOFTWARE INTERFACE

The host serial I/O port of the module's serial data interface supports full duplex communication between the module and the user. The default serials are shown in Table below:

Port	Protocol	Description
Port A	NMEA 0183	GGA, GSA, GSV, GLL, RMC, VTG
Port A	OSP(SiRF Binary) Optional	Optional – can send command to switch to OSP. See SiRF OSP Protocol Manual

### ***8.1 NMEA input and output messages***

A complete description of each message is contained in the SiRF NMEA reference manual.

### ***8.2 SiRF Binary Protocol***

A complete description of each binary message is contained in the SiRF Binary Protocol reference manual.

## 9 Product Compliance Considerations

**RoHS:** Restriction of Hazardous Substances (RoHS) directive has come into force since 1st July 2006 all electronic products sold in the EU must be free of hazardous materials, such as lead.

## 10 ORDERING INFORMATION

Part number	Description	Package	Temperature
ISM420R1-CT	GPS module	Surface Mount Tray	-35C- 80 °C
ISM420EVB	Evaluation Board	UART/SDIO/SPI with antenna	
ISM420INT	Interposer Board	DIP format	

## 11 REVISION CONTROL

Document : ISM420INT	GPS Interposer
ECO: Release 1	Production release
8/23/2010 – Release 1.1.1	Release : FMT
Internal	Internal Release

## 12 CONTACT INFORMATION

Inventek Systems  
2 Republic Road  
Billerica Ma, 01862  
Tel : 978-667-1962

[www.inventeksys.com](http://www.inventeksys.com)

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