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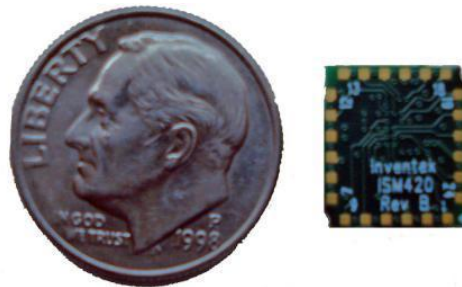
# Inventek Systems

Embedding Connectivity Everywhere

## **Inventek Systems**

**OEM GPS Module**

**Part No. ISM420R1**



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# 1 GENERAL DESCRIPTION



The [Inventek](#) ISM420R1 is a 48 channel global positioning system (GPS) receiver in a very compact Surface Mount Device (SMD) GPS module with high sensitivity, high gain, and low power. The small form factor GP receiver is designed for a broad spectrum of OEM applications and is based on the fast and deep GPS signal search capabilities of CSR , SiRFstarIV™ architecture.

Several key features about this module are:

- ✦ The module is capable of generating and storing extended ephemeris data to an external device for much faster hot starts in weak signal environments.
- ✦ Built-in jamming detection and mitigation to permit fast and accurate navigation solutions in high noise environments.
- ✦ Ability to use an external MEMS device for wakeup when motion is detected, thus reducing power consumption for tracking devices.
- ✦ An addition 4 dB in tracking sensitivity and 5 dB navigation sensitivity over the world class SiRFstar III devices.
- ✦ < 10 mW @ 1.8 volts required to maintain fixes in Trickle Power mode for the ultimate in low power requirements.

## ***Applications***

- ✦ Industrial Handhelds
- ✦ Hand-held Device for Personal Positioning and Navigation
- ✦ PDA, Pocket PC, computing devices
- ✦ Fleet Management / Asset Tracking
- ✦ AVL and Location-Based Services
- ✦ Cellular handsets
- ✦ Cameras, Asset tracking
- ✦ Patient/Child/Pet tracking

# 2 PART NUMBER DETAIL DESCRIPTION

## **Ordering Information**

| <b>Device</b> | <b>Description</b>   | <b>Ordering Number</b> |
|---------------|--|------------------------|
| ISM420R1      | GPS Module, Form Factor 1, Commercial Temp (UART,I2C,SPI)                | ISM420R1-C12           |
| ISM420R1      | GPS Module, Form Factor 1, Commercial Temp (UART,I2C,SPI)                | ISM420R1-C33           |
| ISM420-EVB    | Evaluation Board, UART/I2C/SPI, ISM420 Display,Logging,ISM420INT,Antenna | ISM420-EVB             |
| ISM420-INT    | Interposer Board, DIP,UART, ISM420                                       | ISM420-INT             |

### 3 GENERAL FEATURES

- Based on the high performance features of the SiRFstar IV, GSD4e ROM processor.
- Compact module size for easy integration: 9.5x 10.5 x 2.4 mm (shield height included).
- Host UART or SPI or I<sup>2</sup>C interface
- High sensitivity navigation engine (PVT) tracks as low as -163dBm
- 48 track verification channels
- NMEA-0183, or OSP SiRF binary output
- SBAS (WAAS or EGNOS)
- Integrated LNA, SAW Filter, TCXO and RTC
- Altered search strategy for improved weak-signal acquisition
- Client Generated Extended Ephemeris
- Inputs +3.3 V tolerant
- Single power supply voltage 1.8V.
- Incremental ephemeris collection allowing quicker time-to-first-fix TTFF.
- Lead Free Design which is compliant with ROHS requirements
- EMI/EMC Metal Shield for best RF performance in noisy environments and to accommodate for lower RF emissions/signature for easier FCC compliance.
- FCC/CE Compliance Certified (In process).
- Cold, Warm, Hot Start Time: 35, 35, 1 Sec. respectively.
- Reacquisition Time: 1 second.
- Protocols: NMEA-0183 and SiRF OSP Binary.
- SBAS (WAAS or EGNOS)
- Adaptive Micropower Controller:
- Only 50 to 500 $\mu$ A maintains hot start capability
- <10mW required for TricklePower™ mode
- Smart sensor I<sup>2</sup>C interface
- Interrupt input for context change detection
- Operation from single 1.8V supply
- 50 Ohm antenna input
- Field upgradable patch capability with Host EE

## 4 Navigation Performance Features

- ✚ Improved cross-correlation detection resulting in better position solutions by ignoring bad measurements
- ✚ High sensitivity navigation engine (PVT) tracks as low as -163dBm
- ✚ 48 track verification channels
- ✚ SBAS (WAAS or EGNOS)
- ✚ Altered search strategy for improved weak-signal acquisition
- ✚ Improved EGNOS search strategy.

### 4.1 Improved Jamming Mitigation

- ✚ Better identification and dismissal of jamming signals through enhanced Carrier Wave (CW) detection.
- ✚ Removes in-band jammers up to 80 dB-Hz
- ✚ Tracks up to 8 CW jammers
- ✚ Enhanced development tools to identify noise issues for troubleshooting potential system level noise issues

### 4.2 Improved Ephemeris Availability

- ✚ Incremental ephemeris collection allowing quicker time-to-first-fix (TTFF) in environments where satellite signals are periodically blocked – such as highway underpasses
- ✚ Improved ephemeris collection under challenging dynamics – such as a runner's swinging arm

### 4.3 Flexible Power Control

For embedded applications that will be using NMEA OR SiRF OSP protocol, it is possible to control the state of ISM420 by simply toggling the ON/OFF pin (4). This permits the user to save considerable battery energy by keeping the module in the lowest possible energy state where it consumes less than 10uA. When a satellite fix is required simply toggling the ON/OFF pin (4) puts the module back into full power. If the last fix was less than 2 hours ago, the ISM420 will do a hot fix and be able to get a fix in one second in open sky environment. Then the users circuit can toggle the ON/OFF pin (4) again to put the module into the hibernate state. No external battery backup circuits required.

An application requiring location information every minute will save over 98% on the power consumption depending upon frequency of updates. For portable applications, such as in a laptop, that do not have easy access to the actual module pins, the same can be accomplished by send a command via the SiRF binary port to either wake up the module or put the module into hibernate state.

## **4.4 Advantages**

- ✦ Ideal for compact size devices.
- ✦ Data / Power / RF through surface mount pads.
- ✦ Very low power consumption for power sensitive applications.
- ✦ Cost saving through elimination of RF and board to board digital connectors.
- ✦ Flexible and cost effective hardware design for different application requirements.
- ✦ Secure SMD PCB mounting method.

## **5 COMPLIMENTARY DOCUMENTATION**

### **5.1 Inventek Systems**

Inventek Test Report

ISM420EVB Evaluation Board Specification

ISM420INT Interposer Board Specification

ISM420R1-PB-A Product Brief

### **5.2 SiRF / CSR Technology**

<http://www.inventeksys.com/products-page/gps-modules/ism420r1-c12-sirfstar-iv-sip-gps-receiver/>

NMEA Reference Manual

OSP Reference Manual

SiRF Live



## 6 SPECIFICATIONS

### 6.1 General

### 6.2 Module Architecture

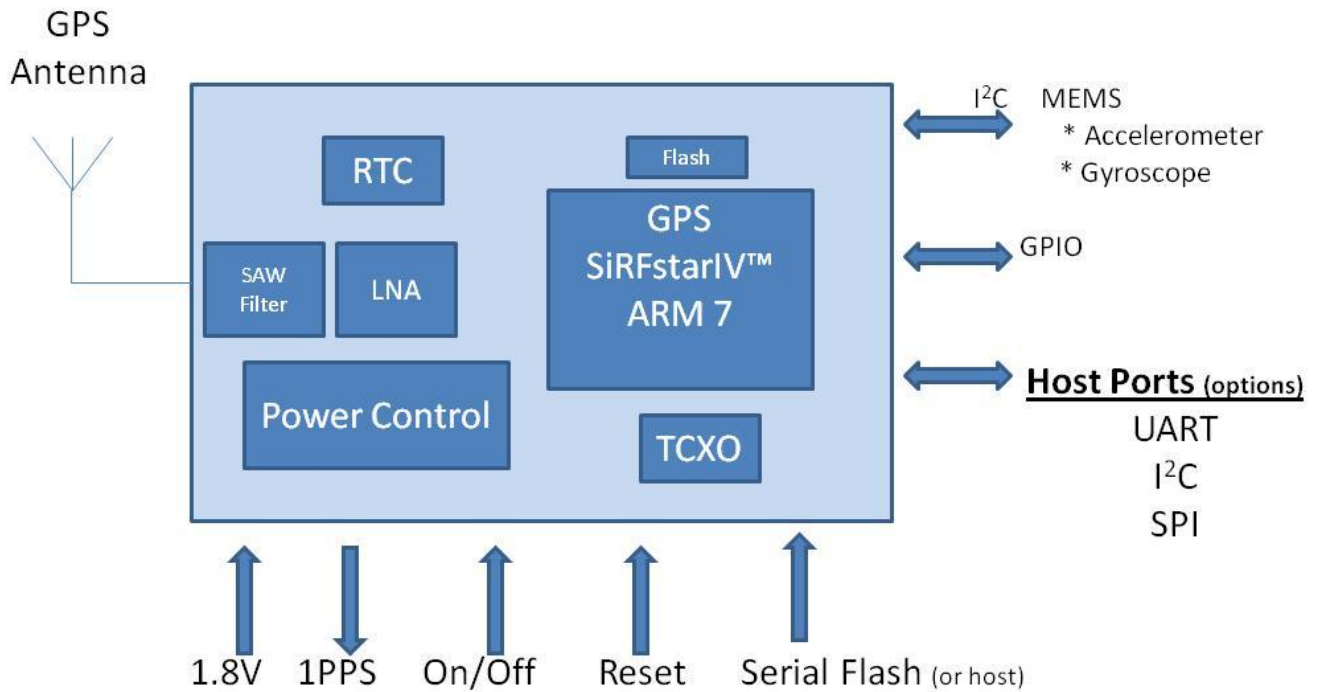


Figure 1 Inventek's ISM420R1-CX General Block Diagram

Section 8.12 for pin descriptions

### **6.3 Hardware Features**

The ISM420 is a complete navigation GPS processor built on a low power SiRF IV GSD4e processor. The module has an ARM7 processor and RF front end with integrated LAN and SAW to complete a standalone or Aided-GPS engine.

The user is able to select the output to the host to be either UART, I2C or SPI and you can boot strap the device to come in any of the above modes. The default output is a SPI outputting.

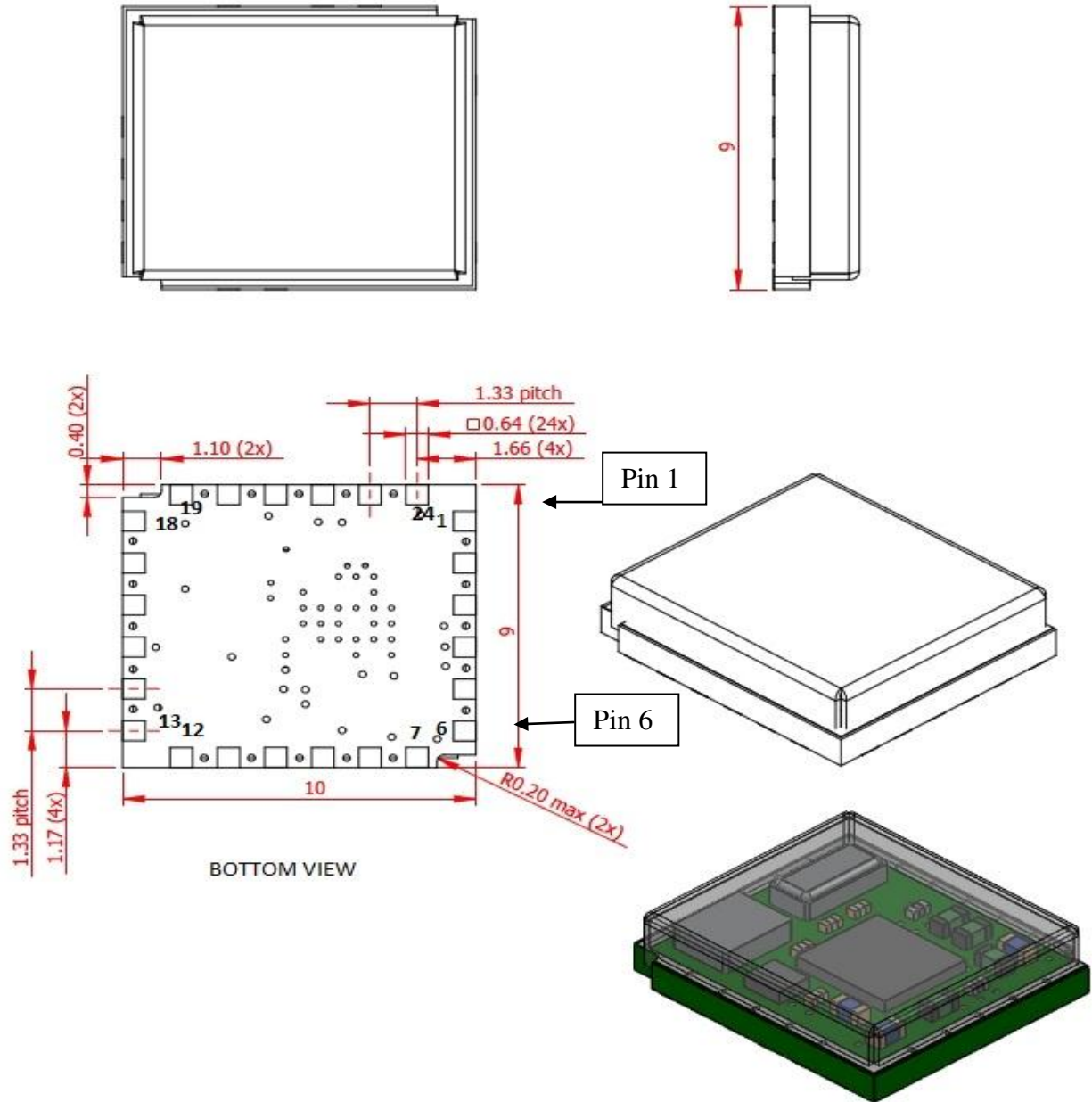
It is recommended you connect an external Flash memory to the ISM420 to allow for both ROM patch space for any future ROM fixes and also this is where the ISM420 will store client generated extended ephemeris. The client generated extended ephemeris allows for quick TTFF and can save significant battery power as well as allow for smaller GPS antenna designs.

### **6.4 Recommended Antenna Specifications**

ISM420R1-CX module is designed for use with an active or passive antenna.

## 6.5 Mechanical Specifications

The Physical dimensions of this GPS Module are as follow:



| Items   | Description                   |
|---------|-------------------------------|
| Length  | 9.5 (-/+0.2 mm)               |
| Width   | 10.5 (-/+0.2 mm)              |
| Height  | 2.4 ± 0.2 mm                  |
| Package | 24 pin LGA, 1.33mm pitch pads |
| Weight  | 3.0 grams                     |

## 6.6 Environmental Specifications

| Item                        | Description                 |
|-----------------------------|-----------------------------|
| Operating temperature range | -35 deg. C to +80 deg. C    |
| Storage temperature range   | -55 deg. C to +100 deg. C   |
| Humidity                    | 95% max non-condensing      |
| Altitude                    | 18,000 m (60,000 ft) max.   |
| Velocity/Speed              | 515 m/Sec (1000 knots) max. |
| Jerk                        | 20 m/Sec <sup>3</sup> (max) |
| Acceleration                | 4 G (max)                   |

## 7 PERFORMANCE

### 7.1 Position and Velocity

| Parameter | Description  |
|-----------|--|
| Position  | 10m, 2D RMS Autonomous, and 5m 2D RMS, SBAS corrected. |
| Velocity  | 0.1 m/Sec  |
| Time      | 1 uSec synchronized to GPS time                        |

2D RMS (Root Mean Square) describes the position accuracy at approximately 95 percent of the data points occur with this distance of a know truth.

### 7.2 Time To First Fix <sup>(See Note 2)</sup> (TTFF)

| Mode  | ISM420R1 |
|---|----------|
| TTFF Hot<br>(valid almanac, position, time & ephemeris)                                 | 1 s      |
| TTFF Warm<br>(valid almanac, position, & time)  | <35 s    |
| TTFF Cold<br>(valid almanac)  | <35 s    |
| Re-Acquisition<br>(<10 secs obstruction with valid almanac, position, time & ephemeris) | 100 ms   |

**Note 2:** Open Sky and Stationary Environments

### 7.3 Dynamic Constraints

| Parameter    | Description                 |
|--------------|-----------------------------|
| Altitude     | 18,000 m (60,000 ft) max.   |
| Velocity     | 515 m/Sec (1000 knots) max. |
| Acceleration | 4 G max                     |
| Jerk         | 20 m/Sec <sup>3</sup> max   |

### 7.4 Timing 1 PPS Output

The 1PPS output width of the ISM420R1-CX Module is ~1 $\mu$ s. The GPS module also outputs a NMEA timestamp message through the serial port. This timestamp message has an approximately a 200ms delay.

### 7.5 Receiver Sensitivity

| Parameter                               | Description |
|---|-------------|
| Tracking Mode Sensitivity               | -163 dBm    |
| Autonomous Acquisition Mode Sensitivity | -148 dBm    |
| Course-aided                            | - 158 dBm   |

Tracking and Autonomous Acquisition Sensitivity specs were determined through the use of 12 Channel Spirent GPS Simulator in a controlled RF Laboratory Environment (Open sky).

### 7.6 Differential GPS (DGPS) Modes

#### 7.6.1 Space Based Augmentation System (SBAS)

The Inventek ISM420R1-CX Module is capable of receiving SBAS (WASS and EGNOS) differential corrections. SBAS improves horizontal position accuracy by correcting GPS signal errors caused by ionosphere disturbances, timing and satellite orbit errors.

## 7.7 Power States

There are several different states the GPS may be in:

Full on: 45 mA Typical  
Tracking: 37 mA Typical  
Hibernate: 20  $\mu$ A Typical  
KA: 10  $\mu$ A Typical

- ✚ Upon initial power on or reset the GPS will be in the KA State.
- ✚ After the GPS receives the On/Off pulse, to turn on, the GPS will go into full Power Mode.
- ✚ Upon a GPS fix, the GPS will automatically go into tracking mode.
- ✚ After the GPS receives an ON/Off pulse, to turn off, the GPS will go back into Hibernate

It is highly recommended that power remains all times, so that the ISM420R1-CX can have fully functional Hot Starts and Warm Starts should the receiver be powered down for any reason. For example:

- A Hot Start will use valid Ephemeris, Almanac, Position, Time and RTC data that have been stored. A hot start will be fully functional up to 2 hours from an initial start up.
- A Warm Start will use valid Almanac, Position Time and RTC data that has been stored. A warm start will occur if the receiver has been powered down for greater than 2 hours.

## 8 HARDWARE ELECTRICAL SPECIFICATIONS

### 8.1 Power Supply Maximum Ratings

| Parameter                          | ISM420 Module |
|------------------------------------|---------------|
| Input voltage                      | 1.8 VDC       |
| Current (avg) at full power (1.8V) | 45 mA         |
| Battery backup voltage             | 1.8 VDC       |
| Battery backup current             | 10 $\mu$ A    |

- In rush current of approx. 55 mA on startup

## 8.1.1 Electrical Specification

### DC Characteristics

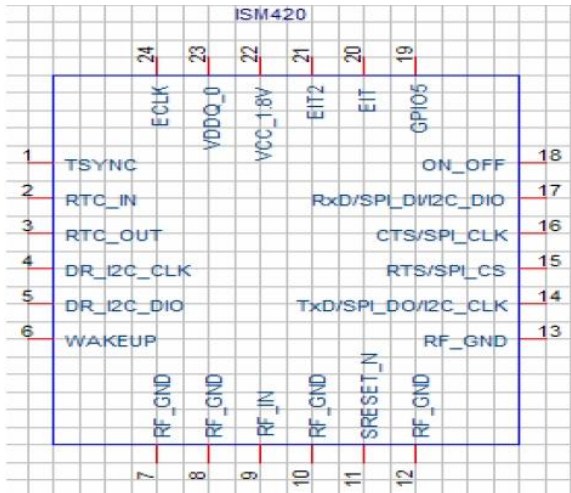
| Parameter             | Symbol           | Mode                             | Min  | Typ | Max  | Units |
|-----------------------|------------------|----------------------------------|------|-----|------|-------|
| Input Voltage         | V <sub>in</sub>  | 1.71                             | 1.71 | 1.8 | 1.89 | V     |
| Power supply Current  | I <sub>cc</sub>  | Acquisition                      |      | 45  |      | mA    |
|                       |                  | Tracking                         |      | 37  |      | mA    |
|                       |                  | Hibernate PTF                    |      | 10  |      | uA    |
| Input Voltage high    | GPIO             |                                  |      |     | 3.5  | V     |
| Input Voltage Low     |                  |                                  |      |     | .5   | V     |
| Input capacitance     |                  |                                  |      | 5   |      | pF    |
| Input Leakage Current |                  | V <sub>in</sub> = 1.8V or 0V     | -10  |     | 10   | uA    |
| Input Leakage Current |                  | V <sub>in</sub> = 1.8V or 0V     | -10  |     | 10   | uA    |
| Output Capacitance    |                  |                                  |      | 5   |      | pF    |
| Input Impedance       | Z <sub>in</sub>  | RF input                         |      | 50  |      | Ohms  |
| Input return loss     | R <sub>Lin</sub> | RF input F <sub>0</sub> 1575.5hz |      | -8  |      | dB    |

### 8.1.2 Pin Positions

| Pin No. | Type | Pin Definition    | Descriptions  |
|---------|------|-------------------|---|
| 1       | O    | TSynch            | GPIO2 programmable I/O 2<br>TSYNC is the time transfer strobe input<br>TM Time Mark output<br>ECLK Boot   |
| 2       | I    | RTC in            | RTC crystal or CMOS RTC clock input   |
| 3       | I    | RTC out           | RTC crystal or open if no crystal   |
| 4       | I/O  | DR I2c clk/ GPIO1 | EEPROM/DR I2C interface/GPIO1 ( see 8.1.3)  |
| 5       | I/O  | DR I2C out/ GPIO0 | EEPROM/DR I2C interface/GPIO0. ( see 8.1.3)   |
| 6       | O    | Wakeup            | Wake up output for control of external memory, or can also enable an external regulator, e.g. battery to 1.8V for the main input to the switch-mode regulator when full current mode is entered |
| 7       | G    | GND               | Ground  |
| 8       | G    | GND               | Ground  |
| 9       | I    | RF-in             | RF IN from antenna  |

|    |     |                   |   |
|----|-----|-------------------|---|
| 10 | G   | GND               | Ground  |
| 11 | I   | Reset             | External reset input, active low  |
| 12 | G   | GND               | Ground  |
| 13 | G   | GND               | Ground  |
| 14 | I/O | TX/MISO/SCL       | SSPI_DO slave SPI data output (MISO)<br>UART_TX UART data transmit (TX)<br>I2C_CLK I <sup>2</sup> C bus clock (SCL)   |
| 15 | I/O | GPIO7/RTS/SPI_CS  | See Section 9   |
| 16 | I/O | GPIO6/CTS/SPI_CLK | See Section 9   |
| 17 | I/O | RX/MOSI/SDA       | SSPI_DI slave SPI data input (MOSI)<br>UART_RX UART data receive (RX)<br>I2C_DIO I <sup>2</sup> C bus data (SDA)  |
| 18 | I   | ON_OFF            | Power control pin   |
| 19 | I/O | GPIO 5            | GPIO5 programmable I/O 5<br>TM Time Mark output timing pulse related to receiver time, GPS time or UTC time.  |
| 20 | I   | EIT               | GPIO4 programmable I/O 4<br>EIT external interrupt input pin  |
| 21 | I/O | EIT 2             | GPIO8 programmable I/O 8<br>EIT2 external interrupt input pin 2. Provides an interrupt on either high or low logic level or edge-sensitive interrupt.<br>RTCCLK buffered output of the RTC clock signal |
| 22 | I   | V in              | Input Voltage , 1.8 V   |
| 23 | I   | VDDQ_0            | Not used, must pull low   |
| 24 | I/O | ECLK              | GPIO3 programmable I/O 3<br>ECLK clock input for frequency aiding applications or as a test clock<br>DAC_DI data input for VCTCXO<br>DAC command word   |





### 8.1.3 Detailed Pin Description

**PIN 1 T Sync:** Do not connect

This is an AGPS feature that we do not recommend using for most applications.

**Pin 2 RTC in:** N/C ( No Connect)

**Pin 3 RTC out:** N/C ( No Connect)

**\*Pin 4 DR I<sup>2</sup>C Clk and \* Pin 5 DR I<sup>2</sup>C out:**

Connect an optional EEPROM for storing patches and CGEE. The software will default to NMEA 4800 when an EEPROM or SPI device is attached, but can be changed via an OSP message. If you do not connect the SPI or EEPROM the table below will be used to determine the initial power on state.

(\* Note: Firmware Release ISM420-R1-C33 see table for multipurpose GPIO 0 and GPIO1) ( This is strapping option is not supported in ISM420-R1-C12)

Table 1: Lists the settings for GPIO0 and GPIO1 to configure the baud rate at start-up. After start-up the GPIOs can be used for other purposes

| GPIO 0 (Pin 5) | GPIO1 (Pin 4 ) | Protocol | Baud Rate |
|----------------|----------------|----------|-----------|
| Pull High      | Pull High      | NMEA     | 4800      |
| Pull High      | Pull Low       | NMEA     | 9600      |
| Pull Low       | Pull High      | NMEA     | 38400     |
| Pull Low       | Pull Low       | OSP      | 115200    |

### **Pin 6 Wakeup:**

This is an output that indicates the state of the GPS.

Low is hibernate and high is active.

You need to monitor Wakeup to know the state of the GPS. Wake up can be used to control / enable external devices.

### **Pin 7 GND**

### **Pin 8 GND**

### **Pin 9 RF-in**

RF IN from antenna

If you want to have your own external RF Connector uses the following guidelines.

\* Make sure to use a standard 50 ohm SMA or similar connection.

\* Make the connection to the trace to Pin 9 - a short PCB trace.

**Please note – care should be taken when laying out the RF IN on your PCB as it is a 50 ohm transmission line. This will match the impedance of the connector pin for minimal transmission loss. Care should be taken to not place switching circuits in close proximity to this trace.**

### **Pin 10 GND**

### **Pin 11 Reset**

External reset input, active low

### **Pin 12 GND**

### **Pin 13 GND**

### **Pin 14 TX (output)**

UART\_TX UART data transmit (TX)

If in SPI mode SSPI\_DO slave SPI data output (MISO)

If in I<sup>2</sup>C mode I<sup>2</sup>C\_CLK I<sup>2</sup>C bus clock (SCL)

\*See section 9 for configuration

### **Pin 15 GPIO7 (input)**

SPI (CS#) active low

UART RTS ( active low)

Host port Strap input

See section 9 for configuration

### Pin 16 GPIO6 (input)

SPI Clk Slave SPI clock input  
UART CTS (active low)  
Host port Strap input  
See section 9 for configuration

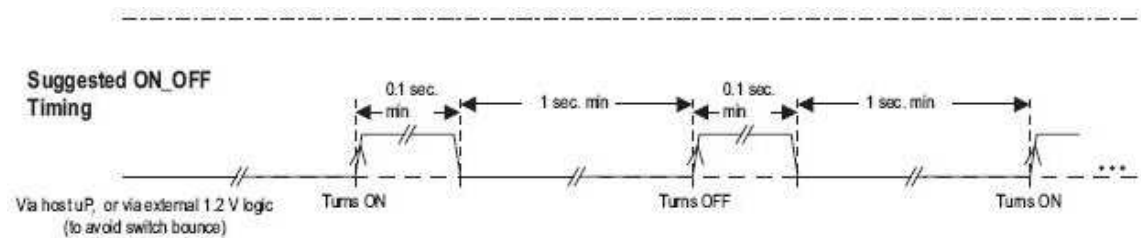
### Pin 17RX (Input)

UART\_RX UART data receive (RX)  
SPI (MOSI)  
I<sup>2</sup>C DIO SDA  
See section 9 for configuration

### Pin 18 ON\_OFF (input)

Power control pin is 3.5 volt tolerant

The input level is a direct hardware connection to the internal Finite State Machine. The RTC clock must be on and stable for this control to be functional. Minimum on pulse duration is two RTC ticks, about 63us. Minimum inter-pulse interval is one second. Minimum off duration is two RTC ticks, about 63us. See Figure below give a guideline for pulse waveform. A critical item to avoid is contact bounce if mechanical switch are used.



### Pin 19GPIO 5

This is the 1pps TM Time Mark output timing pulse related to receiver time, GPS time or UTC time, available after a GPS Fix

### Pin 20EIT N/C (Do not connect)

GPIO4 programmable I/O 4  
DAC\_CLK is the clock for transferring VCTCXO DAC command word  
BLANKING (RF\_ON) RF active input pin from another RF transmitter  
EIT external interrupt input pin

**Pin 21 EIT 2** If not used - pull to ground

GPIO8 programmable I/O 8

EIT2 external interrupt input pin 2.

Provides an interrupt on either high or low logic level or edge-sensitive interrupt.

RTCCLK buffered output of the RTC clock signal

**Pin 22 V\_In**

Input Voltage, 1.8 V and add ripple spec.

**Pin 23 VDDQ\_0** GND

**Pin 24 ECLK** – Do not connect

This is used for AGPS

## 9 BASIC OPERATION (SPI/UART or I<sup>2</sup>C)

The ISM420R1 has three outputs to the host, SPI, I<sup>2</sup>C and UART. All ports are multiplexed on a shared set of pins. At system reset, the host port pins are disabled, so no conflict occurs.

At system reset, you can boot strap the device as follows:

| Port Type     | Pin 16 (GPIO 6)      | Pin 15 (GPIO 7)      |
|---------------|----------------------|----------------------|
| UART          | External pullup10KΩ  | (N/C) Do not connect |
| SPI (Default) | (N/C) Do not connect | (N/C) Do not connect |
| I2C           | (N/C) Do not connect | Add a 10KΩ pull down |

The host ports are configured based on these straps. The software sets up the port pins requirements during low power modes.

### UART Mode

| Port Type | Pin 16              | Pin 15               |
|-----------|---------------------|----------------------|
| UART Mode | External pullup10KΩ | (N/C) Do not connect |

The ISM420R1 will output OSP, 115200 baud, 8-N-1. The transmit and receive channel contain a 64B FIFO.

- TX is GPS output
- RX used for GPS control

- nCTS and nRTS are optionally used for hardware flow control.

Through this UART connection, your host microcontroller can change the baud rate, change the output to OSP ( SiRF Binary) or enable or disable many features of the ISM420R1. Outputs are LVCMOS 1.8V compatible Please refer to GPIO0 and GPI01 for various default outputs at startup

### **SPI Mode**

On initial power on, the GPS module will look at pin 15 and Pin 16 to determine the mode of operation. Your SPI bus should have no pull up or pull down is required. On power up the connection to Pin 15 and Pin 16 must be tri stated on the SPI bus.

| <b>Port Type</b> | <b>Pin 16</b>        | <b>Pin 15</b>        |
|------------------|----------------------|----------------------|
| SPI Mode         | (N/C) Do not connect | (N/C) Do not connect |

The host interface SPI is a slave mode SPI.

- MOSI,MISO,nCS and SCLK
- Transmit and Receive have independent 1024B FIFO buffers.
- An interrupt is provided when the transmit FIFO and output serial register are both empty.
- The transmit and receive have individual software defined 2-byte idle patterns of 0xa7 0xb4.
- Max clock of 6.8Mhz

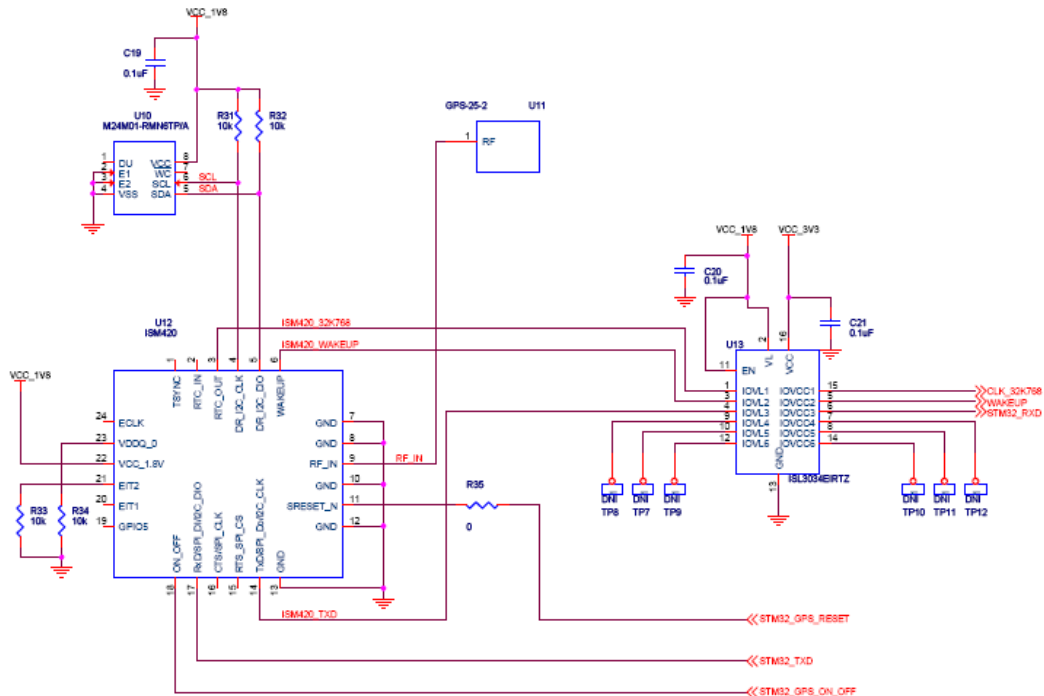
### **I<sup>2</sup>C Mode**

| <b>Port Type</b>      | <b>Pin 16</b>        | <b>Pin 15</b>        |
|-----------------------|----------------------|----------------------|
| I <sup>2</sup> C Mode | (N/C) Do not connect | Add a 10KΩ pull down |

The host interface I<sup>2</sup>C mode.

- Operation up to 400kbps.
- Transmit and Receive have independent FIFO length of 64 bytes.
- The default address is
  - RC: 0x60
  - TX: 0x62
- Multi-master I<sup>2</sup>C mode is default mode

## 10 SCHEMATIC EXAMPLE



The attached schematic is an example of the ISM420R1 being connected to a 3.3v microcontroller. The output on the ISM420R1 is 1.8 Volts only so a translator chip was used in this design. Please note:

- Pin 16 - needs to be strapped high in the UART mode
- Pin 4 and Pin 5 can be used to configure baud rate and Protocol at startup
- U10 – EPROM is used for future patch upgrades and Client Generated Extended Ephemeris ( optional )
- U11 – Shown is a passive patch antenna. If you plan on using an active, you must provide your own power to the antenna
- Monitor Wakeup for state of GPS
- Recommend not using RTC\_out ( Loading on RTC may cause startup issue)
- 50 Ohm trace for RF\_in
- Ensure a clean 1.8V supply

## 11 SOFTWARE INTERFACE

The host serial I/O port of the module's serial data interface supports full duplex communication between the module and the user. The default serials are shown in Table below:

| Port   | Protocol                     | Description  |
|--------|------------------------------|--|
| Port A | NMEA 0183                    | GGA, GSA, GSV, GLL, RMC, VTG   |
| Port A | OSP(SiRF Binary)<br>Optional | Optional – can send command to switch to OSP. See SiRF OSP Protocol Manual |

### 11.1 NMEA input and output messages

A complete description of each message is contained in the SiRF NMEA reference manual.

### 11.2 SiRF Binary Protocol

A complete description of each binary message is contained in the SiRF Binary Protocol reference manual.

## 12 Product Compliance Considerations

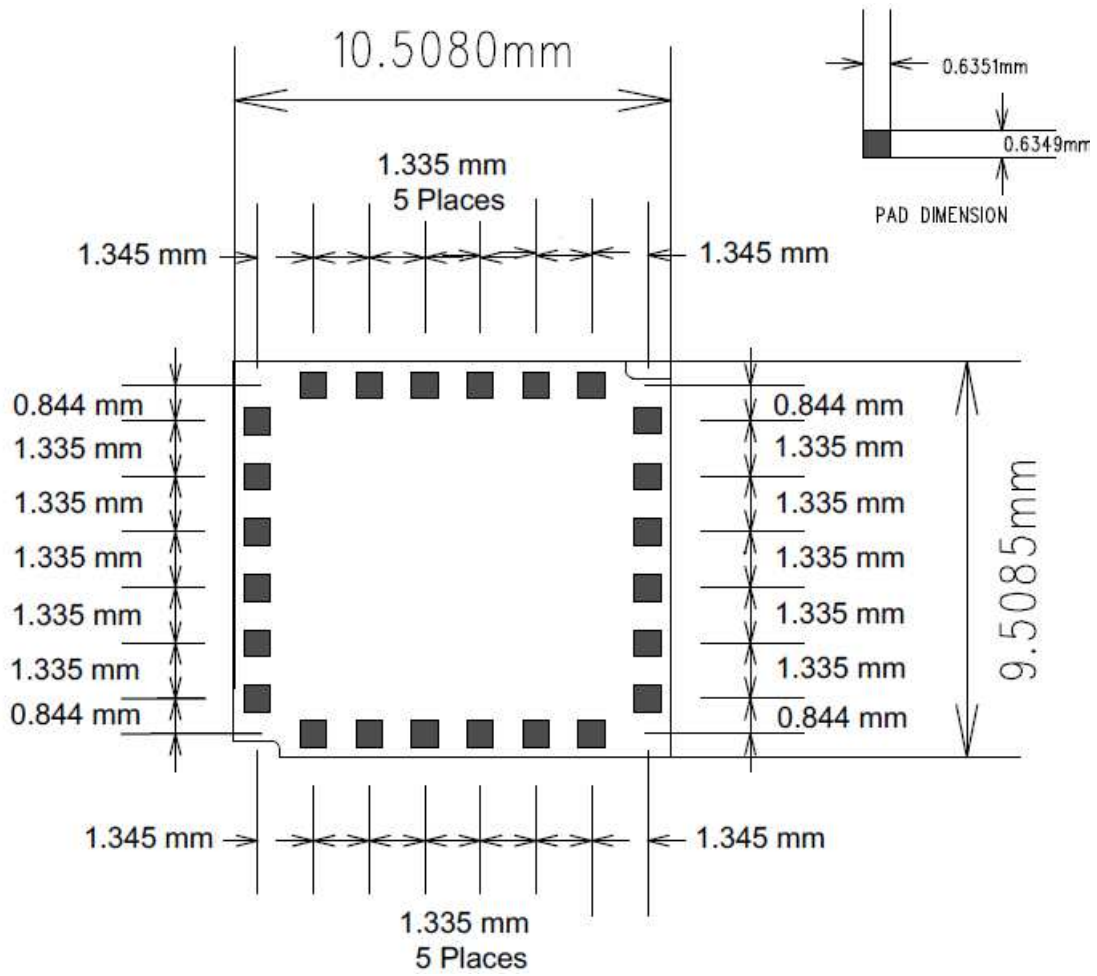
**RoHS:** Restriction of Hazardous Substances (RoHS) directive has come into force since 1st July 2006 all electronic products sold in the EU must be free of hazardous materials, such as lead. Inventek is fully committed to being one of the first to introduce lead-free GPS products while maintaining backwards compatibility and focusing on a continuously high level of product and manufacturing quality.

**EMI/EMC:** The Inventek GPS module design embeds EMI/EMC suppression features and accommodations to allow for higher operational reliability in noisier (RF) environments and easier integration compliance in host (OEM) applications.

**FCC/CE:** The module will be in compliance test for FCC/CE

# 13 ISM420R1-CX FOOTPRINT

## 13.1 Module's package dimensions (mm)





## 14 ORDERING INFORMATION

| Part number  | Description      | Package                              | Temperature |
|--------------|------------------|--------------------------------------|-------------|
| ISM420R1-C12 | GPS module       | Not Available                        |             |
| ISM420R1-C33 | GPS module       | Surface Mount Tray                   | -35C- 80 °C |
| ISM420EVB    | Evaluation Board | UART/SDIO/SPI with antenna connector | -35C- 80 °C |
| ISM420INT    | Interposer Board | DIP format                           | -35C- 80 °C |

## 15 REVISION CONTROL

|                         |                |
|-------------------------|----------------|
| Document : ISM420R1-C33 | GPS module     |
| External Release        | DOC-DS-20001-2 |

| Date      | Author | Revision | Comment  |
|-----------|--------|----------|--|
| 8/23/2010 | FMT    | 1.2.0    | Preliminary  |
| 3/2/2011  | FMT    | 2.0      | Production   |
| 3/7/2011  | FMY    | 2.3      | Footprint  |
| 9/13/2011 | FMT    | 2.4      | Footprint  |
| 5/14/12   | NAR    | 2.5      | Logo/Typo  |
| 12/7/13   | MFT    | 2.6      | New Part number,<br>New Firmware,<br>Default boot OSP<br>15200 |

## 16 CONTACT INFORMATION

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