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ISOFACE™

ISO1I813T

Isolated 8 Channel Digital Input with IEC61131-2 Type 1/2/3 Characteristics

Data Sheet

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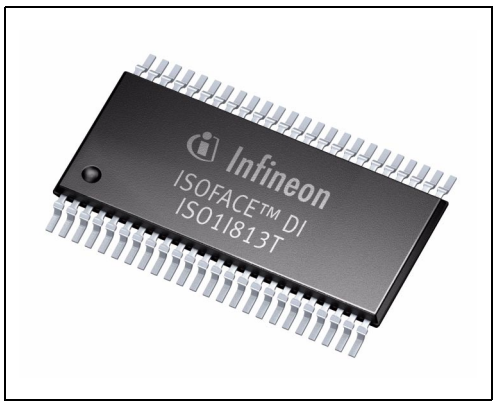
Revision History: 2013-04-30, V 2.0	
Previous Version: Premilinary Data Sheet V1.0	
Page	**Subjects (major changes since last revision)**
V 2.0	Data Sheet
6, **9**, **11**	Description of SEL pin corrected
24	**Chapter 3.6 Programmable Digital Input Filter** updated and information about filter times added
26	**Chapter 3.7 Parallel Interface Mode** updated
29	**Chapter 3.8.1 SPI Modes** write access decription updated
34	**Chapter 3.9 SYNC Operation** updated
35	**Chapter 3.10 Write-Read- Access and Read-Read-Access for Different Applications** added
37	**Table 3 System Insulation Characteristics** Condition for Production test added
45	**Table 15 Parallel Interface** timing updated
46	**Table 16 Serial Interface** timing updated

Isolated 8 Channel Digital Input with IEC61131-2 Type 1/2/3 Characteristics



Product Highlights

- **Minimization of power dissipation due to constant current characteristic**
- **Status LED output for each input**
- **Digital averaging of the input signals to suppress interference pulses**
- **Isolation between Input and Output using Coreless Transformer Technology**

Features

- Complete system integration (digital sensor or switch input, galvanic isolation and intelligent micro-controller or bus-ASIC interface)
- 8-channel input according to IEC61131-2 (Type 1/2/3)
- Integrated galvanic isolation 500VAC (EN60664-1, UL1577)
- 3.3V/5V SPI and parallel micro-controller interface
- Adjustable deglitching filters
- Up to 500 kHz sampling frequency
- Wire-break detection
- VBB under-voltage detection
- Package: TSSOP-48, 8 mm x 12.5 mm

Typical Application

Programmable Logic Controllers(PLC)

Industrial PC

General Control Equipment

Description

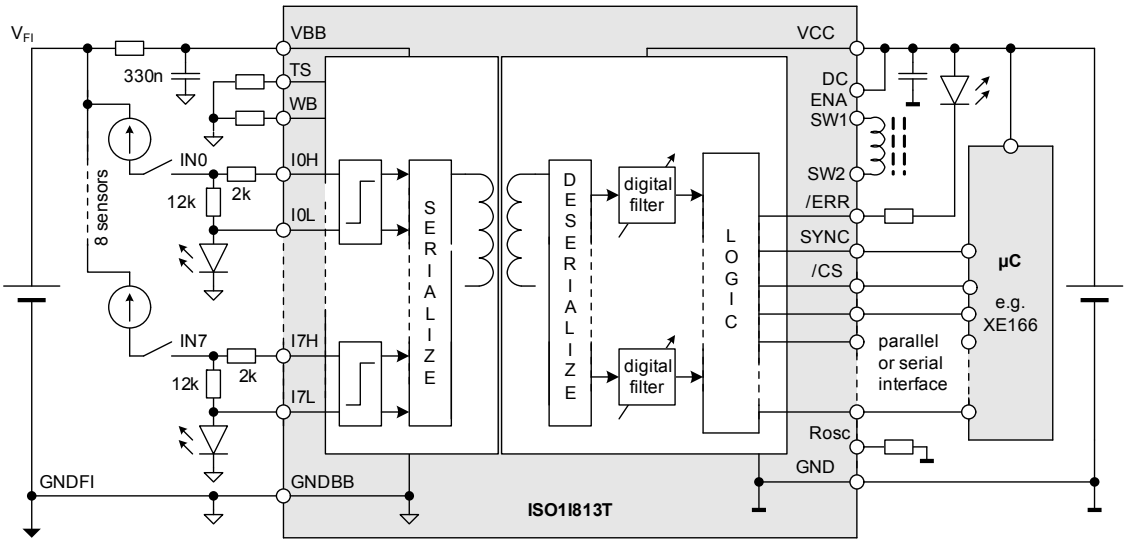
The ISO1I813T is an electrically isolated 8 bit data input interface in TSSOP-48 package.

This part is used to detect the signal states of eight independent input lines according to IEC61131-2 Type 1/2/3 (e.g. two-wire proximity switches) with a common ground (GNDFI).

For operating sensors of type 1/2/3 in accordance with IEC61131-2, it is necessary for the device to be wired with resistors R_V and R_{EXT} (it is recommended to use resistors with an accuracy of 2%, in any case < 5% - is mandatory, temperature-coefficients < 200ppm are allowed).

An 8 bit parallel µC compatible interface allows to connect the IC directly to a µC system. The input interface is designed to operate with 3.3/5V CMOS compatible levels.

The data transfer from input to output side is realized by the integrated Coreless Transformer Technology.



Typical Application for Sensor of Type 1/3

1 Pin Configuration and Functionality

The pin configuration slightly differs for the parallel or the serial interface.

1.1 Pin Configuration

The ordering, type and functions of the IC pins are listed in the **Table 1**.

Table 1 Pin Configuration

Pin	Parallel Interface Mode				Serial Interface Mode			
	Symbol	Ctrl 1)	Type 2)	Function	Symbol	Ctrl. 1)	Type 2)	Function
1	GND		A	Logic Ground	GND			
2	SEL	I	PU	Serial Parallel Mode Select	SEL			
3	SYNC	I	PU	Freeze Data & Diagnostics	SYNC			
4	Rosc		A	Clock Frequency Adjustment	Rosc			
5	VCC		A	Positive 5/3.3V logic supply	VCC			
6	$\overline{\text{ERR}}$	O	OD, PU	Fault Indication output	$\overline{\text{ERR}}$			
7	GND		A	Logic Ground	GND			
8	AD0	IO	PPZ	Data output bit0	SDI	I	PD	SPI Data input
9	AD1	IO	PPZ	Data output bit1	SSO	O	PPZ	SPI Status output
10	AD2	IO	PPZ	Data output bit2	GND			
11	AD3	IO	PPZ	Data output bit3	GND			
12	AD4	IO	PPZ	Data output bit4	$\overline{\text{CRCERR}}$	O	OD, PU	CRC Error output
13	AD5	IO	PPZ	Data output bit5	SCLK	I	PD	SPI Shift Clock input
14	AD6	IO	PPZ	Data output bit6	SSI	I	PD	SPI Status input
15	AD7	IO	PPZ	Data output bit7	SDO	O	PPZ	SPI Data output
16	$\overline{\text{CS}}$	I	PU	Chip Select	$\overline{\text{CS}}$			
17	$\overline{\text{RD}}$	I	PU	Data Read	n.c.			
18	GND		A	Logic Ground	GND			
19	$\overline{\text{WR}}$	I	PU	Data Write	MS0	I	PD	SPI Mode Select bit 0
20	ALE	I	PD	Address Latch Enable	MS1	I	PD	SPI Mode Select bit 1
21	DC_ENA	I	PD	DC-DC Supply Enable	DC_ENA			
22	SW1		A	DC-DC Switch Output 1	SW1			
23	SW2		A	DC-DC Switch Output 2	SW2			
24	GND		A	Logic Ground	GND			
Sensor Side Pins								
25	GNDBB		A	Input Ground	GNDBB			
26	VBB		A	Positive input supply voltage	VBB			
27	I0L		A	Input 0 Low, LED Out	I0L			
28	I0H		A	Input 0 High	I0H			
29	I1L		A	Input 1 Low, LED Out	I1L			
30	I1H		A	Input 1 High	I1H			

Table 1 Pin Configuration

Pin	Parallel Interface Mode				Serial Interface Mode			
	Symbol	Ctrl 1)	Type 2)	Function	Symbol	Ctrl. 1)	Type 2)	Function
31	GNDBB		A	Input Ground	GNDBB			
32	I2L		A	Input 2 Low, LED Out	I2L			
33	I2H		A	Input 2 High	I2H			
34	I3L		A	Input 3 Low, LED Out	I3L			
35	I3H		A	Input 3 High	I3H			
36	TS		A	Sensor Type 1/2/3 Select	TS			
37	GNDBB		A	Input Ground	GNDBB			
38	WB		A	Wire Break Select	WB			
39	I4L		A	Input 4 Low, LED Out	I4L			
40	I4H		A	Input 4 High	I4H			
41	I5L		A	Input 5 Low, LED Out	I5L			
42	I5H		A	Input 5 High	I5H			
43	GNDBB		A	Input Ground	GNDBB			
44	I6L		A	Input 6 Low, LED Out	I6L			
45	I6H		A	Input 6 High	I6H			
46	I7L		A	Input 7 Low, LED Out	I7L			
47	I7H		A	Input 7 High	I7H			
48	GNDBB		A	Input Ground	GNDBB			

1) Direction of the pin: I = input, O = output, IO = Input/Output

2) Type of the pin: A = analog, OD = Open-Drain, PU = internal Pull-Up resistor, PD = internal Pull-Down resistor, PPZ = Push-Pull pin with High-Impedance functionality

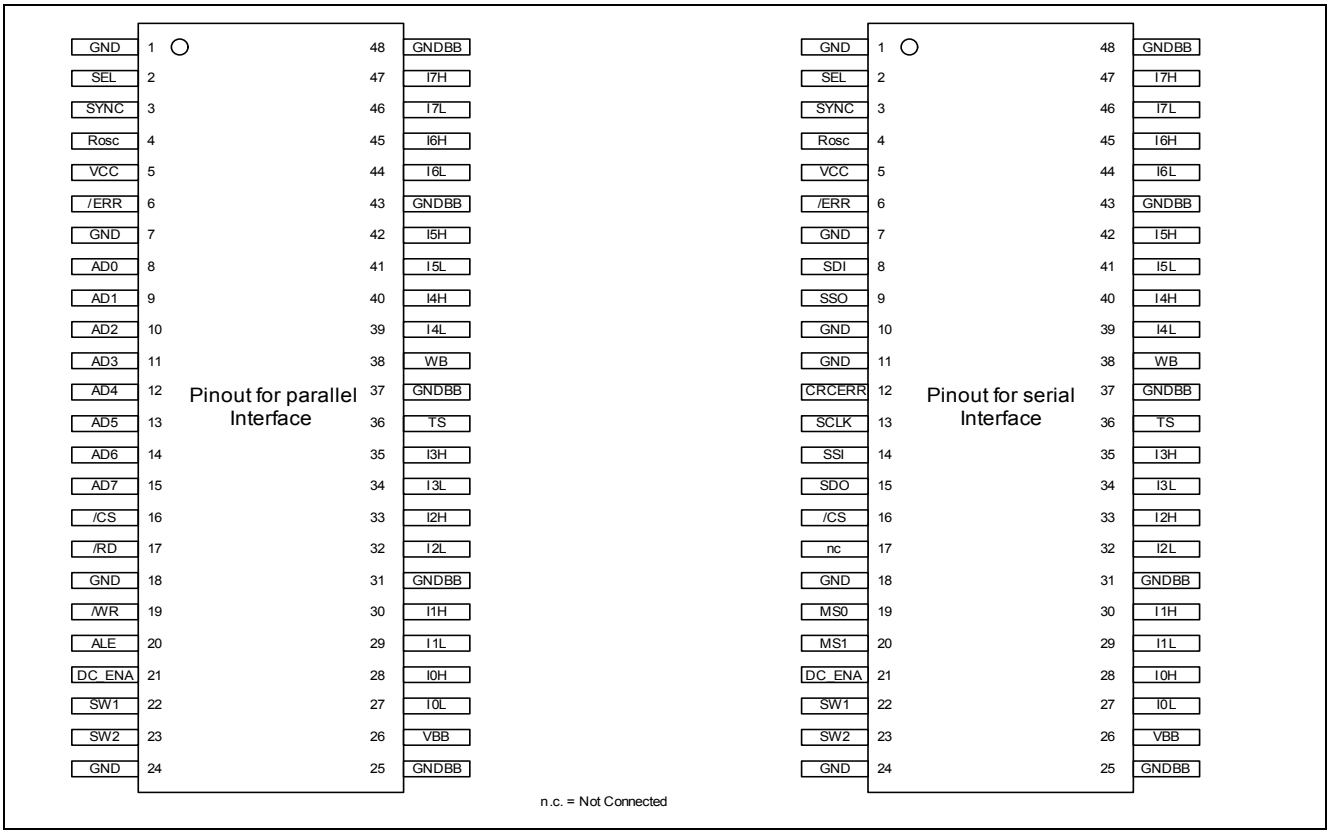


Figure 1 TSSOP-48 Pinout for Parallel and Serial Interface Modes

1.2 Pin Functionality

1.2.1 Pins of Sensor Interface

VBB (Positive supply 9.6-35V sensor supply)

VBB supplies the sensor input stage.

GNDBB (Ground for VBB domain)

This pin acts as the ground reference for the sensor input stage that is supplied by VBB.

I0H... I7H (Input channel 0 ... 7)

Sensor inputs with current sink characteristic according IEC61131-2 Type 1/2/3 which has been selected by pin TS

I0L... I7L (LED output channel 0 ... 7)

This pin provides the output signal to switch on the LED if the input voltage and current has been detected as “High” according to the selected type.

WB (Wire-Break Select)

By connecting a resistor between pin WB and pin GNDBB, the level for the Wire-Break detection can be adjusted (refer to **Table 10** for corresponding resistor value). This pin is for static configuration (pin-strapping). The input voltage at pin WB is not allowed to be changed during operation.

TS (Type Select)

By connecting a resistor between TS and GNDBB the sensor type (Type 1/2/3) can be selected (refer to **Table 10** for corresponding resistor value). This pin is for static configuration (pin-strapping). The input voltage at pin TS is not allowed to be changed during operation.

1.2.2 Pins of Serial and Parallel logic Interface

Some pins are common for both interface types, some others are specific for the parallel or serial access.

VCC (Positive 3.3/5V logic supply)

VCC supplies the output interface that is electrically isolated from the sensor input stage. The interface can be supplied with 3.3/5V.

GND (Ground for VCC domain)

This pin acts as the ground reference for the uC-interface that is supplied by pin VCC.

Rosc (Clock Adjustment)

A high precision resistor has to be connected between pin Rosc and pin GND to set the frequency of the sampling clock.

DC_ENA (DC-DC Converter Enable)

When the DC_ENA pin is connected to VCC, the internal DC-DC driver is activated. When DC_ENA is in the state Low, the switches are not driven. The input voltage must not change during operation. This pin has an internal Pull-Down resistor.

SW1, SW2 (DC-DC switch outputs 1/2)

When the pin DC_ENA is connected to VCC, the outputs SW1 and SW2 switch at the clock-frequency determined by the resistor at pin Rosc to supply the external push-pull converter. The switching frequency can be divided by two by setting the responsible bit in the GLCFG register (see also **Chapter 6**). Both outputs provide an open drain functionality.

$\overline{\text{ERR}}$ (Error)

The active Low $\overline{\text{ERR}}$ signal contains the OR-wired information of the sensor input undervoltage and missing voltage detection, the internal data transmission failure detection unit and the overcurrent fault of the DC-DC-converter. The output pin $\overline{\text{ERR}}$ provides an open drain functionality. During Start Up this pin $\overline{\text{ERR}}$ is pulled to High. This pin $\overline{\text{ERR}}$ has an internal Pull-Up resistor. In normal operation the signal $\overline{\text{ERR}}$ is High. See **Chapter 3.5** for more details.

SEL (Serial or Parallel Mode Select)

When this pin is in a logic Low state, the IC operates in Parallel Mode. For Serial Mode operation the pin has to be pulled into logic High state. During Start Up the IC is operating in Serial Mode. This pin has an internal Pull-Up resistor. This pin must not change during operation.

SYNC

When this pin is in a logic High state, the IC operates in continuous mode with the internal sampling clock. In isochronous mode, the internal data and diagnostics registers are synchronized on each falling edge detected at SYNC. The internal data and diagnostics registers are frozen with the falling edge of SYNC. In logic Low state the internal data and diagnostic registers are not updated. During Start-Up this pin is pulled to High state. This pin has an internal Pull-Up resistor. (see also **Chapter 3.9**)

$\overline{\text{CS}}$ (Chip Select)

When the pin $\overline{\text{CS}}$ pin is logic Low, the IC interface is enabled and data can be transferred. This pin $\overline{\text{CS}}$ has an internal Pull-Up resistor.

The following pins are provided in the parallel interface mode

AD7:AD0 (AddressData input / output bit7 ... bit0)

The pins AD0 .. AD7 are the bidirectional input / outputs for data write and read. Depending on the state of the pins ALE, $\overline{RD}$, $\overline{WR}$ and the AD7 bit register addresses or data can be transferred between the internal registers and the parallel interface of a e.g. micro-controller .

$\overline{RD}$, $\overline{WR}$ (Read / Write)

By pulling one of these pins down, a read or write transaction is initiated on the AddressData bus and the data becomes valid. These pins have internal Pull-Up resistors.

ALE (Address Latch Enable)

The pin ALE is used to select between address (ALE is in a logic High state) or data (ALE is in a logic Low state). Furthermore, a read or write transaction can be selected in conjunction with the AD7 bit. When ALE is pulled high, addresses are transferred and latched over the bit AD0 to AD6. The AD7 bit serves for a read access (AD7 is Low) or a write access (AD7 is High) at this address. During the Low State of ALE all transactions hit the same adress. This pin has an internal Pull-Down resistor.

The following pins are provided in the serial interface mode

MS0, MS1 (Serial Mode Select)

By driving the pins MS, MS1 to Logic High or Logic Low the Serial Interface Mode can be selected. These pins have internal Pull-Down resistors. The mode of the Serial Interface can be changed by the user during operation.

SCLK (Serial interface shift clock)

Input data are sampled with the rising edge and output data are updated with the falling edge of this input clock signal. This pin SCLK has an internal Pull-Down resistor.

SDI, SSI (Serial interface data/status input)

SDI/SSI data is put into a dedicated FIFO to program the filtering time and mask the Wire-Break diagnostic bits of each channel (SPI Mode 2 and 3). It is also used to set the address of the register, which is intended to be accessed. This pin has an internal Pull-Down resistor.

SDO, SSO (Serial interface data/status outputs)

SDO provides the sensor data bits and or the register content, SSO provides the sensor diagnostics bits.

$\overline{CRCERR}$ (CRC Error output)

This pin $\overline{CRCERR}$ is in a logic Low state when CRC errors or Shift-Clock errors are detected internally. This pin $\overline{CRCERR}$ provides an open drain functionality. This pin has an internal Pull-Up resistor.

2 Blockdiagram

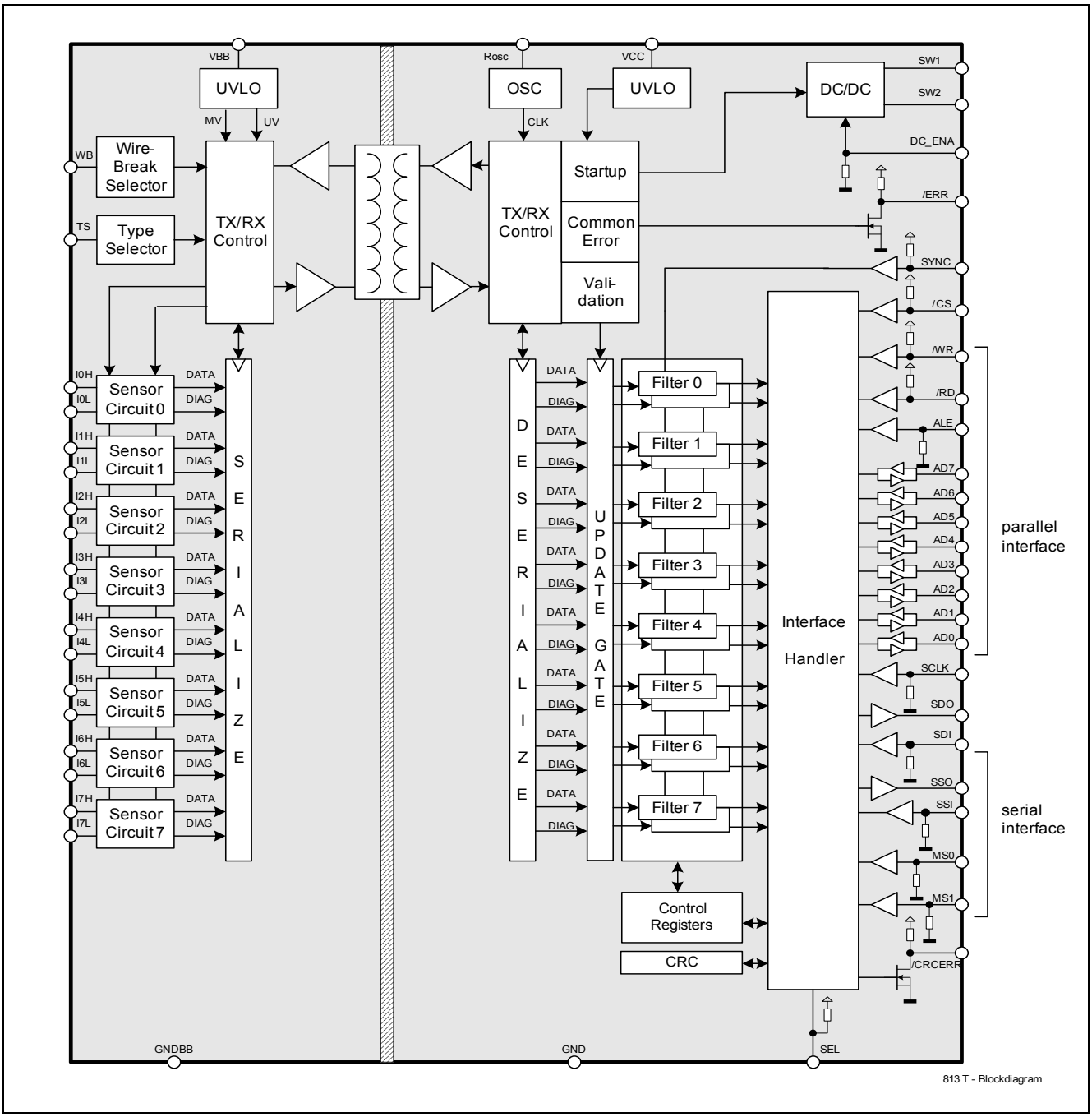


Figure 2 Block Diagram ISO1I813T

3 Functional Description

The ISO1I813T is an electrically isolated 8 bit data input interface. This part is used to detect the signal states of eight independent input lines according to IEC61131-2 Type 1/2/3 (e.g. two-wire proximity switches) with a common ground (GNDBB).

3.1 Introduction

The current in the input circuit is determined by the switching element in state “0” and by the characteristics of the input stage in state “1”.

The octal input device is intended for a configuration comprising two specified external resistors per channel, as shown in **Figure 10 “Typical Application for Sensor Input Type 1, 2 and 3” on Page 19**. As a result the power dissipation within the package is at a minimum.

The voltage dependent current through the external resistor R_{EXT} is compensated by a negative differential resistance of the current sink across pins IxH and IxL, therefore input INx behaves like a constant current sink.

The comparator assigns level 1 or 0 to the voltage present at input IxH. To improve interference protection, the comparator is provided with hysteresis. A status LED is connected in series with the input circuit (R_{EXT} and current sink).

If no LED is used an external resistor of 2 kΩ (type 1 and 3) has to be connected between IxL and GNDBB. The specified switching thresholds may change if the LED is replaced by a resistor.

The internal LED drive short-circuits the status LED if the comparator detects “0”. A constant current sink in parallel with the LED reduces the operating current of the LED, and a voltage limiter ensures that the input circuit remains operational if the LED opens, but the switching thresholds may change.

For each channel an adjustable digital filter is provided which samples the comparator signal at a rate configured by programming internal registers. The digital filter is designed to provide averaging characteristics. If the input value remains the same for the selected number of sampling values, then the output changes to the corresponding state.

The µC compatible interfaces allow a direct connection to the ports of a microcontroller without the need for other components. The diagnostic logic on the chip monitors the internal data transfer as well as the sensor input supply. The information is sent via the internal coreless transformer to the pin $\overline{ERR}$ at the input interface

3.2 Power Supply

The IC contains two electrically isolated voltage domains that are independent from each other. The microcontroller interface is supplied via pin VCC, GND and the input stage is supplied via pin VBB, GNDBB. The different voltage domains can be switched on at different times. **Figure 4** shows the Start Up behaviour if both voltage domains are powered by an external power supply. If the VCC and VBB voltage have reached their operating range and the internal data transmission has been started successfully, the IC indicates the end of the Start Up procedure by setting the pin $\overline{ERR}$ to logic low. In the situation of a supply voltage drop at VBB on the Sense Side - even short - the Sense Chip requires a proper restart and therefore the µController Side control unit needs to react accordingly, especially to guarantee the integrity of the sensor data provided to the filter stage.

3.2.1 Voltage Limits on VBB

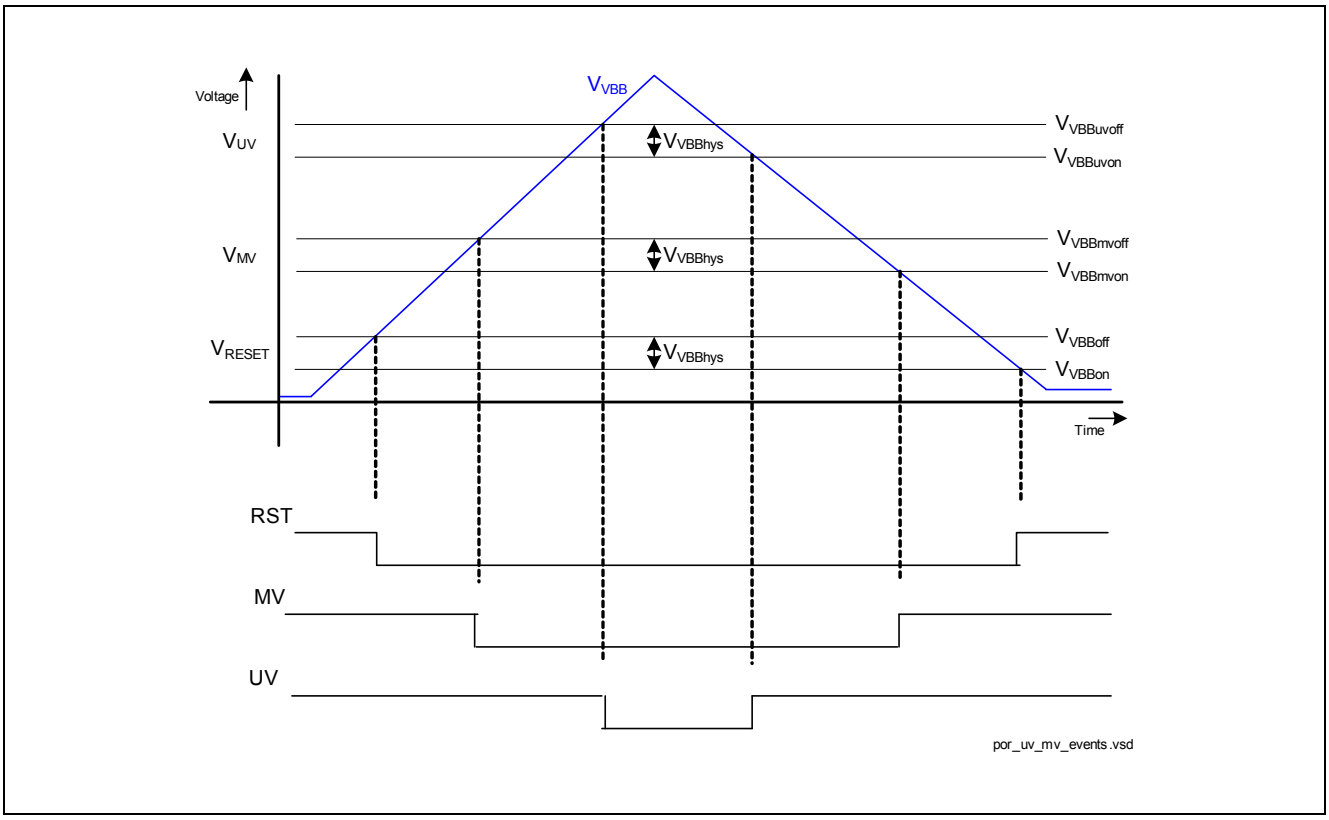


Figure 3 Start Up Procedure with external Power Supply

During UVLO, all registers are reset to their reset values as specified in the **Chapter 6.2**. As a result, the flags TE, UV as well as MV are High and the $\overline{ERR}$ pin is Low (error condition). Immediately after the reset is released, the IC is first configured by “reading“ the logic level of the SEL, MS1, MS0 (when available). The IC powers up as a serial device (SEL has a pull-up resistor).

The supply voltage VBB is monitored during operation by two internal comparators (with typ. 8 µs blanking time @ 500kHz $f_{scantyp}$) detecting:

- VBB Undervoltage: If the voltage drops below the UV threshold (see **Table 7**), the UV-bit in the **GLERR** register is set High. The IC remains in normal operation.
- VBB Missing Voltage: If the voltage further drops below the MV threshold, lower than the previous threshold, the MV-bit in the **GLERR** register is set, the Sense Side of the IC is turned off when reaching the V_{RESET} threshold whereas the Micro-Controller Side remains active.

These 2 thresholds are inactive when the IC operates in Self Power Mode i.e. when the DC_ENA pin is High.

Note: In case DC_ENA is High the integrated DC/DC driver is active. The driver stage is self-protected in overload condition: the internal switches will be turned off as long as the overcurrent condition is detected and the IC will automatically restart once the overload condition disappears.

Important: Since the UV and MV (as well as the TE and W4S) bits used for generating the $\overline{ERR}$ signal are preset to High during UVLO, the $\overline{ERR}$ pin is Low after power up. Therefore the $\overline{ERR}$ signal requires to be explicitly cleared after power up. At least one read access to the GLERR and INTERR registers is needed to update those status bits and thus release the $\overline{ERR}$ pin.

3.2.2 External Supply

Figure 4 shows the Start Up behaviour if both voltage domains are powered by an external power supply. If the VCC and VBB voltage have reached their operating range and the internal data transmission has been started successfully, the IC indicates the end of the Start Up procedure by setting the pin $\overline{ERR}$ to logic low.

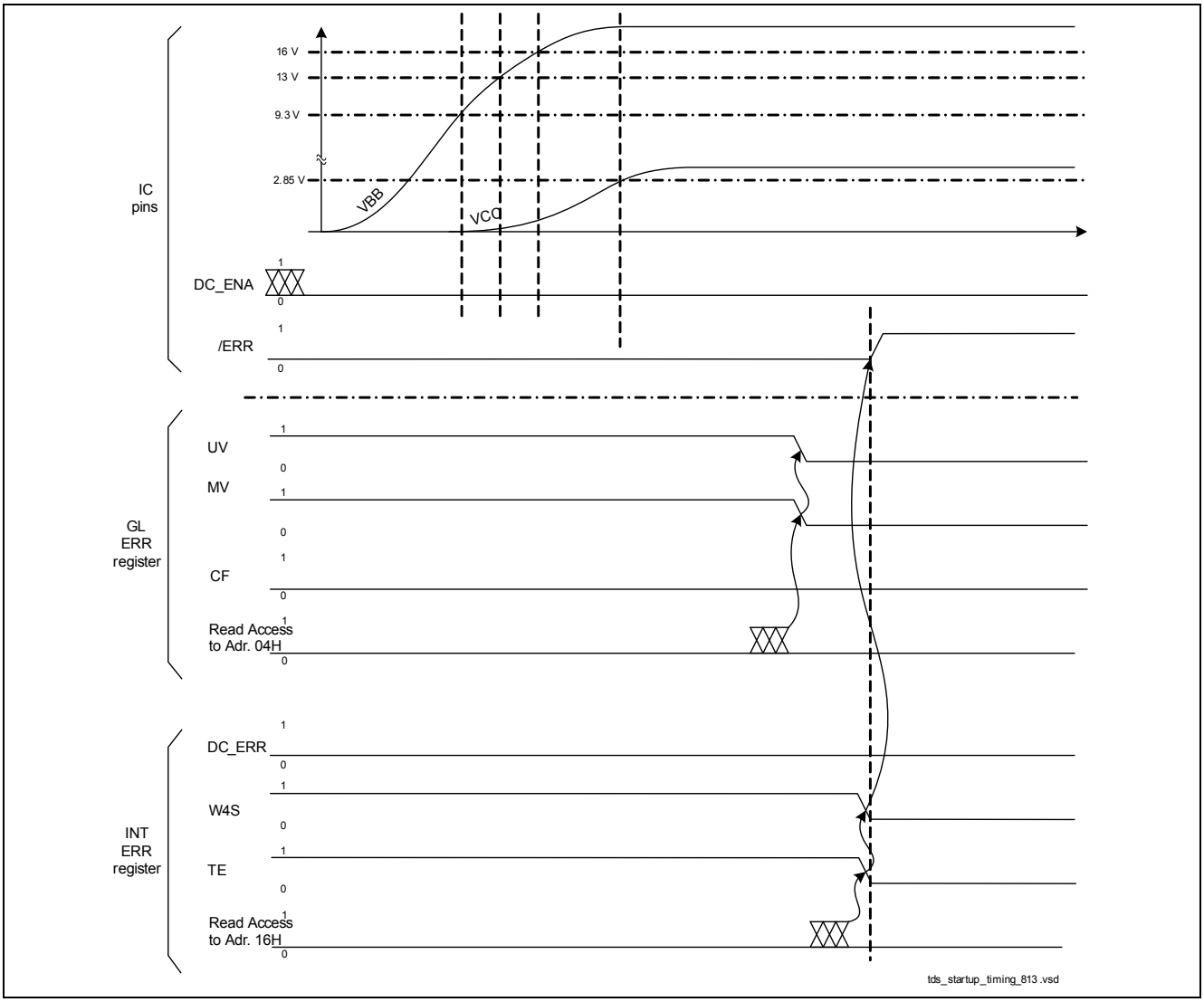


Figure 4 Start Up procedure with external power supply

3.2.3 DC/DC Supply

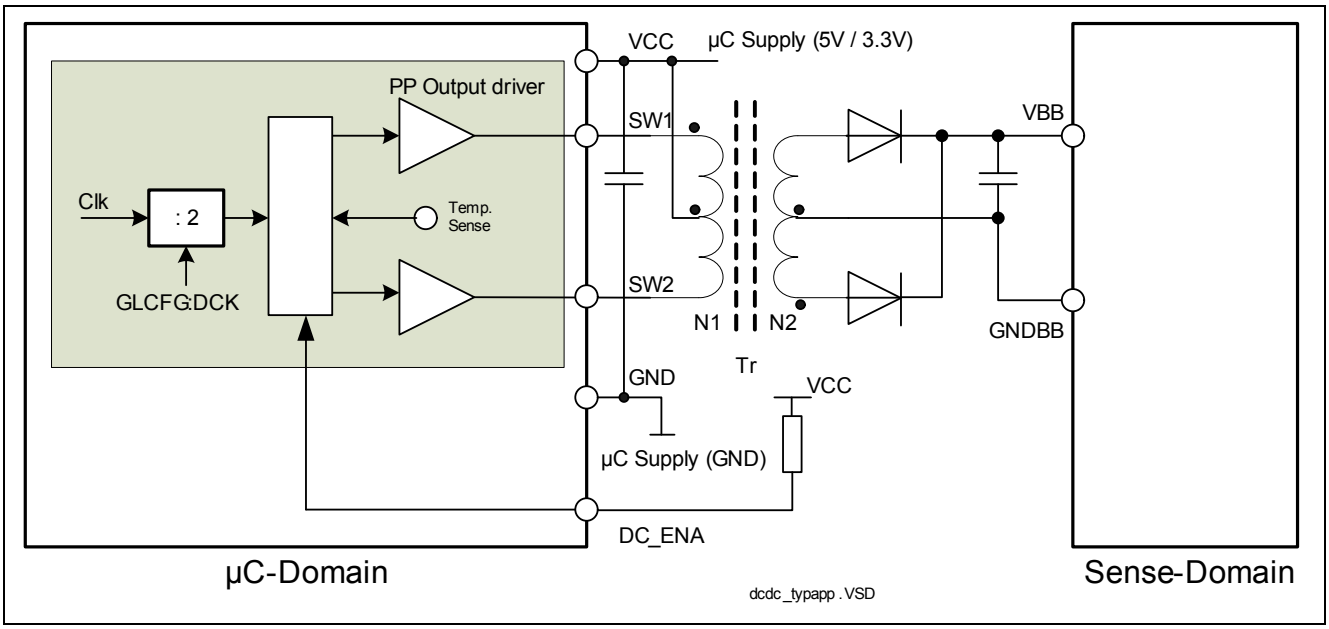


Figure 5 Typical Circuitry for Self Powered Mode with Push-Pull Converter

The IC can as well operate in self powered mode. In this case, the Process Side (Sense-Domain) can be supplied at VBB with an isolated push-pull converter connected to the Micro-controller Side and driven by the pins SW1 and SW2 . The internal driver stage at SW1 and SW2 is designed to power up two ISO1I813T (refer to **Table 8**). The DC/DC-Converter is driven by the internal clock. Parameters are calculated with the internal clock of 500 kHz. By setting the DCK Bit in the GLCFG register a prescaler by 2 can be activated. Should the user adjust the internal clock to a different frequency the transformer has to be adjusted accordingly.

The short-circuit protection uses a temperature sensor located close to the drivers and disables the driver stages when a predefined temperature is reached (**Figure 7**, **Figure 5**). The target value for the switch-off-temperature is 160°C with a hysteresis of < 10°C. That means that the drivers are switched off at a junction temperature of 160 °C and switched on at a junction temperature of <=150°C

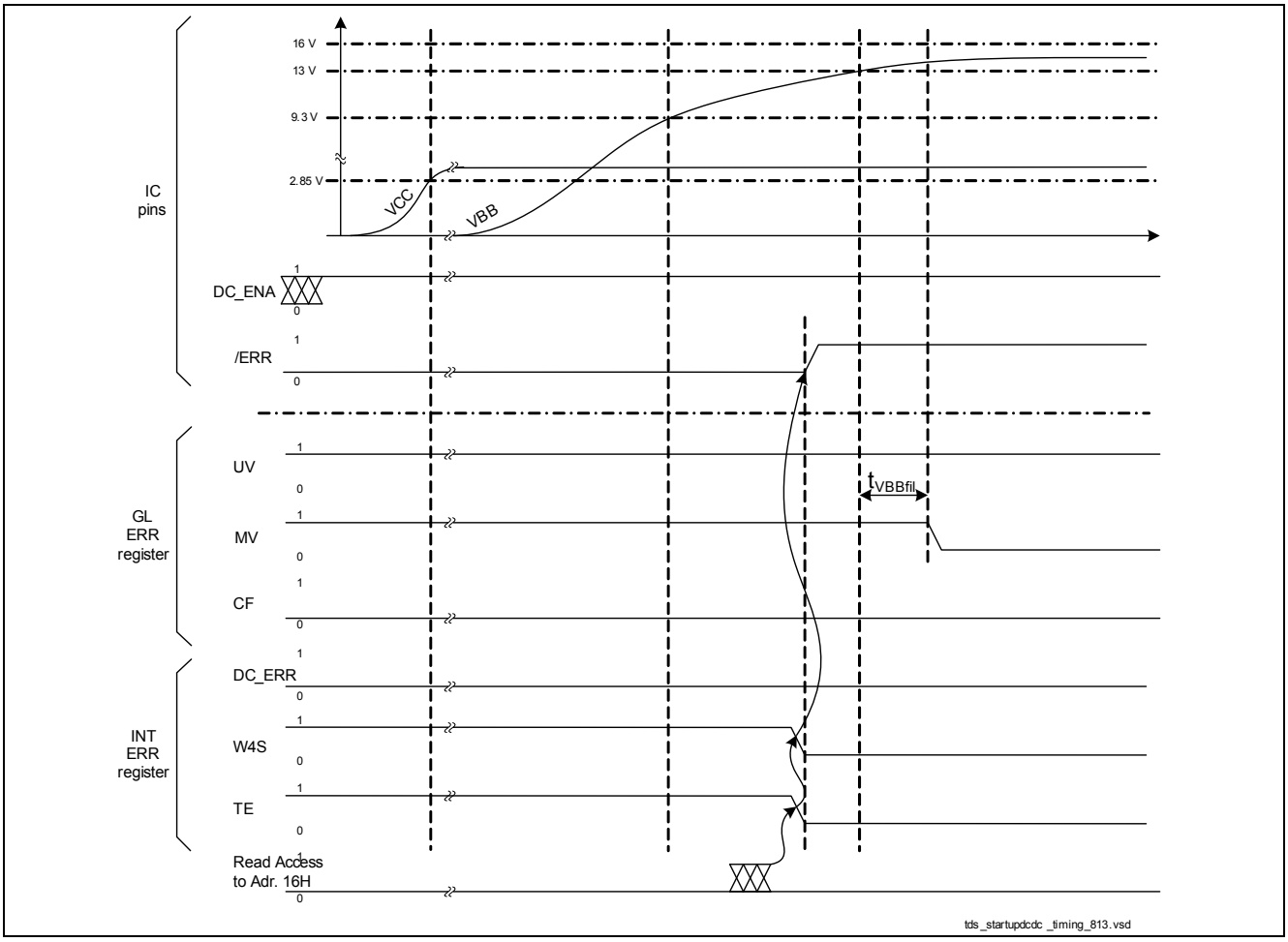


Figure 6 Start Up Procedure with DC/DC Supply

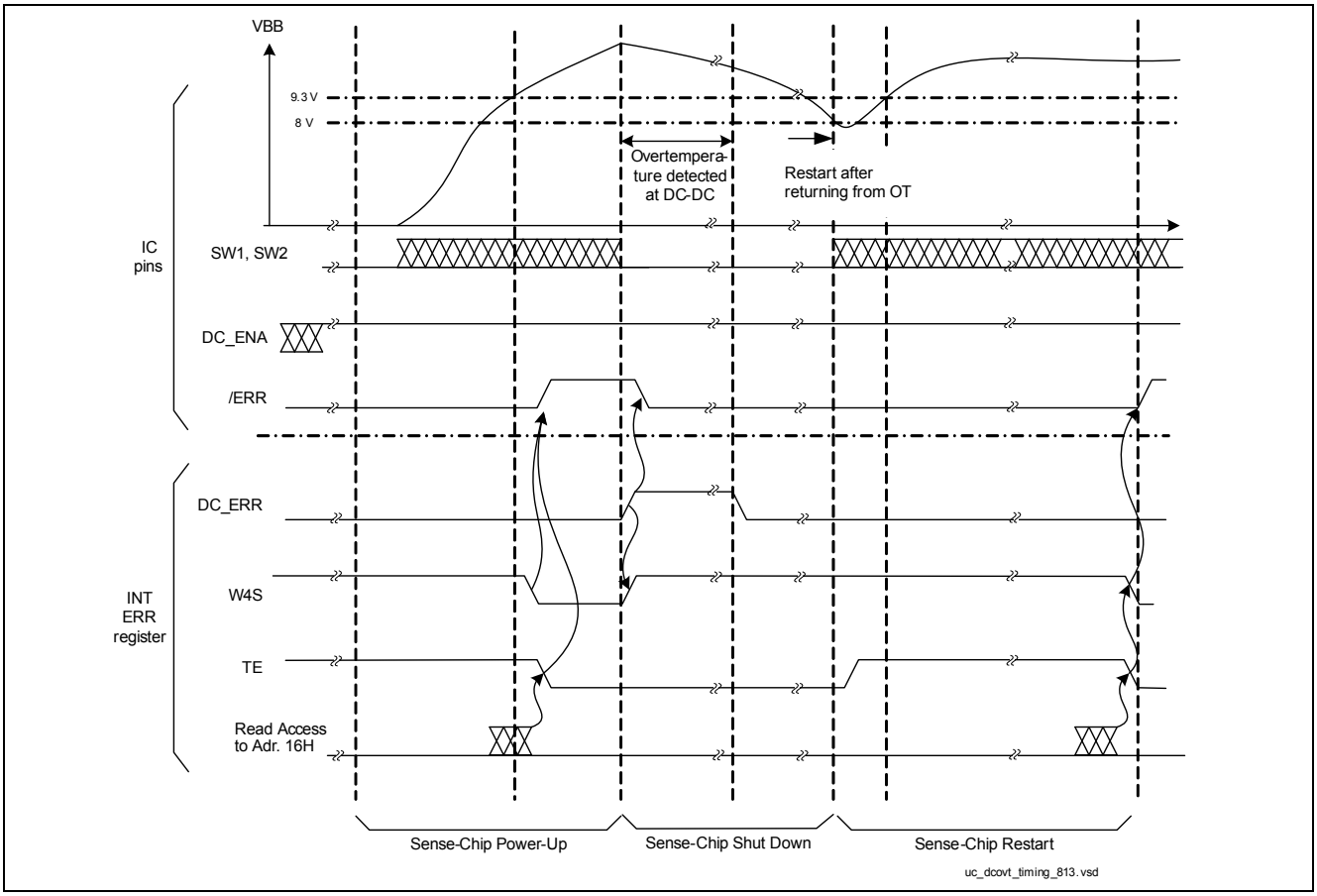


Figure 7 Restart Procedure after VBB drop due to DC/DC Supply Overtemperature

3.3 Internal Oscillator

An external resistor has to be connected to Rosc and allows the adjustment of the frequency as shown in **Figure 8**.

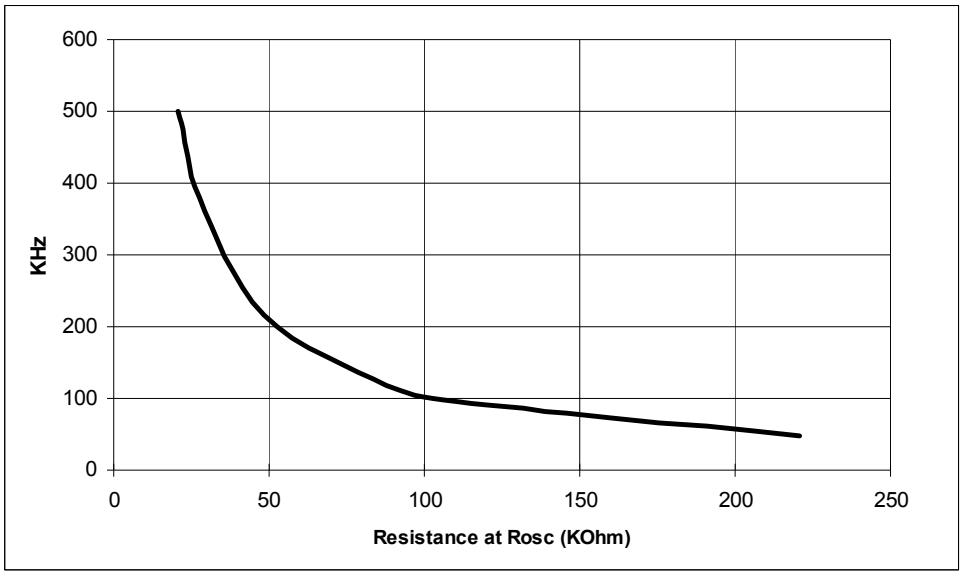


Figure 8 Internal Frequency Setting at Rosc

The internal oscillator provides the scan clock for the sampling of the sensor data and diagnostics as well as for the internal digital averaging filters. Therefore the filter times as defined in the **Table 11** for the typical frequency of 500 KHz will change accordingly. As an example, it is possible to define filter time longer than 20 ms by reducing the internal oscillator frequency.

Moreover, in the applications where the IC current consumption is critical, it is possible to reduce the internal oscillator frequency by increasing the R_{OSC} (see **Figure 9**).

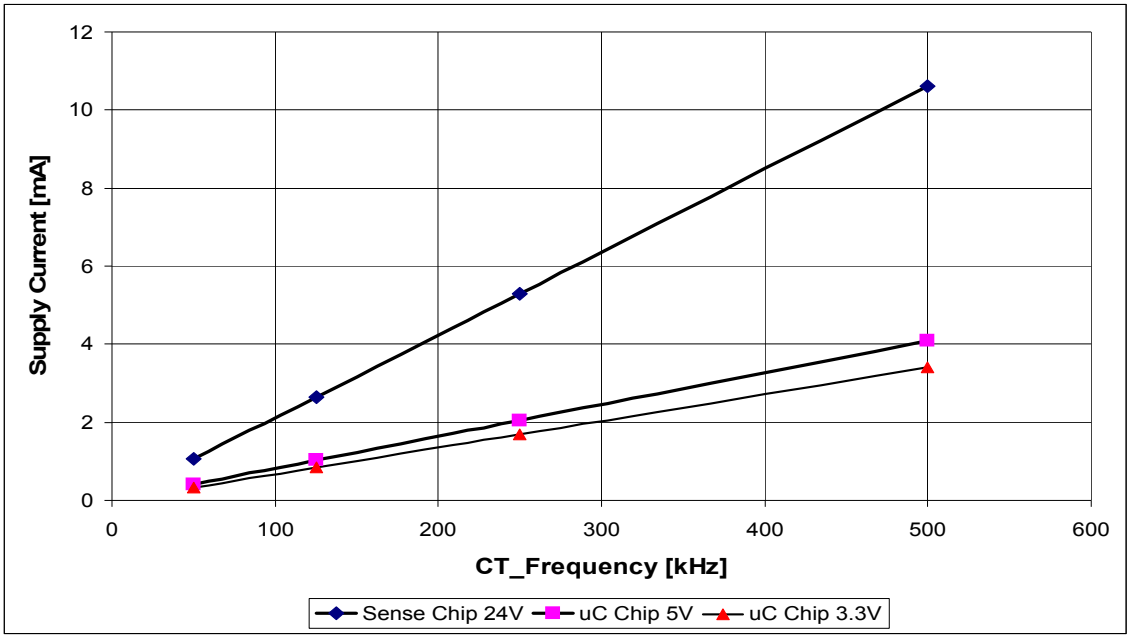
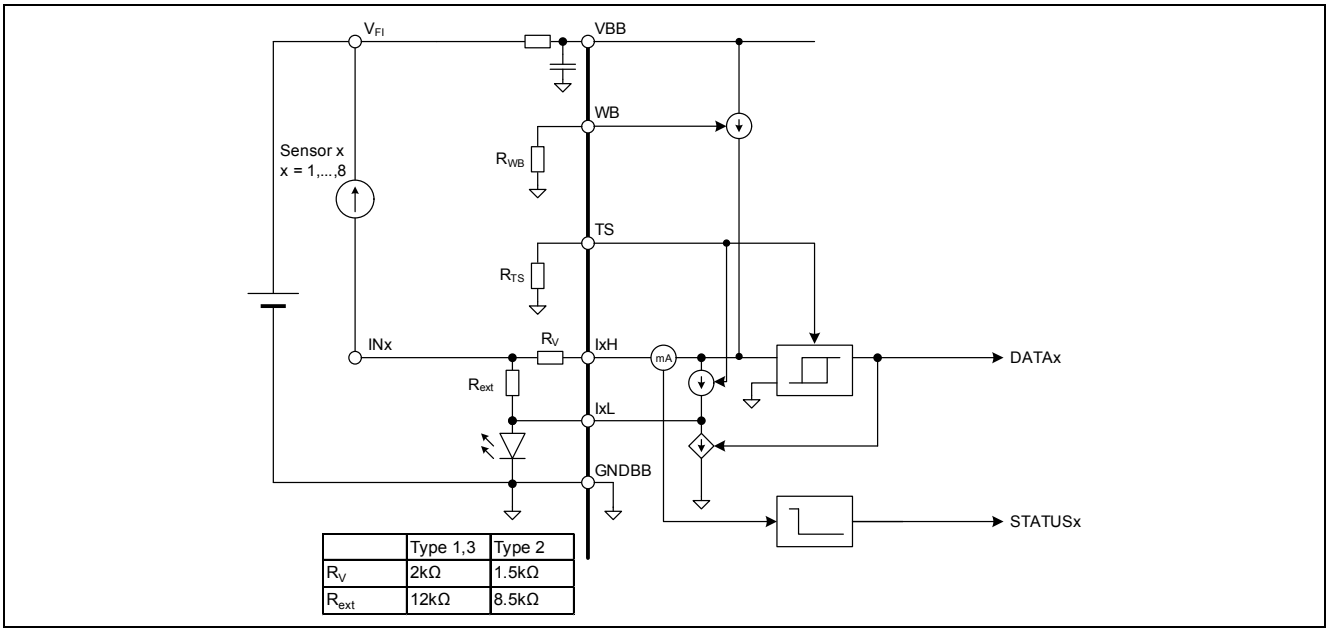


Figure 9 IC Current Consumption in function of the internal frequency

3.4 Sensor Input

3.4.1 Input Type Select

The sensor input structures are shown in **Figure 10** (Type 1,2,3). Due to its active current a V-I-characteristic as shown in **Figure 11** is maintained. This V-I-curve is well within the IEC 61131 standard requirements of Type 1, Type 2 and Type 3 sensors, respectively. The **Figure 12** shows the typical application for sensor of type 2. It is recommended to choose for the external resistors R_{EXT}, R_V, R_{LED} an accuracy of 2 % (< 5% is mandatory) otherwise the V/I-characteristic shown in **Figure 11** cannot be guaranteed.



	Type 1,3	Type 2
R_V	2kΩ	1.5kΩ
R_{ext}	12kΩ	8.5kΩ

Figure 10 Typical Application for Sensor Input Type 1, 2 and 3

The filtered input-data information is visible in the Input Channel Data Register : **INPDATA** and is also described by the nomenclature : input-data.

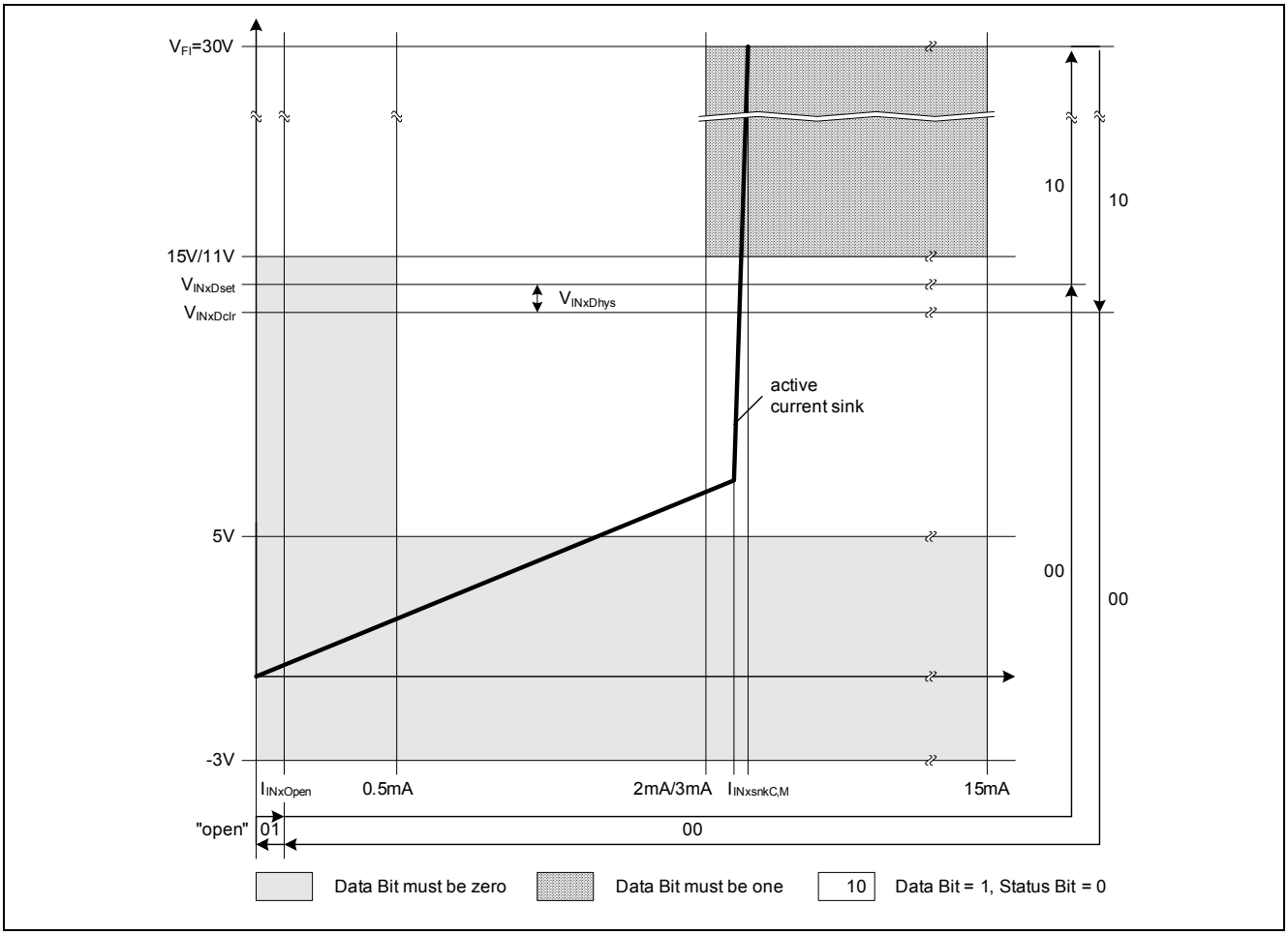


Figure 11 Sensor Input Characteristics

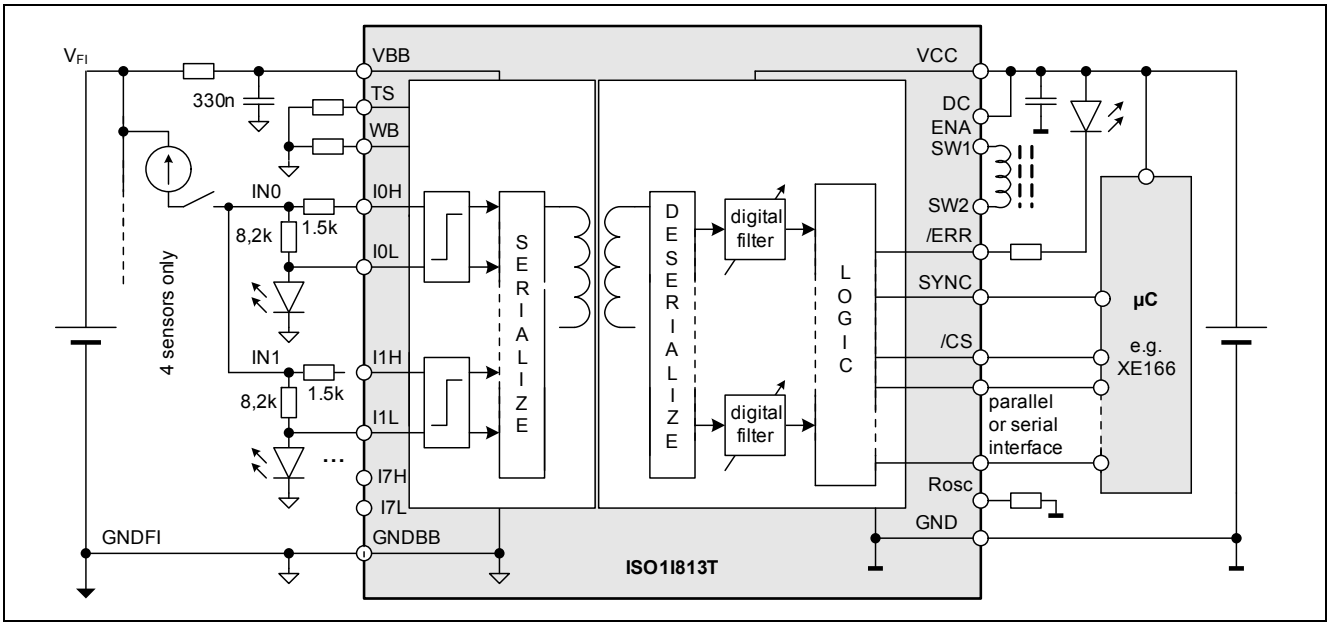


Figure 12 Typical Application for Sensor Type 2

3.4.2 Wire Break Detection

The wire-break current can be adjusted by the R_{WB}-resistor value connected to the pin WB (**Figure 13**). The minimum wirebreak-current can be choosen only when a LED- or Zener-Diode is connected to the pin IxL with a forward current in the range of few uA in the voltage range below 1 V. In the case of a connected resistor at IxL a large current is flowing across the external resistor Rext and the IxL-resistor (R_{LED}). This part cannot be measured internally and has to be added to the internal current part. In this case the minimum adjustable current is 230uA (R_{LED} = 2kOhm). The WB bits in the status register have a sticky (latched) property and remains set as long as they are not cleared by a read access and the fault condition is not detected anymore.

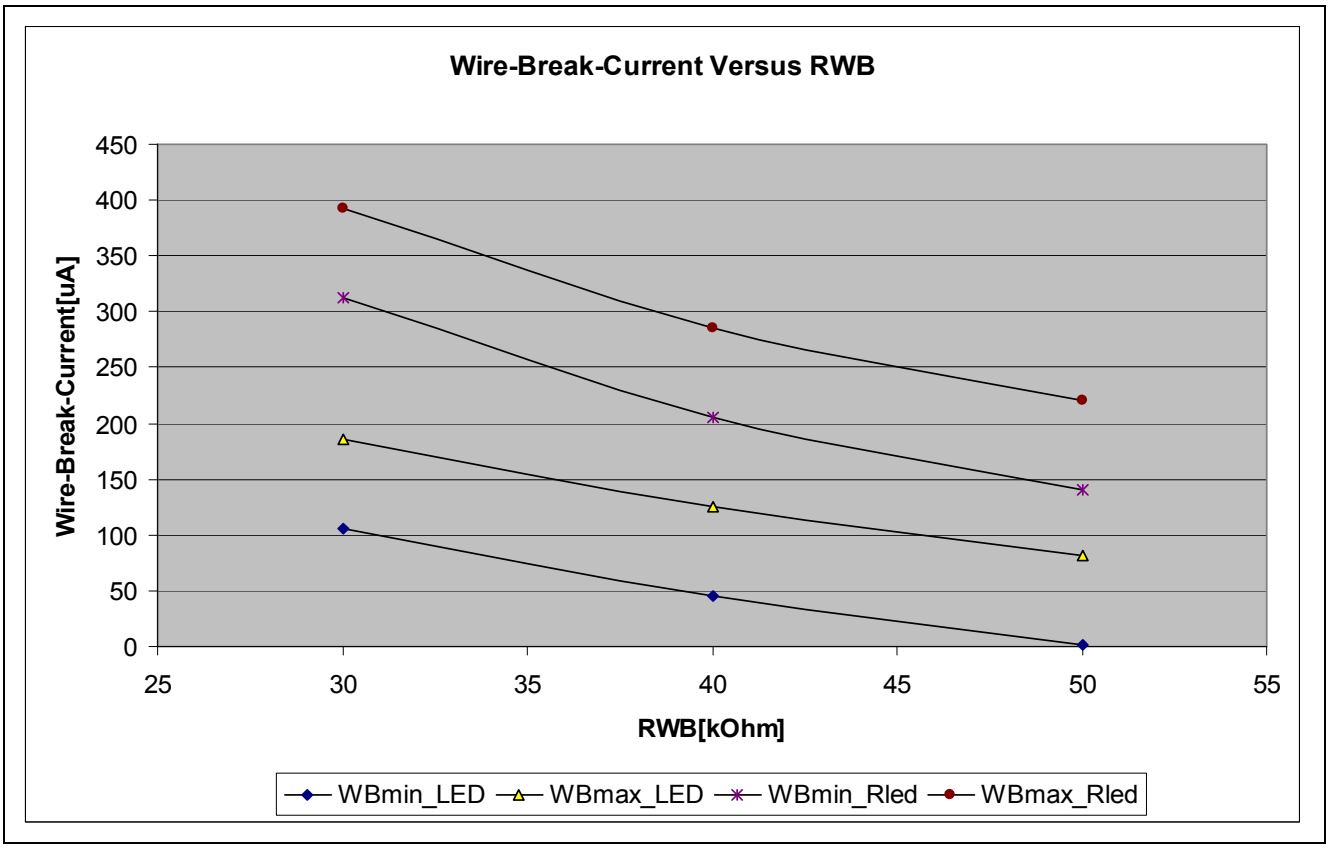


Figure 13 Wire Break Detection for Type 1,3 (typ. @ 25°C)

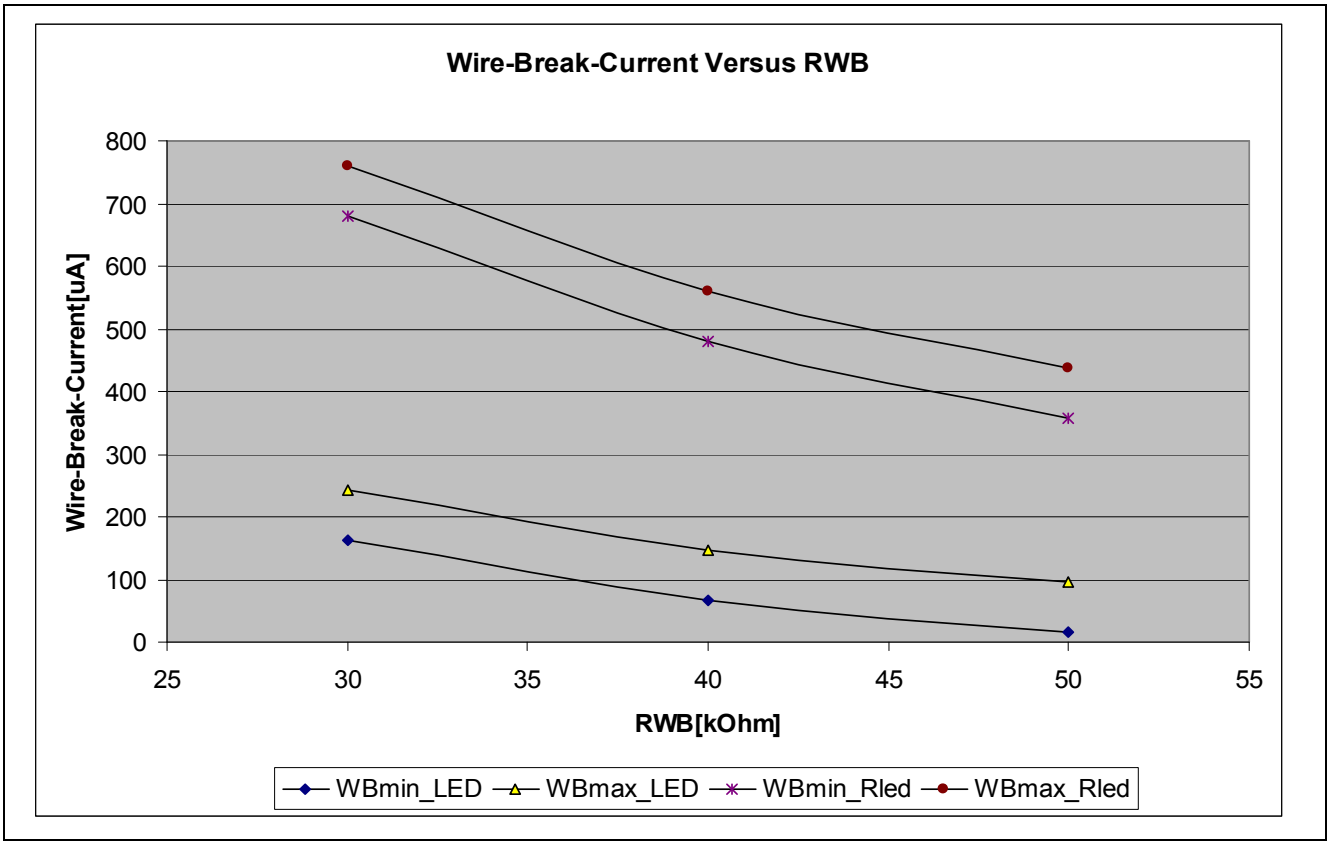


Figure 14 Wire Break Detection for Type 2 (typ. @ 25°C)

In the case of Type 2 two sense inputs are switched in parallel to achieve 2 * 3 mA (**Figure 12**). In each sense input a mimimum wirebreak current of 60 µA can be measured which means in sum a minimum wirebreak current of 120 µA. It is not recommended to use external resistors at the pins IxL in case of wirebreak measurements. The recommended value would be R_{LED} = 1.2 kΩ which has been choosen in order not to produce a large voltage drop between IxL and GNDBB which in turn would limit the voltage drop across the sink. The low value of R_{LED} would cause a high external current in case of wirebreak-measurements which has to be multiplied by two due to the parallel circuitry of the sense inputs.

The filtered wirebreak-diagnosis is visible in the Collective Diagnostic Register : **DIAG** and is also described by the nomenclature: status.

3.5 Common Error Output

The input (VBB) undervoltage and missing voltage status which are transmitted via the integrated coreless transformer to the output block and the internal data transmission monitoring information are evaluated in the common error output block, see **Figure 15**. In self-powered mode, extra information in case of over-current at SW1/2 is evaluated as well.

In case of an internal data transmission error the data and status bits are replaced by the last valid transmission. Moreover, if four consecutive erroneous data transmissions (TE1=1) occur, an internal error signal (TE4=1) is set. The averaging filters are reset and this status is held until four consecutive error-free transmissions (TE1=0) occur. An example timing diagram is shown in **Figure 15**.

This internal error signal is OR-wired with the current VBB undervoltage and missing voltage status. Additionally in the ISO1I813T, the Collective Diagnostics flag is combined in the $\overline{ERR}$. Since the output error signal is active-Low, the OR-wired result is negated.

Functional Description

In the Self Powered mode, the UV and MV are masked out. Instead the DC_ERR bit of the register **INTERR** is combined with the Transmission Error signal and output at the pin $\overline{ERR}$.

The output stage at pin $\overline{ERR}$ has an open drain functionality with a pull-up resistor. See **Table 13** for the electrical characteristics.

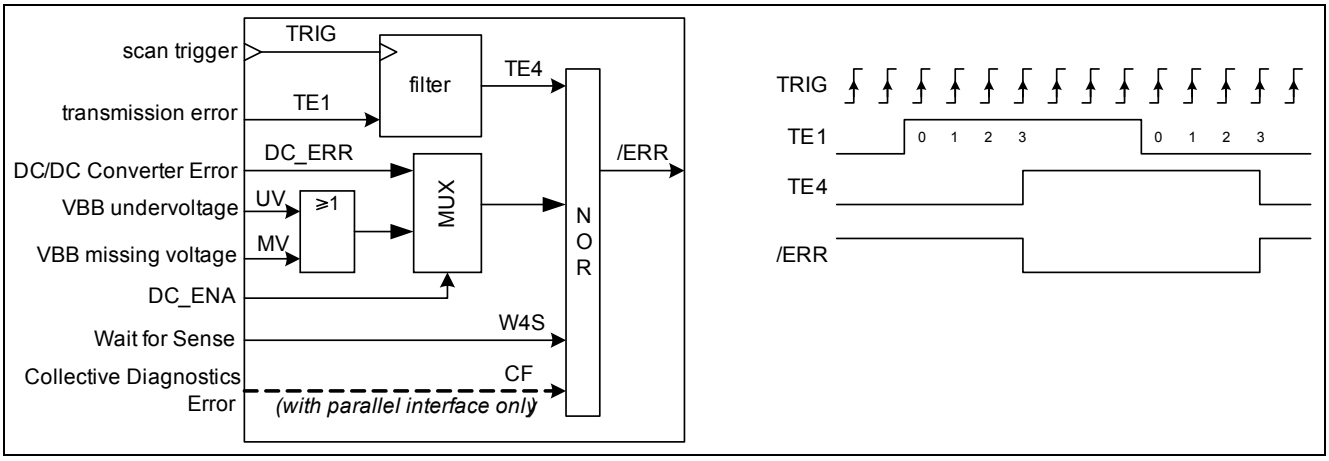


Figure 15 Common Error Output

3.6 Programmable Digital Input Filter

The sensor data and diagnosis bits of each input channel can be filtered by a configurable digital input filter. If selected, the filter changes its output according to an averaging rule with a selectable average length. When the sensor state changes without any spikes and noise the change is delayed by the averaging length. Sensor spikes that are shorter than the averaging length are suppressed. **Figure 16** shows the behaviour of the filter. The clock of the Digital Filter is supplied from the internal oscillator. Therefore the filtertime depends on the oscillator frequency setting. For the filtering times of 1.6 msec , 3.2 msec , 10 msec , 20 msec a prescaler was used. Therefore the update interval was choosen to be 4 usec, 8 usec, 64 usec , 64 usec respectively (based on 500 kHz clock).

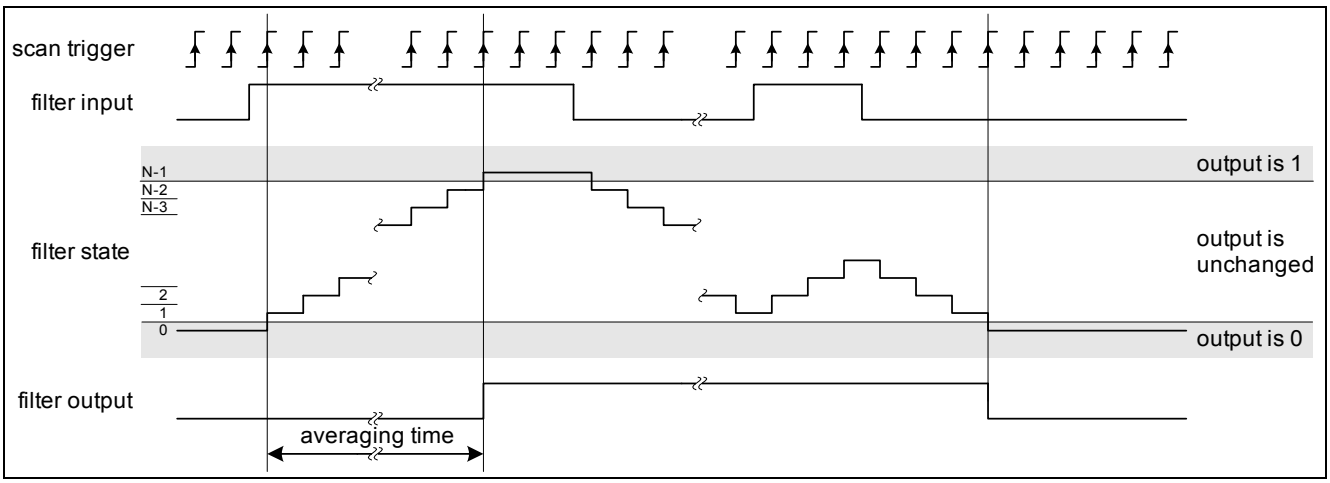


Figure 16 Digital Filter Behavior

The averaging length is selected for each channel individually using the configuration registers **COEFIL0-7**. The programmed filter time apply for both the data and the diagnostics of one channel. See **Table 11** for the different setting options including filter bypass.

Figure 17 and **Table 17** describe the timing for changing filter-coefficients. Especially timing restrictions have to be obeyed implying a minimal processing time until the new configuration and the filtered data are valid and can e.g. be frozen with the pin SYNC. Changing the filter coefficients means resetting always the related filter.

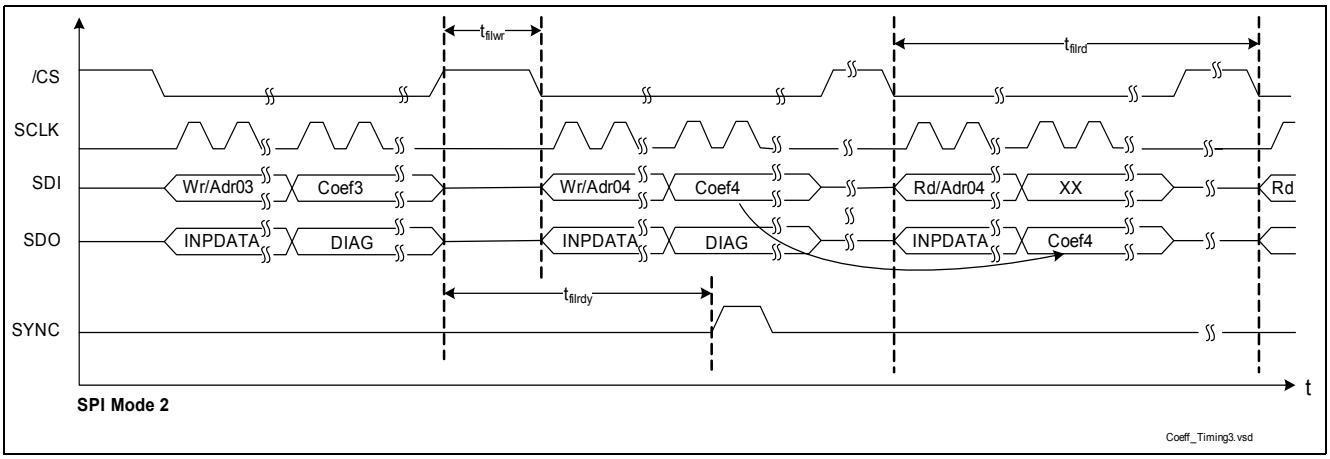


Figure 17 Filter Time Programming and Update Timing

Whereas the absolute filter time depends on the internal oscillator frequency accuracy, the maximal jitter per channel of the IC is 1.5 %. The channel jitter defined in the **Figure 18** is due to the sampling error of the sensor data with the internal clock and applies equally for all the channels.

Furthermore, a fixed propagation delay has to be taken into account due to the data transmission over the Coreless Transformer.

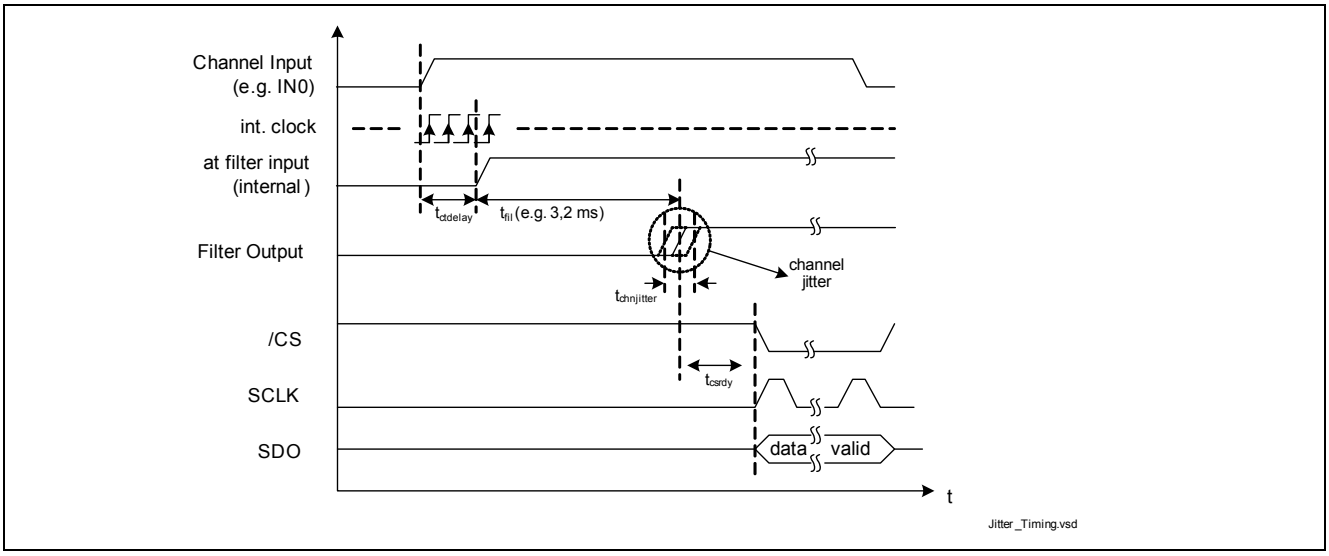


Figure 18 Channel Jitter Definition