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ISOFACE™

ISO2H823V2.5

Galvanic Isolated 8 Channel High-Side Switch

Datasheet

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Power Management & Multimarket

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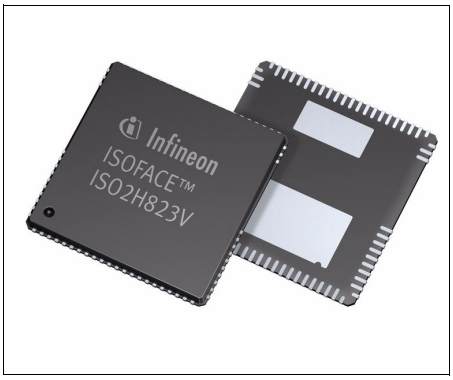
1 Overview



PG-VQFN-70-2

Infineon Technologies 2nd generation ISOFACE™ 8-channel high-side driver IC ISO2H823V2.5 offers integrated 2.5kV galvanic isolation, thus meets the IEC 61131-2 requirements for reinforced isolation. Concurrently, the ISO2H823V2.5 sets a new standard for system-level diagnostics. Each of the 8 channels is equipped with 5-fold diagnostic monitoring capabilities: Open Load (Active Mode - Driver On and Inactive Mode - Driver Off) , Short-to-Vbb, Overcurrent (= Short-to-GND), Overtemperature.
With the ever increasing level of complexity and integration in industrial control systems comprehensive diagnostic monitoring is highly valuable in a vast range of industrial applications, both for preventive maintenance as well as to shorten costly un-scheduled down-times

Product Highlights

- 2.5 kV Galvanic isolation integrated (UL508 & CSA22.2 certified)
  Meets IEC 61131-2 requirements for reinforced isolation
- 8 - channel high-side switches of 0.6 A each
- 5 different types of diagnostic feedback for each channel
- µController compatible 8-bit parallel/serial interface
- 12 mm x 12 mm PG-VQFN-70-2 package

Key Features

- Interface 3.3V CMOS operation compatible
- Parallel/Serial µC interface
- High common mode transient immunity
- Integrated Diagnostics:
  – 5 different types for diagnostic feedback per output channel
  – 5 types of diagnostic feedback on global level
- Common output disable pin
- Common error indication pin
- Resynchronization to achieve a low-jitter switching on and off of high-side switches
- Active output current limitation for short circuit protection
- Reverse Output Voltage protection
- Undervoltage shutdown with autorestart and hysteresis
- Integrated clamping to switch inductive loads up to 150 mJ energy per channel
- Thermal shutdown and diagnostics per channel with auto-restart
- V_{BB} range from 11 V to 35 V designed for 24 V systems

Type	Package
ISO2H823V2.5	PG-VQFN-70-2

- ESD protection
- RoHS compliant

Typical Application

- Isolated switch for industrial applications:
  PLC, distributed control systems, industial PCs, robotics, etc.
- All types of resistive, inductive and capacitive loads
- µController compatible power switch for 24 V DC applications
- Driver for solenoid, relays and resistive loads

Description

The ISO2H823V2.5 is a galvanically isolated 8-bit data interface in PG-VQFN-70-2 package that provides 8 fully protected high-side power switches that are able to handle currents up to 730 mA per channel.

An 8-bit parallel µController compatible interface or a serial SPI-interface allows to connect the IC directly to a µController system. The input interface supports also a direct control mode for writing driver information and is designed to operate with 3.3 V CMOS compatible levels.

The data transfer from input to output side is realized by the integrated Coreless Transformer Technology.

This product is the second generation of isolated 8 channel digital output device (ISO2H823V2.5) and provides a robust integrated diagnosis for switches with low R_{DSon} as well as an upgraded µController interface.

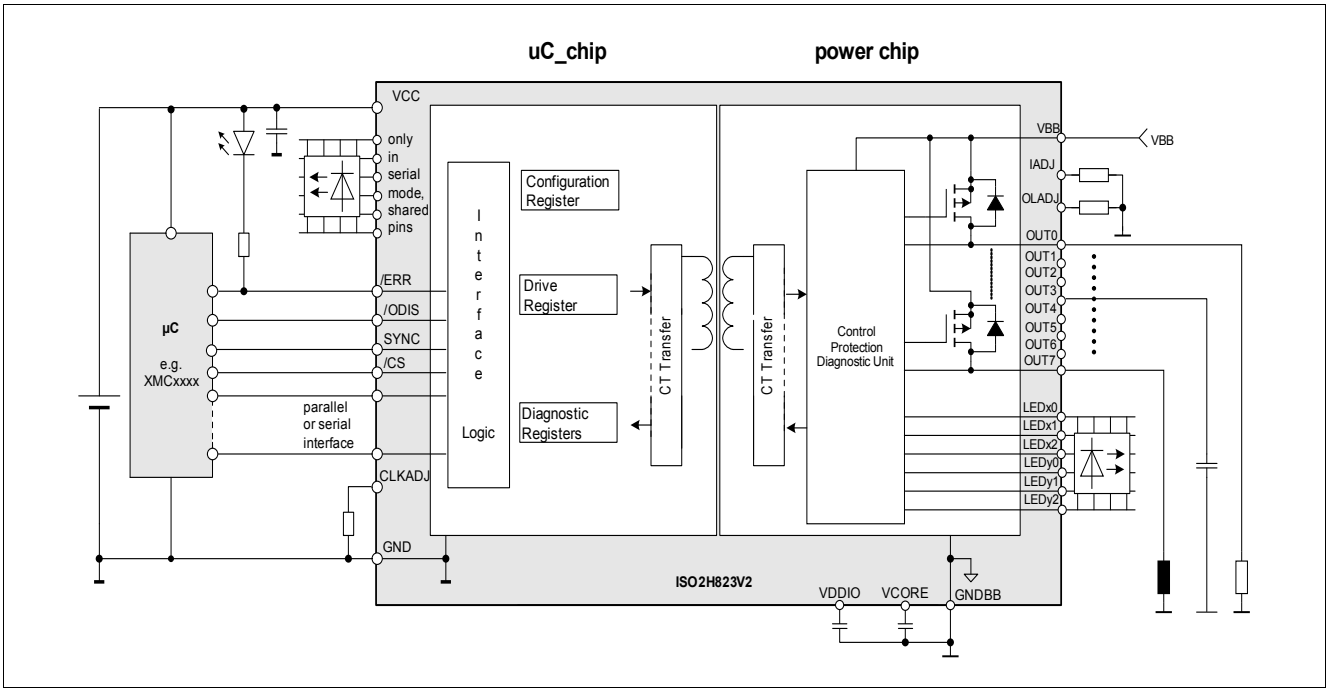


Figure 1 Typical Application

Infineon Ordering Code :

SP001225470

2 Pin Configuration and Functionality

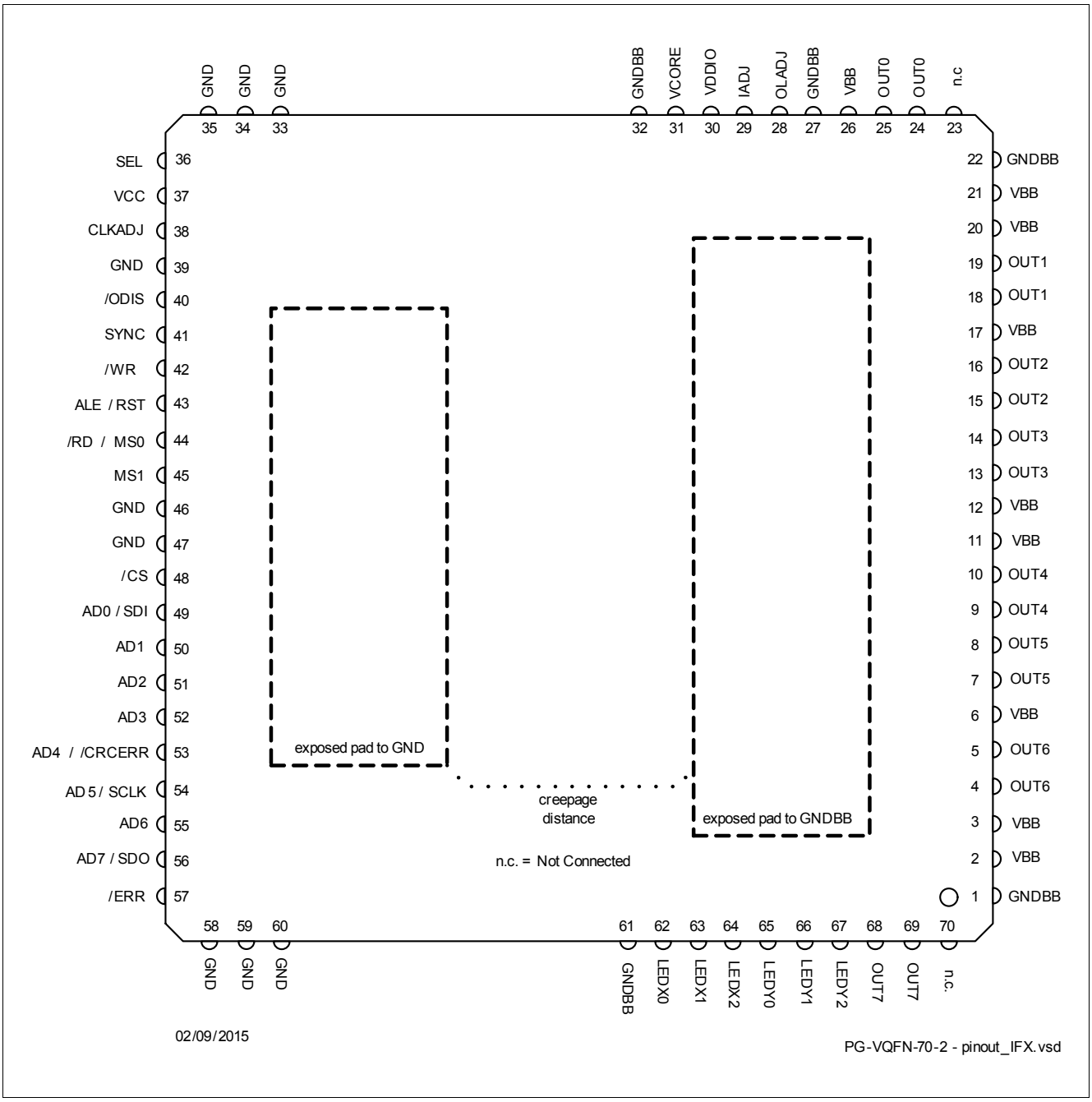


Figure 2 Power PG-VQFN-70-2 (430 mil)

Table 1 Pin Configuration

Pin	Parallel Interface Mode				Serial Interface Mode			
	Symbol	Ctrl [1]	Type [2]	Function	Symbol	Ctrl	Type	Function
top side pins								
1	GNDBB		A	Output Stage Ground	GNDBB			
2	VBB		A	Output Stage Positive Supply	VBB			
3	VBB		A	Output Stage Positive Supply	VBB			
4	OUT6		A	Switch Output 6	OUT6			
5	OUT6		A	Switch Output 6	OUT6			
6	VBB		A	Output Stage Positive Supply	VBB			
7	OUT5		A	Switch Output 5	OUT5			
8	OUT5		A	Switch Output 5	OUT5			
9	OUT4		A	Switch Output 4	OUT4			
10	OUT4		A	Switch Output 4	OUT4			
11	VBB		A	Output Stage Positive Supply	VBB			
12	VBB		A	Output Stage Positive Supply	VBB			
13	OUT3		A	Switch Output 3	OUT3			
14	OUT3		A	Switch Output 3	OUT3			
15	OUT2		A	Switch Output 2	OUT2			
16	OUT2		A	Switch Output 2	OUT2			
17	VBB		A	Output Stage Positive Supply	VBB			
18	OUT1		A	Switch Output 1	OUT1			
19	OUT1		A	Switch Output 1	OUT1			
20	VBB		A	Output Stage Positive Supply	VBB			
21	VBB		A	Output Stage Positive Supply	VBB			
22	GNDBB		A	Output Stage Ground	GNDBB			
23	n.c.	not connected			n.c.	not connected		
24	OUT0		A	Switch Output 0	OUT0			
25	OUT0		A	Switch Output 0	OUT0			
26	VBB		A	Output Stage Positive Supply, Supply of Reference Voltages	VBB			
27	GNDBB		A	Output Stage Ground	GNDBB			

Table 1 Pin Configuration (cont'd)

Pin	Parallel Interface Mode				Serial Interface Mode			
	Symbol	Ctrl [1]	Type [2]	Function	Symbol	Ctrl	Type	Function
28	OLADJ		A	Open Load Adjust	OLADJ			
29	IADJ		A	Current Reference Adjust	IADJ			
30	VDDIO		A	CT Blocking Capacitor	VDDIO			
31	VCORE		A	Digital Core Supply	VCORE			
32	GNDBB		A	Output Stage Ground	GNDBB			
gap used for creepage distance								
33	GND		A	Logic Ground	GND			
34	GND		A	Logic Ground	GND			
35	GND		A	Logic Ground	GND			
36	SEL	I	PD	Serial / Parallel Mode Select	SEL			
37	VCC		A	Positive 3.3 V logic supply	VCC			
38	CLKADJ		A	Clock Frequency Adjustment	CLKADJ			
39	GND		A	Logic Ground	GND			
40	$\overline{\text{ODIS}}$	I	PD	Output Disable	$\overline{\text{ODIS}}$			
41	SYNC	I	PU	Synchronize and Freeze Diagnostics	SYNC			
42	$\overline{\text{WR}}$	I	PU	Data Write Input	n.c.	high impedance "Z"		
43	ALE/RST	I	PD	Address Latch Enable / Reset	RST	I	PD	Reset
44	$\overline{\text{RD}}$	I	PU	Data Read Input	MS0	I	PD	SPI Mode Select bit 0
45	n.c.			not connected	MS1	I	PD	SPI Mode Select bit 1
46	GND		A	Logic Ground	GND			
47	GND		A	Logic Ground	GND			
48	$\overline{\text{CS}}$	I	PU	Chip Select	$\overline{\text{CS}}$			
49	AD0	IO	PPZ	Addr-Data in/output bit0	SDI	I	PD	SPI Data input
50	AD1	IO	PPZ	Addr-Data in/output bit1	n.c.			high impedance "Z"
51	AD2	IO	PPZ	Addr-Data in/output bit2	n.c.			high impedance "Z"
52	AD3	IO	PPZ	Addr-Data in/output bit3	n.c.			high impedance "Z"
53	AD4	IO	PPZ	Addr-Data in/output bit4	$\overline{\text{CRCERR}}$	OD	PU	CRC Error output
54	AD5	IO	PPZ	Addr-Data in/output bit5	SCLK	I	PD	SPI Shift Clock input
55	AD6	IO	PPZ	Addr-Data in/output bit6	n.c.			high impedance "Z"
56	AD7	IO	PPZ	Addr-Data in/output bit7	SDO	O	PPZ	SPI Data Output
57	$\overline{\text{ERR}}$	OD	PU	Fault indication	$\overline{\text{ERR}}$			
58	GND		A	Logic Ground	GND			
59	GND		A	Logic Ground	GND			
60	GND		A	Logic Ground	GND			
gap used for creepage distance								

Table 1 Pin Configuration (cont'd)

Pin	Parallel Interface Mode				Serial Interface Mode			
	Symbol	Ctrl [1]	Type [2]	Function	Symbol	Ctrl	Type	Function
61	GNDBB		A	Output Stage Ground	GNDBB			
62	LEDX0		A	LED Output Row 0	LEDX0			
63	LEDX1		A	LED Output Row 1	LEDX1			
64	LEDX2		A	LED Output Row 2	LEDX2			
65	LEDY0		A	LED Output Column 0	LEDY0			
66	LEDY1		A	LED Output Column 1	LEDY1			
67	LEDY2		A	LED Output Column 2	LEDY2			
68	OUT7		A	Switch Output 7	OUT7			
69	OUT7		A	Switch Output 7	OUT7			
70	n.c.	not connected			n.c.	not connected		

1) Direction of the digital pins : I = input, O = output, IO = Input/Output

2) Type of the pin: A = analog, OD = Open-Drain, PU = internal Pull-Up resistor, PD = internal Pull-Down resistor, PPZ = Push-Pull pin with High-Impedance functionality

In case of serial mode six pins can be used to drive a LED-matrix on the uC-side (**Table 2**). For this purpose the bit LEDON in register GLCFG has to be set to "1".

Table 2 Pin Configuration for LED-Application on the uC-Side

Pin	Serial Interface Mode			
	Symbol	Ctrl	Type	Function
top side pins				
55	AD6		OD	LEDR0
52	AD3		OD	LEDR1
51	AD2		OD	LEDR2
42	$\overline{WR}$		OD	LEDC0
43	ALE/RST		OD	LEDC1
50	AD1		OD	LEDC2

2.1 Pin Functionality

This section describes the pins of the µController Interface as well as the Process Interface.

2.1.1 Pins of Power Interface

VBB (Positive supply 11-35 V output stage)

V_{BB} supplies the output stage. An external circuitry for reverse polarity protection is required (see Electrical Characteristics).

A ceramic capacitor of minimum 2.2 µF must be connected between VBB and GNDBB.

GNDBB (Ground for VBB domain)

This pin acts as the ground reference for the output stage that is supplied by V_{BB}.

OUT0... OUT7 (Output channel 0 ... 7)

Due to EMI-requirements (Radio-Frequency-Common-Mode and burst-application) a capacitor of min.10 nF (±10%, recommended value 12 nF ± 10%) for each output pin has to be connected to GNDBB.

LEDX0... LEDX2 (LED Row output channel 0 ... 2)

Low side switches

LEDY0... LEDY2 (LED Column output channel 0 ... 2)

High side drivers

IADJ (Current Adjust)

Reference current input, must be connected to GNDBB through a reference resistor of typ. 6.81 KΩ (E96 series). The DC-level V_{IADJ} is 1.215 V.

OLADJ (Open Load Adjust)

The current for the Open load detection can be adjusted by connecting a resistor between this pin and GNDBB (from the E96 series : 25 kΩ - 2.3 kΩ).The DC-level V_{OLADJ} is 1.215 V.

VDDIO (3.3 V Supply Blocking Capacitor)

A 1 µF ceramic capacitor must be connected between VDDIO and GNDBB.

VCORE (Blocking Capacitor for 1.5 V Digital Core)

A 470 nF ceramic capacitor must be connected between VCORE and GNDBB.

2.1.2 Pins of Serial and Parallel Logic Interface

Some pins are common for both interface types, some others are specific for the parallel or serial access.

VCC (Positive 3.3 V logic supply)

V_{CC} supplies the output interface that is electrically isolated from the output power stage. The interface can be supplied with 3.3 V. A ceramic capacitor of minimum 2.2 µF must be connected between VCC and GND.

GND (Ground for VCC domain)

This pin acts as the ground reference for the uC-interface that is supplied by V_{CC}.

CLKADJ (Clock Adjust)

A high precision resistor of 10 KΩ has to be connected between CLKADJ and GND. The DC-level V_{CLKADJ} is 0.5 V.

$\overline{\text{ERR}}$ (Fault Indication)

The low active $\overline{\text{ERR}}$ signal contains the OR-wired diagnostic information depending on choosen serial or parallel mode (VBB undervoltage or missing voltage detection, the internal data transmission failure detection unit and the fault(s) of the output switch).The output pin $\overline{\text{ERR}}$ provides an open drain functionality.This pin has an internal Pull-Up resistor. In normal operation the signal $\overline{\text{ERR}}$ is high.

$\overline{\text{ODIS}}$ (Output Disable)

The low active $\overline{\text{ODIS}}$ signal immediately switches off the output channels OUT0-OUT7. This pin has an internal Pull-Down resistor. In normal operation the signal $\overline{\text{ODIS}}$ is high. Setting $\overline{\text{ODIS}}$ to Low clears the **DRIVE** register as well. The minimum width of the $\overline{\text{ODIS}}$ signal is 5 µs.

SEL (Serial or Parallel Mode Select)

When this pin is in a logic Low state, the IC operates in Parallel Mode. For Serial Mode operation the pin has to be pulled into logic High state. During Start Up the IC is operating in Parallel Mode. This pin has an internal Pull-Down resistor and a 200 ns blanking time[1)].

SYNC

In isochronous mode (clock-sync-mode) the transfer of the latched output data register into the output-stages is controlled by the SYNC signal. When the SYNC-signal is in low state, the output-stage won't be updated any longer, the last value is frozen. With the rising edge of SYNC the information of the latched output data registers will be transferred to the output stages. It can be choosen by a configuration bit whether all the channel diagnostic bits will be latched into the DIAG channel register every data cycle or only when the SYNC-signal is in high state. In the last case when the SYNC-signal is in low state, the DIAG channel register wouldn't be updated any longer, the last value would be frozen. SYNC is also used for resynchronization of the data transmission with the target to achieve a low jitter. This pin has an internal Pull-Up resistor and a 20 ns blanking time[1)].

$\overline{\text{CS}}$ (Chip Select)

When this pin is in a logic Low state, the IC interface is enabled and data can be transferred. This pin has an internal Pull-Up resistor and a 20 ns blanking time[1)].

When the $\overline{\text{CS}}$ pin is held Low whereas the ALE pin is High for at least 100 µs, the device is reset.

The following pins are provided in the parallel interface mode

AD7:AD0 (AddressData input / output bit7 ... bit0)

The pins AD0 .. AD7 are the bidirectional input / outputs for data write and read. Depending on the state of the ALE pin and the AD7 pin, register addresses or data can be transferred between the internal registers and e.g. the micro-controller. By connecting $\overline{\text{CS}}$ and $\overline{\text{WR}}$ and ALE/RST pins to GND and $\overline{\text{RD}}$ to VCC, the parallel direct mode is activated.

$\overline{\text{WR}}$ (Write)

By pulling this pin down, a write transaction is initiated on the AddressData bus and the data has to be valid on the rising edge of $\overline{\text{WR}}$. The AD7-bit of the register address has to be set to '1'. This pin has an internal Pull-Up resistor and a 20 ns blanking time[1)].

$\overline{\text{RD}}$ (Read)

By pulling this pin down, a read transaction is initiated on the AddressData bus and the data becomes valid on the rising edge of $\overline{\text{RD}}$. The AD7-bit of the register address has to be set to '0'. This pin has an internal Pull-Up resistor and a 20 ns blanking time[1)].

ALE (Address Latch Enable)/RST

The pin ALE is used to select between address (ALE is in a logic High state) or data (ALE is in a logic Low state). Furthermore, a read or write transaction can be selected with the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ pin. When ALE is pulled high, address is transferred and latched over the bit AD0 to AD7. During the time interval where ALE = High $\overline{\text{RD}}$ or $\overline{\text{WR}}$ has to be pulled to High. During the Low State of ALE all transactions hit the same address. This pin has an internal Pull-Down resistor and a 20 ns blanking time[1)]. For the reset-function see comment under the item: $\overline{\text{CS}}$.

1) the signal must be stable for the duration of the blanking time before it is accepted as valid

The following pins are provided in the serial interface mode

MS0, MS1 (Serial Mode Select)

By driving these pins to Logic High or Low the Serial Interface Mode (number of bits - 8, 16, 24 - to be transferred, CRC) can be selected. These pins have both an internal Pull-Down resistor and a 200 ns blanking time[1)].

SCLK (Serial Interface Shift Clock)

Input data are sampled with rising edge and output data are updated with the falling edge of this input clock signal. This pin has an internal Pull-Down resistor and a 20 ns blanking time[1)].

SDI (Serial Interface Input Data)

SDI is put into a dedicated FIFO (clocked by SCLK) to program the DRIVE register and the internal address and the write data. This pin has an internal Pull-Down resistor and a 20 ns blanking time[1)].

SDO (Serial Interface Data Output)

SDO provides the serial output data bits

$\overline{\text{CRCERR}}$ (CRC Error Output)

This pin is in a logic Low state when CRC errors or Shift-Clock errors are detected internally. This pin has an open drain functionality and an internal Pull-Up resistor.

3 Block Diagram

The IC is divided into an uC_chip and into a power chip due to the galvanical isolation.The uC_chip contains the uC-interface and the power chip the power switches.

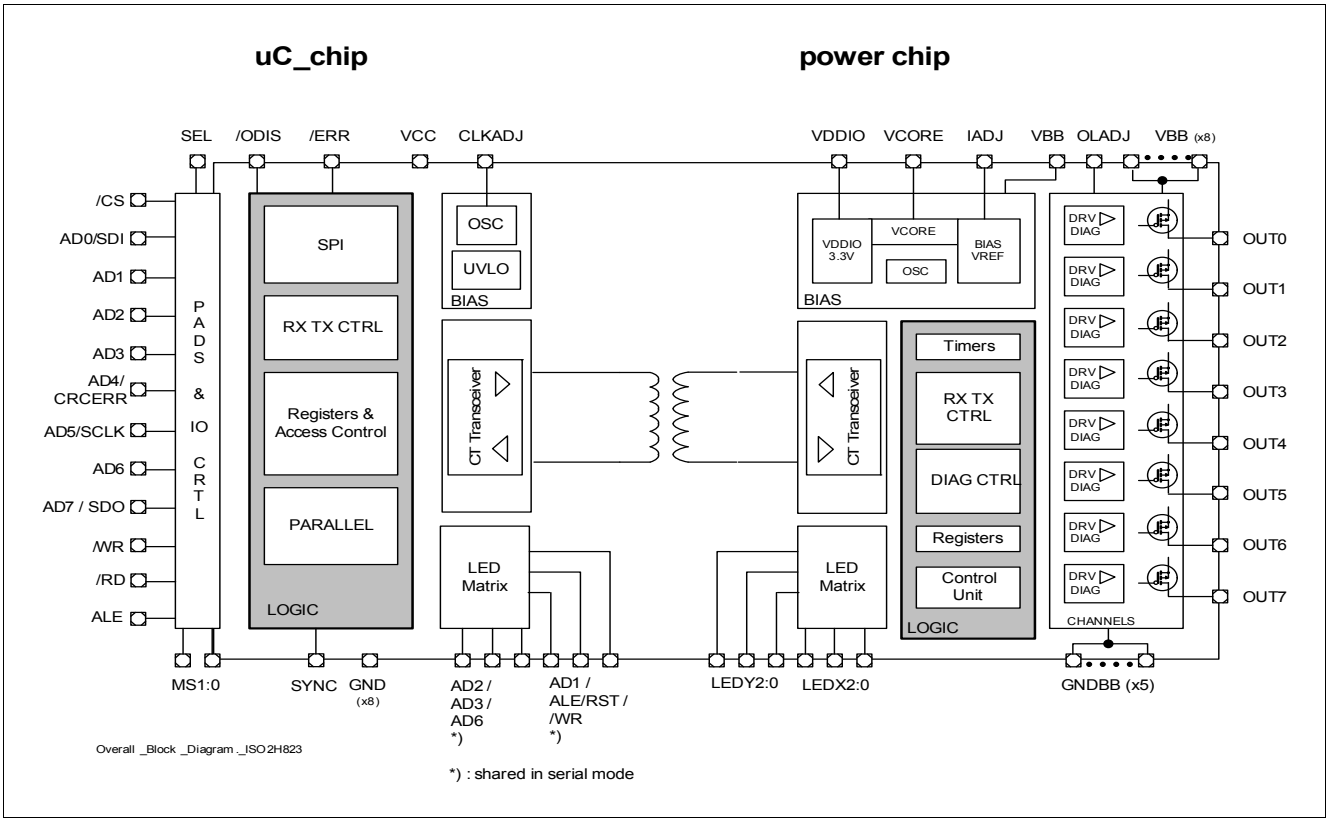


Figure 3 Block Diagram

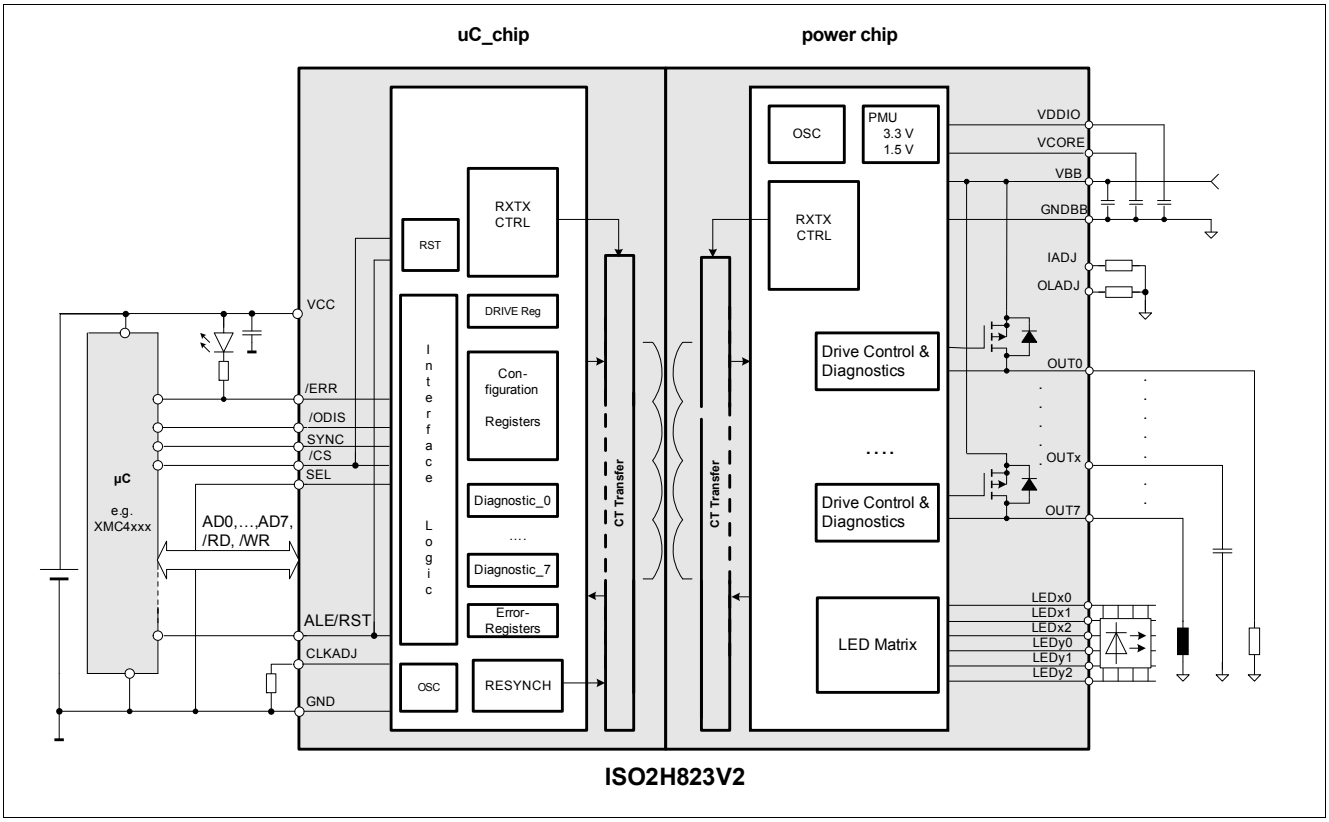


Figure 4 Application with Parallel Interface

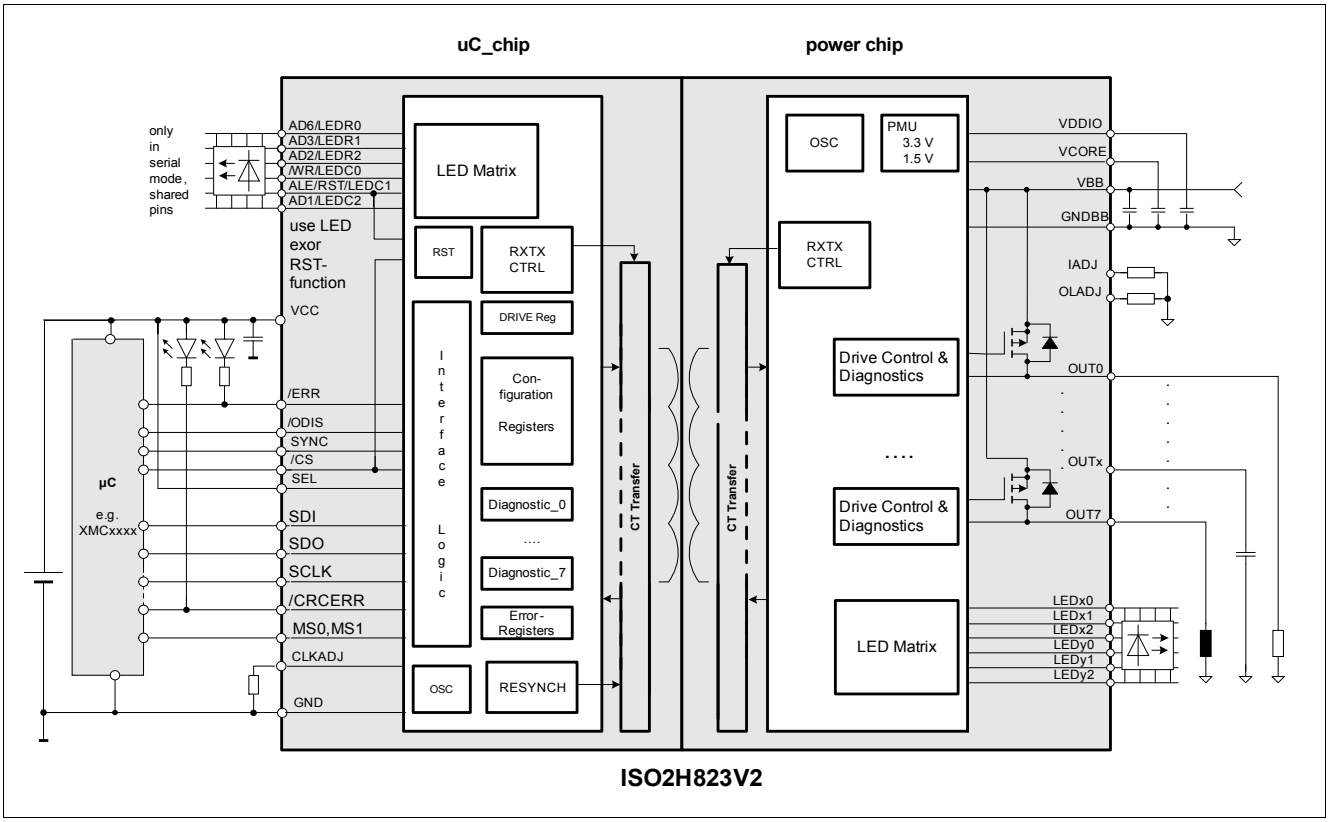


Figure 5 Application with Serial Interface

4 Functional Description

4.1 Introduction

The IC contains 2 galvanic isolated voltage domains that are independent from each other. The input interface (µC-chip) is supplied at V_{CC} and the output stage (power chip) is supplied at V_{BB}. The different voltage domains can be switched on at different time. The output stage is only enabled once the input stage enters a stable state. The power chip generates out of V_{BB} two internal voltages V_{DDIO} = 3.3 V (± 10 %) and V_{CORE} = 1.5 V (± 10%) which have to be buffered externally.

The ISOFACE ISO2H823V2.5 includes 8 high-side power switches that are controlled by means of the integrated parallel/serial interface. The interface is 8-bit µController compatible. Furthermore a direct control mode can be selected that allows the direct control of the outputs OUT0 … OUT7 (power chip) by means of the inputs AD0 … AD7 (µC-chip) without any additional logic signal. The IC can replace 8 optocouplers and the 8 high-side switches in conventional I/O-Applications as a galvanic isolation is implemented by means of the integrated coreless transformer technology. The µController compatible interface allows a direct connection to the ports of a microcontroller without the need for other components. Each of the 8 high-side power switches is protected against overload, overtemperature and against overvoltage by an active zener clamp.

4.2 Microcontroller Interface

The microcontroller interface can be configured as a parallel or serial interface via the SEL pin.

4.2.1 Parallel Interface Mode

The ISO2H823V2.5 device contains a parallel interface that can be selected by pulling the SEL Pin to logic Low state. The interface can be directly controlled by the µController output ports (see **Figure 6**). The output pins AD7:AD0 are in state “Z” as long as $\overline{CS}$=1, $\overline{RD}$=1 and $\overline{WR}$=1.

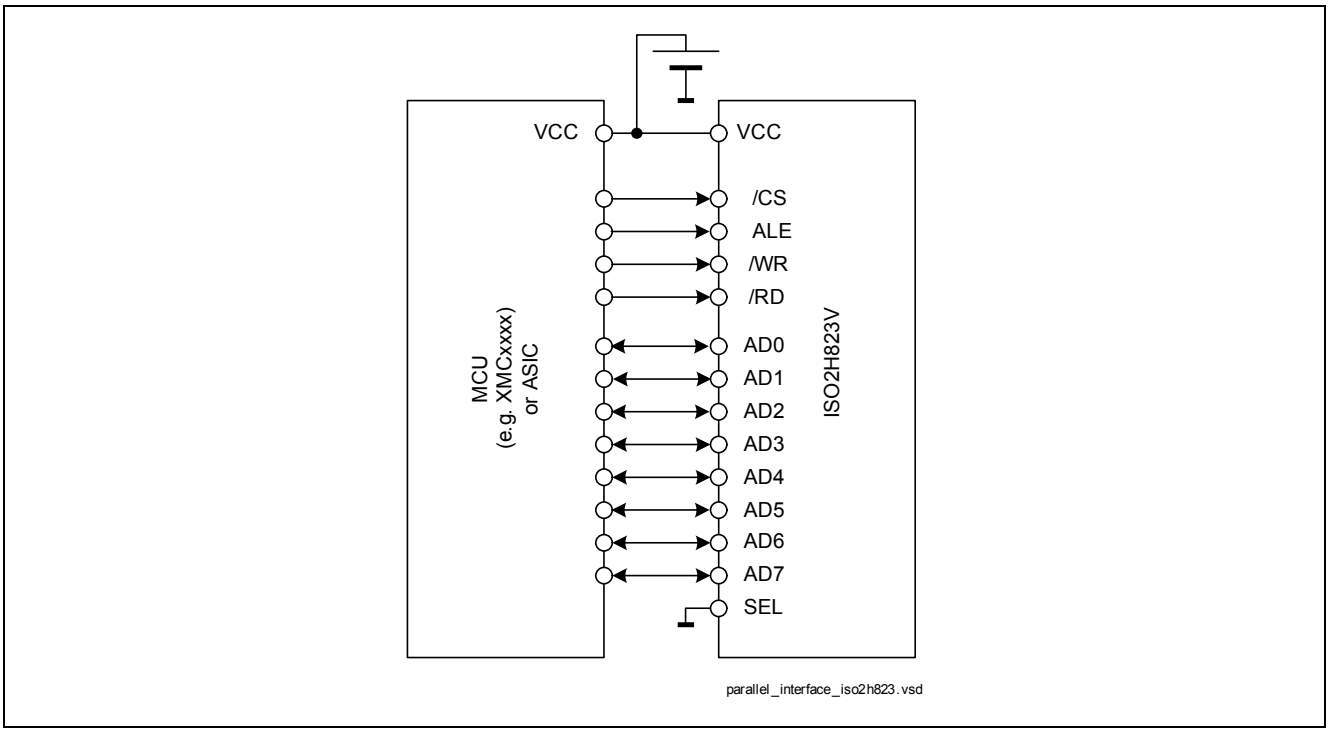


Figure 6 Bus Configuration for Parallel Mode

The timing requirements for the parallel interface are shown in **Figure 7** (Read), **Figure 8** (Write) and **Table 23**.

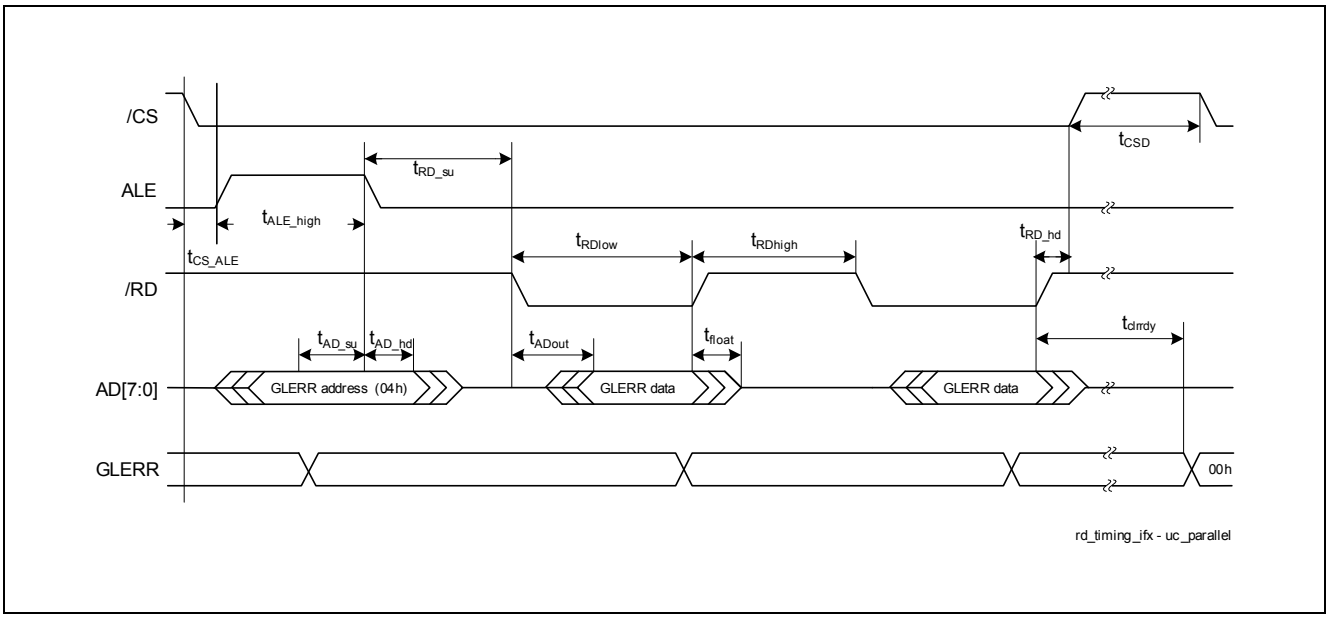


Figure 7 Timing by Parallel Read Access (e.g. GLERR Register)

For a reading access to internal registers the MSB of the address register has to be set to “0”.

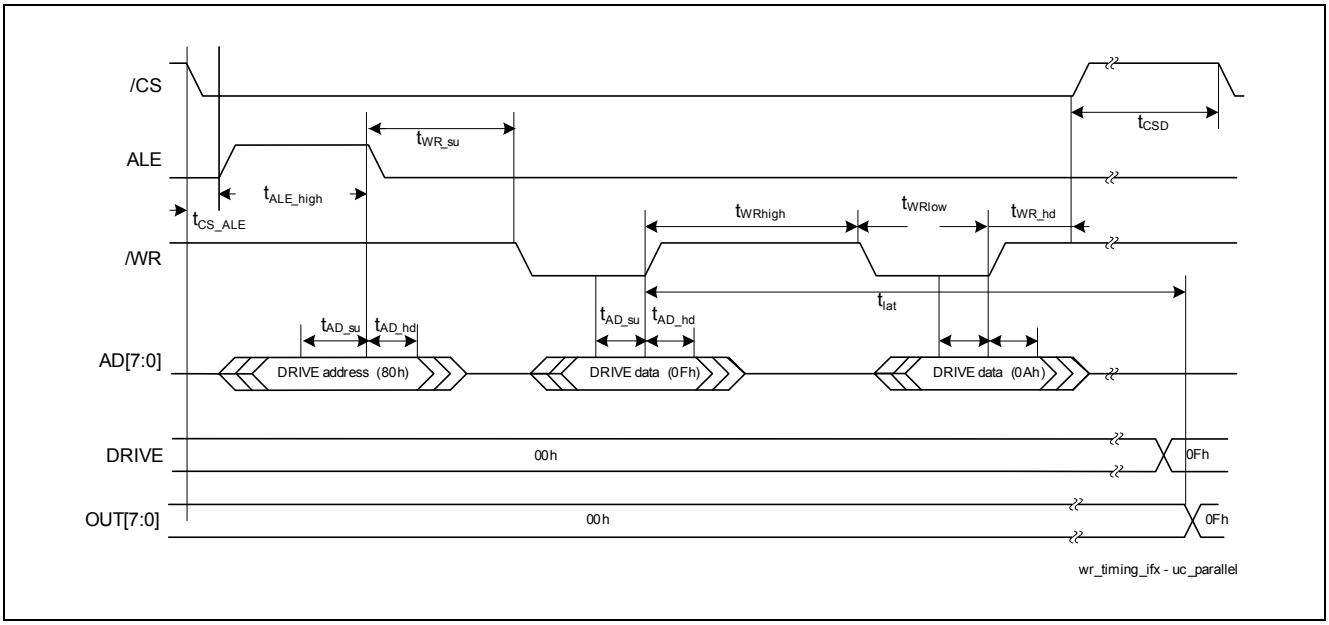


Figure 8 Timing by Parallel Write Access (e.g. DRIVE Register)

For a writing access to internal registers the MSB of the address register has to be set to “1”.

4.2.1.1 Parallel Direct Mode

The parallel interface can be also used in a direct mode that allows direct changes of the output OUT0...OUT7 by means of the corresponding inputs D0-D7 without additional logic signals. To activate the parallel direct mode $\overline{CS}$, $\overline{WR}$ and ALE pins have to be wired to ground and $\overline{RD}$ has to be wired to V_{CC} as shown in the **Figure 9**. Although the diagnostics cannot be read in this operation mode, the faults as specified in **Table 3** are still reported at the $\overline{ERR}$ pin (volatile).

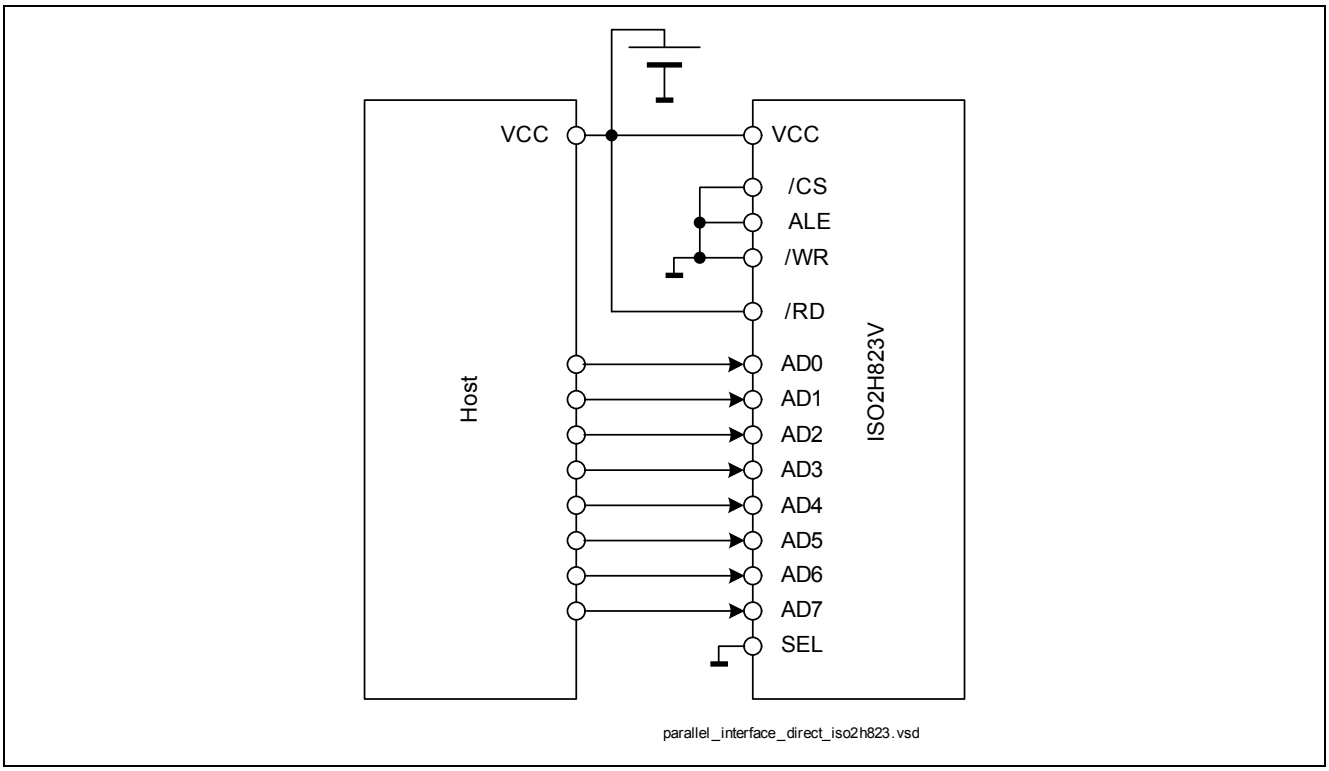


Figure 9 Parallel Direct Mode

The direct mode is intended to be an additional parallel mode which is invoked directly after reset. In this case internal settings have already been realized (f.e. MSB of the address register is set to “1”).

4.2.2 Serial Interface Mode

The ISO2H823V2.5 device contains a serial interface that can be activated by pulling the SEL pin to logic High state. The interface can be directly controlled by the µController output ports. The output pin SDO is in state “Z” as long as $\overline{CS}$=1. Otherwise, the bits at the SDI input are sampled with the rising edge of SCLK and registered into the input FIFO buffer of length dependent on the selected SPI-mode (8, 16, 24 bits, **Figure 12**, **Figure 13**, **Figure 14**, **Figure 15**). With every falling edge of SCLK the bits to be read are provided serially to the pin SDO.

The timing requirements for the serial interface are shown in **Figure 10** and in **Table 24**.

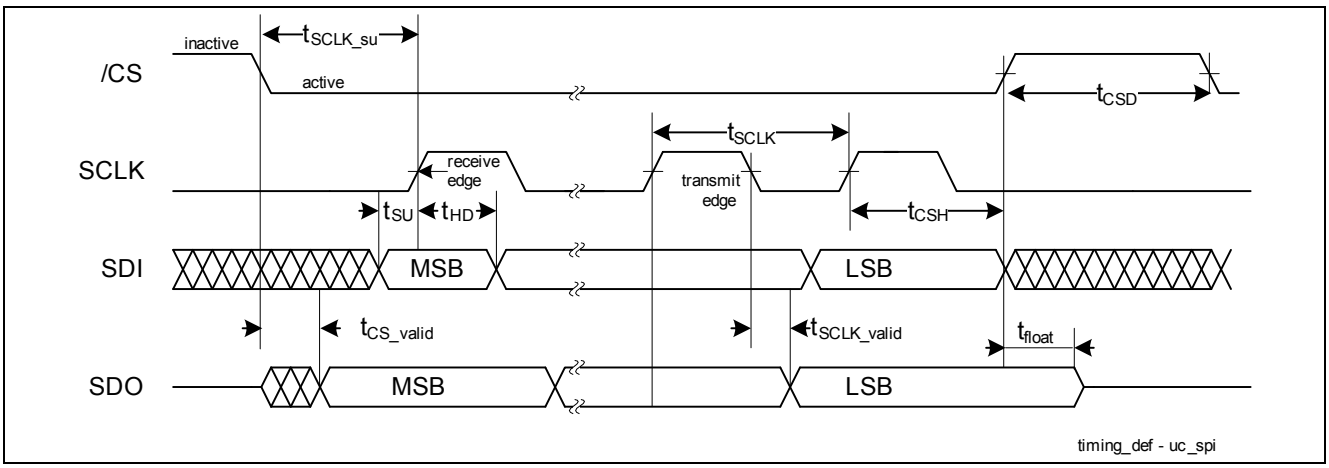


Figure 10 Serial Bus Timing

Several SPI topologies are supported: pure bus topology, daisy chain and any combinations (**Figure 11**). Of course independent individual control with a dedicated SPI controller interfaces for each slave IC is possible, as well.

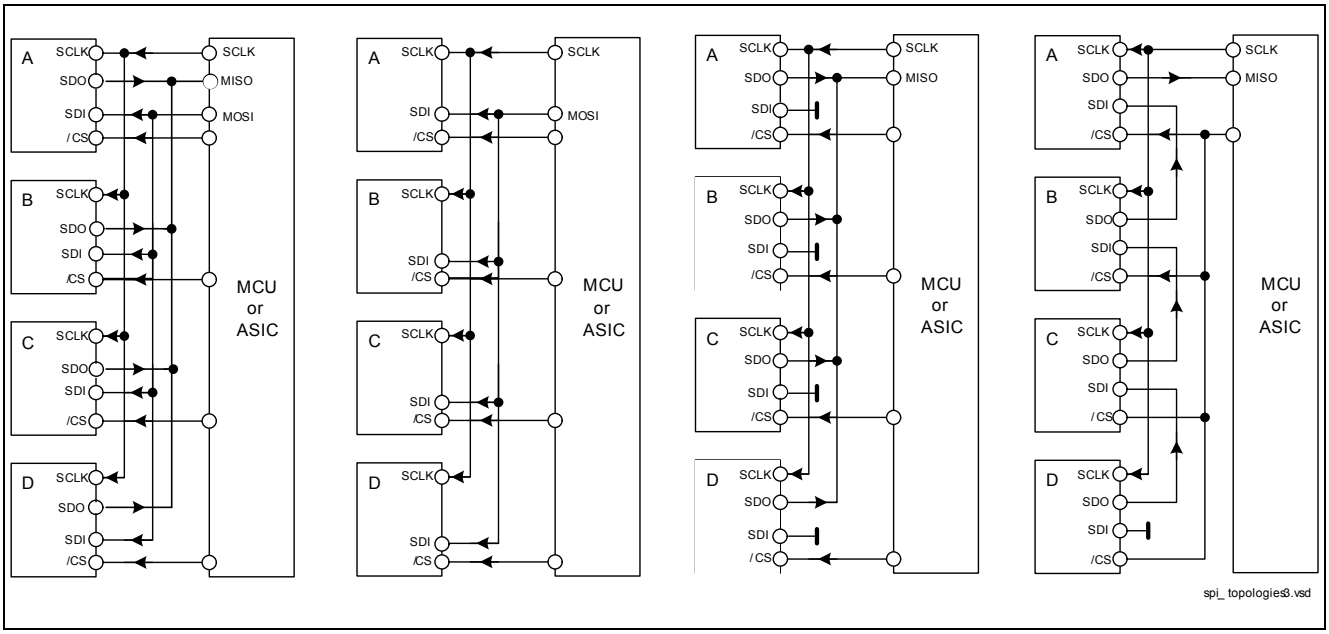


Figure 11 Example SPI Topologies

4.2.2.1 SPI Modes

Four different SPI-modes can be distinguished (**Figure 12** - **Figure 15**).

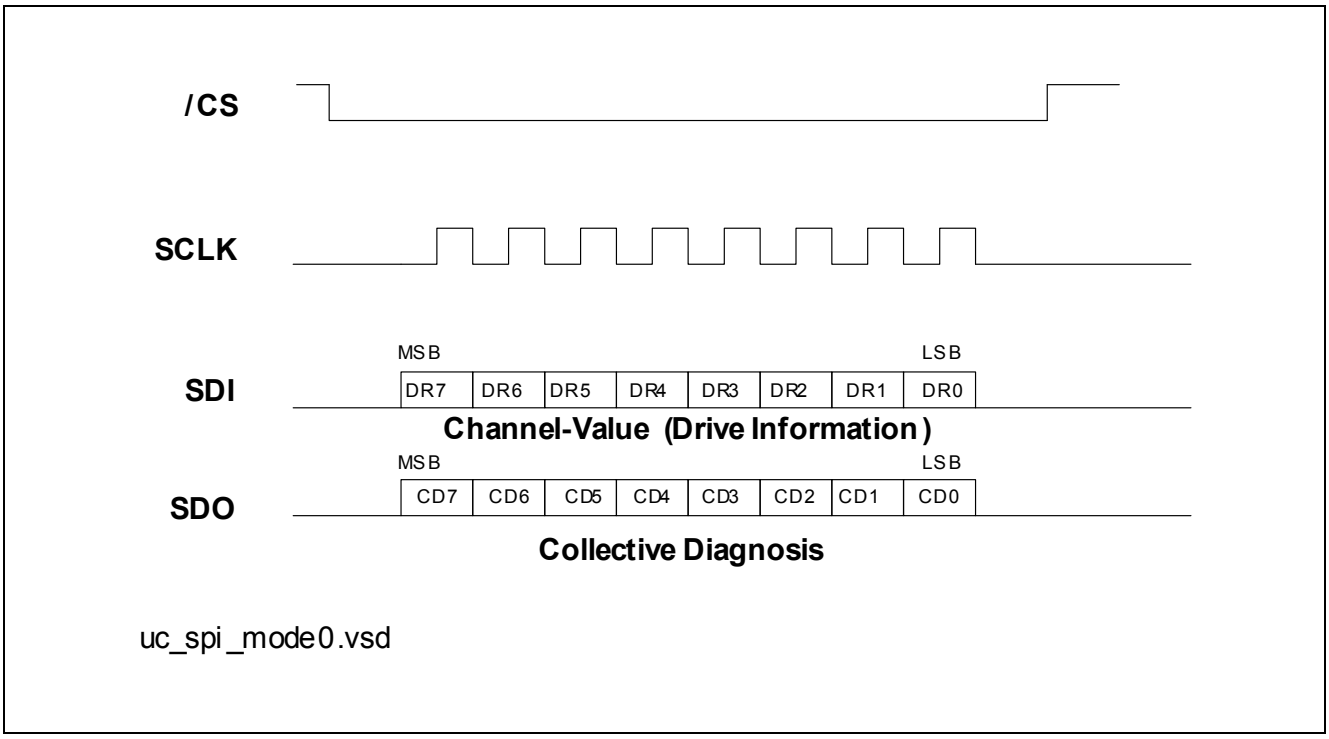


Figure 12 SPI Mode 0, MS0 = 0, MS1 = 0, Daisy Chain Supported

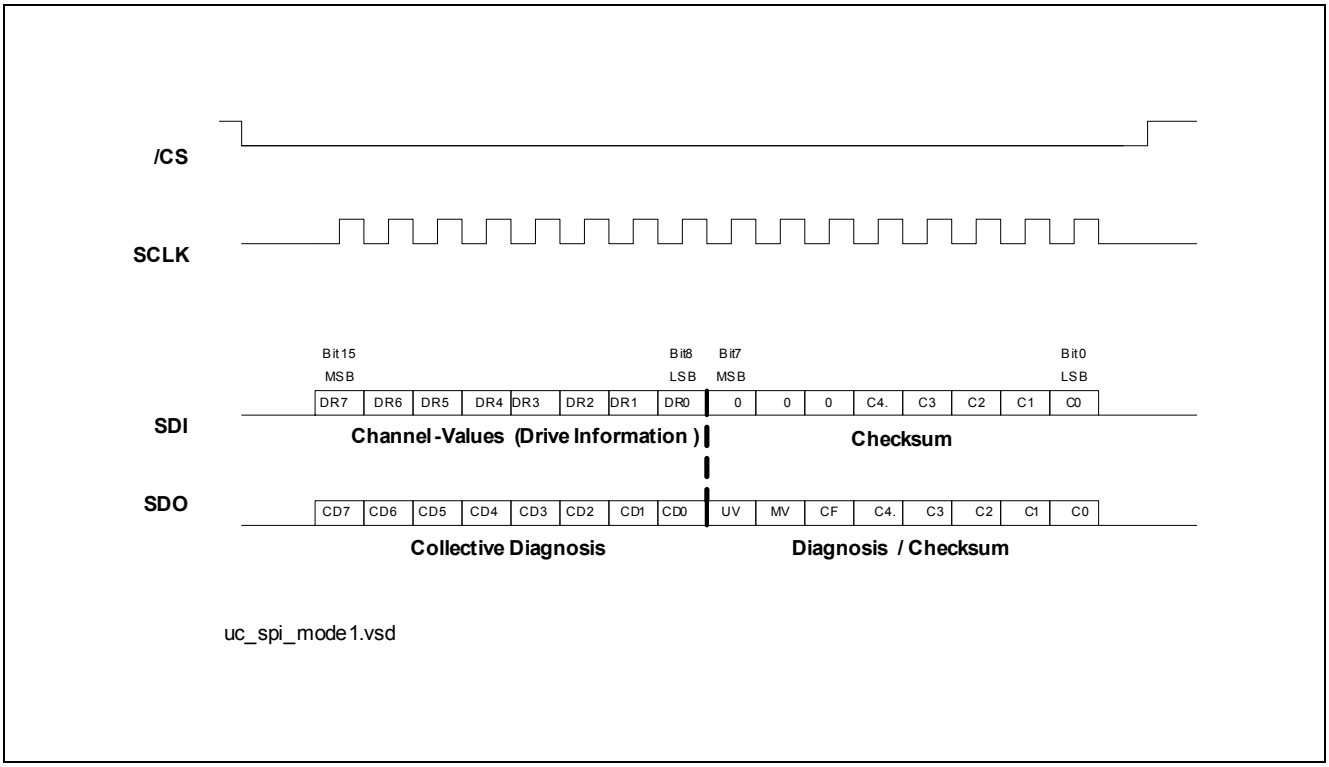


Figure 13 SPI Mode 1, MS0 = 1, MS1 = 0, Daisy Chain Supported

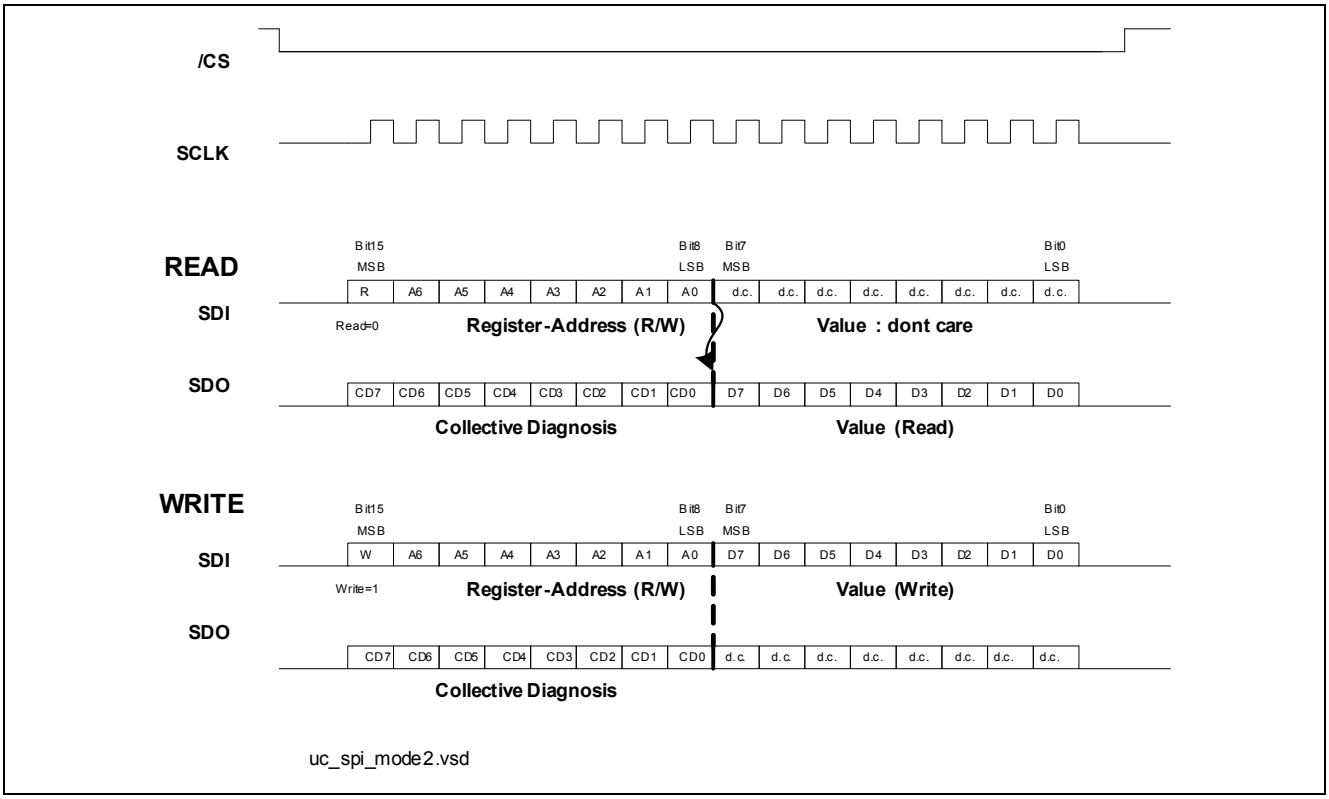


Figure 14 SPI Mode 2, MS0 = 0, MS1 = 1

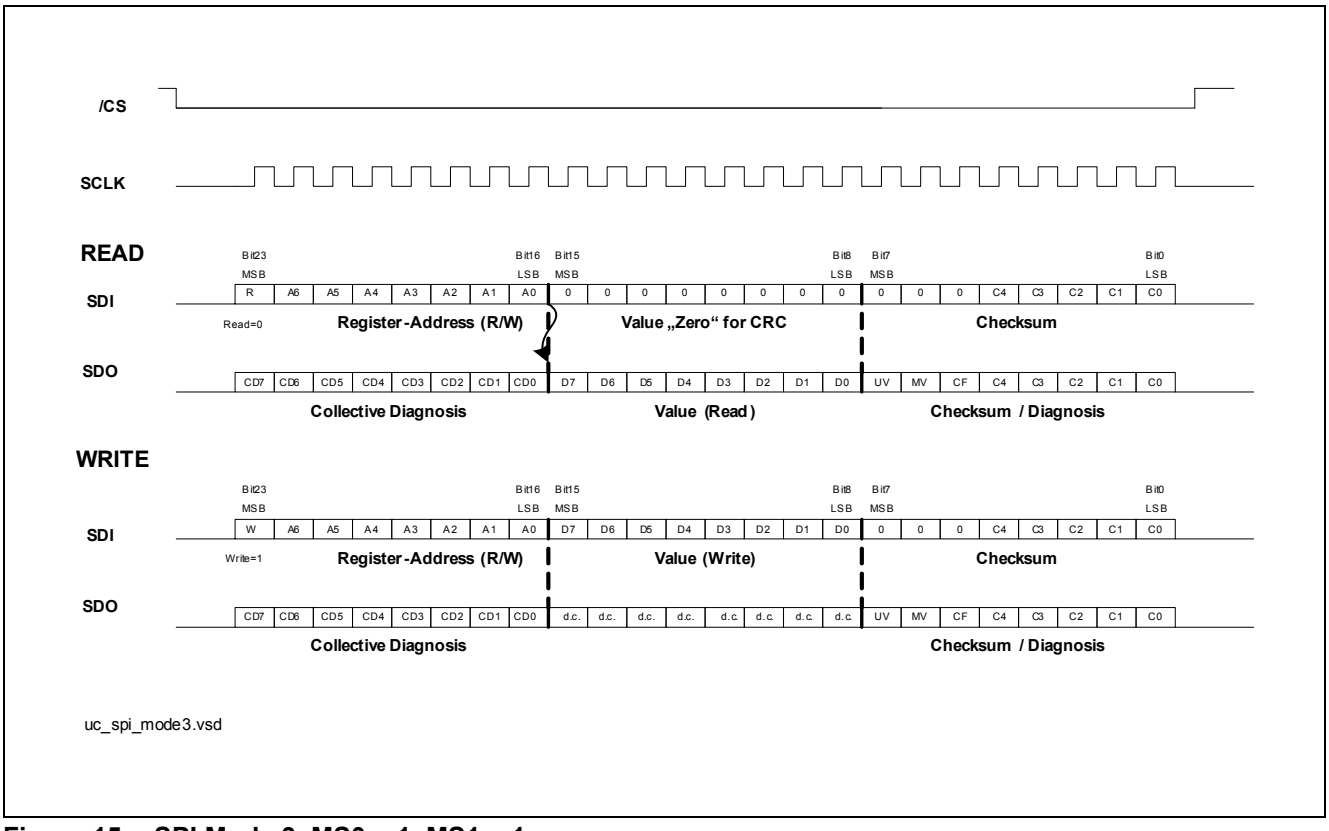


Figure 15 SPI Mode 3, MS0 = 1, MS1 = 1

4.2.2.2 Daisy Chain Mode

Up to 4 devices can be connected together as shown in the **Figure 16** to operate in the daisy chain mode. Serial modes 0 and 1 can be operated in daisy chain mode. In this case, the SDO output of one device is directly connected to the SDI input of the next device. The SPI chain has to be connected to the µC or Bus ASIC (MOSI, MISO and common SCLK and $\overline{CS}$ signals). If the received SCLK pulses are not fulfilling the modulo(8)-condition the $\overline{CRCERR}$ pin will be activated.

In the serial mode 1 the CRC-generation has to be reset after 16 SCLK-cycles. At the rising edge of $\overline{CS}$ each connected daisy-chain-device checks its related 16 bit-stream concerning CRC-consistency.

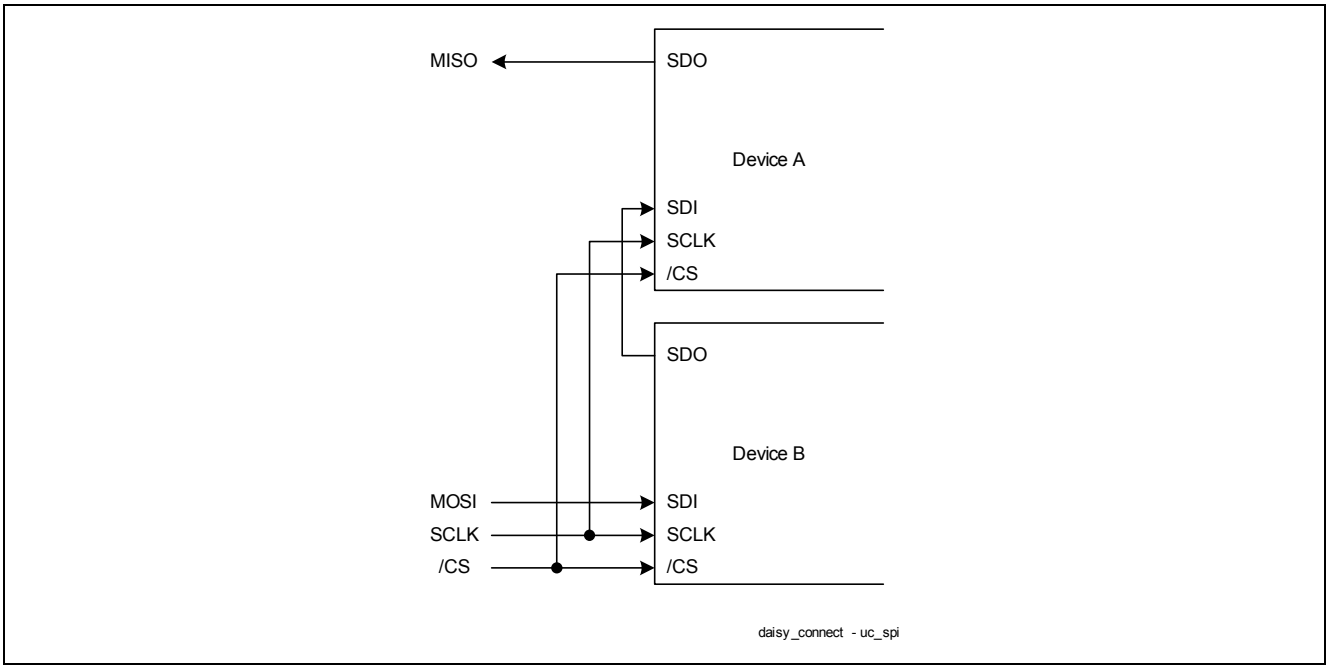


Figure 16 Connecting Two Devices for Daisy Chain Mode

The data shifted in the first device SDI input is shifted out at the SDO output after the first byte for the serial mode 0 (after the second byte for the mode 1) while $\overline{CS}$ remains Low as shown in the **Figure 17**.

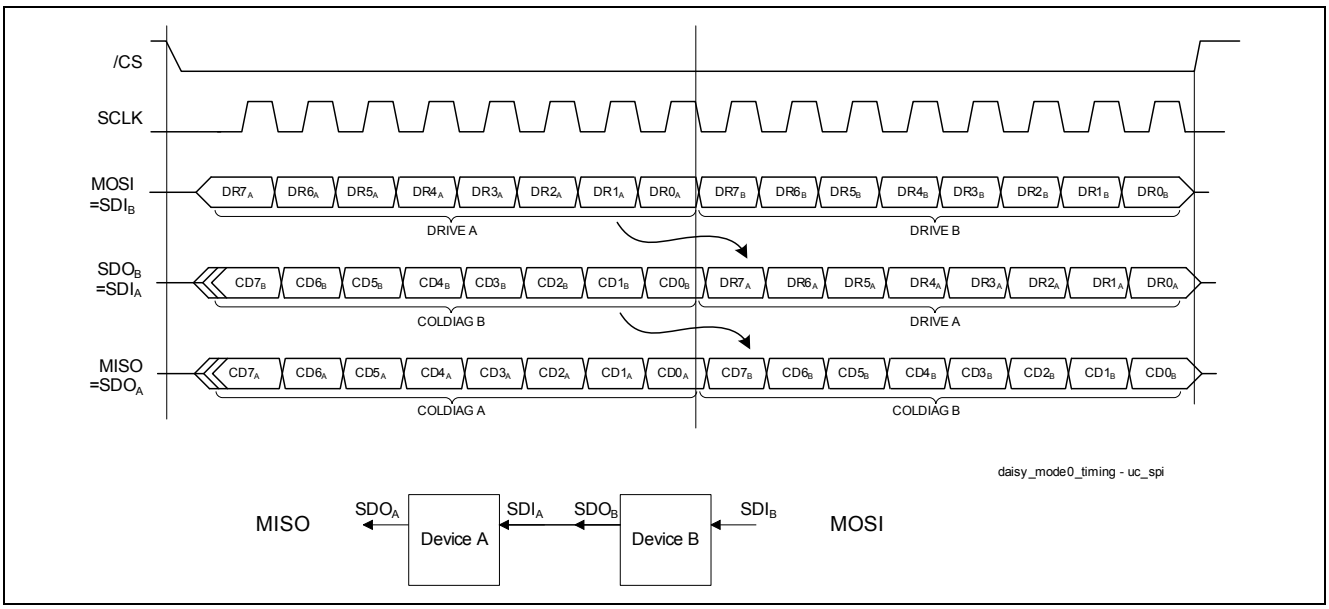


Figure 17 Typical Timing Diagram of Daisy Chain Operation (Serial Mode 0)