ISO8200BQ

Galvanic isolated octal high-side smart power solid state-relay

Datasheet - production data

TFQFPN32

Features

Type	V_{demag}[1]	$R_{DS(on)}$[1]	I_{OUT}[1]	V_{cc}
ISO8200BQ	V_{cc}- 45 V	0.11 Ω	0.7 A	45 V

Notes:

[1] Per channel.

- Parallel input interface
- Direct and synchronous control mode
- High common mode transient immunity
- Output current: 0.7 A per channel
- Short-circuit protection
- Channel overtemperature protection
- Thermal independence of separate channels
- Common output disable pin
- Case overtemperature protection
- Loss of GND_{cc} and V_{cc} protection
- Undervoltage shutdown with auto-restart and hysteresis
- Overvoltage protection (V_{cc} clamping)
- Very low supply current
- Common fault open-drain output
- 5 V and 3.3 V TTL/CMOS compatible I/Os
- Fast demagnetization of inductive loads
- Reset function for IC output disable
- ESD protection
- IEC 61000-4-2, IEC 61000-4-4, IEC 61000-4-5 and IEC 61000-4-8 compliant

Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines
- Drivers for all types of loads (resistive, capacitive, inductive)

Description

The ISO8200BQ is a galvanic isolated 8-channel driver featuring a very low supply current. It contains 2 independent galvanic isolated voltage domains (V_{cc} for the power stage and V_{dd} for the digital stage). Additional embedded functions are: loss of GND protection, undervoltage shutdown with hysteresis, and reset function for immediate power output shutdown.

IC is intended to drive any kind of load with one side connected to ground. Active channel current limitation combined with thermal shutdown, (independent for each channel), and automatic restart, protect the device against overload and short-circuit. In overload conditions, if junction temperature overtakes threshold, the channel involved is turned off and on again automatically after the IC temperature decreases below a reset threshold. If this condition causes case temperature to reach TCR limit threshold, the overloaded channel is turned off and it only restarts when case and junction temperature decrease down to the reset thresholds. Non-overloaded channels continue operating normally. An internal circuit provides an OR-wired non-latched common $\overline{\text{FAULT}}$ indicator signaling the channel OVT. The $\overline{\text{FAULT}}$ pin is an open-drain active low fault indication pin.

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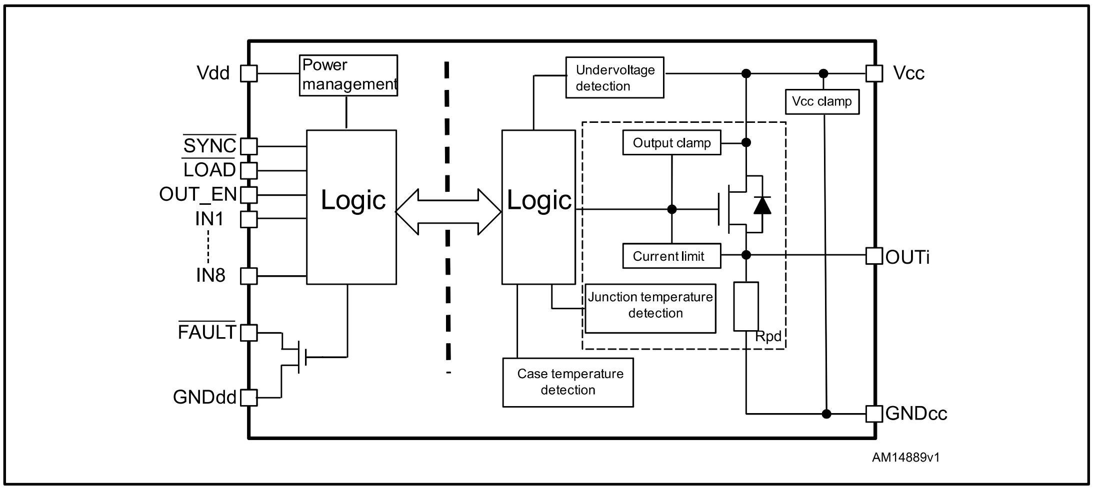
Figure 1: Block diagram



2 Pin connection

Figure 2: Pin connection (top through view)

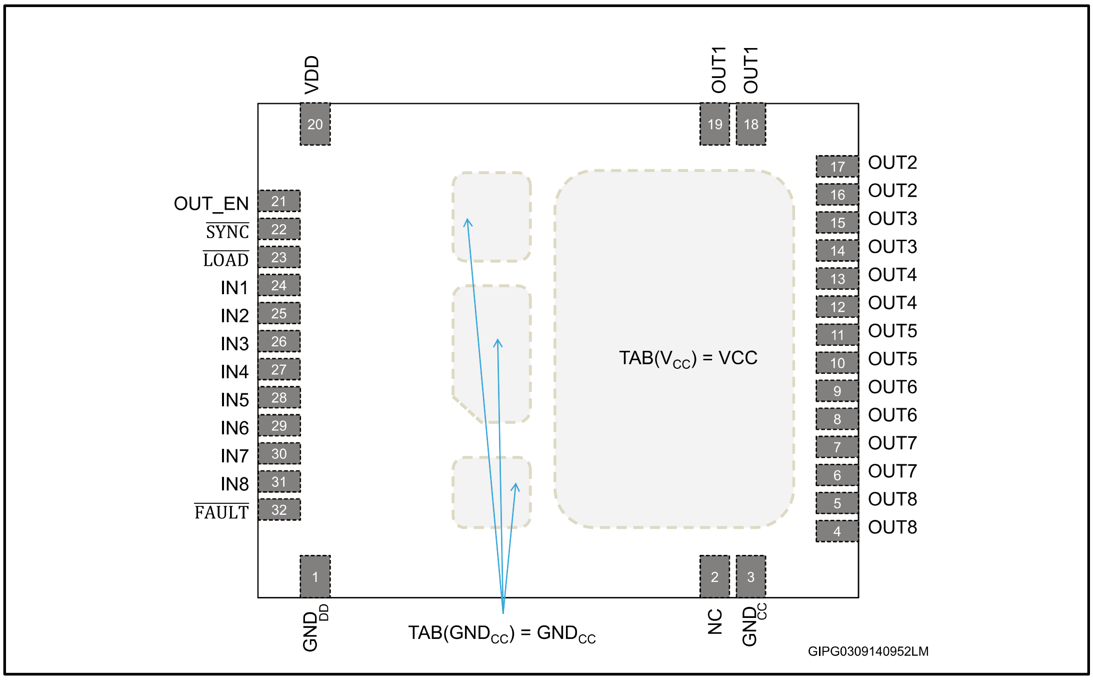


Table 1: Pin description

Pin	Name	Description
1	GND_{DD}	Input logic ground, negative logic supply
2	NC	Not connected
3	GND_{CC}	Output power ground
4	OUT8	Channel 8 power output
5	OUT8	
6	OUT7	Channel 7 power output
7	OUT7	
8	OUT6	Channel 6 power output
9	OUT6	
10	OUT5	Channel 5 power output
11	OUT5	
12	OUT4	Channel 4 power output
13	OUT4	
14	OUT3	Channel 3 power output
15	OUT3	
16	OUT2	Channel 2 power output
17	OUT2	
18	OUT1	Channel 1 power output
19	OUT1	

Pin	Name	Description
20	VDD	Positive logic supply
21	OUT_EN	Output enable
22	$\overline{\text{SYNC}}$	Input-to-output synchronization signal. Active low, see *Section 6.3: "Synchronous control mode (SCM)"*
23	$\overline{\text{LOAD}}$	Load input data signal. Active low, see *Section 6.3: "Synchronous control mode (SCM)"*
24	IN1	Channel 1 input
25	IN2	Channel 2 input
26	IN3	Channel 3 input
27	IN4	Channel 4 input
28	IN5	Channel 5 input
29	IN6	Channel 6 input
30	IN7	Channel 7 input
31	IN8	Channel 8 input
32	$\overline{\text{FAULT}}$	Common fault indication, active low
TAB(V_{CC})	V_{CC}	Exposed tab internally connected to V_{CC}, positive power supply voltage
TAB(GND_{CC})	GND_{CC}	Exposed tab internally connected to GND_{CC}

3 Absolute maximum ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Power supply voltage	-0.3	45	V
V_{dd}	Digital supply voltage	-0.3	6.5	V
V_{IN}	DC input pin voltage (INx, OUT_EN, $\overline{\text{LOAD}}$, $\overline{\text{SYNC}}$)	-0.3	+6.5	V
V_{FAULT}	Fault pin voltage	-0.3	+6.5	V
I_{GNDdd}	DC digital ground reverse current		-25	mA
I_{OUT}	Channel output current (continuous)		Internally limited	A
I_{GNDcc}	DC power ground reverse current		-250	mA
I_R	Reverse output current (per channel)		-5	A
I_{IN}	DC input pin current (INx, OUT_EN, $\overline{\text{LOAD}}$, $\overline{\text{SYNC}}$)	-10	+ 10	mA
I_{FAULT}	Fault pin current	-10	+ 10	mA
V_{ESD}	Electrostatic discharge with human body model (R = 1.5 kΩ; C = 100 pF)		2000	V
E_{AS}	Single pulse avalanche energy per channel not simultaneously @T_{amb}= 125 °C, I_{OUT} = 0.5 A		1.8	J
	Single pulse avalanche energy per channel, all channels driven simultaneously @T_{amb}= 125 °C, I_{OUT} = 0.5 A		0.35	
P_{TOT}	Power dissipation at T_c = 25 °C		Internally limited (1)	W
T_J	Junction operating temperature		Internally limited(1)	°C
T_{STG}	Storage temperature		-55 to 150	°C

Notes:

(1)Protection functions are intended to avoid IC damage in fault conditions and are not intended for continuous operation. Continuous or repetitive operations of protection functions may reduce the IC lifetime.

4 Thermal data

Table 3: Thermal data

Symbol	Parameter	Max. value	Unit
$R_{thj\text{-}case}$	Thermal resistance, junction-case(1)	2	°C/W
$R_{thj\text{-}amb}$	Thermal resistance, junction-ambient (2)	15	°C/W

Notes:

(1) For each channel.

(2) TFQFPN32 mounted on the product evaluation board (FR4, 4 layers, 8 cm^2 for each layer, copper thickness 35 mm).

5 Electrical characteristics

(10.5 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C, unless otherwise specified)

Table 4: Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC(THON)}$	V_{CC} undervoltage turn-ON threshold			9.5	10.5	V
$V_{CC(THOFF)}$	V_{CC} undervoltage turn-OFF threshold		8	9		V
$V_{CC(hys)}$	V_{CC} undervoltage hysteresis		0.25	0.5		V
$V_{CCclamp}$	Clamp on V_{CC} pin	I_{clamp} = 20 mA	45	50	52	V
$R_{DS(on)}$	On-state resistance [(1)]	I_{OUT} = 0.5 A, T_J = 25 °C				Ω
		I_{OUT} = 0.5 A T_J = 125 °C		0.12	0.24	
R_{pd}	Output pull-down resistor			210		kΩ
I_{CC}	Power supply current	All channels in OFF-state		5		mA
		All channels in ON-state		9		
I_{LGND}	Ground disconnection output current	V_{CC} = V_{GND} = 0 V V_{OUT} = -24 V			500	µA
V_{OUT}(OFF)	Off-state output voltage	Channel OFF and I_{OUT} = 0 A			1	V
I_{OUT}(OFF)	Off-state output current	Channel OFF and V_{OUT} = 0 V			5	µA

Notes:

(1)See *Figure 3: "RDS(on) measurement"*

Table 5: Digital supply voltage

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{dd}	Operating voltage		2.75		5.5	V
$V_{dd(THON)}$	V_{dd} undervoltage turn-ON threshold		2.55		2.75	V
$V_{dd(THOFF)}$	V_{dd} undervoltage turn-OFF threshold		2.45		2.65	V
$V_{dd(hys)}$	V_{dd} undervoltage hysteresis		0.04	0.1		V
I_{dd}	I_{dd} supply current	V_{dd} = 5 V and input channel with a steady logic level		4.5	6	mA
		V_{dd} = 3.3 V and input channel with a steady logic level		4.4	5.9	mA

Table 6: Diagnostic pin and output protection function

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{FAULT}	$\overline{\text{FAULT}}$ pin open-drain voltage output low	I_{FAULT} = 10 mA			0.4	V
I_{LFAULT}	$\overline{\text{FAULT}}$ output leakage current	V_{FAULT} = 5 V			1	µA
I_{PEAK}	Maximum DC output current before limitation	V_{CC} = 24 V R_{LOAD} = 0 Ω		1.6		A
I_{LIM}	Short-circuit current limitation		0.7	1.3	1.9	A
H_{yst}	I_{LIM} tracking limits			0.3		A
T_{JSD}	Junction shutdown temperature		150	170		°C
T_{JR}	Junction reset temperature			150		°C
T_{HIST}	Junction thermal hysteresis			20		°C
T_{CSD}	Case shutdown temperature		115	130	145	°C
T_{CR}	Case reset temperature			110		°C
T_{CHYST}	Case thermal hysteresis			20		°C
V_{demag}	Output voltage at turn-OFF	I_{OUT} = 0.5 A I_{LOAD} > = 1 mH	V_{CC}-45	V_{CC}-50	V_{CC}-52	V

Table 7: Power switching characteristics (VCC = 24 V; -40 °C < TJ < 125 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
dV/dt(ON)	Turn-ON voltage slope	I_{OUT} = 0.5 A, resistive load 48 Ω	-	5.6	-	V/µs
dV/dt(OFF)	Turn-OFF voltage slope	I_{OUT} = 0.5 A, resistive load 48 Ω	-	2.81	-	V/µs
t_d(ON)	Turn-ON delay time (1)	I_{OUT} = 0.5 A, resistive load 48 Ω	-	17	22	µs
t_d(OFF)	Turn-OFF delay time (1)	I_{OUT} = 0.5 A, resistive load 48 Ω	-	22	40	µs
t_f	Fall time (1)	I_{OUT} = 0.5 A, resistive load 48 Ω	-	5	-	µs
t_r	Rise time (1)	I_{OUT} = 0.5 A, resistive load 48 Ω	-	5	-	µs

Notes:

(1)See *Figure 3: "RDS(on) measurement"*, *Figure 4: "dV/dT"* and *Figure 6: "td(ON)-td(OFF) direct control mode"*.

Figure 3: RDS(on) measurement

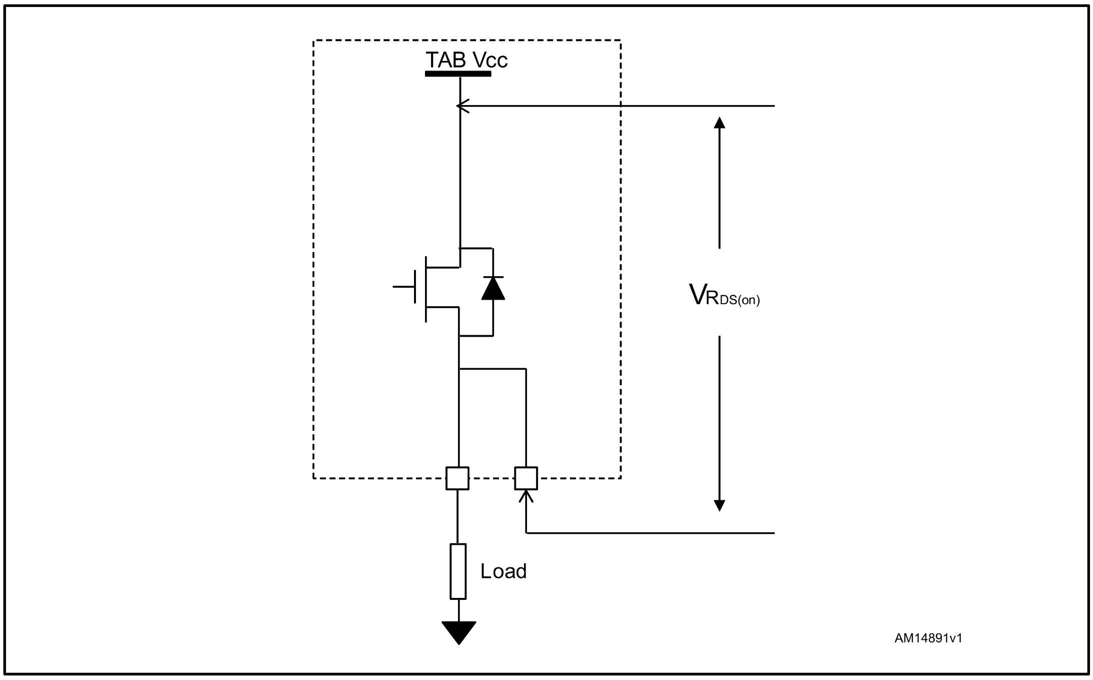


Figure 4: dV/dT

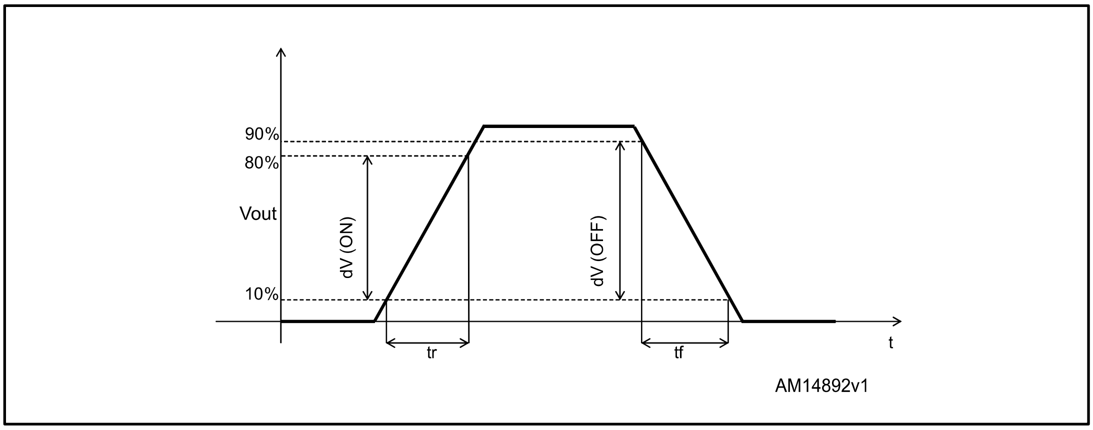


Figure 5: td(ON)-td(OFF) synchronous mode

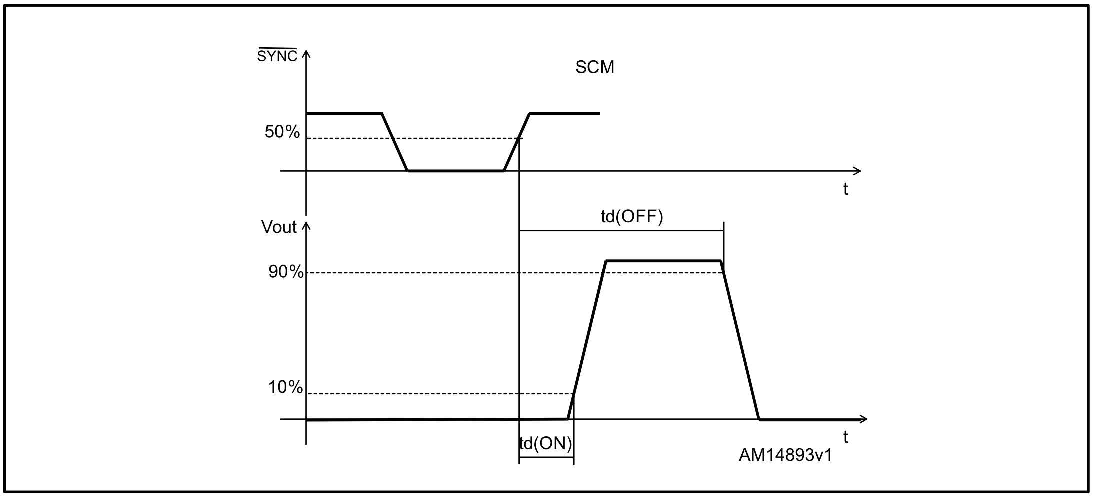


Figure 6: td(ON)-td(OFF) direct control mode

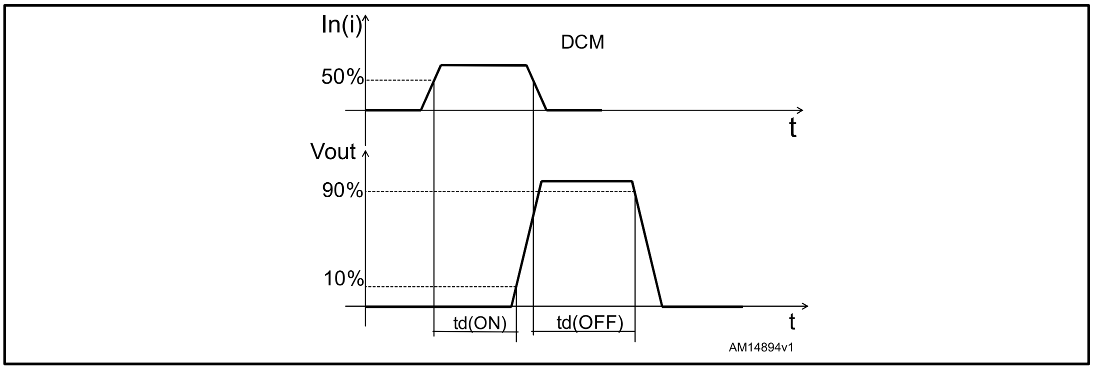


Table 8: Logic input and output

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Logic input pin low level voltage (INx, OUT_EN, $\overline{\text{LOAD}}$, $\overline{\text{SYNC}}$)		-0.3		0.3 x V_{dd}	V
V_{IH}	Logic input pin high level voltage (INx, OUT_EN, $\overline{\text{LOAD}}$, SYNC)		0.7 x V_{dd}		V_{dd} + 0.3	V
$V_{I(HYST)}$	Logic input hysteresis voltage (INx, OUT_EN, $\overline{\text{LOAD}}$, $\overline{\text{SYNC}}$)	V_{dd} = 5 V		100		mV
I_{IN}	Logic input pin current (INx, OUT_EN, $\overline{\text{LOAD}}$, $\overline{\text{SYNC}}$)	V_{IN} = 5 V	10			µA
t_{WM}	Power side watchdog time		272	320	400	µs

Table 9: Parallel interface timings (Vdd = 5 V; VCC= 24 V; -40 °C < T_J < 125 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{dis(SYNC)}$	$\overline{\text{SYNC}}$ disable time	Sync. control mode	10			µs
$t_{dis(DCM)}$	$\overline{\text{SYNC}}$, $\overline{\text{LOAD}}$ disable time	Direct control mode	80			ns
$t_{w(SYNC)}$	$\overline{\text{SYNC}}$ negative pulse width	Sync. control mode	20		195	µs
$t_{su(LOAD)}$	$\overline{\text{LOAD}}$ setup time	Sync. control mode	80			ns
$t_{h(LOAD)}$	$\overline{\text{LOAD}}$ hold time	Sync. control mode	400			ns
$t_{w(LOAD)}$	$\overline{\text{LOAD}}$ pulse width	Sync. control mode	240			ns
$t_{su(IN)}$	Input setup time		80			ns
$t_{h(IN)}$	Input hold time		10			ns
$t_{w(IN)}$	Input pulse width	Sync. control mode	160			ns
		Direct control mode	20			µs
t_{INLD}	IN to $\overline{\text{LOAD}}$ time	Direct control mode From IN variation to $\overline{\text{LOAD}}$ falling edge	80			ns
t_{LDIN}	$\overline{\text{LOAD}}$ to IN time	Direct control mode From $\overline{\text{LOAD}}$ falling edge to IN variation	400			ns
$t_{w(OUT\_EN)}$	OUT_EN pulse width		150			ns
$t_{p(OUT\_EN)}$	OUT_EN propagation delay			22	40	µs
$t_{jitter(SCM)}$	Jitter on single channel	Sync. mode			6	µs
$t_{jitter(DCM)}$		Direct mode			20	
$f_{refresh}$	Refresh delay			15		kHz

Table 10: Insulation and safety-related specifications

Symbol	Parameter	Test conditions	Value	Unit
CLR	Clearance (minimum external air gap)	Measured from input terminals to output terminals, the shortest distance through air	3.3	mm
CPG	Creepage (minimum external tracking)	Measured from input terminals to output terminals, the shortest distance path analog body	3.3	mm
CTI	Comparative tracking index (tracking resistance)	DIN IEC 112/VDE 0303 part 1	≥ 600	V
	Isolation group	Material group (DIN VDE 0110, 1/89), table 1	I	-

Table 11: IEC 60747-5-2 insulation characteristics

Symbol	Parameter	Test conditions	Value	Unit
V_{PR}	Input-to-output test voltage	Method a, type test $V_{PR} = V_{IORM} \times 1.6$, t_m= 10 s partial discharge < 5 pC	1500	V_{PEAK}
		Method b, 100% production test $V_{PR} = V_{IORM} \times 1.875$, t_m = 1 s partial discharge < 5 pC	1758	V_{PEAK}
V_{IOTM}	Transient overvoltage	Type test t_{ini} = 60 s	4245	V_{PEAK}
V_{IOSM}	Maximum surge insulation voltage	Type test	4245	V_{PEAK}
R_{IO}	Insulation resistance	V_{IO} = 500 V at t_s	$>10^9$	Ω
V_{ISO}	Insulation withstand voltage	1 min. type test	2500/3536	V_{rms}\\V_{PEAK}
$V_{ISO\ test}$	Insulation withstand test	1 s 100% production	3000/4245	V_{rms}\\V_{PEAK}

6 Functional description

6.1 Parallel interface

Smart parallel interface built-in ISO8200BQ offers three interfacing signals easily managed by a microcontroller.

The $\overline{\text{LOAD}}$ signal enables the input buffer storing the value of the channel inputs.

The $\overline{\text{SYNC}}$ signal copies the input buffer value into the transmission buffer and manages the synchronization between low voltage side and the channel outputs on the isolated side.

The OUT_EN signal enables the channel outputs.

An internal refresh signal updates the configuration of the channel outputs with a $f_{refresh}$ frequency. This signal can be disabled forcing low the $\overline{\text{SYNC}}$ input when $\overline{\text{LOAD}}$ is high.

$\overline{\text{SYNC}}$ and $\overline{\text{LOAD}}$ pins can be in direct control mode (DCM) or synchronous control mode (SCM).

The operation of these two signals is described as follows:

Table 12: Interface signal operation (general)

$\overline{\text{LOAD}}$	$\overline{\text{SYNC}}$	OUT_EN	Device behavior
Don't care	Don't care	Low (1)	The outputs are disabled (turned off)
High	High	High	The outputs are left unchanged
Low	High	High	The input buffer is enabled The outputs are left unchanged
High	Low	High	The internal refresh signal is disabled The transmission buffer is updated The outputs are left unchanged
Low	Low	High	The device operates in direct control mode as described in the respective paragraph

Notes:

(1)The outputs are turned off on OUT_EN falling edge and they are kept disabled as long as it is low.

6.1.1 Input signals (IN1 to IN8)

Inputs from IN1 to IN8 are the driving signals of the corresponding OUT1 to OUT8 outputs. Data are direct loaded on related outputs if $\overline{\text{SYNC}}$ and $\overline{\text{LOAD}}$ inputs are low (DCM operation) or stored into input buffer when $\overline{\text{LOAD}}$ is low and $\overline{\text{SYNC}}$ is high.

6.1.2 Load input data $\overline{\text{LOAD}}$

The input is active low; it stores the data from IN1 to IN8 into the input buffer.

6.1.3 Output synchronization $\overline{\text{SYNC}}$

The input is active low; it enables the ISO8200BQ transmission buffer loading input buffer data and manages the transmission between the two isolated sides of the device.

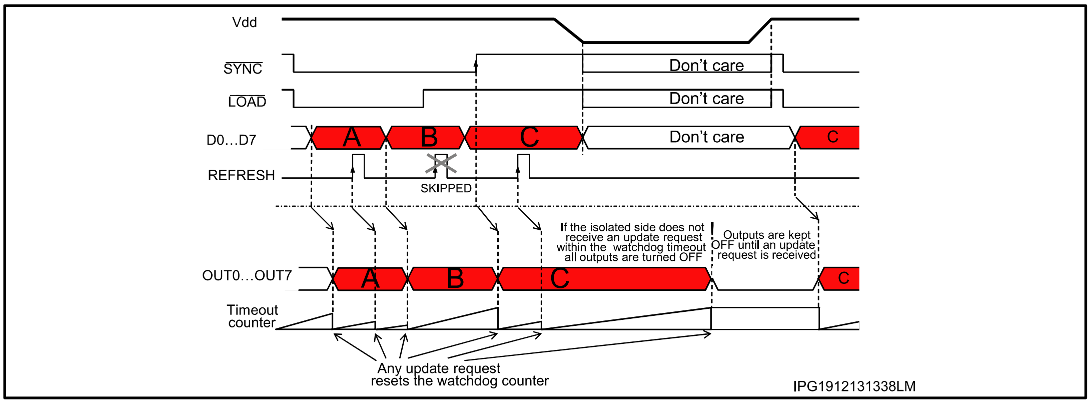
6.1.4 Watchdog

The isolated side of the device provides a watchdog function in order to guarantee a safe condition when V_{dd} supply voltage is missing.

If the logic side does not update the output status within t_{WD}, all outputs are disabled until a new update request is received.

The refresh signal is also considered a valid update signal, so the isolated side watchdog does not protect the system from a failure of the host controller (MCU freezing).

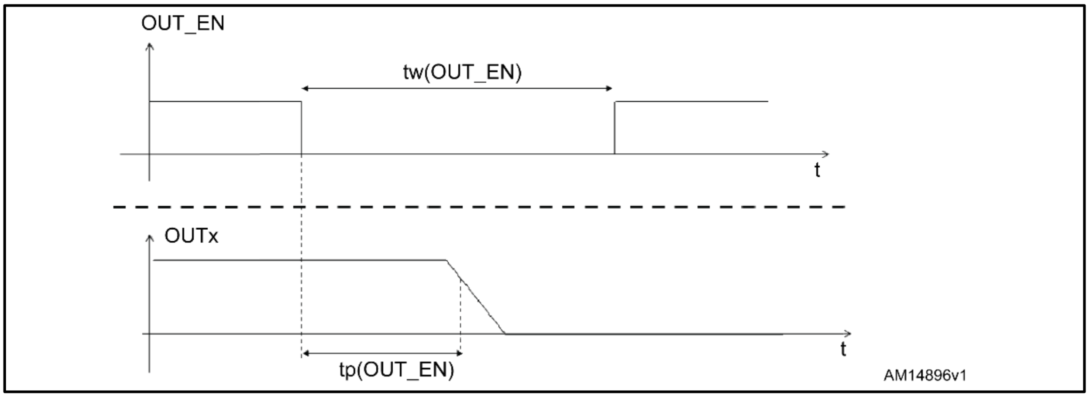
Figure 7: Watchdog behavior



6.1.5 Output enable (OUT_EN)

This pin provides a fast way to disable all outputs simultaneously. When the OUT_EN pin is driven low the outputs are disabled. To enable the output stage, the OUT_EN pin has to be raised. This timing execution is compatible with an external reset push, safety requirement, and allows, in a PLC system, the microcontroller polling to obtain all internal information during a reset procedure.

Figure 8: Output channel enable timing



6.2 Direct control mode (DCM)

When $\overline{\text{SYNC}}$ and $\overline{\text{LOAD}}$ inputs are driven by the same signal, the device operates in direct control mode (DCM).

In DCM the $\overline{\text{SYNC}}$ / $\overline{\text{LOAD}}$ signal operates as an active low input enable:

- when the signal is high, the current output configuration is kept regardless the input values
- when the signal is low, each channel input directly drives the respective output

This operation mode can also be set shorting both signals to the digital ground; in this case the channel outputs are always directly driven by the inputs except when OUT_EN is low (outputs disabled).

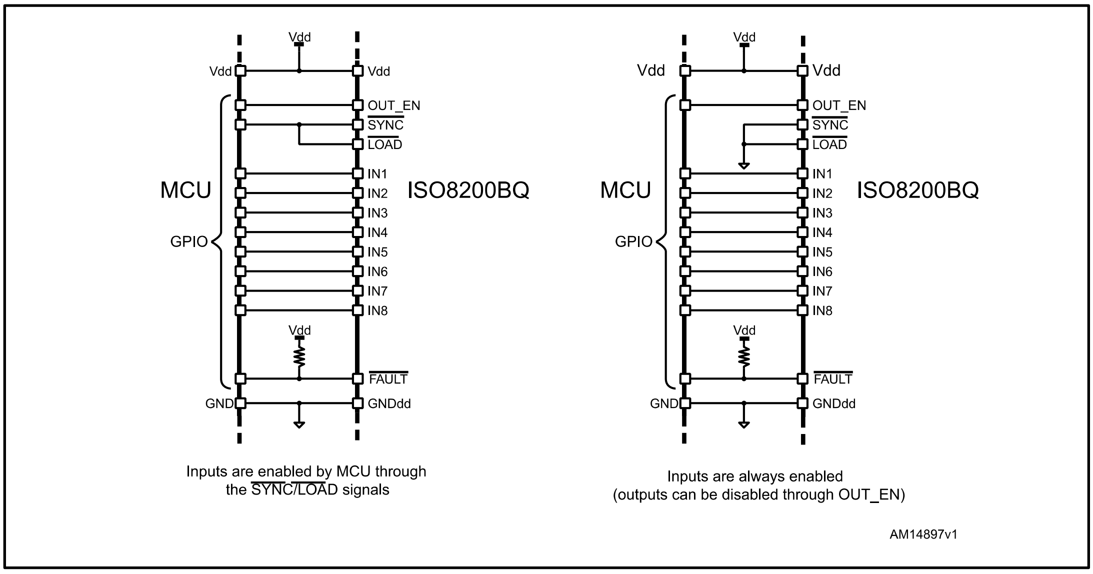
Table 13: Interface signal operation in direct control mode

$\overline{\text{SYNC}}$ / $\overline{\text{LOAD}}$	OUT_EN	Device behavior
Don’t care	Low (1)	The outputs are disabled (turned off)
High	High	The outputs are left unchanged
Low	High	The channel inputs drive the outputs

Notes:

(1) The outputs are turned off on OUT_EN falling edge and they are kept disabled as long as it is low.

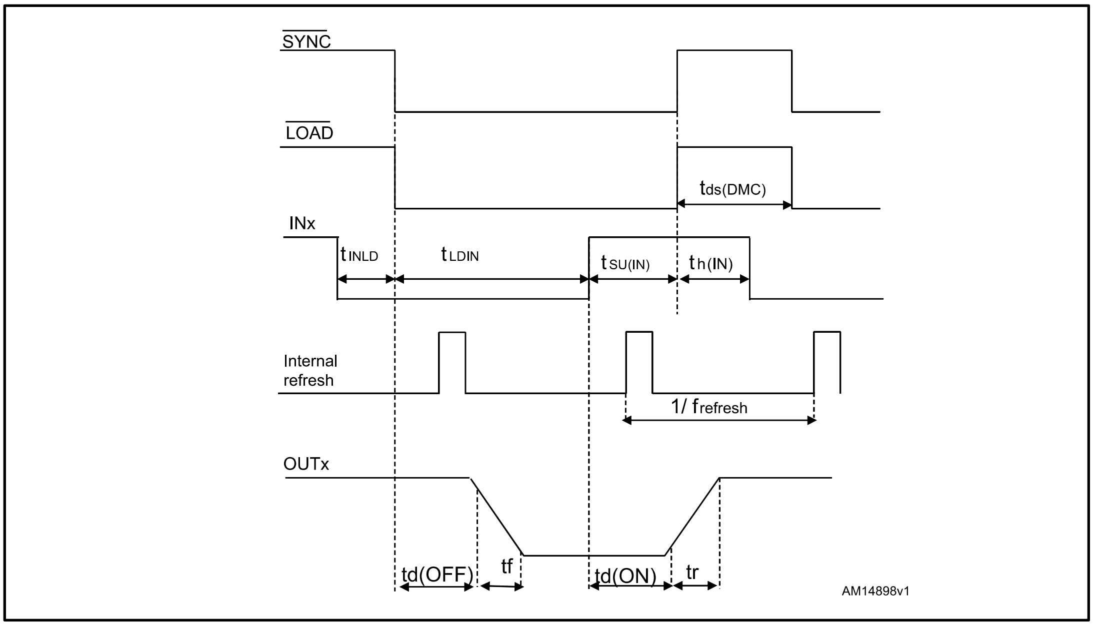
Figure 9: Direct control mode IC configuration



Inputs are enabled by MCU through the $\overline{\text{SYNC}}$/$\overline{\text{LOAD}}$ signals

Inputs are always enabled (outputs can be disabled through OUT_EN)

Figure 10: Direct control mode time diagram



6.3 Synchronous control mode (SCM)

When $\overline{\text{SYNC}}$ and $\overline{\text{LOAD}}$ inputs are independently driven, the device can operate in synchronous control mode (SCM). The SCM is used to reduce the jittering of the outputs and to drive all outputs of different devices at the same time.

In SCM the $\overline{\text{LOAD}}$ signal is forced low to update the input buffer while the $\overline{\text{SYNC}}$ signal is high. The $\overline{\text{LOAD}}$ signal is raised and the $\overline{\text{SYNC}}$ one is forced low for at least $t_{SYNC(SCM)}$. During this period, the internal refresh is disabled and any pending transmission between the low voltage and the isolated side is completed. When the $\overline{\text{SYNC}}$ signal is raised the channel output configuration is changed according to the one stored in the input. If the $t_{SYNC(SCM)}$ limit is met, the maximum jitter of the channel outputs is t_{jitter}(SCM).

If more devices share the same $\overline{\text{SYNC}}$ signal, all device outputs change simultaneously with a maximum jitter related to maximum delay and maximum jitter for single device.

Table 14: Interface signal operation in synchronous control mode

$\overline{\text{LOAD}}$	$\overline{\text{SYNC}}$	OUT_EN	Device behavior
Don't care	Don't care	Low (1)	The outputs are disabled (turned off)
High	High	High	The outputs are left unchanged
Low	High	High	The input buffer is enabled The outputs are left unchanged
High	Low	High	The internal refresh signal is disabled The transmission buffer is updated The outputs are left unchanged
High	Rising edge	High	The outputs are updated according to the current transmission buffer value

$\overline{\text{LOAD}}$	$\overline{\text{SYNC}}$	OUT_EN	Device behavior
Low	Low	High	Should be avoided (DCM operation only)

Notes:

[1] The outputs are turned off on OUT_EN falling edge and they are kept disabled as long as it is low.

Figure 11: Synchronous control mode IC configuration

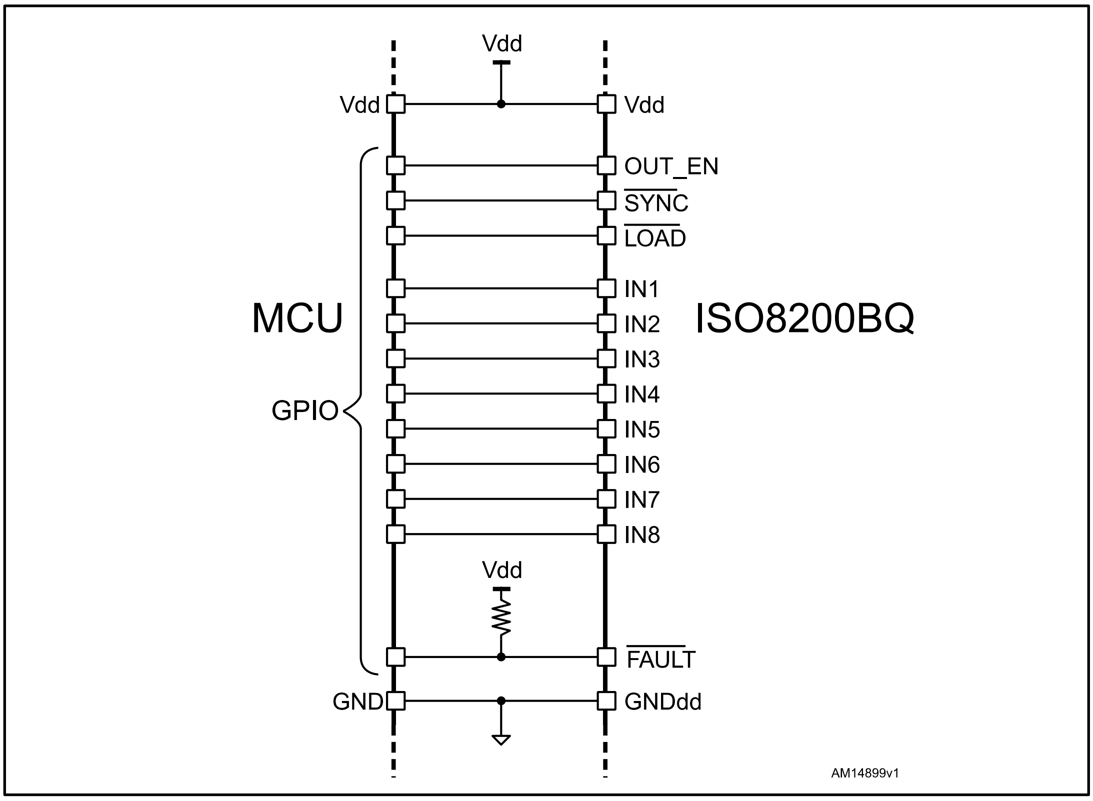


Figure 12: Synchronous control mode time diagram

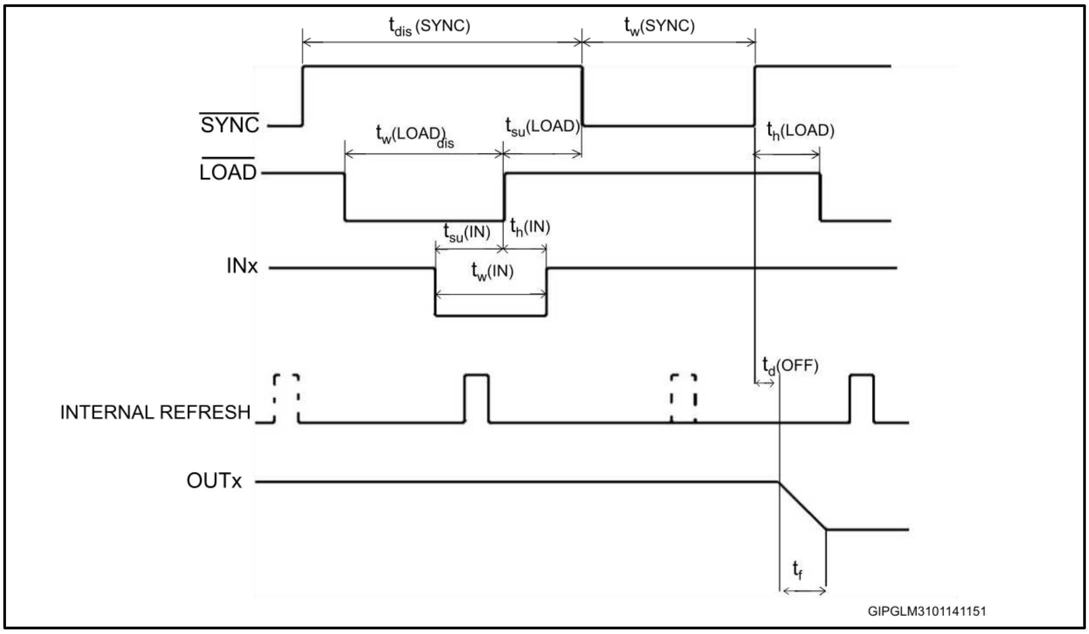
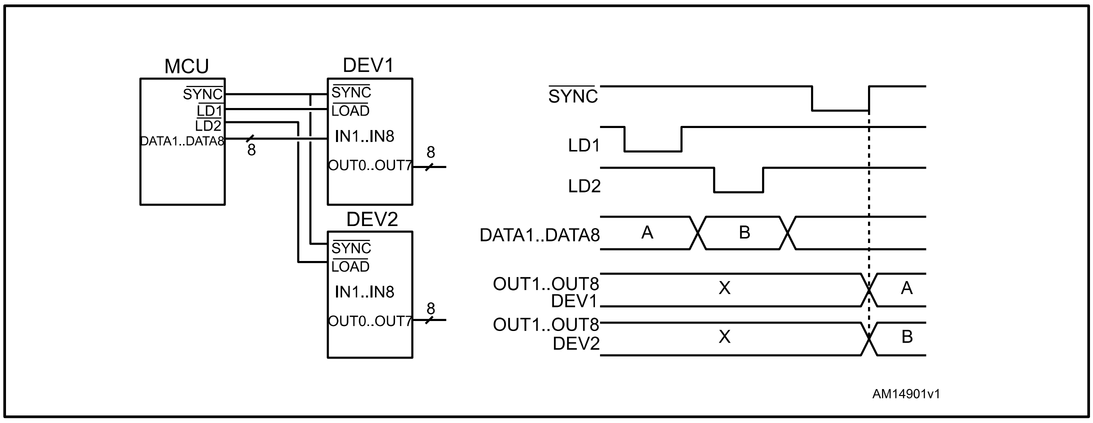


Figure 13: Multiple device synchronous control mode



6.4 Fault indication

The $\overline{\text{FAULT}}$ pin is an active low open-drain output indicating fault conditions. This pin is active when at least one of the following conditions occurs:

- Junction overtemperature of one or more channels ($T_J > T_{TJSD}$)
- Communication error

The communication error is intended as an internal data corruption event in the data transfer through isolation. In case of communication error the outputs are initially kept in the previous status and then reset (turned off) at the first communication error during data transfer of the refresh signal.

6.4.1 Junction overtemperature and case overtemperature

The thermal status of the device is updated during each transmission sequence between the two isolated sides.

In SCM operation, when the $\overline{\text{LOAD}}$ signal is high and the $\overline{\text{SYNC}}$ one is low, the communication is disabled. In this case the thermal status of the device cannot be updated and the $\overline{\text{FAULT}}$ indication can be different from the current status.

In any case, the thermal protection of the channel outputs is always operative.

Figure 14: Thermal status update (DCM)

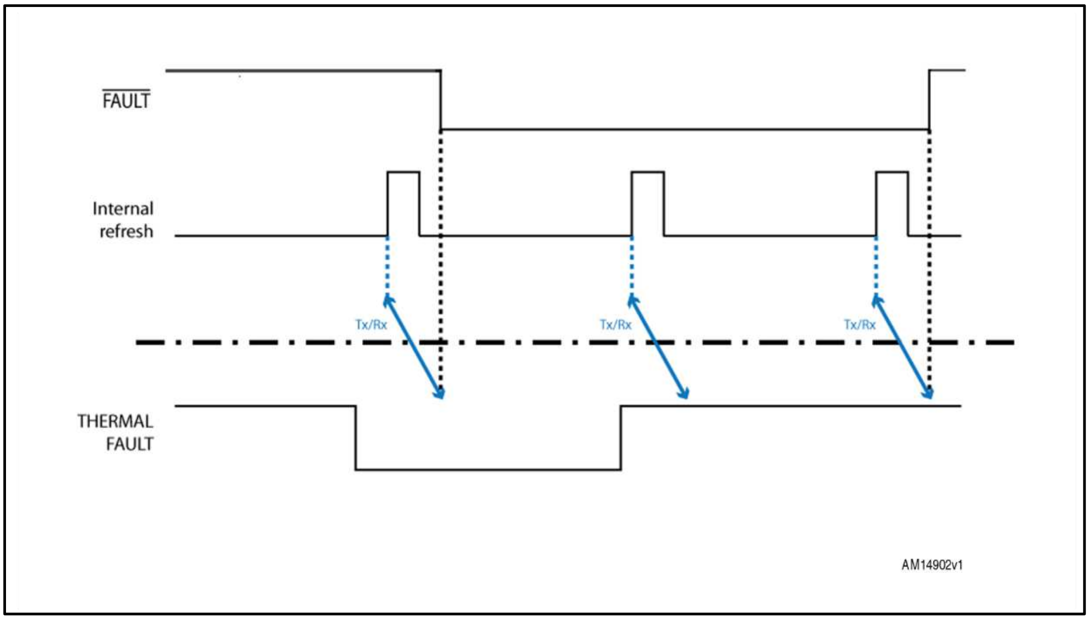
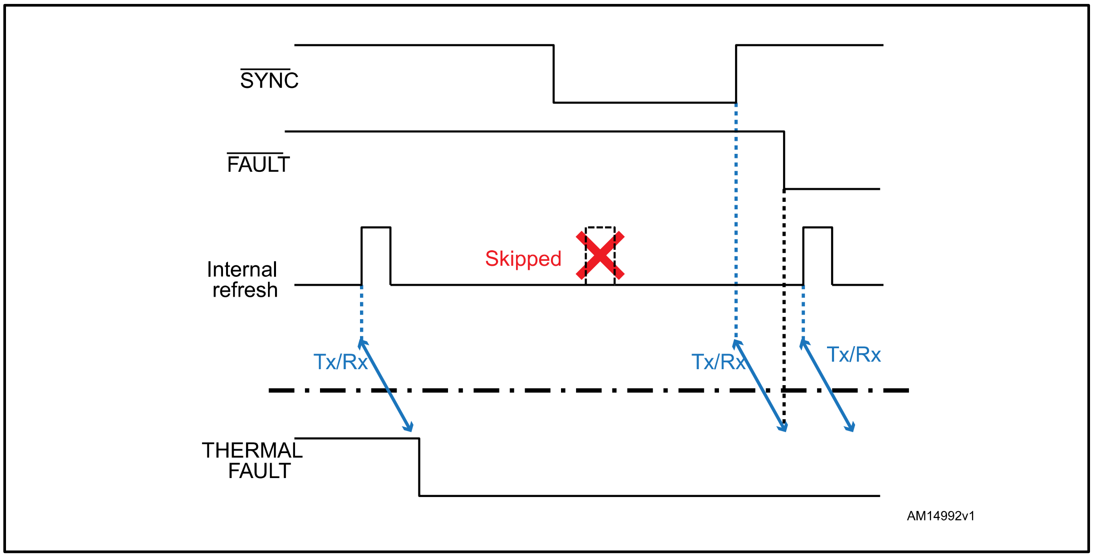


Figure 15: Thermal status update (SCM)



7 Power section

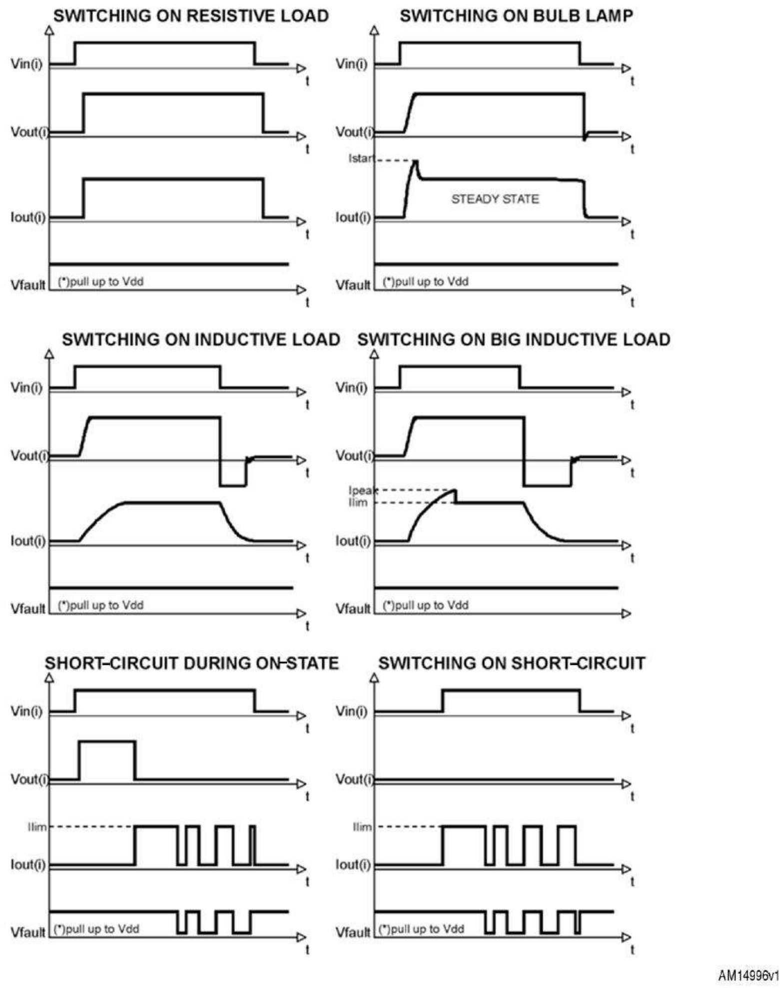
7.1 Current limitation

The current limitation process is active when the current sense connected on the output stage measures a current value, which is higher than a fixed threshold.

When this condition is verified the gate voltage is modulated to avoid the increase of the output current over the limitation value.

Figure below shows typical output current waveforms with different load conditions.

Figure 16: Current limitation with different load conditions



7.2 Thermal protection

The device is protected against overheating in case of overload conditions. During the driving period, if the output is overloaded, the device suffers two different thermal stresses, the former related to the junction, and the latter related to the case.

The two faults have different trigger thresholds: the junction protection threshold is higher than the case protection one; generally the first protection, that is active in thermal stress conditions, is the junction thermal shutdown. The output is turned off when the temperature is higher than the related threshold and turned back on when it goes below the reset threshold. This behavior continues until the fault on the output is present.

If the thermal protection is active and the temperature of the package increases over the fixed case protection threshold, the case protection is activated and the output is switched off and back on when the junction temperature of each channel in fault and case temperature is below the respective reset thresholds.

Figure 17: "Thermal protection flowchart" shows the thermal protection behavior, while *Figure 18: "Thermal protection"* reports typical temperature trends and output vs. input state.

Figure 17: Thermal protection flowchart

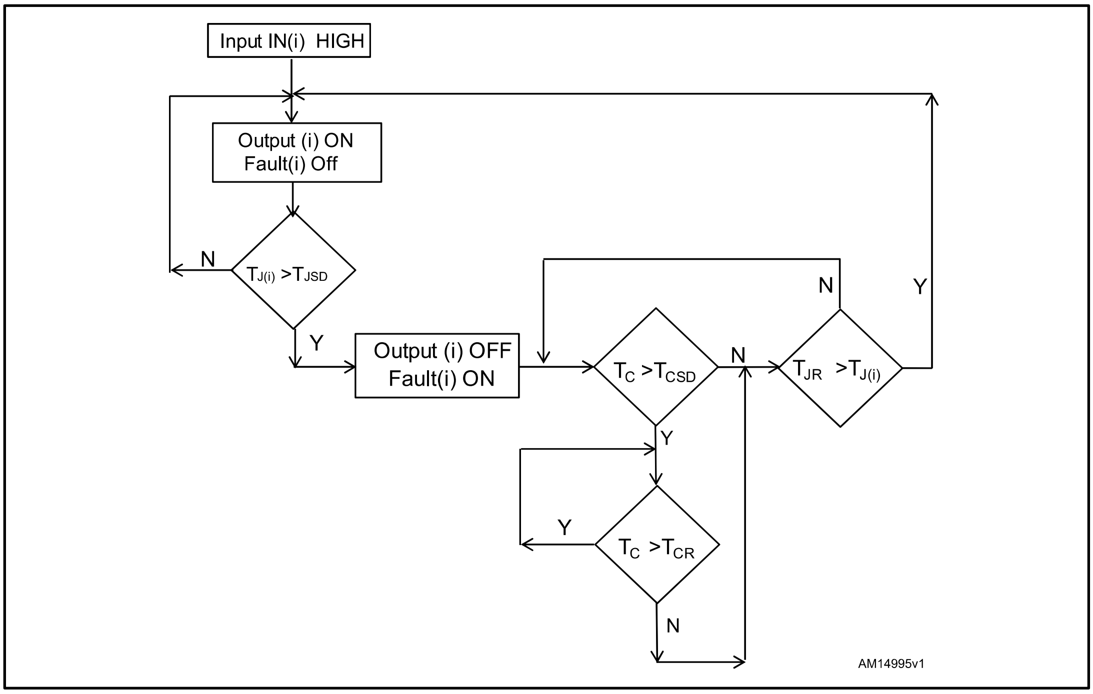


Figure 18: Thermal protection