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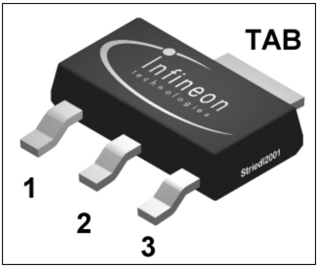
Smart Lowside Power Switch
For Industrial Applications

HITFET® ISP 75N

Data Sheet V 1.4

Features

- Lead free
- Logic Level Input
- Input protection (ESD)
- Thermal shutdown with auto restart
- Overload protection
- Short circuit protection
- Overvoltage protection
- Current limitation



Application

- All kinds of resistive, inductive and capacitive loads in industrial applications
- µC compatible power switch for 12 V and 24 V DC applications and for 42 Volt Powernet
- Replaces electromechanical relays and discrete circuits

General Description

N channel vertical power FET in Smart Power Technology, protected by embedded protection functions.

Type	Ordering Code	Package
HITFET® ISP 75N	on request	PG-SOT223-4

Product Summary

Parameter	Symbol	Value	Unit
Continuous drain source voltage	V_{DS}	60	V
On-state resistance	$R_{DS(ON)}$	550	mΩ
Current limitation	$I_{D(lim)}$	1	A
Nominal load current	$I_{D(Nom)}$	0.7	A
Clamping energy	E_{AS}	550	mJ

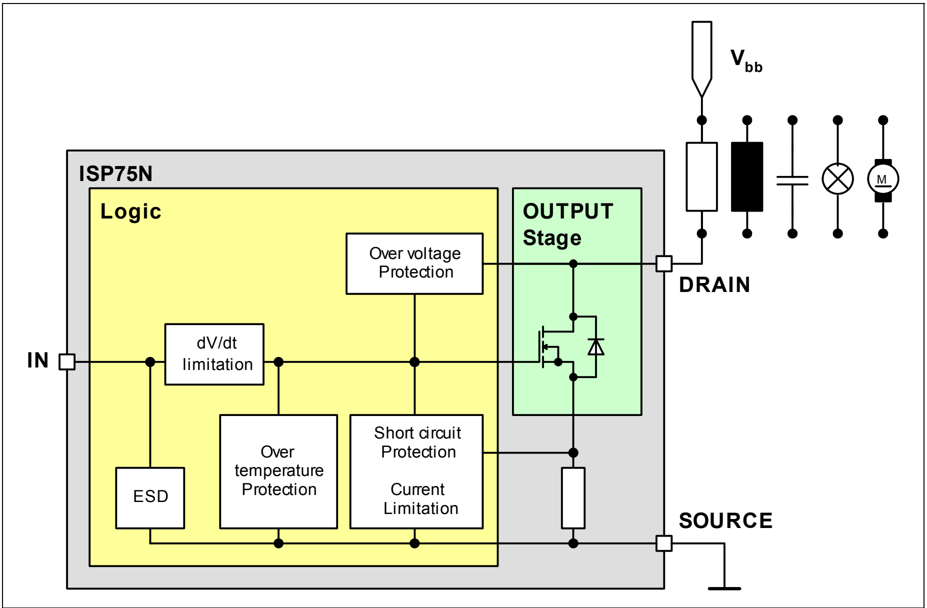


Figure 1 Block Diagram

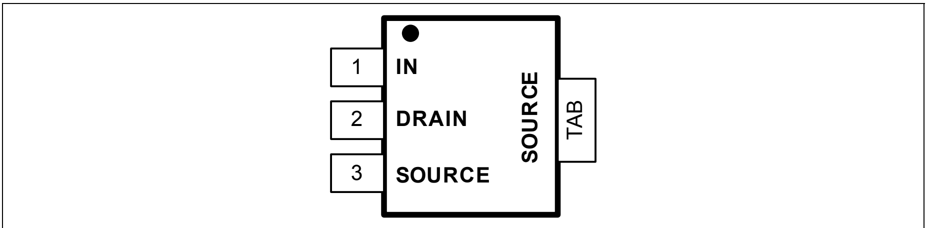


Figure 2 Pin Configuration

Pin Definitions and Functions

Pin No.	Symbol	Function
1	IN	**Input**; activates output and supplies internal logic
2	DRAIN	**Output to the load**
3 + TAB	SOURCE	**Ground**; pin3 and TAB are internally connected

Circuit Description

The ISP 75N is a monolithic power switch in Smart Power Technology (SPT) with a logic level input, an open drain DMOS output stage and integrated protection functions. It is designed for all kind of resistive and inductive loads (relays, solenoid) in industrial applications.

Protection Functions

Note: The device provides embedded protection functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operation.

- **Over voltage protection:** An internal clamp limits the output voltage at $V_{DS(AZ)}$ (min. 60V) when inductive loads are switched off.
- **Current limitation:** By means of an internal current measurement the drain current is limited at $I_{D(lim)}$ (1.4 - 1.5 A typ.). If the current limitation is active the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. This operation leads to an increasing junction temperature until the over temperature threshold is reached.
- **Over temperature and short circuit protection:** This protection is based on sensing the chip temperature. The location of the sensor ensures a fast and accurate junction temperature detection. Over temperature shutdown occurs at minimum 150 °C. A hysteresis of typ. 10 K enables an automatic restart by cooling.

The device is ESD protected according Human Body Model (4 kV) and load dump protected (see Maximum Ratings).

Absolute Maximum Ratings

T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Values	Unit	Remarks
Continuous drain source voltage [1]	V_{DS}	60	V	–
Drain source voltage for short circuit protection	V_{DS}	36	V	–
Continuous input voltage	V_{IN}	-0.2 … +10	V	–
Peak input voltage	V_{IN}	-0.2 … +20	V	–
Continuous Input Current -0.2V ≤ V_{IN} ≤ 10V V_{IN}<-0.2V or V_{IN}>10V	I_{IN}	 no limit | I_{IN} |≤ 2mA	mA	–
Junction Temperature Operating temperature range Storage temperature range	T_j T_a T_{stg}	150 -30 … +85 -40 … +105	°C	–
Power dissipation (DC)	P_{tot}	1.8	W	–
Unclamped single pulse inductive energy	E_{AS}	550	mJ	$I_{D(ISO)}$ = 0.7 A; V_{bb} =32V
Load dump protection [2] IN = low or high (8 V); R_L = 50 Ω IN = high (8 V); R_L = 22 Ω	$V_{LoadDump}$	 80 47	V	$V_{LoadDump}$ = V_P + V_S; V_P = 13.5 V R_I[3] = 2 Ω; t_d = 400 ms;
Electrostatic discharge voltage (Human Body Model) according to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 - 1993	V_{ESD}	4000	V	–
JEDEC humidity category J-STD-20-C	–	MSL3/260	–	–
IEC climatic category, DIN IEC 68-1	–	40/150/56	–	–

Thermal Resistance

Junction soldering point	R_{thJS}	≤ 10	K/W	–
Junction - ambient[4]	R_{thJA}	≤ 70	K/W	–

1) See also **Figure 7** and **Figure 10**.

2) $V_{LoadDump}$ is setup without DUT connected to the generator per ISO 7637-1 and DIN 40 839. See also **page 7**.

3) R_I = internal resistance of the load dump test pulse generator LD200.

[4)] Device on epoxy pcb 40 mm × 40 mm × 1.5 mm with 6 cm^2 copper area for pin 4 connection.

Electrical Characteristics

T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Static Characteristics						
Drain source clamp voltage	$V_{DS(AZ)}$	60	–	75	V	I_D = 10 mA, T_j = -40 … +150 °C
Off state drain current	I_{DSS}	–	–	5	µA	V_{IN} = 0 V, V_{DS} = 32 V, T_j = -40 … +150 °C
Input threshold voltage	$V_{IN(th)}$	1	1.8	2.5	V	I_D = 10 mA
Input current:					µA	V_{IN} = 5 V
normal operation, $I_D < I_{D(lim)}$:	$I_{IN(1)}$	–	100	200		
current limitation mode, $I_D = I_{D(lim)}$:	$I_{IN(2)}$	–	250	400		
After thermal shutdown, I_D = 0 A:	$I_{IN(3)}$	1000	1500	2000		
On-state resistance	$R_{DS(on)}$				mΩ	I_D = 0.7 A, V_{IN} = 5 V
T_j = 25 °C		–	490	675		
T_j = 150 °C		–	850	1350		
On-state resistance	$R_{DS(on)}$				mΩ	I_D = 0.7 A, V_{IN} = 10 V
T_j = 25 °C		–	430	550		
T_j = 150 °C		–	750	1000		
Nominal load current	$I_{D(Nom)}$	0.7	–	–	A	V_{BB} = 12 V, V_{DS} = 0.5 V, T_S = 85 °C, T_j < 150 °C
Current limit	$I_{D(lim)}$	1	1.5	1.9	A	V_{IN} = 10 V, V_{DS} = 12 V
Dynamic Characteristics [1)]						
Turn-on time V_{IN} to 90% I_D:	t_{on}	–	10	20	µs	R_L = 22 Ω, V_{IN} = 0 to 10 V, V_{BB} = 12 V

Electrical Characteristics (cont'd)
T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Turn-off time V_{IN} to 10% I_D:	t_{off}	–	10	20	µs	R_L = 22 Ω, V_{IN} = 10 to 0 V, V_{BB} = 12 V
Slew rate on 70 to 50% V_{BB}:	$-dV_{DS}/dt_{on}$	–	5	10	V/µs	R_L = 22 Ω, V_{IN} = 0 to 10 V, V_{BB} = 12 V
Slew rate off 50 to 70% V_{BB}:	dV_{DS}/dt_{off}	–	10	15	V/µs	R_L = 22 Ω, V_{IN} = 10 to 0 V, V_{BB} = 12 V

Protection Functions[2)]

Thermal overload trip temperature	T_{jt}	150	165	180	°C	–
Thermal hysteresis	ΔT_{jt}	–	10	–	K	–
Unclamped single pulse inductive energy T_j = 25 °C	E_{AS}	550	–	–	mJ	$I_{D(ISO)}$ = 0.7 A, V_{BB} = 32 V
T_j = 150 °C		200	–	–		

Inverse Diode

Continuous source drain voltage	V_{SD}	–	1	–	V	V_{IN} = 0 V, $-I_D$ = 2 × 0.7 A

1) See also **Figure 9**.

2) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous, repetitive operation.

EMC-Characteristics

The following EMC-Characteristics outline the behavior of typical devices. They are not part of any production test.

Table 1 Test Conditions

Parameter	Symbol	Value	Unit	Remark
Temperature	T_A	23 ±5	°C	–
Supply Voltage	V_S	13.5	V	–
Load	R_L	27	Ω	ohmic
Operation mode	PWM DC	– –	– –	f_{INx}=100Hz, D=0.5 ON / OFF
DUT specific	V_{IN}('HIGH')=5V			

Fast electrical transients

acc. to ISO 7637

Test[1)] Pulse	Max. Test Level	Test Result		Pulse Cycle Time and Generator Impedance
		ON	OFF	
1	-200V	C	C	500ms ; 10Ω
2	+200V	C	C	500ms ; 10Ω
3a	-200V	C	C	100ms ; 50Ω
3b	+200V	C	C	100ms ; 50Ω
4	-7V	C	C	0.01Ω
5	175V	E(65V)	E(75V)	400ms ; 2Ω

1) The test pulses are applied at V_S

Definition of functional status

Class	Content
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more function of a device does not perform as designed after exposure and can not be returned to proper operation without repairing or replacing the device. The value after the character shows the limit.

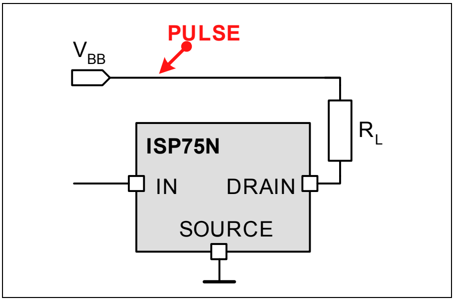
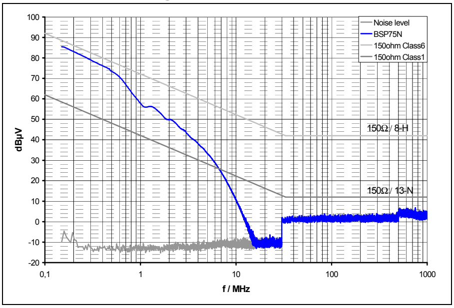


Figure 3 Test circuit for ISO pulse

Conducted Emissions

Acc. IEC 61967-4 (1Ω/150Ω method)

Typ. V_{bb} Emissions at PWM-mode with 150Ω-matching network



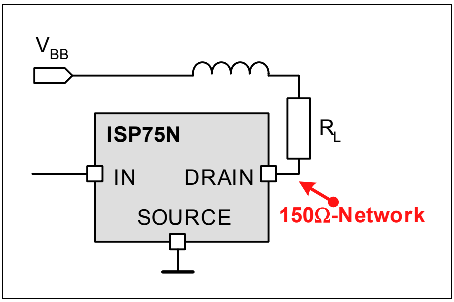


Figure 4 Test circuit for conducted emission [1)]

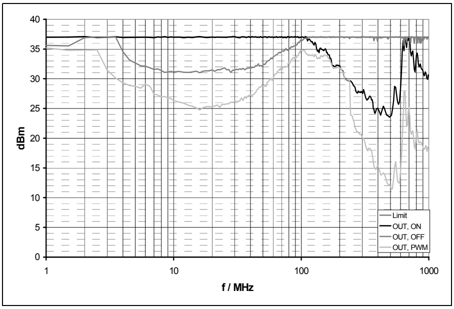
Conducted Susceptibility

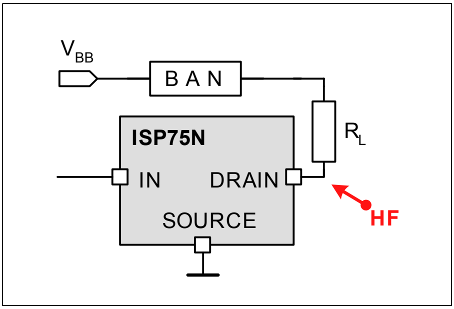
Acc. 47A/658/CD IEC 62132-4 (Direct Power Injection)

Direct Power Injection: Forward Power CW

Failure Criteria: Amplitude or frequency variation max. 10% at OUT

Typ. V_{bb} Susceptibility at DC-ON/OFF and at PWM





Test circuit for conducted susceptibility [2)]

---

1) For defined de coupling and high reproducibility a defined choke (5µH at 1MHz) is inserted in the Vbb-Line.

2) Broadband Artificial Network (short: BAN) consists of the same choke (5µH at 1MHz) and the same 150 Ohm-matching network as for emission measurement for defined de coupling and high reproducibility.

Block diagram

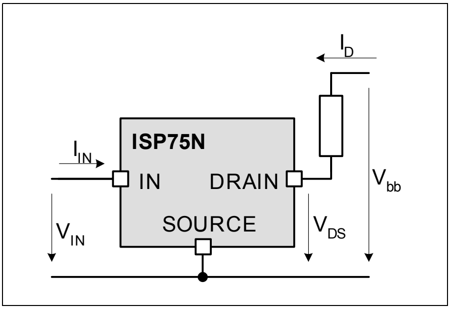


Figure 5 Terms

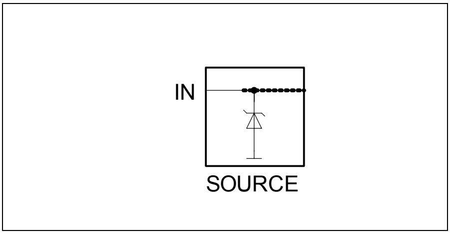


Figure 6 Input Circuit (ESD protection)

ESD zener diodes are not designed for DC current.

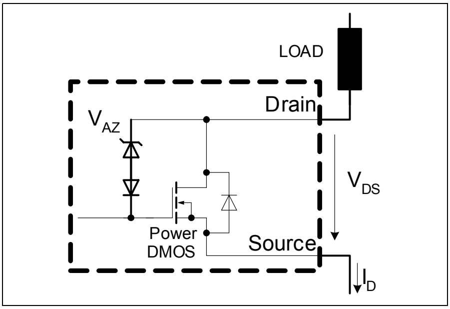


Figure 7 Inductive and Over voltage Output Clamp

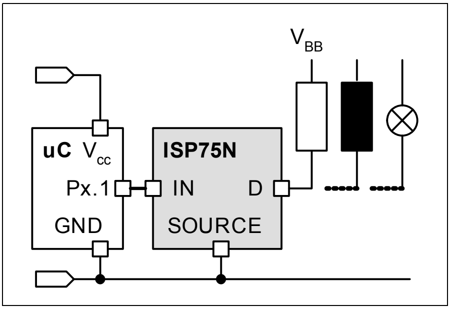


Figure 8 Application Circuit

Timing diagrams

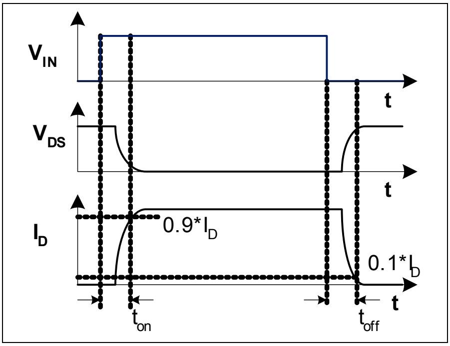


Figure 9 **Switching a Resistive Load**

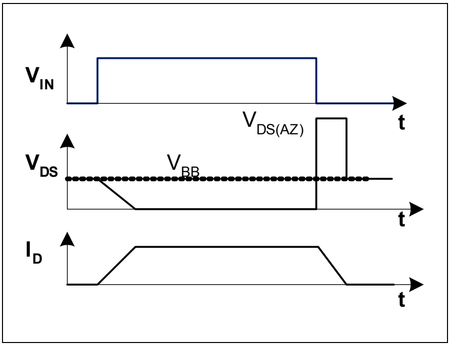


Figure 10 **Switching an Inductive Load**

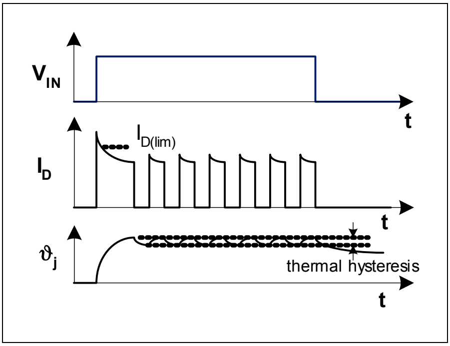
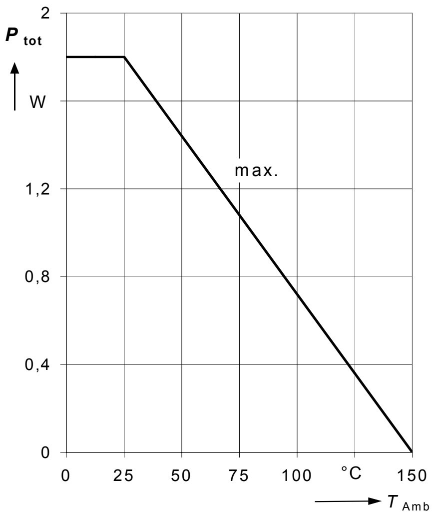
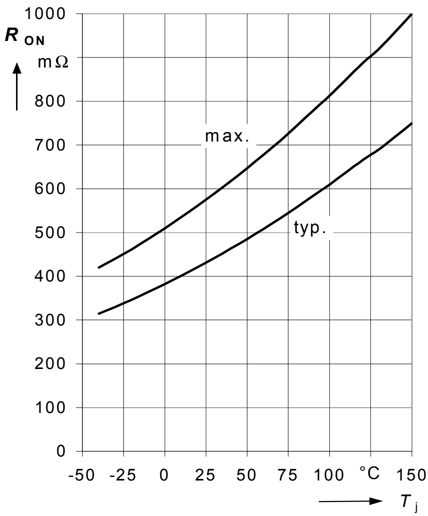


Figure 11 **Short circuit**

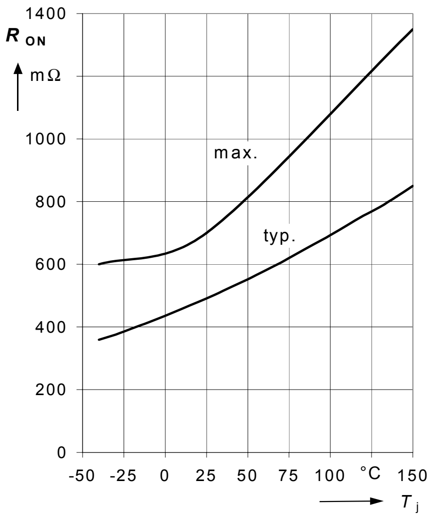
1 Max. allowable power dissipation
$P_{tot} = f(T_{Amb})$



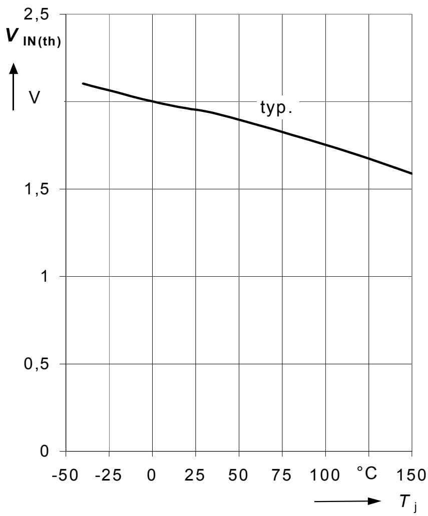
2 On-state resistance $R_{ON} = f(T_j)$;
$I_D = 0.7$ A; $V_{IN} = 10$ V



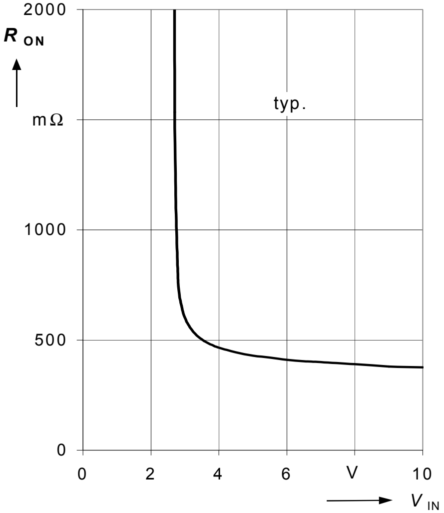
3 On-state resistance $R_{ON} = f(T_j)$;
$I_D = 0.7$ A; $V_{IN} = 5$ V



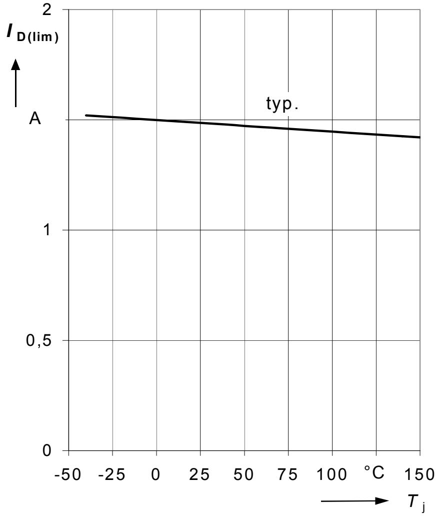
4 Typ. input threshold voltage
$V_{IN(th)} = f(T_j)$; $I_D = 10$ mA; $V_{DS} = 12$ V



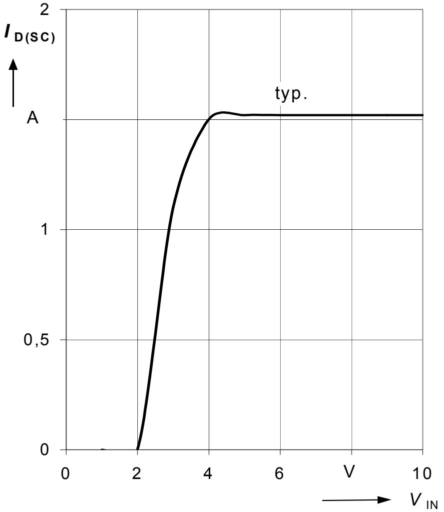
5 Typ. on-state resistance $R_{ON} = f(V_{IN})$;
I_D = 0.7 A; T_j = 25 °C



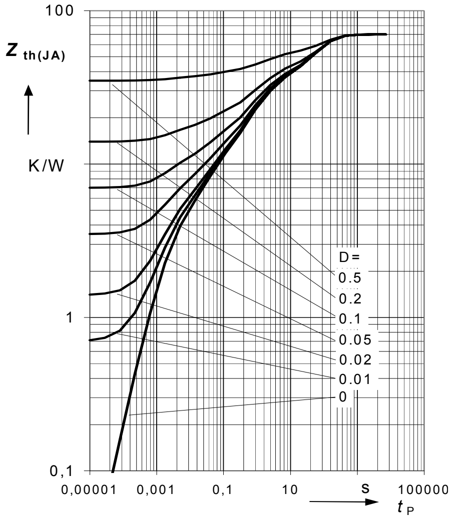
6 Typ. current limitation $I_{D(lim)} = f(T_j)$;
V_{DS} = 12 V, V_{IN} = 10 V



7 Typ. short circuit current
$I_{D(SC)} = f(V_{IN})$; V_{DS} = 12 V, T_j = 25 °C



8 Max. transient thermal impedance
$Z_{thJA} = f(t_p)$ @ 6cm²; Parameter: D = t_p/T



1 Package Outlines HITFET® ISP 75N

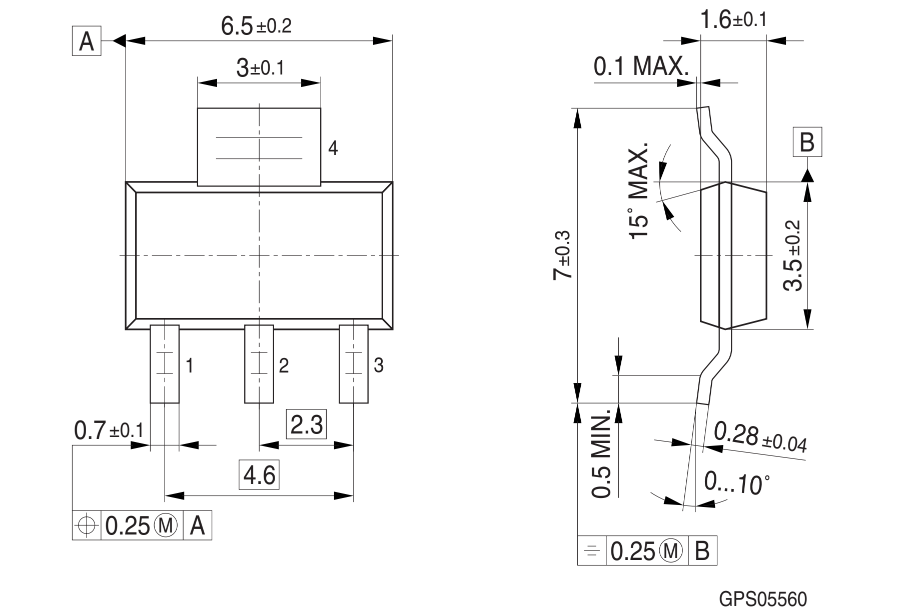


Figure 12 PG-SOT223-4

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Dimensions in mm

2 Revision History

Version	Date	Changes
V1.4	2008-04-14	package naming updated to PG-SOT223-4
V1.3	2006-11-20	changed the term “industry” to “industrial” to make it clear that this device is not targeted for automotive use
V1.2	2006-08-08	added Junction Temperature in maximum ratings
V1.1	2006-08-02	first released version

Edition 2008-04-14

**Published by Infineon Technologies AG,
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