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ispLSI® 1016 Device Datasheet

September 2010

All Devices Discontinued!

Product Change Notifications (PCNs) have been issued to discontinue all devices in this data sheet.

The original datasheet pages have not been modified and do not reflect those changes. Please refer to the table below for reference PCN and current product status.

Product Line	Ordering Part Number	Product Status	Reference PCN
ispLSI 1016	ispLSI 1016-60LJ	**Discontinued**	PCN#13-10
	ispLSI 1016-80LJ		
	ispLSI 1016-90LJ		
	ispLSI 1016-110LJ		
	ispLSI 1016-60LJI		
	ispLSI 1016-60LT44		
	ispLSI 1016-80LT44		
	ispLSI 1016-90LT44		
	ispLSI 1016-60LT44I		
	ispLSI 1016-60LH/883 5962-9476201MXC		PCN#05A-10

ispLSI® 1016

In-System Programmable High Density PLD

Lattice Semiconductor Corporation

Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - **High-Speed Global Interconnect**
  - **2000 PLD Gates**
  - **32 I/O Pins, Four Dedicated Inputs**
  - **96 Registers**
  - **Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **Small Logic Block Size for Random Logic**
  - **Security Cell Prevents Unauthorized Copying**

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **$f$max = 110 MHz Maximum Operating Frequency**
  - **$f$max = 60 MHz for Industrial and Military/883 Devices**
  - **$t$pd = 10 ns Propagation Delay**
  - **TTL Compatible Inputs and Outputs**
  - **Electrically Erasable and Reprogrammable**
  - **Non-Volatile E²CMOS Technology**
  - **100% Tested**

- **IN-SYSTEM PROGRAMMABLE**
  - **In-System Programmable™ (ISP™) 5-Volt Only**
  - **Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality**
  - **Reprogram Soldered Devices for Faster Debugging**

- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEX-IBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **Three Dedicated Clock Input Pins**
  - **Synchronous and Asynchronous Clocks**
  - **Flexible Pin Placement**
  - **Optimized Global Routing Pool Provides Global Interconnectivity**

Functional Block Diagram
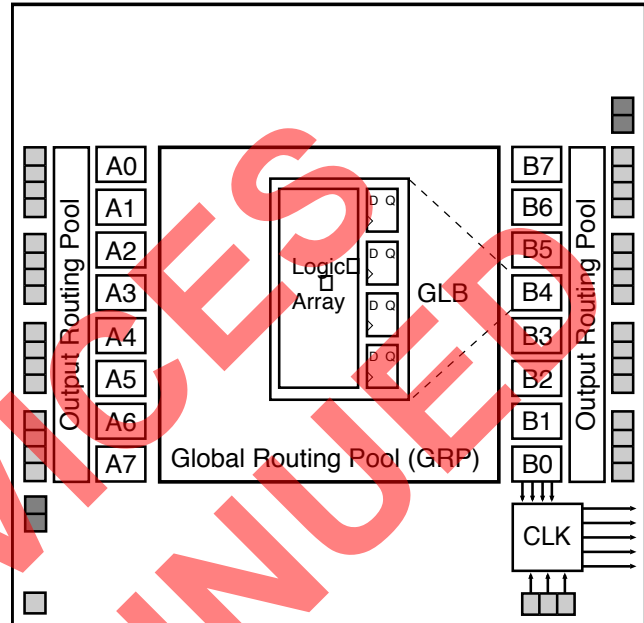
Description

The ispLSI 1016 is a High-Density Programmable Logic Device containing 96 Registers, 32 Universal I/O pins, four Dedicated Input pins, three Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1016 features 5-Volt in-system programming and in-system diagnostic capabilities. It is the first device which offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 1016 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. B7 (see figure 1). There are a total of 16 GLBs in the ispLSI 1016 device. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

Functional Block Diagram

Figure 1. ispLSI 1016 Functional Block Diagram
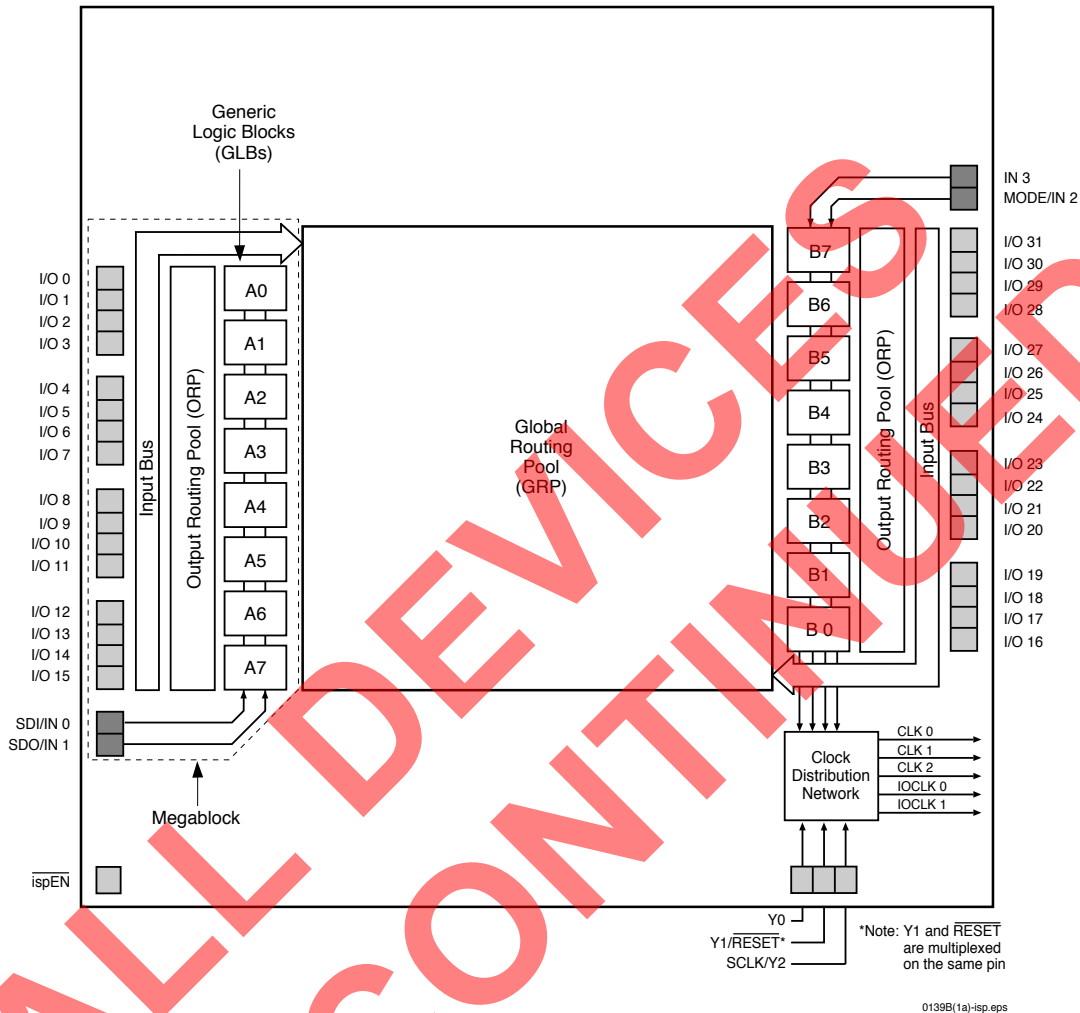
The device also has 32 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The ispLSI 1016 device contains two of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 1016 device are selected using the Clock Distribution Network. Three dedicated clock pins (Y0, Y1 and Y2) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (B0 on the ispLSI 1016 device). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings [1]

Supply Voltage V$_{CC}$ .... -0.5 to +7.0V

Input Voltage Applied .... -2.5 to V$_{CC}$ +1.0V

Off-State Output Voltage Applied ..... -2.5 to V$_{CC}$ +1.0V

Storage Temperature .... -65 to 150°C

Case Temp. with Power Applied .... -55 to 125°C

Max. Junction Temp. (T$_J$) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V$_{CC}$	Supply Voltage	Commercial	T$_A$ = 0°C to +70°C	4.75	5.25	V
		Industrial	T$_A$ = -40°C to +85°C	4.5	5.5	
		Military/883	T$_C$ = -55°C to +125°C	4.5	5.5	
V$_{IL}$	Input Low Voltage			0	0.8	V
V$_{IH}$	Input High Voltage			2.0	V$_{CC}$ + 1	V

Table 2- 0005Aisp w/mil.eps

Capacitance (T$_A$=25°C, f=1.0 MHz)

SYMBOL	PARAMETER		MAXIMUM	UNITS	TEST CONDITIONS
C$_1$	Dedicated Input Capacitance	Commercial/Industrial	8	pf	V$_{CC}$=5.0V, V$_{IN}$=2.0V
		Military	10	pf	V$_{CC}$=5.0V, V$_{IN}$=2.0V
C$_2$	I/O and Clock Capacitance		10	pf	V$_{CC}$=5.0V, V$_{I/O}$, V$_Y$=2.0V

1. Guaranteed but not 100% tested.

Table 2- 0006

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	—	Years
Erase/Reprogram Cycles	10000	—	Cycles

Table 2- 0008B

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

3-state levels are measured 0.5V from steady-state active level.

Table 2- 0003

Figure 2. Test Load
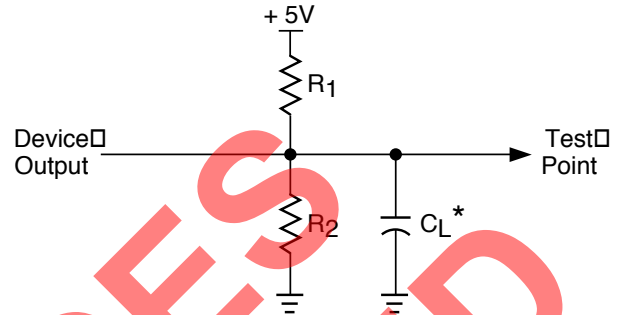
*C_L includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

Table 2- 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)		–	–	-10	μA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}		–	–	10	μA
I_{IL-isp}	isp Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)		–	–	-150	μA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	μA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2,4]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V f_{TOGGLE} = 1 MHz	Commercial	–	100	150	mA
			Industrial/Military	–	100	170	mA

1. One output at a time for a maximum duration of one second. V_{out} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using four 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this datasheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC}.

Table 2-0007A-16 w/mil

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-110 MIN.	-110 MAX.	-90 MIN.	-90 MAX.	UNITS
t_{pd1}	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	—	10	—	12	ns
t_{pd2}	A	2	Data Propagation Delay, Worst Case Path	—	14.5	—	17	ns
f_{max} (Int.)	A	3	Clock Frequency with Internal Feedback[3]	111	—	90.9	—	MHz
f_{max} (Ext.)	—	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	70.1	—	58.8	—	MHz
f_{max} (Tog.)	—	5	Clock Frequency, Max Toggle[4]	125	—	125	—	MHz
t_{su1}	—	6	GLB Reg. Setup Time before Clock, 4PT bypass	4.5	—	6	—	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP bypass	—	7	—	8	ns
t_{h1}	—	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	—	0	—	ns
t_{su2}	—	9	GLB Reg. Setup Time before Clock	7.5	—	9	—	ns
t_{co2}	—	10	GLB Reg. Clock to Output Delay	—	8.5	—	10	ns
t_{h2}	—	11	GLB Reg. Hold Time after Clock	0	—	0	—	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	—	14	—	15	ns
t_{rw1}	—	13	Ext. Reset Pulse Duration	10	—	10	—	ns
t_{en}	B	14	Input to Output Enable	—	15	—	15	ns
t_{dis}	C	15	Input to Output Disable	—	15	—	15	ns
t_{wh}	—	16	Ext. Sync. Clock Pulse Duration, High	4	—	4	—	ns
t_{wl}	—	17	Ext. Sync. Clock Pulse Duration, Low	4	—	4	—	ns
t_{su5}	—	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y1, Y2)	2	—	2	—	ns
t_{h5}	—	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y1, Y2)	5.5	—	6.5	—	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. f_{max} (Toggle) may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Table 2-0030-16/110,90C

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-80 MIN.	-80 MAX.	-60 MIN.	-60 MAX.	UNITS
t_{pd1}	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	15	–	20	ns
t_{pd2}	A	2	Data Propagation Delay, Worst Case Path	–	20	–	25	ns
f_{max} (Int.)	A	3	Clock Frequency with Internal Feedback[3]	80	–	60	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback$\left(\frac{1}{t_{su2} + t_{co1}}\right)$	50	–	38	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	100	–	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	7	–	9	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP bypass	–	10	–	13	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	10	–	13	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	12	–	16	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	17	–	22.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	10	–	13	–	ns
t_{en}	B	14	Input to Output Enable	–	18	–	24	ns
t_{dis}	C	15	Input to Output Disable	–	18	–	24	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	5	–	6	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	5	–	6	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y1, Y2)	2	–	2.5	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y1, Y2)	6.5	–	8.5	–	ns

Table 2-0030-16/80,60C

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. f_{max} (Toggle) may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Specifications *ispLSI 1016*

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-110 MIN.	-110 MAX.	-90 MIN.	-90 MAX.	UNITS
Inputs							
t_{iobp}	20	I/O Register Bypass	–	0.8	–	1.0	ns
t_{iolat}	21	I/O Latch Delay	–	1.7	–	2.0	ns
t_{iosu}	22	I/O Register Setup Time before Clock	4.1	–	4.5	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	1.8	–	2.0	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	1.7	–	2.0	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	2.1	–	2.5	ns
t_{din}	26	Dedicated Input Delay	–	1.7	–	2.0	ns
GRP							
t_{grp1}	27	GRP Delay, 1 GLB Load	–	0.6	–	0.7	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	0.8	–	1.0	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	1.5	–	1.8	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	2.1	–	2.6	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	2.8	–	3.4	ns
GLB							
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	5.3	–	6.5	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	6.1	–	7.0	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	6.6	–	8.0	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	8.2	–	9.5	ns
t_{gbp}	37	GLB Register Bypass Delay	–	0.5	–	0.5	ns
t_{gsu}	38	GLB Register Setup Time before Clock	0.3	–	1.0	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	2.9	–	3.5	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	1.6	–	1.5	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	2.1	–	2.5	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	8.2	–	10.0	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	9.0	–	9.0	ns
t_{ptck}	44	GLB Product Term Clock Delay	2.8	6.2	3.5	7.5	ns
ORP							
t_{orp}	45	ORP Delay	–	2.0	–	2.5	ns
t_{orpbp}	46	ORP Bypass Delay	–	0.4	–	0.5	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-110		-90		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	47	Output Buffer Delay	–	2.1	–	2.5	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	3.3	–	4.0	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	3.3	–	4.0	ns
Clocks							
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	2.9	2.9	3.5	3.5	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.1	3.8	2.5	4.5	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	4.2	1.0	5.0	ns
$t_{ioy1/2}$	53	Clock Delay, Y1 or Y2 to I/O Cell Global Clock Line	2.1	3.8	2.5	4.5	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	4.2	1.0	5.0	ns
Global Reset							
t_{gr}	55	Global Reset to GLB and I/O Registers	–	7.9	–	7.5	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_iobp	20	I/O Register Bypass	–	2.0	–	2.7	ns
t_iolat	21	I/O Latch Delay	–	3.0	–	4.0	ns
t_iosu	22	I/O Register Setup Time before Clock	5.5	–	7.3	–	ns
t_ioh	23	I/O Register Hold Time after Clock	1.0	–	1.3	–	ns
t_ioco	24	I/O Register Clock to Out Delay	–	3.0	–	4.0	ns
t_ior	25	I/O Register Reset to Out Delay	–	2.5	–	3.3	ns
t_din	26	Dedicated Input Delay	–	4.0	–	5.3	ns
GRP							
t_grp1	27	GRP Delay, 1 GLB Load	–	1.5	–	2.0	ns
t_grp4	28	GRP Delay, 4 GLB Loads	–	2.0	–	2.7	ns
t_grp8	29	GRP Delay, 8 GLB Loads	–	3.0	–	4.0	ns
t_grp12	30	GRP Delay, 12 GLB Loads	–	3.8	–	5.0	ns
t_grp16	31	GRP Delay, 16 GLB Loads	–	4.5	–	6.0	ns
GLB							
t_4ptbp	33	4 Product Term Bypass Path Delay	–	6.5	–	8.6	ns
t_1ptxor	34	1 Product Term/XOR Path Delay	–	7.0	–	9.3	ns
t_20ptxor	35	20 Product Term/XOR Path Delay	–	8.0	–	10.6	ns
t_xoradj	36	XOR Adjacent Path Delay[3]	–	9.5	–	12.7	ns
t_gbp	37	GLB Register Bypass Delay	–	1.0	–	1.3	ns
t_gsu	38	GLB Register Setup Time before Clock	1.0	–	1.3	–	ns
t_gh	39	GLB Register Hold Time after Clock	4.5	–	6.0	–	ns
t_gco	40	GLB Register Clock to Output Delay	–	2.0	–	2.7	ns
t_gr	41	GLB Register Reset to Output Delay	–	2.5	–	3.3	ns
t_ptre	42	GLB Product Term Reset to Register Delay	–	10.0	–	13.3	ns
t_ptoe	43	GLB Product Term Output Enable to I/O Cell Delay	–	9.0	–	12.0	ns
t_ptck	44	GLB Product Term Clock Delay	3.5	7.5	4.6	9.9	ns
ORP							
t_orp	45	ORP Delay	–	2.5	–	3.3	ns
t_orpbp	46	ORP Bypass Delay	–	0.5	–	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	47	Output Buffer Delay	–	3.0	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	5.0	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	5.0	–	6.7	ns
Clocks							
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	4.5	4.5	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	3.5	5.5	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.0	5.0	1.3	6.6	ns
$t_{ioy1/2}$	53	Clock Delay, Y1 or Y2 to I/O Cell Global Clock Line	3.5	5.5	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.0	5.0	1.3	6.6	ns
Global Reset							
t_{gr}	55	Global Reset to GLB and I/O Registers	–	9.0	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI 1016 Timing Model
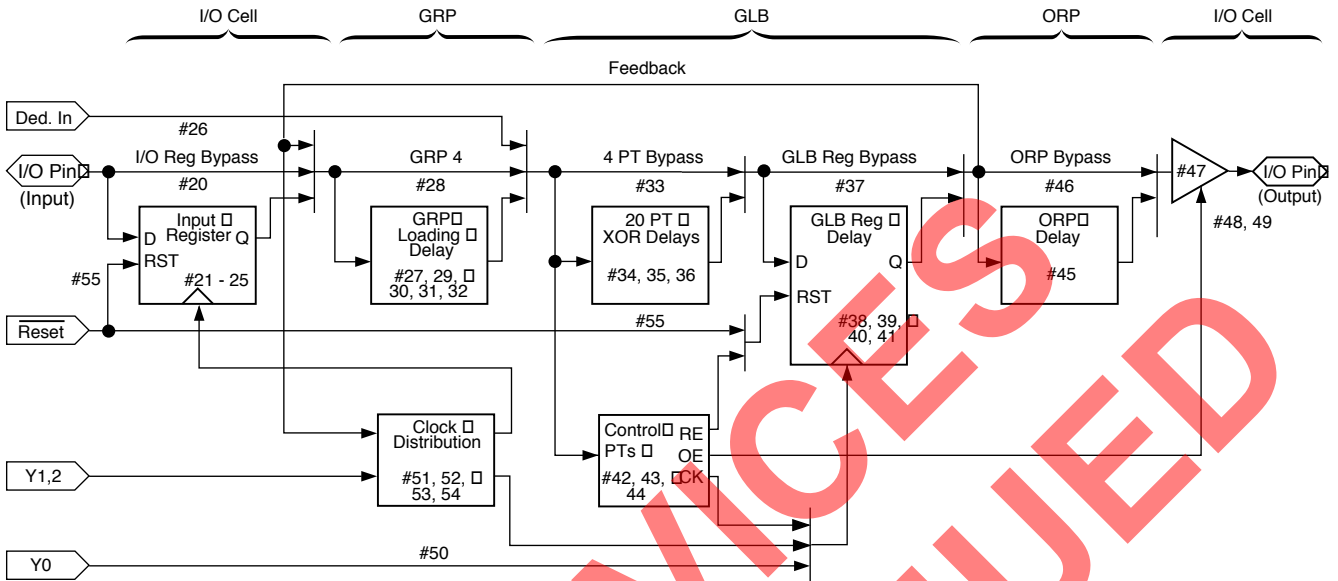
## Derivations of t_{su}, t_h and t_{co} from the Product Term Clock[1]

$$
\begin{aligned}
t_{su} &= \text{Logic} + \text{Reg su} - \text{Clock (min)} \\
&= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)}) \\
&= (\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44) \\
5.5\ ns &= (1.0 + 1.0 + 8.0) + (1.0) - (1.0 + 1.0 + 3.5)
\end{aligned}
$$

$$
\begin{aligned}
t_{h} &= \text{Clock (max)} + \text{Reg h} - \text{Logic} \\
&= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
&= (\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35) \\
3.0\ ns &= (1.0 + 1.0 + 7.5) + (3.5) - (1.0 + 1.0 + 8.0)
\end{aligned}
$$

$$
\begin{aligned}
t_{co} &= \text{Clock (max)} + \text{Reg co} + \text{Output} \\
&= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
&= (\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47) \\
16.0\ ns &= (1.0 + 1.0 + 7.5) + (1.5) + (2.5 + 2.5)
\end{aligned}
$$

Derivations of t_{su}, t_h and t_{co} from the Clock GLB[1]

$$
\begin{aligned}
t_{su} &= \text{Logic} + \text{Reg su} - \text{Clock (min)} \\
&= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)}) \\
&= (\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52) \\
5.0\ ns &= (1.0 + 1.0 + 8.0) + (1.0) - (3.5 + 1.5 + 1.0)
\end{aligned}
$$

$$
\begin{aligned}
t_{h} &= \text{Clock (max)} + \text{Reg h} - \text{Logic} \\
&= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
&= (\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35) \\
3.5\ ns &= (3.5 + 1.5 + 5.0) + (3.5) - (1.0 + 1.0 + 8.0)
\end{aligned}
$$

$$
\begin{aligned}
t_{co} &= \text{Clock (max)} + \text{Reg co} + \text{Output} \\
&= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
&= (\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47) \\
16.5\ ns &= (3.5 + 1.5 + 5.0) + (1.5) + (2.5 + 2.5)
\end{aligned}
$$

1. Calculations are based upon timing specifications for the ispLSI 1016-90.
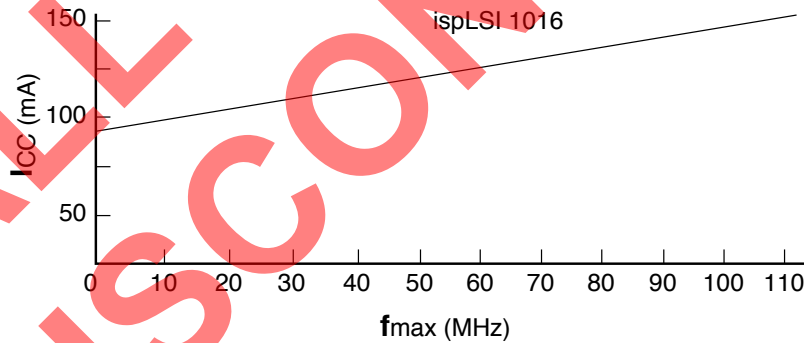
Maximum GRP Delay vs GLB Loads
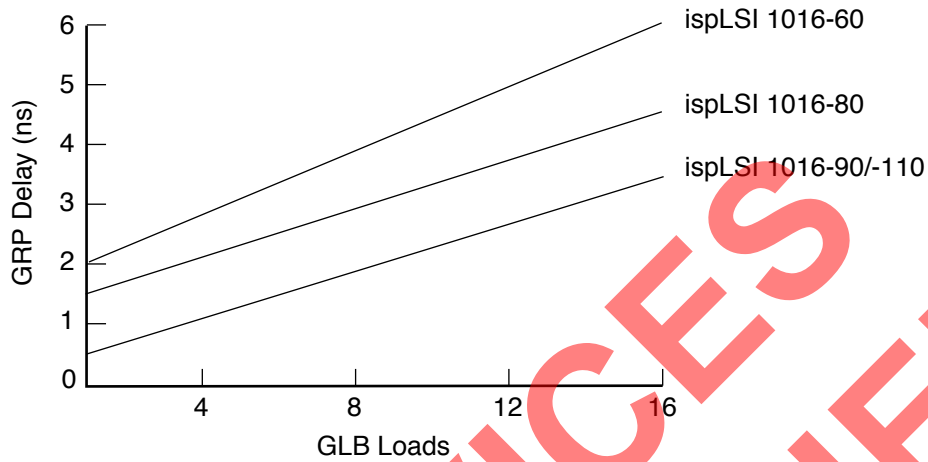
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Power Consumption

Power consumption in the ispLSI 1016 device depends on two primary factors: the speed at which the device is operating, and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax

Notes: Configuration of Four 16-bit Counters
Typical Current at 5V, 25ßC

I_{CC} can be estimated for the ispLSI 1016 using the following equation:

I_{CC} = 31 + (# of PTs * 0.45) + (# of nets * Max. freq * 0.009) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.
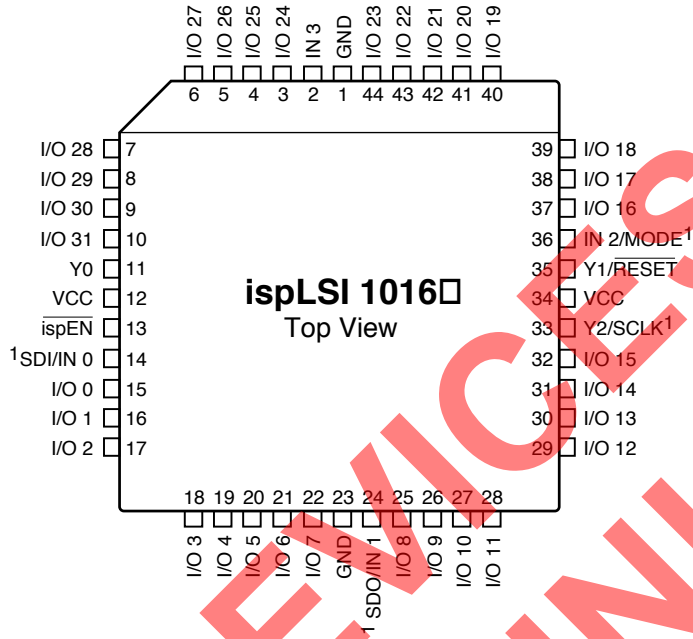
Pin Description

NAME	PLCC PIN NUMBERS	TQFP PIN NUMBERS	JLCC PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 41, 42, 43, 44, 3, 4, 5, 6, 7, 8, 9, 10	9, 10, 11, 12, 13, 14, 15, 16, 19, 20, 21, 22, 23, 24, 25, 26, 31, 32, 33, 34, 35, 36, 37, 38, 41, 42, 43, 44, 1, 2, 3, 4	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 41, 42, 43, 44, 3, 4, 5, 6, 7, 8, 9, 10	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 3	2	40	2	Dedicated input pins to the device.
$\overline{\text{ispEN}}$	13	7	13	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI/IN 0 [1]	14	8	14	Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE/IN 2 [1]	36	30	36	Input – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as a pin to control the operation of the isp state machine.
SDO/IN 1 [1]	24	18	24	Input/Output – This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as an output pin to read serial shift register data.
SCLK/Y2 [1]	33	27	33	Input – This pin performs two functions. It is a dedicated clock input when ispEN is logic high. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. When ispEN is logic low, it functions as a clock pin for the Serial Shift Register.
Y0	11	5	11	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1/$\overline{\text{RESET}}$	35	29	35	This pin performs two functions: – Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. – Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
GND Vcc	1, 23 12, 34	17, 39 6, 28	1, 23 12, 34	Ground (GND) V_{CC}

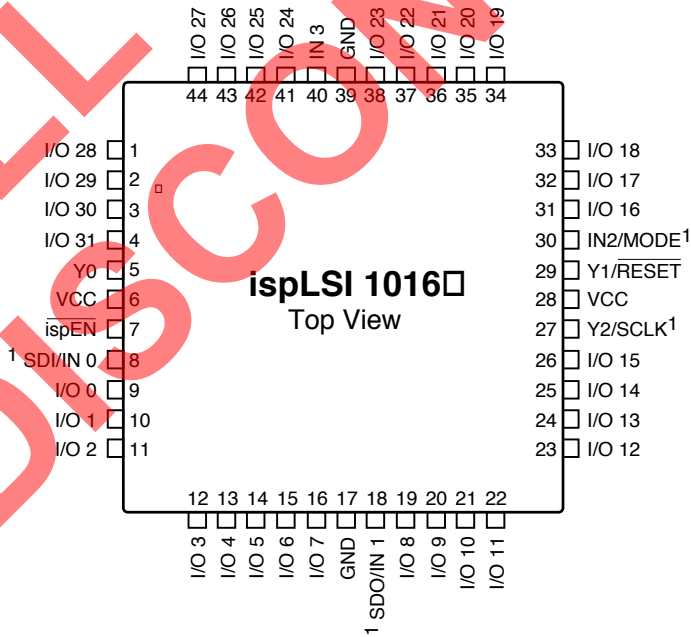1. Pins have dual function capability.

Table 2 - 0002C-16-isp

![Lattice Semiconductor Corporation logo]

Pin Configuration

ispLSI 1016 44-Pin PLCC Pinout Diagram

Top pins (6 5 4 3 2 1 44 43 42 41 40): I/O 27, I/O 26, I/O 25, I/O 24, IN 3, GND, I/O 23, I/O 22, I/O 21, I/O 20, I/O 19

Left pins:
- I/O 28 — 7
- I/O 29 — 8
- I/O 30 — 9
- I/O 31 — 10
- Y0 — 11
- VCC — 12
- $\overline{ispEN}$ — 13
- [1]SDI/IN 0 — 14
- I/O 0 — 15
- I/O 1 — 16
- I/O 2 — 17

ispLSI 1016□
Top View

Right pins:
- 39 — I/O 18
- 38 — I/O 17
- 37 — I/O 16
- 36 — IN 2/MODE[1]
- 35 — Y1/$\overline{RESET}$
- 34 — VCC
- 33 — Y2/SCLK[1]
- 32 — I/O 15
- 31 — I/O 14
- 30 — I/O 13
- 29 — I/O 12

Bottom pins (18 19 20 21 22 23 24 25 26 27 28): I/O 3, I/O 4, I/O 5, I/O 6, I/O 7, GND, [1]SDO/IN 1, I/O 8, I/O 9, I/O 10, I/O 11

1. Pins have dual function capability.

0123A-isp1016

ispLSI 1016 44-Pin TQFP Pinout Diagram

Top pins (44 43 42 41 40 39 38 37 36 35 34): I/O 27, I/O 26, I/O 25, I/O 24, IN 3, GND, I/O 23, I/O 22, I/O 21, I/O 20, I/O 19

Left pins:
- I/O 28 — 1
- I/O 29 — 2
- I/O 30 — 3
- I/O 31 — 4
- Y0 — 5
- VCC — 6
- $\overline{ispEN}$ — 7
- [1] SDI/IN 0 — 8
- I/O 0 — 9
- I/O 1 — 10
- I/O 2 — 11

ispLSI 1016□
Top View

Right pins:
- 33 — I/O 18
- 32 — I/O 17
- 31 — I/O 16
- 30 — IN2/MODE[1]
- 29 — Y1/$\overline{RESET}$
- 28 — VCC
- 27 — Y2/SCLK[1]
- 26 — I/O 15
- 25 — I/O 14
- 24 — I/O 13
- 23 — I/O 12

Bottom pins (12 13 14 15 16 17 18 19 20 21 22): I/O 3, I/O 4, I/O 5, I/O 6, I/O 7, GND, [1]SDO/IN 1, I/O 8, I/O 9, I/O 10, I/O 11

1. Pins have dual function capability.

0851-16/TQFP

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Pin Configuration

ispLSI 1016 44-Pin JLCC Pinout Diagram

1. Pins have dual function capability.

0123-16-isp/JLCC

Lattice
Semiconductor
Corporation
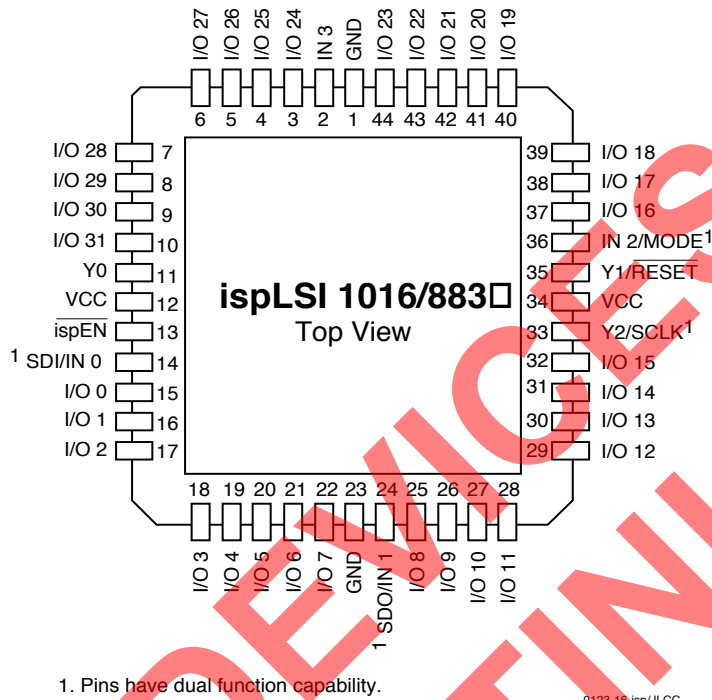
Part Number Description

ispLSI 1016 —XXX X XXX X

Device Family
ispLSI

Device Number

Speed
110 = 110 MHz **f**max
90 = 90 MHz **f**max
80 = 80 MHz **f**max
60 = 60 MHz **f**max

Grade
Blank = Commercial
I = Industrial
/883 = 883 Military Process

Package
J = PLCC
T44 = TQFP
H = JLCC

Power
L = Low

0212-80B-isp1016
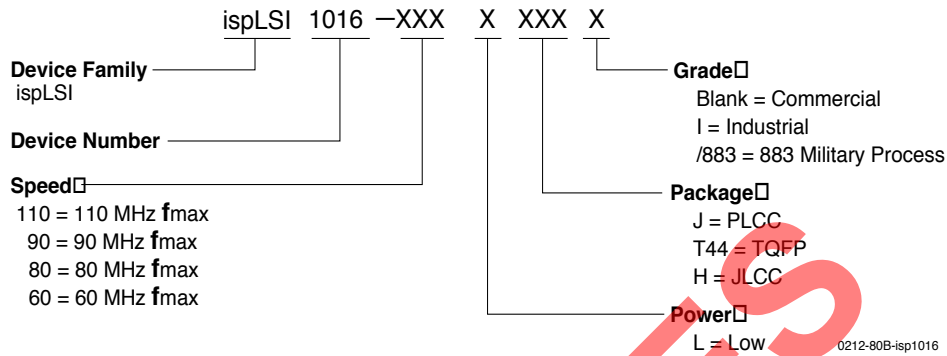
Ordering Information

COMMERCIAL

Family	**f**max (MHz)	**t**pd (ns)	Ordering Number	Package
ispLSI	110	10	ispLSI 1016-110LJ	44-Pin PLCC
	90	12	ispLSI 1016-90LJ	44-Pin PLCC
	90	12	ispLSI 1016-90LT44	44-Pin TQFP
	80	15	ispLSI 1016-80LJ	44-Pin PLCC
	80	15	ispLSI 1016-80LT44	44-Pin TQFP
	60	20	ispLSI 1016-60LJ	44-Pin PLCC
	60	20	ispLSI 1016-60LT44	44-Pin TQFP

INDUSTRIAL

Family	**f**max (MHz)	**t**pd (ns)	Ordering Number	Package
ispLSI	60	20	ispLSI 1016-60LJI	44-Pin PLCC
	60	20	ispLSI 1016-60LT44I	44-Pin TQFP

MILITARY/883

Family	**f**max (MHz)	**t**pd (ns)	Ordering Number	SMD #	Package
ispLSI	60	20	ispLSI 1016-60LH/883	5962-9476201MXC	44-Pin JLCC

Note: Lattice Semiconductor recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number is recommended.

Table 2-0041-16-isp1016