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ispClock™5300S Family

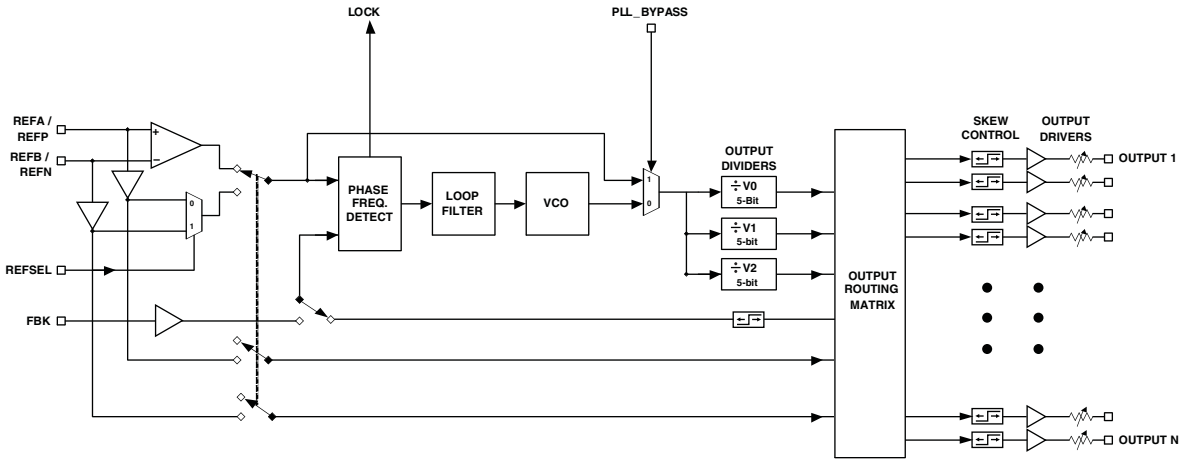
In-System Programmable, Zero-Delay Universal Fan-Out Buffer, Single-Ended

October 2007 **Preliminary Data Sheet DS1010**

Features

- **Four Operating Configurations**
  - Zero delay buffer
  - Zero delay and non-zero delay buffer
  - Dual non-zero delay buffer
  - Non-zero delay buffer with output divider
- **8MHz to 267MHz Input/Output Operation**
- **Low Output to Output Skew (<100ps)**
- **Low Jitter Peak-to-Peak (< 70 ps)**
- **Up to 20 Programmable Fan-out Buffers**
  - Programmable single-ended output standards and individual enable controls
    - LVTTL, LVCMOS, HSTL, eHSTL, SSTL
  - Programmable output impedance
    - 40 to 70Ω in 5Ω increments
  - Programmable slew rate
  - Up to 10 banks with individual V_{CCO} and GND
    - 1.5V, 1.8V, 2.5V, 3.3V
- **Fully Integrated High-Performance PLL**
  - Programmable lock detect
  - Three “Power of 2” output dividers (5-bit)
  - Programmable on-chip loop filter
  - Compatible with spread spectrum clocks
  - Internal/external feedback
- **Precision Programmable Phase Adjustment (Skew) Per Output**
  - 8 settings; minimum step size 156ps
    - Locked to VCO frequency
  - Up to +/- 5ns skew range
  - Coarse and fine adjustment modes
- **Up to Three Clock Frequency Domains**
- **Flexible Clock Reference and External Feedback Inputs**
  - Programmable single-ended or differential input reference standards
    - LVTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL, Differential HSTL, Differential SSTL
  - Clock A/B selection multiplexer
  - Programmable Feedback Standards
    - LVTTL, LVCMOS, SSTL, HSTL
  - Programmable termination
- **All Inputs and Outputs are Hot Socket Compliant**
- **Full JTAG Boundary Scan Test In-System Programming Support**
- **Exceptional Power Supply Noise Immunity**
- **Commercial (0 to 70°C) and Industrial (-40 to 85°C) Temperature Ranges**
- **48-pin and 64-pin TQFP Packages**
- **Applications**
  - Circuit board common clock distribution
  - PLL-based frequency generation
  - High fan-out clock buffer
  - Zero-delay clock buffer

ispClock5300S Family Functional Diagram



General Description

The ispClock5300S is an in-system-programmable zero delay universal fan-out buffer for use in clock distribution applications. The ispClock5312S, the first member of the ispClock5300S family, provides up to 12 single-ended ultra low skew outputs. Each pair of outputs may be independently configured to support separate I/O standards (LVTTL, LVCMOS -3.3V, 2.5V, 1.8, SSTL, HSTL) and output frequency. In addition, each output provides independent programmable control of termination, slew-rate, and timing skew. All configuration information is stored on-chip in non-volatile $E^2CMOS^®$ memory.

The ispClock5300S devices provide extremely low propagation delay (zero-delay) from input to output using the on-chip low jitter high-performance PLL. A set of three programmable 5-bit counters can be used to generate three frequencies derived from the PLL clock. These counters are programmable in powers of 2 only (1, 2, 4, 8, 16, 32). The clock output from any of the V-dividers can then be routed to any clock output pin through the output routing matrix. The output routing matrix, in addition, also enables routing of reference clock inputs directly to any output.

The ispClock5300S device can be configured to operate in four modes: zero delay buffer mode, dual non-zero delay buffer mode, non-zero delay buffer mode with output dividers, and combined zero-delay and non-zero delay buffer mode.

The core functions of all members of the ispClock5300S family are identical. Table 1 summarizes the ispClock5300S device family.

Table 1. ispClock5300S Family

Device	Number of Programmable Clock Inputs	Number of Programmable Single-Ended Outputs
ispClock5320S	1 Differential, 2 Single-Ended	20
ispClock5316S	1 Differential, 2 Single-Ended	16
ispClock5312S	1 Differential, 2 Single-Ended	12
ispClock5308S	1 Differential, 2 Single-Ended	8
ispClock5304S	1 Differential, 2 Single-Ended	4

Figure 1. ispClock5304S Functional Block Diagram

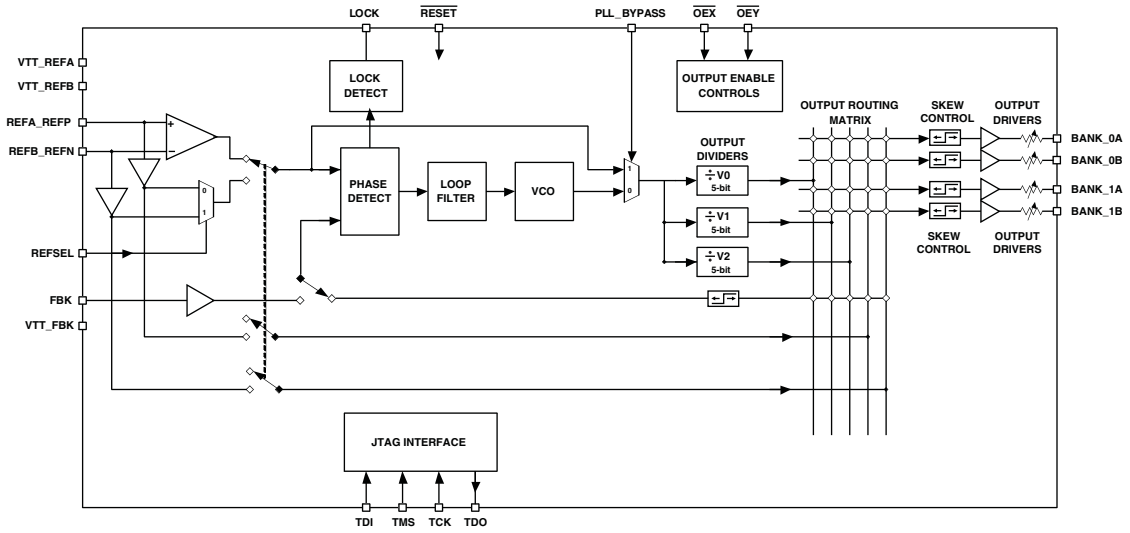


Figure 2. ispClock5308S Functional Block Diagram

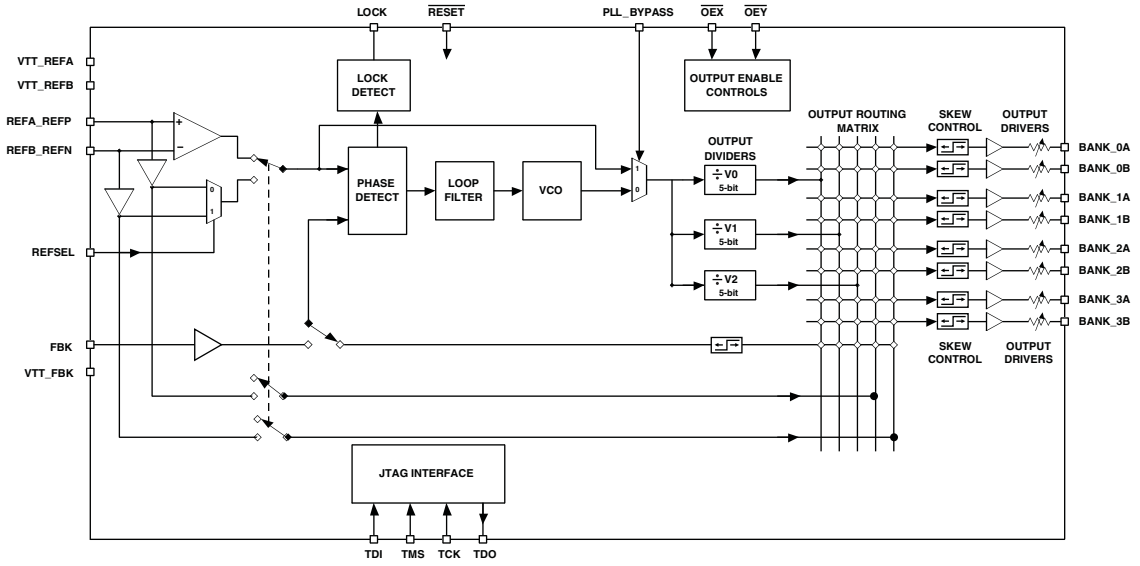


Figure 3. ispClock5312S Functional Block Diagram

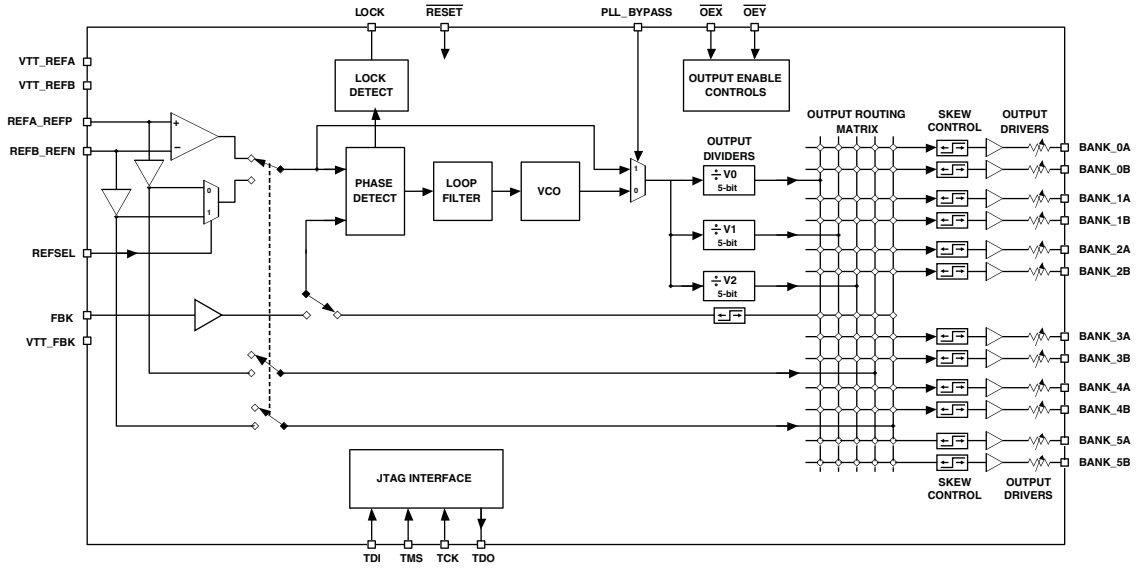


Figure 4. ispClock5316S Functional Block Diagram

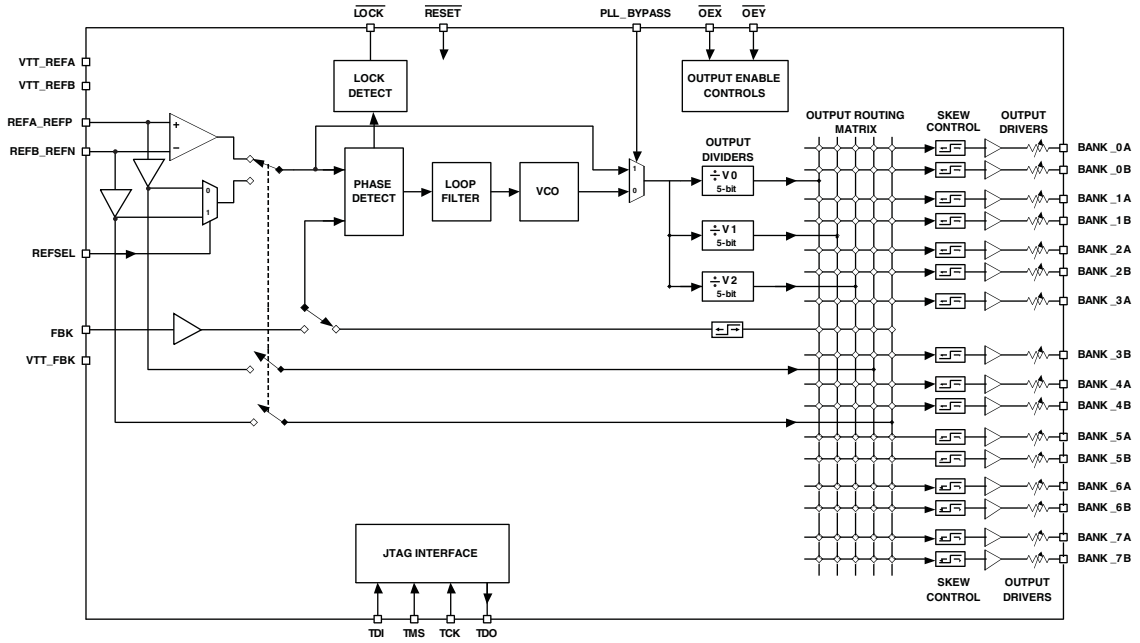
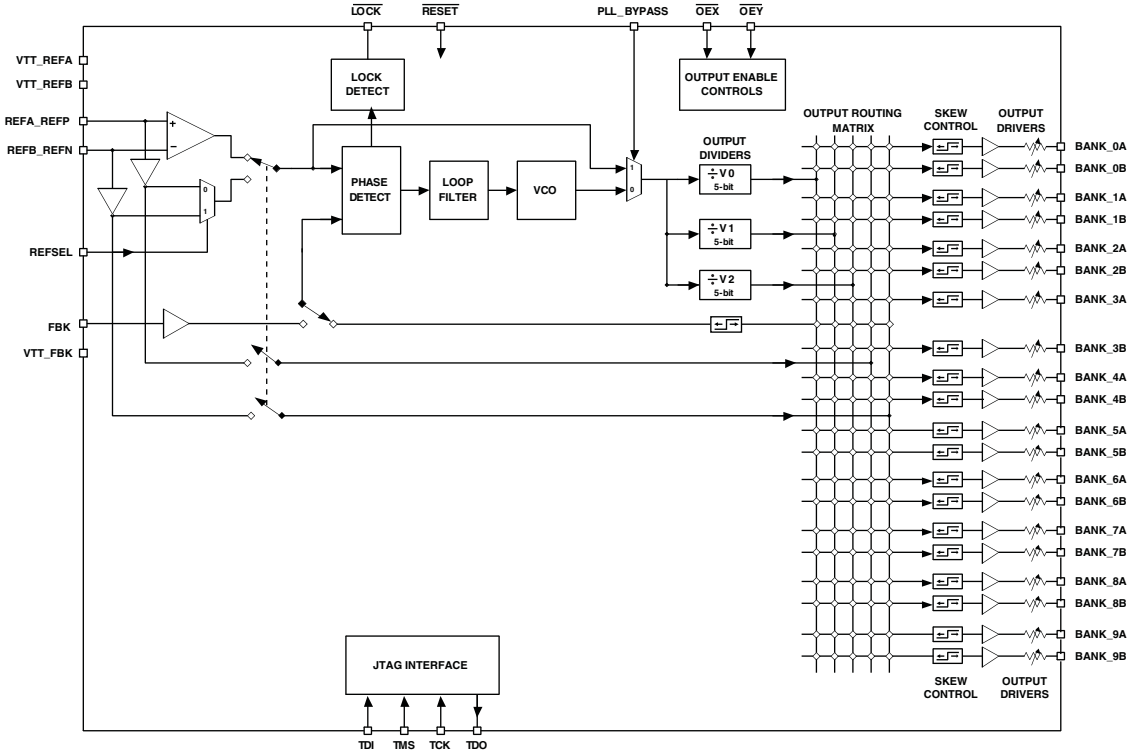


Figure 5. ispClock5320S Functional Block Diagram



Absolute Maximum Ratings

	ispClock5300S
Core Supply Voltage V_{CCD}	-0.5 to 5.5V
PLL Supply Voltage V_{CCA}	-0.5 to 5.5V
JTAG Supply Voltage V_{CCJ}	-0.5 to 5.5V
Output Driver Supply Voltage V_{CCO}	-0.5 to 4.5V
Input Voltage	-0.5 to 4.5V
Output Voltage[1]	-0.5 to 4.5V
Storage Temperature	-65 to 150°C
Junction Temperature with power supplied	-40 to 130°C

1. When applied to an output when in high-Z condition

Recommended Operating Conditions

Symbol	Parameter	Conditions	ispClock5300S		Units
			Min.	Max.	
V_{CCD}	Core Supply Voltage		3.0	3.6	V
V_{CCJ}	JTAG I/O Supply Voltage		1.62	3.6	V
V_{CCA}	Analog Supply Voltage		3.0	3.6	V
$V_{CCXSLEW}$	V_{CC} Turn-on Ramp Rate	All supply pins	—	0.33	V/µs
T_{JOP}	Operating Junction Temperature	Commercial	0	120	°C
		Industrial	-40	130	
T_A	Ambient Operating Temperature	Commercial	0	70[1]	°C
		Industrial	-40	85[1]	

1. Device power dissipation may also limit maximum ambient operating temperature.

Recommended Operating Conditions – V_{CCO} vs. Logic Standard

Logic Standard	V_{CCO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL	3.0	3.3	3.6	—	—	—	—	—	—
LVCMOS 1.8V	1.71	1.8	1.89	—	—	—	—	—	—
LVCMOS 2.5V	2.375	2.5	2.625	—	—	—	—	—	—
LVCMOS 3.3V	3.0	3.3	3.6	—	—	—	—	—	—
SSTL1.8	1.71	1.8	1.89	0.84	0.90	0.95	—	0.5 x V_{CCO}	—
SSTL2 Class 1	2.375	2.5	2.625	1.15	1.25	1.35	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL3 Class 1	3.0	3.3	3.6	1.30	1.50	1.70	V_{REF} - 0.05	V_{REF}	V_{REF} + 0.05
HSTL Class 1	1.425	1.5	1.575	0.68	0.75	0.90	—	0.5 x V_{CCO}	—
eHSTL Class 1	1.71	1.8	1.89	0.84	0.90	0.95	—	0.5 x V_{CCO}	—

Note: '—' denotes V_{REF} or V_{TT} not applicable to this logic standard

E²CMOS Memory Write/Erase Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Erase/Reprogram Cycles		1000	—	—	

Performance Characteristics – Power Supply

Symbol	Parameter	Conditions	Typ.	Max.	Units
I_{CCD}	Core Supply Current[2]	f_{VCO} = 400MHz Feedback Output Active	110	150	mA
$I_{CCDADDER}$	Incremental I_{CCD} per Active Output	f_{OUT} = 267MHz		1.5	mA
I_{CCA}	Analog Supply Current[2]	f_{VCO} = 400MHz	5.5	7	mA
I_{CCO}	Output Driver Supply Current (per Bank)	V_{CCO} = 1.8V[1], LVCMOS, f_{OUT} = 267MHz	16	20	mA
		V_{CCO} = 2.5V[1], LVCMOS, f_{OUT} = 267MHz	21	27	mA
		V_{CCO} = 3.3V[1], LVCMOS, f_{OUT} = 267MHz	27	35	mA
I_{CCJ}	JTAG I/O Supply Current (static)	V_{CCJ} = 1.8V		300	µA
		V_{CCJ} = 2.5V		400	µA
		V_{CCJ} = 3.3V		400	µA

1. Supply current consumed by each bank, both outputs active, 5pF load.
2.All unused REFCLK and feedbacks connected to ground.

DC Electrical Characteristics – Single-Ended Logic

Logic Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min.	Max.	Min.	Max.				
LVTTL/LVCMOS 3.3V	-0.3	0.8	2	3.6	0.4	V_{CCO} - 0.4	12[3]	-12[3]
LVCMOS 1.8V	-0.3	0.68	1.07	3.6	0.4	V_{CCO} - 0.4	12[3]	-12[3]
LVCMOS 2.5V	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	12[3]	-12[3]
SSTL2 Class 1	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54[1]	V_{CCO} - 0.81[1]	7.6	-7.6
SSTL3 Class 1	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.9[1]	V_{CCO} - 1.3[1]	8	-8
HSTL Class 1	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4[2]	V_{CCO} - 0.4[2]	8	-8
eHSTL Class 1	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4[2]	V_{CCO} - 0.4[2]	8	-8

1. Specified for 40Ω internal series output termination.
2. Specified for ≈20Ω internal series output termination, fast slew rate setting.
3. For slower slew rate setting, I_{OH}, I_{OL} should be limited to 8mA.

DC Electrical Characteristics – LVDS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{ICM}	Common Mode Input Voltage		V_{THD}/2		2.325	V
V_{THD}	Differential Input Threshold	$V_{ICM} \leq 2V$	±100	—	—	mV
		$2V < V_{ICM} < 2.325V$	±150	—	—	mV
V_{IN}	Input Voltage		0	—	2.4	V

DC Electrical Characteristics – Differential LVPECL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input Voltage High	V_{CCD} = 3.0 to 3.6V	V_{CCD} - 1.17	—	V_{CCD} - 0.88	V
		V_{CCD} = 3.3V	2.14	—	2.42	
V_{IL}	Input Voltage Low	V_{CCD} = 3.0 to 3.6V	V_{CCD} - 1.81	—	V_{CCD} - 1.48	V
		V_{CCD} = 3.3V	1.49	—	1.83	

Electrical Characteristics – Differential SSTL18

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IL}	Low-Logic Level Input Voltage				0.61	V
V_{IH}	Hi Logic Level Input Voltage		1.17			V
V_{IX}	Input Pair Differential Crosspoint Voltage		V_{REF} -175mV		V_{REF} +175mV	V

Electrical Characteristics – Differential SSTL2

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{SWING(DC)}$	DC Differential Input Voltage Swing		-0.03		3.225	V
$V_{SWING(AC)}$	AC Input Differential Voltage		0.62		3.225	V_{PP}
V_{IX}	Input Pair Differential Crosspoint Voltage		V_{REF} - 200 mV		V_{REF} + 200 mV	V

Electrical Characteristics – Differential HSTL

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{SWING(DC)}$	DC Differential Input Voltage Swing		-0.03		3.325	V
$V_{SWING(AC)}$	AC Input Differential Voltage		0.4		3.325	V_{PP}
V_{IX}	Input Pair Differential Crosspoint Voltage		0.68		0.9	V

Electrical Characteristics – Differential eHSTL

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{SWING(DC)}$	DC Differential Input Voltage Swing		-0.03		3.325	V
$V_{SWING(AC)}$	AC Input Differential Voltage		0.4		3.325	V_{PP}
V_{IX}	Input Pair Differential Crosspoint Voltage		0.68		0.9	V

DC Electrical Characteristics – Input/Output Loading

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{LK}	Input Leakage	Note 1	—	—	±10	µA
I_{PU}	Input Pull-up Current	Note 2	—	80	120	µA
I_{PD}	Input Pull-down Current	REFSEL, PLL_BYPASS	—	120	150	µA
		$\overline{OEX}$, $\overline{OEY}$, 2.5V CMOS Logic Standard	—	120	150	µA
		$\overline{OEX}$, $\overline{OEY}$, & 3.3V CMOS Logic Standard	—	200	400	µA
I_{OLK}	Tristate Leakage Output	Note 4	—	—	±10	µA
C_{IN}	Input Capacitance	Notes 2, 3, 5	—	8	10	pF
		Note 6	—	10	11	pF

1. Applies to clock reference inputs when termination 'open'.
2. Applies to TDI, TMS and $\overline{RESET}$ inputs.
3. Applies to REFSEL and PLL_BYPASS, $\overline{OEX}$, $\overline{OEY}$.
4. Applies to all logic types when in tristated mode.
5. Applies to $\overline{OEX}$, $\overline{OEY}$, TCK, $\overline{RESET}$ inputs.
6. Applies to REFA_REFP, REFB_REFN, FBK.

Switching Characteristics – Timing Adders for I/O Modes

Adder Type	Description	Min.	Typ.	Max.	Units
t_{IOI} Input Adders[2]					
LVTTL_in	Using LVTTL Standard		0.00		ns
LVCMOS18_in	Using LVCMOS 1.8V Standard		0.10		ns
LVCMOS25_in	Using LVCMOS 2.5V Standard		0.00		ns
LVCMOS33_in	Using LVCMOS 3.3V Standard		0.00		ns
SSTL2_in	Using SSTL2 Standard		0.00		ns
SSTL3_in	Using SSTL3 Standard		0.00		ns
HSTL_in	Using HSTL Standard		1.15		ns
eHSTL_in	Using eHSTL Standard		1.10		ns
LVDS_in	Using LVDS Standard		0.60		ns
LVPECL_in	Using LVPECL Standard		0.60		ns
t_{IOO} Output Adders[1, 3]					
LVTTL_out	Output Configured as LVTTL Buffer		0.25		ns
LVCMOS18_out	Output Configured as LVCMOS 1.8V Buffer		0.25		ns
LVCMOS25_out	Output Configured as LVCMOS 2.5V Buffer		0.25		ns
LVCMOS33_out	Output Configured as LVCMOS 3.3V Buffer		0.25		ns
SSTL18_out	Output Configured as SSTL18 Buffer		0.00		ns
SSTL2_out	Output Configured as SSTL2 Buffer		0.00		ns
SSTL3_out	Output Configured as SSTL3 Buffer		0.00		ns
HSTL_out	Output Configured as HSTL Buffer		0.00		ns
eHSTL_out	Output Configured as eHSTL Buffer		0.00		ns
t_{IOS} Output Slew Rate Adders[1]					
Slew_1	Output Slew_1 (Fastest)	—	0.00	—	ps
Slew_2	Output Slew_2	—	475	—	ps
Slew_3	Output Slew_3	—	950	—	ps
Slew_4	Output Slew_4 (Slowest)	—	1900	—	ps

1. Measured under standard output load conditions – see Figures 6 and 7.
2. All input adders referenced to LVTTL.
3. All output adders referenced to SSTL/HSTL/eHSTL.

Output Rise and Fall Times – Typical Values[1, 2]

Output Type	Slew 1 (Fastest)		Slew 2		Slew 3		Slew 4 (Slowest)		Units
	t_R	t_F	t_R	t_F	t_R	t_F	t_R	t_F	
LVTTL	0.54	0.76	0.60	0.87	0.78	1.26	1.05	1.88	ns
LVCMOS 1.8V	0.75	0.69	0.88	0.78	0.83	1.11	1.20	1.68	ns
LVCMOS 2.5V	0.57	0.69	0.65	0.78	0.99	0.98	1.65	1.51	ns
LVCMOS 3.3V	0.55	0.77	0.60	0.87	0.78	1.26	1.05	1.88	ns
SSTL18	0.55	0.40	—	—	—	—	—	—	ns
SSTL2	0.50	0.40	—	—	—	—	—	—	ns
SSTL3	0.50	0.45	—	—	—	—	—	—	ns
HSTL	0.60	0.45	—	—	—	—	—	—	ns
eHSTL	0.55	0.40	—	—	—	—	—	—	ns

1. See Figures 6 and 7 for test conditions.
2. Measured between 20% and 80% points.

Output Test Loads

Figures 6 and 7 show the equivalent termination loads used to measure rise/fall times, output timing adders and other selected parameters as noted in the various tables of this data sheet.

Figure 6. CMOS Termination Load

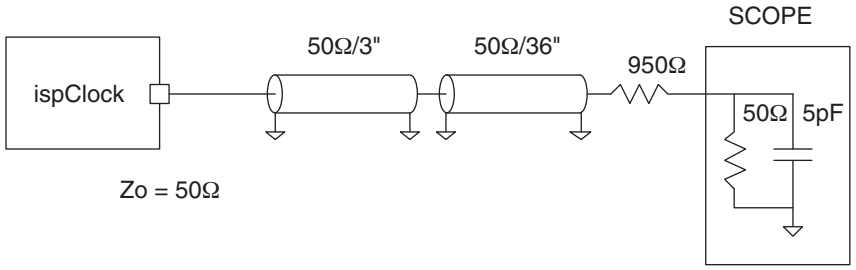
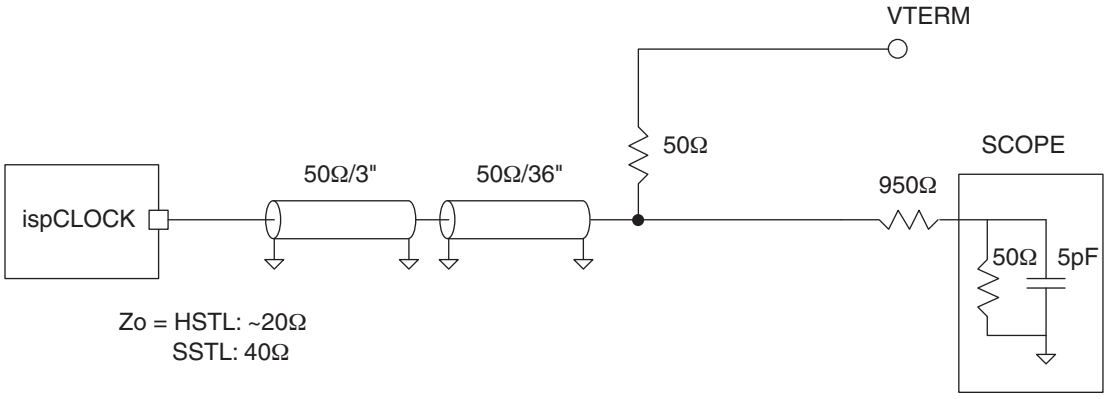


Figure 7. eHSTL/HSTL/SSTL Termination Load



Programmable Input and Output Termination Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R_{IN}	Input Resistance	Rin=40Ω setting	36	—	44	Ω
		Rin=45Ω setting	40.5	—	49.5	
		Rin=50Ω setting	45	—	55	
		Rin=55Ω setting	49.5	—	60.5	
		Rin=60Ω setting	54	—	66	
		Rin=65Ω setting	59	—	71.5	
		Rin=70Ω setting	61	—	77	
R_{OUT}	Output Resistance	Rout≈20Ω setting T_A = 25°C	—	14	—	Ω
		Rout≈40Ω setting T_A = 25°C	36	38	44	
		Rout≈45Ω setting T_A = 25°C	41	45	51	
		Rout≈50Ω setting T_A = 25°C	45	50	55	
		Rout≈55Ω setting T_A = 25°C	50	55	61	
		Rout≈60Ω setting T_A = 25°C	54	59	66	
		Rout≈65Ω setting T_A = 25°C	59	65	71	
		Rout≈70Ω setting T_A = 25°C	63	72	78	
R_{OUT_TEMPCO}	Output Resistor Temperature Coefficient		—	500	—	PPM/°C

Performance Characteristics – PLL

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{REF}, f_{FBK}	Reference and feedback input frequency range		8		267	MHz
$t_{CLOCKHI}$, $t_{CLOCKLO}$	Reference and feedback input clock HIGH and LOW times		1.25			ns
t_{RINP}, t_{FINP}	Reference and feedback input rise and fall times	Measured between 20% and 80% levels			5	ns
f_{PFD}	Phase detector input frequency range		8		267	MHz
f_{VCO}	VCO operating frequency		160		400	MHz
V_{DIV}	Output divider range (Power of 2)		1		32	
f_{OUT}	Output frequency range[1]	Fine Skew Mode	5		267	MHz
		Coarse Skew Mode	2.5		200	MHz
t_{JIT} (cc)	Output adjacent-cycle jitter[5] (1000 cycle sample)	$f_{PFD} \geq$ 100MHz			70	ps (p-p)
t_{JIT} (per)	Output period jitter[5] (10000 cycle sample)	$f_{PFD} \geq$ 100MHz			9	ps (RMS)
$t_{JIT(\phi)}$	Reference clock to output jitter[5] (2000 cycle sample)	$f_{PFD} \geq$ 100MHz			50	ps (RMS)
$t\phi$	Static phase offset[4]	PFD input frequency ≥100MHz[3]	-40		100	ps
$t\phi_{DYN}$	Dynamic phase offset	100MHz, Spread Spectrum Modulation index = 0.5%		2	8	ps
DC_{ERR}	Output duty cycle error	Output type LVCMOS 3.3V[2] f_{OUT} >100 MHz	47		53	%
$t_{PDBYPASS}$	Reference clock to output propagation delay	V=1		6.5		ns
t_{PD_FOB}	Reference to output propagation delay in Non-Zero Delay Buffer Mode	V=1	2.5	3.5	5	ns
t_{DELAY}	Reference to output delay with internal feedback mode[3]	V=1		500		ps
t_{LOCK}	PLL lock time	From Power-up event		150		µs
		From $\overline{\text{RESET}}$ event		15		µs
t_{RELOCK}	PLL relock time	To same reference frequency		15		µs
		To different frequency		150		µs
PSR	Power supply rejection, period jitter vs. power supply noise	$f_{IN} = f_{OUT}$ = 100MHz $V_{CCA} = V_{CCD} = V_{CCO}$ modulated with 100kHz sinusoidal stimulus		0.05		$\frac{ps(RMS)}{mV(p\text{-}p)}$

1. In PLL Bypass mode (PLL_BYPASS = HIGH), output will support frequencies down to 0Hz (divider chain is a fully static design).
2. See Figures 6 and 7 for output loads.
3. Input and outputs LVCMOS mode
4. Inserted feedback loop delay < 7ns
5. Measured with f_{OUT} = 100MHz, f_{VCO} = 400MHz, input and output interface set to LVCMOS.

Timing Specifications

Skew Matching

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{SKEW}	Output-output Skew	Between any two identically configured and loaded outputs regardless of bank.	—	—	100	ps

Programmable Skew Control

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{SKRANGE}$	Skew Control Range[1]	Fine Skew Mode, f_{VCO} = 160 MHz	—	2.73	—	ns
		Fine Skew Mode, f_{VCO} = 400 MHz	—	1.09	—	
		Coarse Skew Mode, f_{VCO} = 160 MHz	—	5.46	—	
		Coarse Skew Mode, f_{VCO} = 400 MHz	—	2.19	—	
SK_{STEPS}	Skew Steps per Range		—	8	—	
t_{SKSTEP}	Skew Step Size[2]	Fine Skew Mode, f_{VCO} = 160 MHz	—	390	—	ps
		Fine Skew Mode, f_{VCO} = 400 MHz	—	156	—	
		Coarse Skew Mode, f_{VCO} = 160 MHz	—	780	—	
		Coarse Skew Mode, f_{VCO} = 400 MHz	—	312	—	
t_{SKERR}	Skew Time Error[3]	Fine skew mode	—	30	—	ps
		Coarse skew mode	—	50	—	

1. Skew control range is a function of VCO frequency (f_{VCO}). In fine skew mode $T_{SKRANGE} = 7/(16 \times f_{VCO})$. In coarse skew mode $T_{SKRANGE} = 7/(8 \times f_{VCO})$.
2. Skew step size is a function of VCO frequency (f_{VCO}). In fine skew mode $T_{SKSTEP} = 1/(16 \times f_{VCO})$. In coarse skew mode $T_{SKSTEP} = 1/(8 \times f_{VCO})$.
3. Only applicable to outputs with non-zero skew settings.

Control Functions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{DIS/OE}$	Delay Time, $\overline{OEX}$ or $\overline{OEY}$ to Output Disabled/ Enabled		—	10	20	ns
t_{PLL_RSTW}	PLL $\overline{RESET}$ Pulse Width[1]		1	—	—	ms
t_{RSTW}	Logic $\overline{RESET}$ Pulse Width[2]		20	—	—	ns
RST_SLEW	Reset Signal Slew Rate		0.1			V/µs

1. Will completely reset PLL.
2. Will only reset digital logic.

Static Phase Offset vs. Reference Clock Logic Type

Symbol	Reference Clock Logic (REFA/REFB)	Feedback Input Logic (FBK)	Feedback Output Logic (BANK_xA/BANK_xB)	Min.	Max.	Units
$t_{(\phi)}$ – Static Phase Offset	LVCMOS 33	LVCMOS33	LVCMOS33	-40	100	ps
	LVCMOS 25	LVCMOS25	LVCMOS25	-70	80	ps
	LVCMOS 18	LVCMOS18	LVCMOS18	-80	80	ps
	SSTL3	SSTL3	SSTL3	-70	390	ps
	SSTL2	SSTL2	SSTL2	-70	340	ps
	HSTL(1.5V)	HSTL(1.5V)	HSTL(1.5V)	-100	360	ps
	eHSTL(1.8V)	eHSTL(1.8V)	eHSTL(1.8V)	-100	360	ps
	LVDS (2.5V)[1]	LVDS-Single Ended	LVCMOS25	140	530	ps
	LVPECL[1]	LVPECL-Single Ended	LVCMOS33	80	300	ps

1. The output clock to feedback can be skewed to center the static phase offset spread.

Boundary Scan Logic

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK (BSCAN Test) Clock Cycle	40	—	ns
t_{BTCH}	TCK (BSCAN Test) Pulse Width High	20	—	ns
t_{BTCL}	TCK (BSCAN Test) Pulse Width Low	20	—	ns
t_{BTSU}	TCK (BSCAN Test) Setup Time	8	—	ns
t_{BTH}	TCK (BSCAN Test) Hold Time	10	—	ns
t_{BRF}	TCK (BSCAN Test) Rise and Fall Rate	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	10	ns
t_{BTOZ}	TAP Controller Falling Edge of Clock to Data Output Disable	—	10	ns
t_{BTVO}	TAP Controller Falling Edge of Clock to Data Output Enable	—	10	ns
$t_{BVTCPSU}$	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCPH}	BSCAN Test Capture Register Hold Time	10	—	ns
t_{BTUCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	25	ns
t_{BTUOZ}	BSCAN Test Update Register, Falling Edge of Clock to Output Disable	—	25	ns
t_{BTUOV}	BSCAN Test Update Register, Falling Edge of Clock to Output Enable	—	25	ns

JTAG Interface and Programming Mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum TCK Clock Frequency		—	—	25	MHz
t_{CKH}	TCK Clock Pulse Width, High		20	—	—	ns
t_{CKL}	TCK Clock Pulse Width, Low		20	—	—	ns
t_{ISPEN}	Program Enable Delay Time		15	—	—	µs
t_{ISPDIS}	Program Disable Delay Time		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Program		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Erase		200	—	—	µs
t_{CEN}	Falling Edge of TCK to TDO Active		—	—	15	ns
t_{CDIS}	Falling Edge of TCK to TDO Disable		—	—	15	ns
t_{SU1}	Setup Time		8	—	—	ns
t_{H}	Hold Time		10	—	—	ns
t_{CO}	Falling Edge of TCK to Valid Output		—	—	15	ns
t_{PWV}	Verify Pulse Width		30	—	—	µs
t_{PWP}	Programming Pulse Width		20	—	—	ms
t_{BEW}	Bulk Erase Pulse Width		200	—	—	ms

Timing Diagrams

Figure 8. Erase (User Erase or Erase All) Timing Diagram

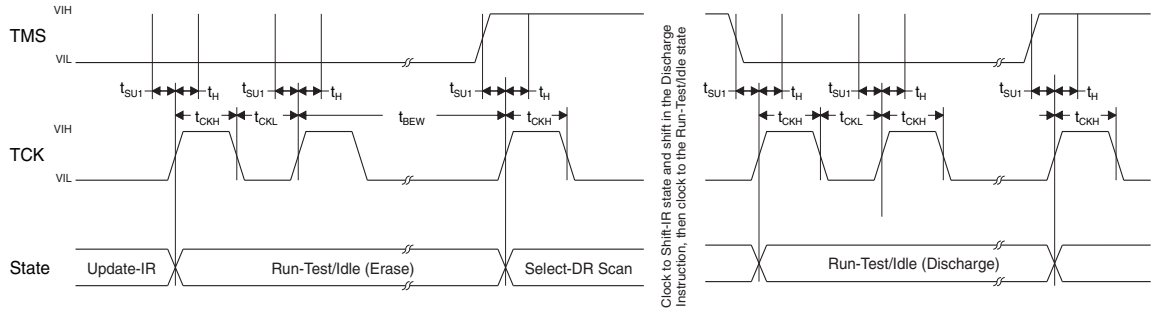


Figure 9. Programming Timing Diagram

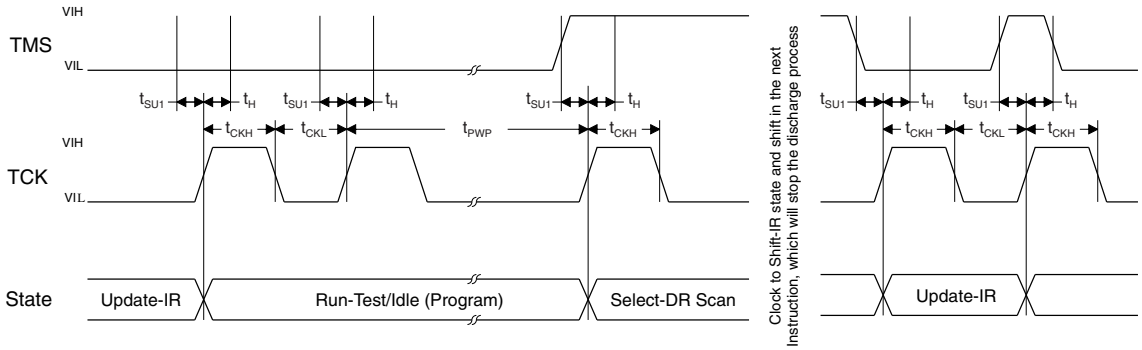


Figure 10. Verify Timing Diagram

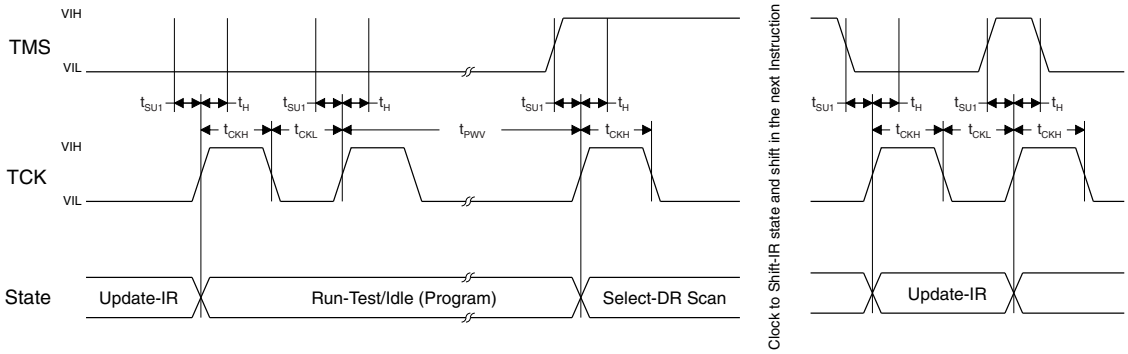
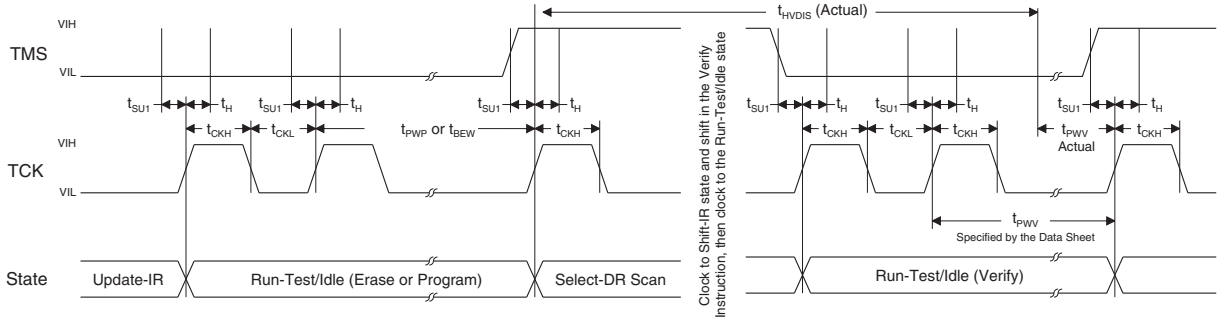
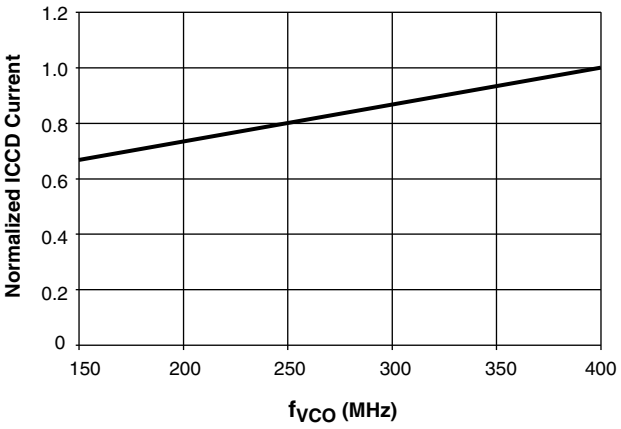


Figure 11. Discharge Timing Diagram

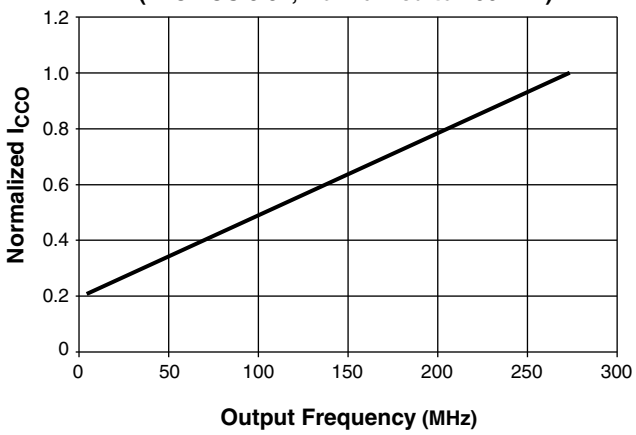


Typical Performance Characteristics

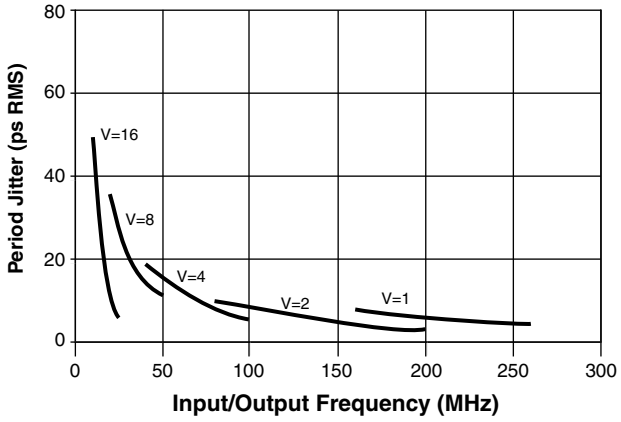
I_{CCD} vs. f_{VCO} (Normalized to 400MHz)



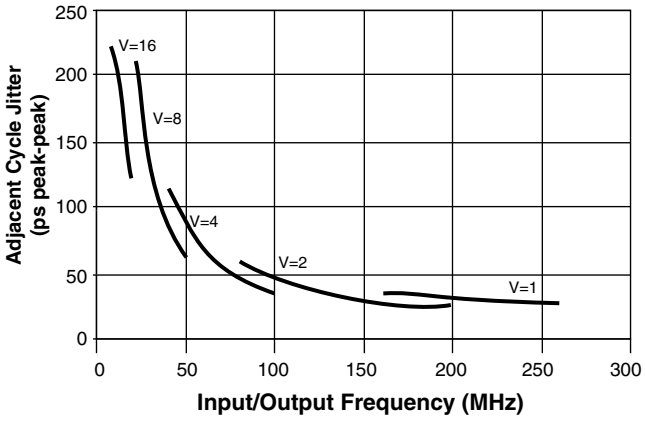
I_{CCO} vs. Output Frequency (LVCMOS 3.3V, Normalized to 266MHz)



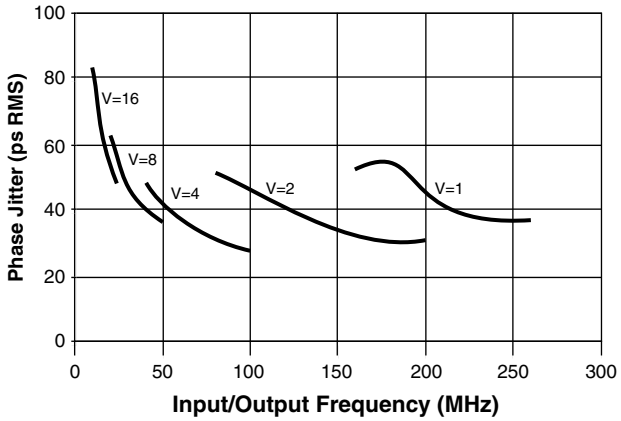
Period Jitter vs. Input/Output Frequency



Adjacent Cycle Jitter vs. Input/Output Frequency



Phase Jitter vs. Input/Output Frequency



Detailed Description

PLL Subsystem

The ispClock5300S provides an integral phase-locked-loop (PLL) which may be used to generate output clock signals at lower, higher, or the same frequency as a user-supplied input reference signal. The core functions of the PLL are an edge-sensitive phase detector, a programmable loop filter, and a high-speed voltage-controlled oscillator (VCO). Additionally, a set of programmable feedback dividers (V[0, 1, 2]) is provided to support the synthesis of different output frequencies.

Phase/Frequency Detector
The ispClock5300S provides an edge-sensitive phase/frequency detector (PFD), which means that the device will function properly over a wide range of input clock reference duty cycles. It is only necessary that the input reference clock meet specified minimum HIGH and LOW times ($t_{CLOCKHI,}$ $t_{CLOCKLO}$) for it to be properly recognized by the PFD. The PFD's output is of a classical charge-pump type, outputting charge packets which are then integrated by the PLL's loop filter.

A lock-detection feature is also associated with the PFD. When the ispClock5300S is in a LOCKED state, the LOCK output pin goes HIGH. The number of cycles required before asserting the LOCK signal in frequency-lock mode can be set from 16 through 256.

When the lock condition is lost the LOCK signal will be de-asserted (Logic '0') immediately.

Loop Filter: The loop filter parameters for each profile are automatically selected by the PAC-Designer software depending on the following:

- Maximum VCO operating frequency

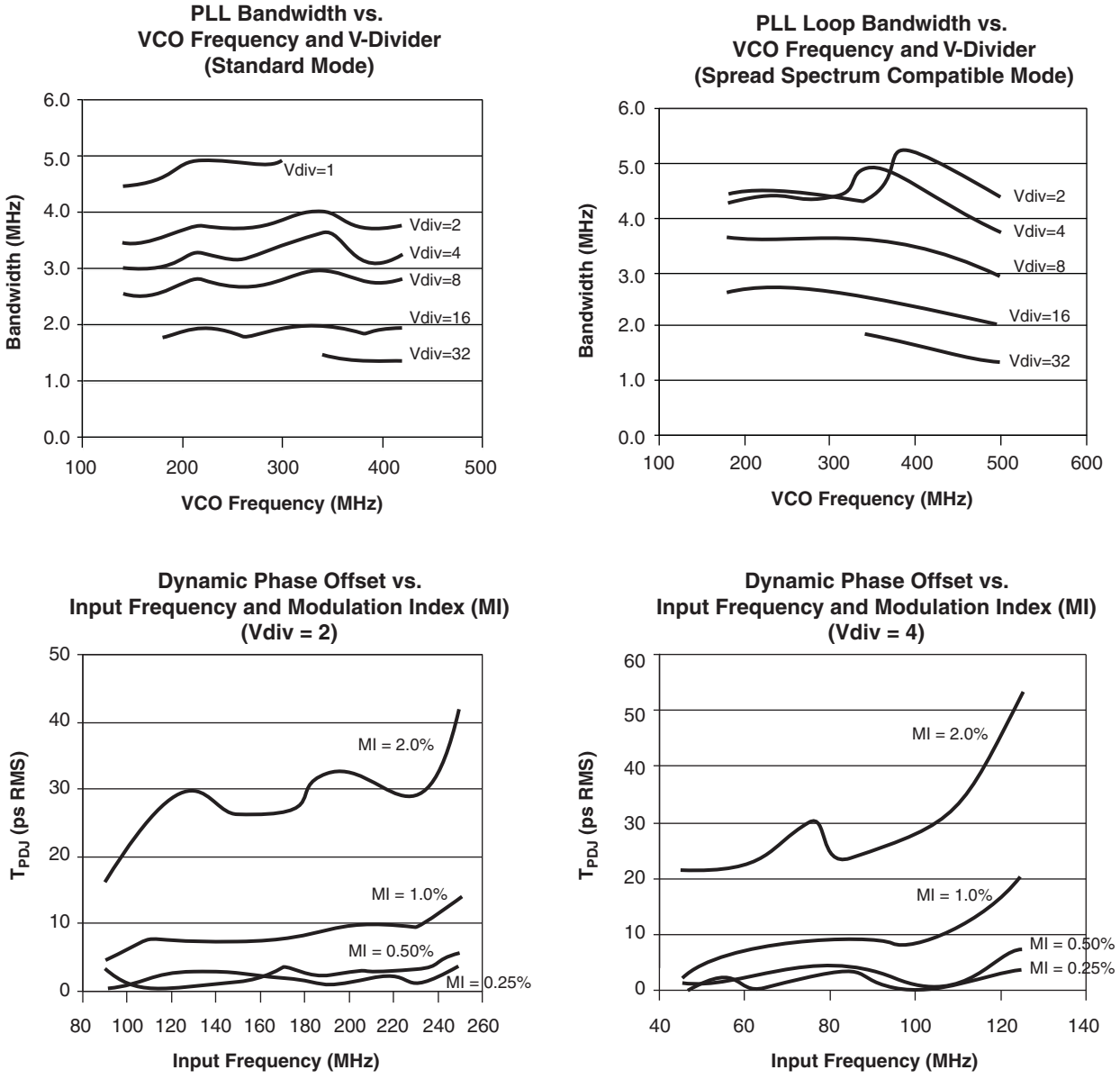
Spread Spectrum Support: The reference clock inputs of the ispClock5300S device are spread spectrum clock tolerant. The tolerance limits are:

- Center spread ±0.125% to ±2%
- Down spread -0.25% to 0.5%
- 30-33kHz modulation frequency

The ispClock5300S PLL has two modes of operation:

- Spread Spectrum setting turned on - Spread Spectrum modulation is transferred from input to output with minimal attenuation.
- Spread Spectrum setting turned off - Spread Spectrum modulation transfer from input to output is attenuated. The extent of attenuation depends on the VCO operating frequency and the feedback divider value.

Figure 12. PLL Loop Bandwidth vs. Feedback Divider Setting (Nominal)



VCO

The ispClock5300S provides an internal VCO which provides an output frequency ranging from 160MHz to 400MHz. The VCO is implemented using differential circuit design techniques which minimize the influence of power supply noise on measured output jitter. The VCO is also used to generate output clock skew as a function of the total VCO period. Using the VCO as the basis for controlling output skew allows for highly precise and consistent skew generation, both from device-to-device, as well as channel-to-channel within the same device.

Output V Dividers

The ispClock5300S incorporates a set of three 5-bit programmable Power of 2 dividers which provide the ability to synthesize output frequencies differing from that of the reference clock input.

Each one of the three V dividers can be independently programmed to provide division ratios ranging from 1 to 32 in Power of 2 steps (1, 2, 4, 8, 16, 32).

When the PLL is selected (PLL_BYPASS=LOW) and locked, the output frequency of each V divider (f_k) may be calculated as:

$$f_k = f_{ref} \frac{V_{fbk}}{V_k} \quad (1)$$

where

f_k is the frequency of V divider k
f_{ref} is the input reference frequency
V_{fbk} is the setting of the V divider used to close the PLL feedback path
V_k is the output divider K

Note that because the feedback may be taken from any V divider, V_k and V_{fbk} may refer to the same divider.

Because the VCO has an operating frequency range spanning 160 MHz to 400 MHz, and the V dividers provide division ratios from 1 to 32, the ispClock5300S can generate output signals ranging from 2.5 MHz to 267 MHz.

PLL_BYPASS Mode
The PLL_BYPASS mode is provided so that input reference signals can be coupled through to the outputs without using the PLL functions. When PLL_BYPASS mode is enabled (PLL_BYPASS=HIGH), the reference clock is routed directly to the inputs of the V dividers. The output frequency for a given V divider (f_K) will be determined by

$$f_k = \frac{f_{REF}}{V_K} \quad (2)$$

When PLL_BYPASS mode is enabled, features such as lock detect and skew generation are unavailable and the output clock is inverted when V_K=1.

Internal/External Feedback Support

The PLL feedback path can be sourced internally or externally through an output pin. When the internal feedback path is selected, one can use all output pins for clock distribution. The programmable skew feature for the feedback path is available in both feedback modes.

Reference and External Feedback Inputs

The ispClock5300S provides configurable, internally-terminated inputs for both clock reference and feedback signals.

The reference clock inputs pins can be interfaced with either one differential input (REFP, REFN) or two single-ended (REFA, REFB) inputs with the active clock selection control through REFSEL pin. The following diagram shows the possible reference clock configurations. Note: When the reference clock inputs are configured as differential input, the REFSEL pin should be grounded.

Table 2. REFSEL Operation for ispClock5300S Programmed as Single-Ended Clock Inputs

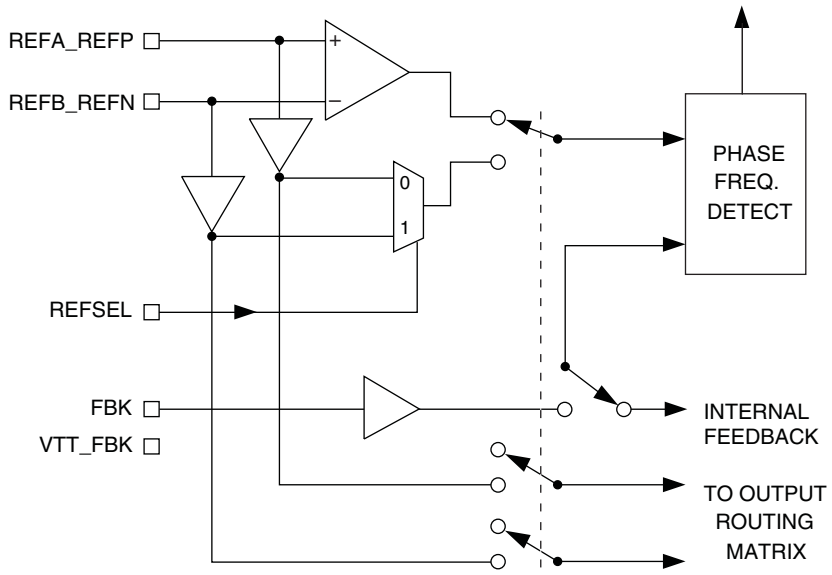
REFSEL	Selected Input
0	REFA
1	REFB

Supported input logic reference standards:

- LVTTL (3.3V)
- LVCMOS (1.8V, 2.5V, 3.3V)
- SSTL2
- SSTL3
- HSTL

- eHSTL
- Differential SSTL1.8
- Differential SSTL2
- Differential SSTL3
- Differential HSTL
- LVDS
- LVPECL (differential, 3.3V)

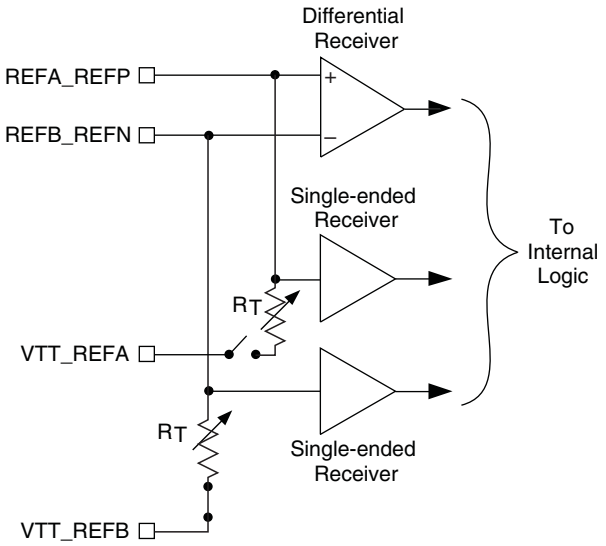
Figure 13. Reference and Feedback Input



Each input features internal programmable termination resistors as shown in Figure 14. The REFA and REFB inputs terminate to VTT_REFA and VTT_REFB respectively. In order to interface to differential clock input one should connect VTT_REFA and VTT_REFB pins together on circuit board and if necessary connect the common node to VTT supply.

The direct connection from REFA and REFB pins to the output routing matrix becomes unavailable when the REFA and REFB pins are configured as differential input pins.

Figure 14. Input Receiver Termination Configuration



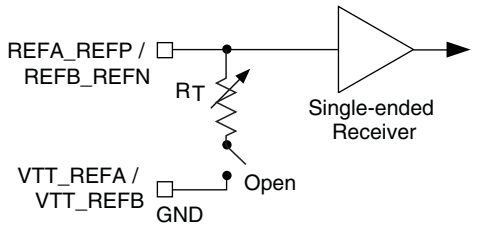
Feedback input is terminated to the VTT_FBK pin through a programmable resistor.

The following usage guidelines are suggested for interfacing to supported logic families.

LVTTL (3.3V), LVCMOS (1.8V, 2.5V, 3.3V)

The receiver should be set to LVCMOS or LVTTL mode, and the input signal can be connected to either the REFA or REFB pins. CMOS transmission lines are generally source terminated, so all termination resistors should be set to the OPEN state. Figure 15 shows the proper configuration. Please note that because switching thresholds are different for LVCMOS running at 1.8V, there is a separate configuration setting for this particular standard. Unused reference inputs and VTT pins should be grounded.

Figure 15. LVCMOS/LVTTL Input Receiver Configuration

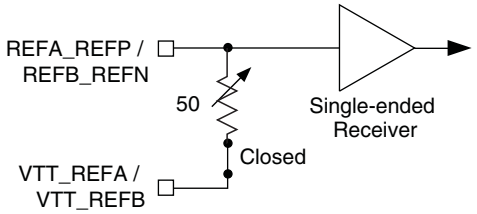


HSTL, eHSTL, SSTL2, SSTL3

The receiver should be set to HSTL/SSTL mode, and the input signal can be connected to the REFA or REFB terminal of the input pair and the associated VTT_REFA or VTT_REFB terminal should be tied to a VTT termination supply. The terminating resistor should be set to 50Ω and the engaging switch should be closed. Figure 16 shows an appropriate configuration. Refer to the "Recommended Operating Conditions - Supported Logic Standards" table in this data sheet for suitable values of V_{REF} and V_{TT}.

One important point to note is that the termination supplies must have low impedance and be able to both source and sink current without experiencing fluctuations. These requirements generally preclude the use of a resistive divider network, which has an impedance comparable to the resistors used, or of commodity-type linear voltage regulators, which can only source current. The best way to develop the necessary termination voltages is with a regulator specifically designed for this purpose. Because SSTL and HSTL logic is commonly used for high-performance memory busses, a suitable termination voltage supply is often already available in the system.

Figure 16. SSTL2, SSTL3, eHSTL, HSTL Receiver Configuration

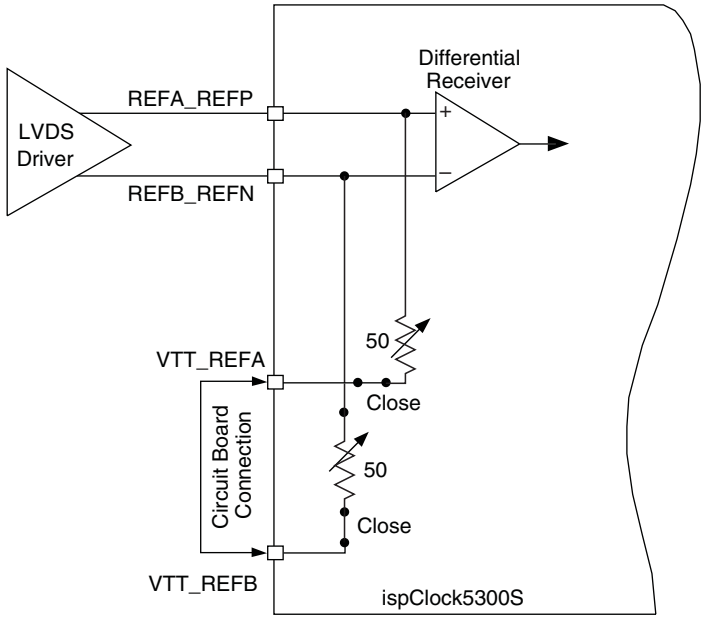


Differential LVPECL/LVDS

The receiver should be set to LVDS or LVPECL mode as required and both termination resistors should be engaged and set to 50Ω. The VTT_REFA and VTT_REFB pins, however, should be connected. This creates a floating 100Ω differential termination resistance across the input terminals. The LVDS termination configuration is shown in Figure 17.

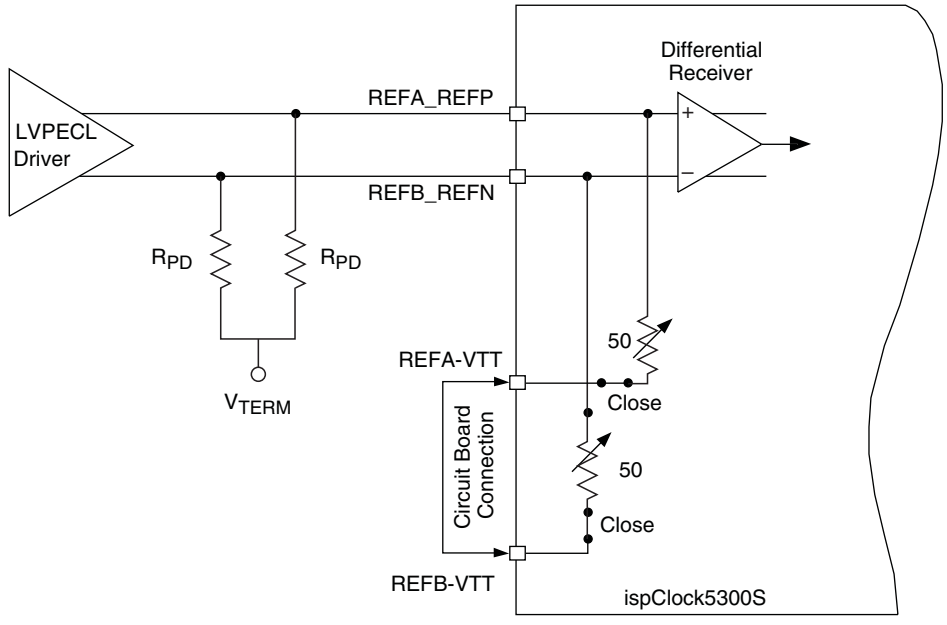
Note: the REFSEL pin should be grounded when the input receiver is configured as differential.

Figure 17. LVDS Input Receiver Configuration



Note that while a floating 100Ω resistor forms a complete termination for an LVDS signal line, additional circuitry may be required to satisfactorily terminate a differential LVPECL signal. This is because a true bipolar LVPECL output driver typically requires an external DC 'pull-down' path to a V_{TERM} termination voltage (typically VCC-2V) to properly bias its open emitter output stage. When interfacing to an LVPECL input signal, the ispClock5300S internal termination resistors should not be used for this pull-down function, as they may be damaged from excessive current. The pull-down should be implemented with external resistors placed close to the LVPECL driver (Figure 18)

Figure 18. LVPECL Input Receiver Configuration



Please note that while the above discussions specify using 50Ω termination impedances, the actual impedance required to properly terminate the transmission line and maintain good signal integrity may vary from this ideal. The

actual impedance required will be a function of the driver used to generate the signal and the transmission medium used (PCB traces, connectors and cabling). The ispClock5300S's ability to adjust input impedance over a range of 40Ω to 70Ω allows the user to adapt his circuit to non-ideal behaviors from the rest of the system without having to swap out components.

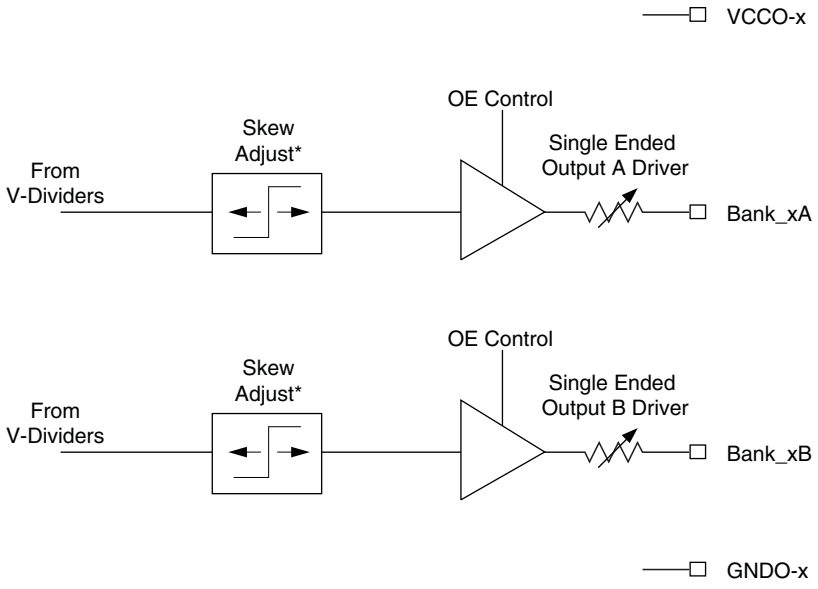
Output Drivers

The ispClock5300S provides multiple banks, with each bank supporting two high-speed clock outputs which are configurable and internally terminated. There are ten banks in the ispClock5320S, eight banks in the ispClock5316S, six banks in the ispClock5312S, four banks in the ispClock5308S and two banks in the ispClock5304S. Programmable internal source-series termination allows the ispClock5300S to be matched to transmission lines with impedances ranging from 40 to 70Ω. The outputs may be independently enabled or disabled, either from E^2CMOS configuration or by external control lines. Additionally, each can be independently programmed to provide a fixed amount of signal delay or skew, allowing the user to compensate for the effects of unequal PCB trace lengths or loading effects. Figure 19 shows a block diagram of a typical ispClock5300S output driver bank and associated skew control.

Because of the high edge rates which can be generated by the ispClock5300S clock output drivers, the VCCO power supply pin for each output bank should be individually bypassed. Low ESR capacitors with values ranging from 0.01 to 0.1 µF may be used for this purpose. Each bypass capacitor should be placed as close to its respective output bank power pins (VCCO and GNDO) pins as is possible to minimize interconnect length and associated parasitic inductances.

In the case where an output bank is unused, the associated VCCO pin may be either left floating or tied to ground to reduce quiescent power consumption. We recommend, however, that all unused VCCO pins be tied to ground where possible. All GNDO pins must be tied to ground, regardless of whether or not the associated bank is used.

Figure 19. ispClock5300S Output Driver and Skew Control



*Skew Adjust Mechanism is applicable only to outputs connected to one of the three V-Dividers and when PLL is active (PLL-Bypass pin = 0). For all other conditions, Skew Adjust Mechanism is bypassed.

Each of the ispClock5300S's output driver banks can be configured to support the following logic outputs:

- LVTTL
- LVCMOS (1.8V, 2.5V, 3.3V)
- SSTL2
- SSTL3
- HSTL
- eHSTL

To provide LVTTL, LVCMOS, SSTL2, SSTL3, HSTL and eHSTL outputs, the CMOS output drivers in each bank are enabled. These circuits provide logic outputs which swing from ground to the VCCO supply rail. The choice of VCCO to be supplied to a given bank is determined by the logic standard to which that bank is configured. Because each pair of outputs has its own VCCO supply pin, each bank can be independently configured to support a different logic standard. Note that the two outputs associated with a bank must necessarily be configured to the same logic standard. The source impedance of each of the two outputs in each bank may be independently set over a range of 40Ω to 70Ω in 5Ω steps. A low impedance option (≈20Ω) is also provided for cases where low source termination is desired on a given output.

Control of output slew rate is also provided in LVTTL, LVCMOS, SSTL2, SSTL3, HSTL and eHSTL output modes. Four output slew-rate settings are provided, as specified in the "Output Rise Times" and "Output Fall Times" tables in this data sheet.

Polarity control (true/inverted) is available for all output drivers. In the case of single-ended output standards, the polarity of each of the two output signals from each bank may be controlled independently.

Suggested Usage

Figure 20 shows a typical configuration for the ispClock5300S output driver when configured to drive an LVTTL or LVCMOS load. The ispClock5300S output impedance should be set to match the characteristic impedance of the transmission line being driven. The far end of the transmission line should be left open, with no termination resistors.

Figure 20. Configuration for LVTTL/LVCMOS Output Modes

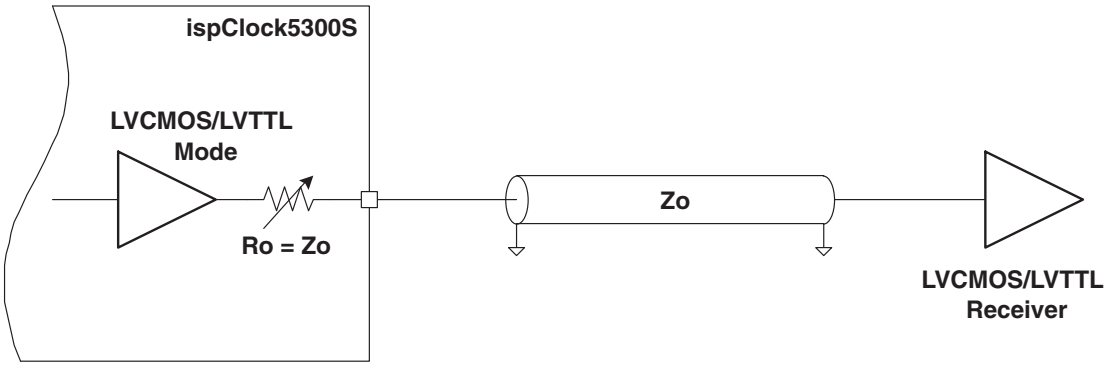


Figure 21 shows a typical configuration for the ispClock5300S output driver when configured to drive SSTL2, SSTL3, HSTL or eHSTL loads. The ispClock5300S output impedance should be set to 40Ω for driving SSTL2 or SSTL3 loads and to the ≈20Ω setting for driving HSTL and eHSTL. The far end of the transmission line must be terminated to an appropriate VTT voltage through a 50Ω resistor.