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ispClock™5400D Family

In-System Programmable, Ultra-Low Jitter Zero Delay and Fan-Out Buffer, Differential

December 2011 **Preliminary Data Sheet DS1025**

Features

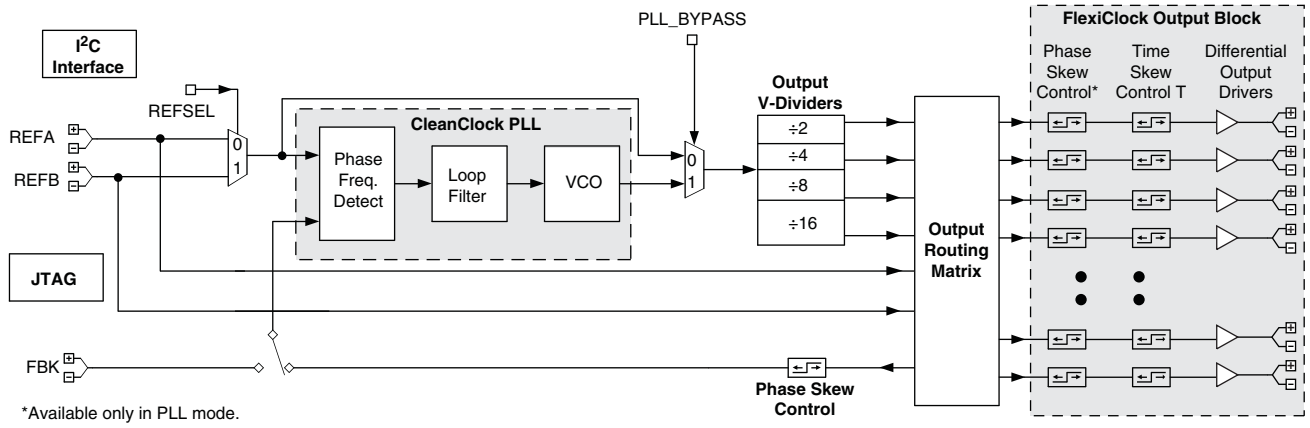
CleanClock™ PLL

- **Ultra Low Period Jitter 2.5ps**
- **Ultra Low Phase Jitter 6.5ps**
- **Fully Integrated High-Performance PLL**
  - Programmable lock detect
  - Four output dividers
  - Programmable on-chip loop filter
  - Compatible with Spread Spectrum clocks
  - Internal/external feedback
- **Flexible Clock Reference and External Feedback Inputs**
  - Programmable differential input reference/feedback standards
    - LVDS, LVPECL, HSTL, SSTL, HCSL, MLVDS
  - Programmable termination
  - Clock A/B selection multiplexer

FlexiClock™ I/O

- **40 MHz to 400 MHz Input/Output Operation**
- **Dual Programmable Skew Per Output**
  - Programmable phase adjustment
    - 16 settings; minimum step size 156 ps
    - Up to +/- 9.4 ns skew range
    - Coarse and fine adjustment modes
  - Programmable time delay adjustment
    - 16 settings; 18 ps
- **Dynamic Skew Control Through I^2C**
- **Low Output-to-Output Skew (<100ps)**
- **Up to 10 Programmable Fan-out Buffers**
  - Programmable differential output standards and individual enable controls
    - LVDS, LVPECL, HSTL, SSTL, HCSL, MLVDS
  - Up to 10 banks with individual VCCO and GND
    - 1.5V, 1.8V, 2.5V, 3.3V
- **All I/Os are Hot Socket Compliant**
- **Operating Modes**
  - Fan-out buffer with programmable output skew control
  - Zero delay buffer with dual programmable skew controls
- **Dynamic Reconfiguration through I^2C**
- **Full JTAG Boundary Scan Test In-System Programming Support**
- **Exceptional Power Supply Noise Immunity**
- **Commercial (0° to 70°C) and Industrial (-40° to 85°C) Temperature Ranges**
- **48-Pin and 64-pin QFNS Packages**
- **Applications**
  - Low-cost clock source for SERDES
  - ATCA, MicroTCA, AMC, PCI Express
  - Differential Clock Distribution
  - Generic Source Synchronous Clock Management
  - Zero-delay clock buffer

ispClock5400D Family Functional Diagram



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General Description

The ispClock5400D family integrates a CleanClock PLL and a FlexiClock Output block. The CleanClock PLL provides an ultra-low-jitter clock source to a set of four V-dividers. The FlexiClock output block receives the clock output from these V-dividers through an output switch matrix and distributes them to the output pin using a programmable logic interface. There are two members in the ispClock5400D family, the ispClock5410D (10-output FlexiCLock block) and the ispClock5406D (6-output FlexiClock block). Each of the outputs may be independently configured to support separate I/O standards (LVDS, LVPECL, SSTL, HSTL, MLVDS, HCSL) and output frequency. In addition, the skew of each of the outputs can be independently controlled. All configuration information is stored on-chip in non-volatile E^2CMOS® memory.

The ispClock5400D devices provide extremely low propagation delay (zero-delay) from input to output using the CleanClock PLL. The PLL VCO output clock frequency is divided down by a set of four V- dividers. The output frequencies from these V-dividers, $f_{VCO} \div 2$, $f_{VCO} \div 4$, $f_{VCO} \div 8$ and $f_{VCO} \div 16$ are connected to the output routing matrix. The output routing matrix enables any output pin to derive its clock from any of the V-dividers outputs. Additionally, the reference input clock can be connected directly to any output through the output routing matrix.

The FlexiClock block supports dual skew mechanisms: Phase Skew Control and Time Skew Control. These skew control mechanisms enable fixed output clock skew control during power-up and variable skew during operation.

The ispClock5400D device can be configured to operate in four modes: zero delay buffer mode, dual non-zero delay buffer mode, non-zero delay buffer mode with output dividers, and combined zero-delay and non-zero delay buffer mode.

The I^2C interface can be used to dynamically control the ispClock5400D configuration: Output clock frequency, Phase Skew, Time skew, Fan-out buffer mode, Output enable.

The core functions of both members of the ispClock5400D family are identical. Table 1 summarizes the ispClock5400D device family.

Table 1. ispClock5400D Family

Device	Number of Programmable Differential Clock Inputs	Number of Programmable Differential Outputs
ispClock5410D	2	10
ispClock5406D	2	6

Figure 1. ispClock5410D Functional Block Diagram

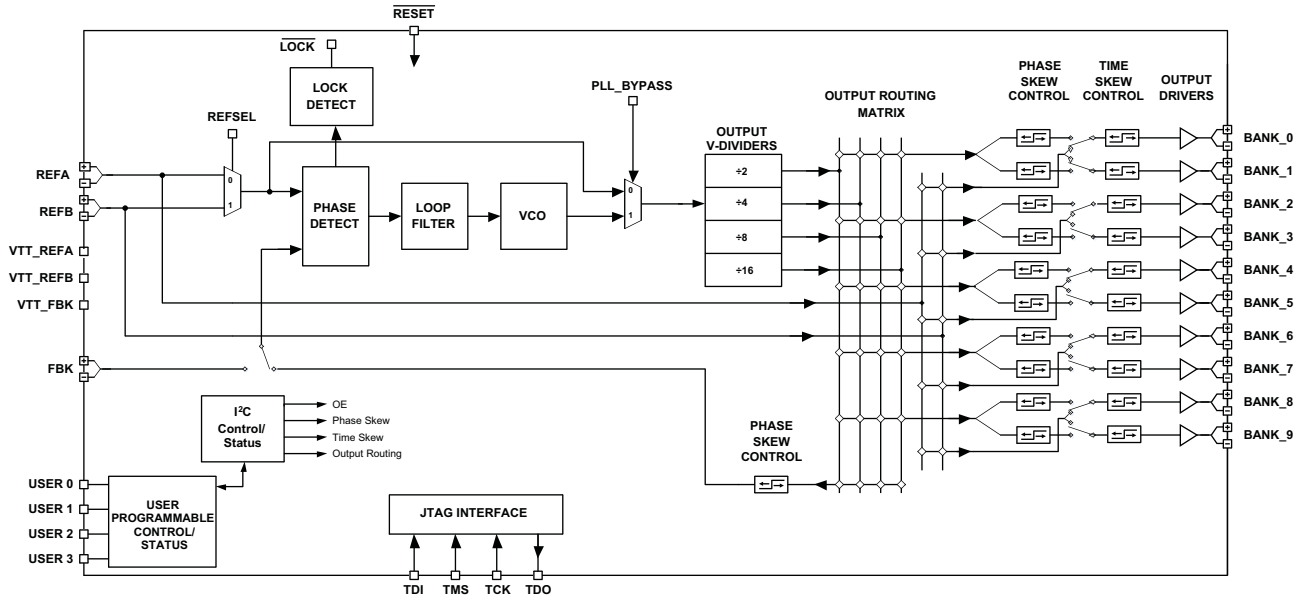
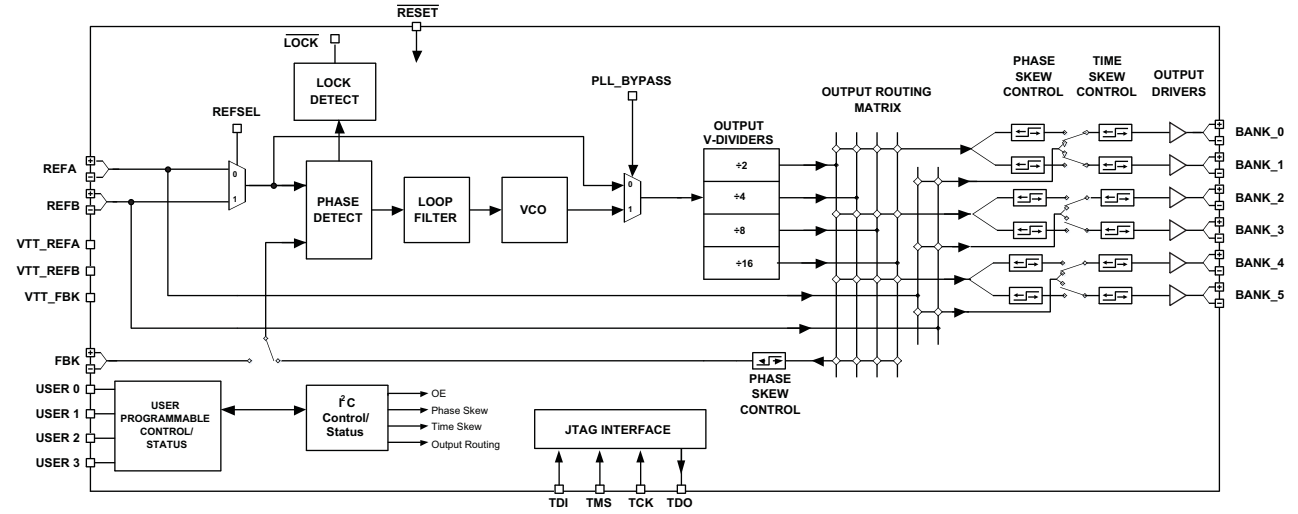


Figure 2. ispClock5406D Functional Block Diagram



Absolute Maximum Ratings

	ispClock5400D
Core Supply Voltage V_{CCD}	-0.5 to 5.5V
PLL Supply Voltage V_{CCA}	-0.5 to 5.5V
JTAG Supply Voltage V_{CCJ}	-0.5 to 5.5V
Output Driver Supply Voltage V_{CCO}	-0.5 to 4.5V
Input Voltage	-0.5 to 4.5V
Output Voltage[1]	-0.5 to 4.5V
Storage Temperature	-65 to 150°C
Junction Temperature with power supplied	-40 to 125°C

1. When applied to an output when in high-Z condition

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CCD}	Core Supply Voltage		3.0	3.6	V
V_{CCJ}	JTAG I/O Supply Voltage		2.25	3.6	V
V_{CCA}	Analog Supply Voltage		3.0	3.6	V
$V_{CCXSLEW}$	V_{CC} Turn-on Ramp Rate	All supply pins	—	0.33	V/µs
T_{JCOM}	Junction Temperature	Commercial	0	85	°C
T_{JIND}		Industrial	-40	100	

Recommended Operating Conditions – V_{CCO} vs. Logic Standard

Logic Standard	V_{CCO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
HCSL	3.135	3.3	3.465						
SSTL15	1.425	1.5	1.575	0.7	0.75	0.8		0.5 x V_{CCO}	
SSTL18	1.7	1.8	1.9	0.84	0.9	0.95		0.5 x V_{CCO}	
SSTL2 Class 1	2.3	2.5	2.7	1.15	1.25	1.35	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
HSTL Class 1	1.4	1.5	1.6	0.68	0.75	0.9		0.5 x V_{CCO}	
eHSTL Class 1	1.65	1.8	1.95	0.84	0.9	0.95		0.5 x V_{CCO}	
LVPECL	2.97	3.3	3.63						
LVDS25	2.25	2.5	2.75						
LVDS33	2.97	3.3	3.63						
MLVDS	2.25	2.5	2.75						

ESD Performance

Pin Group	ESD Stress	Min.	Units
All pins	HBM	2000	V
	CDM	1000	V

E²CMOS Memory Write/Erase Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Erase/Reprogram Cycles		1000	—	—	

Performance Characteristics – Power Supply

Symbol	Parameter	Conditions	Typ.	Max	Units
I_{CCD}	Core Supply Current[1]	f_{VCO} = 800MHz, Internal Feedback	94	99	mA
		PLL Bypassed	65	71	mA
$I_{CCDADDER}$	Incremental ICCD Per Active Output	f_{OUT} = 400 MHz	2.8	3.2	mA
$I_{CCDADDER-TSK}$	Incremental ICCD for the First T-Skew Block		4.0	4.9	mA
$I_{CCDADDER-HCSL}$	Incremental ICCD For the First HCSL Output		4.0	5.2	mA
$I_{CCDADDER-REFB}$	Incremental ICCD Due to Active REFB INPUT	F_{IN} = 400 MHz	6.0	10	mA
I_{CCA}	Analog Supply Current[1]	f_{VCO} = 800MHz, Internal Feedback	23	30	mA
I_{CCO}	Output Driver Supply Current	Output Logic Standard = SSTL15, f_{OUT} = 400MHz	21	22	mA
		Output Logic Standard = SSTL18 f_{OUT} = 333MHz	24	27	mA
		Output Logic Standard = SSTL2 f_{OUT} = 267MHz	34	37	mA
		Output Logic Standard = HSTL f_{OUT} = 333MHz	19	21	mA
		Output Logic Standard = eHSTL f_{OUT} = 333MHz	19	21	mA
		Output Logic Standard = LVPECL f_{OUT} = 400MHz	20	22	mA
		Output Logic Standard = LVDS33 f_{OUT} = 400MHz	10	11	mA
		LVDS25 f_{OUT} = 400MHz	8	9	mA
		Output Logic Standard = MLVDS f_{OUT} = 266MHz	16	19	mA
		Output Logic Standard = HCSL[2] f_{OUT} = 150MHz	22	24	mA
I_{CCJ}	JTAG I/O Supply Current (Static)	V_{CCJ} = 2.5V	350	500	µA
		V_{CCJ} = 3.3V	350	500	µA

1. All unused REFCLK and FBK pins grounded. Fin = 50 MHz, internal feedback.
2. 6x HCSL current setting.

DC Electrical Characteristics – Single-Ended Logic for USER, RESET and JTAG Pins

Logic Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min.	Max.	Min.	Max.				
LVTTL/LVCMOS 3.3V	-0.3	0.8	2	3.6	0.4	V_{CCO} - 0.4	4	-4
LVCMOS 1.8V[1]	-0.3	0.68	1.07	3.6	0.4	V_{CCO} - 0.4	4	-4
LVCMOS 2.5V	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	4	-4
User I/O in I²C Mode	-0.3	0.3 x V_{CCD}	0.7 x V_{CCD}	3.6V	0.4	V_{CCD} - 0.4	8	—

1. User and reset pins only.

Differential Input Characteristics (Applicable to REFA, REFB, FBK)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{ICM}	Common Mode Input Voltage - LVDS		0.1	—	2.35	V
V_{THD}	Differential Input Threshold - LVDS	100mV < V_{ICM} < 300mV	±100	—	—	mV
		300mV <V_{ICM} < 2.35V	±50	—	—	mV
V_{IX}	Input Pair Differential Crosspoint Voltage	SSTL15, SSTL18, HSTL, eHSTL, LVPECL, HCSL	0.3		2.35	V

Output Electrical Characteristics – LVDS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	R_T = 100Ω	—	1.375	1.6	V
V_{OL}	Output Low Voltage	R_T = 100Ω	0.9	1.03	—	V
V_{OD}	Output Voltage Differential	R_T = 100Ω	250	400	450	mV
ΔV_{OD}	Change in V_{OD} Between H and L		—	—	50	mV
V_{OS}	Output Voltage Offset	Common Mode Output Voltage	1.1	1.2	1.375	V
ΔV_{OS}	Change in V_{OD} Between H and L		—	—	50	mV
I_{SA}	Output Short Circuit Current	V_{OD} = 0V, Outputs Shorted to GND, LVDS25	—	—	24	mA
		V_{OD} = 0V, Outputs Shorted to GND, LVDS33			35	mA
I_{SAB}	Output Short Circuit Current	V_{OD} = 0V, Outputs Shorted to Each Other	—	—	5	mA
DC_{CKOUT}	Output Clock Duty Cycle		48		52	%
DC-ERROR	Error in Duty Cycle[1]	LVDS25 (Figure 3)	-50		50	ps
		LVDS33 (Figure 3)	-65		65	ps
t_{RF}	Rise and Fall Time[1]	LVDS25 (Figure 3)	250		550	ps
		LVDS33 (Figure 3)	260		400	ps

1. Measured at f_{OUT} = 400 MHz.

Output Electrical Characteristics – Differential LVPECL

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage[1]	V_{CCO} = 3.0V to 3.6V	V_{CCO} - 1.1	—	V_{CCO} - 0.88	V
		V_{CCO} = 3.3V	2.20	—	2.42	V
V_{OL}	Output Low Voltage[1]	V_{CCO} = 3.0V to 3.6V	V_{CCO} - 1.86	—	V_{CCO} - 1.62	V
		V_{CCO} = 3.3V	1.44	—	1.68	V
V_{OD}	Output Voltage Differential		0.6	—	1	V
DC_{CKOUT}	Output Clock Duty Cycle[2]	Figure 3	47		53	%
t_{RF}	Rise and Fall Time[2]	Figure 3	300		400	ps

1. 100Ω differential termination.
2. Measured at f_{OUT} = 400 MHz.

Electrical Characteristics – Differential SSTL15

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	V_{CCO} = 1.425V (Test Circuit) I_{OH} = -8mA	V_{CCO} - 0.4			V
V_{OL}	Output Low Voltage	V_{CCO} = 1.425V (Test Circuit) I_{OL} = 8mA			0.4	mV
V_{OX}	Output Differential Pair Crosspoint Voltage	Figure 6	$V_{CCO}/2$ - 0.1		$V_{CCO}/2$ + 0.1	V
DC_{CKOUT}	Output Clock Duty Cycle[1]	Figure 6	45		55	%
t_{RF}	Rise and Fall Time[1]	Figure 6	350		460	ps

1. Measured at f_{OUT} = 400 MHz.

Electrical Characteristics – Differential SSTL18

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	I_{OH} = -9mA, V_{CCO} = 1.7V	1.1			V
V_{OL}	Output Low Voltage	I_{OL} = 9mA, V_{CCO} =1.7V			0.6	mV
V_{OX}	Output Differential Pair Crosspoint Voltage	Figure 6	$V_{CCO}/2$ - 0.05		$V_{CCO}/2$ + 0.2	V
DC_{CKOUT}	Output Clock Duty Cycle[1]	Figure 6	45		55	%
t_{RF}	Rise and Fall Time[1]	Figure 6	230		380	ps

1. Measured at f_{OUT} = 333 MHz.

Electrical Characteristics – Differential SSTL2

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	I_{OH} = -8mA, V_{CCO} = 2.3V	1.74			V
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CCO} = 2.3V			0.56	mV
V_{OX}	Output Differential Pair Crosspoint Voltage	Figure 6	V_{REF} - 200 mV		V_{REF} + 200 mV	V
DC_{CKOUT}	Output Clock Duty Cycle[1]	Figure 6	45		55	%
t_{RF}	Rise and Fall Time[1]	Figure 6	260		400	ps

1. Measured at f_{OUT} = 267 MHz.

Electrical Characteristics – Differential HSTL

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	I_{OH} = -8.1mA, V_{CCO} = 1.4V	V_{CCO} - 0.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.1mA, V_{CCO} =1.4V			0.4	mV
V_{OX}	Output Differential Pair Crosspoint Voltage	Figure 5	$V_{CCO}/2$ - 0.1		$V_{CCO}/2$ + 0.1	V
DC_{CKOUT}	Output Clock Duty Cycle[1]	Figure 5	45		55	%
t_{RF}	Rise and Fall Time[1]	Figure 5	300		460	ps

1. Measured at f_{OUT} = 333 MHz.

Electrical Characteristics – Differential eHSTL

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	I_{OH} = -8.1mA, V_{CCO} = 1.65V	V_{CCO} - 0.45			V
V_{OL}	Output Low Voltage	I_{OL} = 8.1mA, V_{CCO} =1.65V			0.45	mV
V_{OX}	Output Differential Pair Crosspoint Voltage	Figure 5	V_{CCO}/2 - 0.05		V_{CCO}/2 + 0.2	V
DC_{CKOUT}	Output Clock Duty Cycle[1]	Figure 5	45		55	%
t_{RF}	Rise and Fall Time[1]	Figure 5	250		400	ps

1. Measured at f_{OUT} = 333 MHz.

Electrical Characteristics – MLVDS

Symbol	Description	Conditions	Min.	Typ.	Max.	Units
V_{OD}	Differential Output Voltage Magnitude	Figure 8b	480		650	mV
ΔV_{OD}	Change in Differential Output Voltage Magnitude Between Logic States	Figure 8b	-50		+50	mV
V_{OS}	Output Voltage Offset	Figure 8a	1		1.4	V
ΔV_{OS}	Change in V_{OS} Between H and L		-50		50	mV
V_{OC}	Output Open Circuit Steady State Voltage		0		2.4	V
I_{SAB}	Output Short Circuit Current, Outputs Shorted				24	mA
I_{SA}	Output Short Circuit Current	Figure 8c			43	mA
DC_{CKOUT}	Output Clock Duty Cycle[1]	Figure 4	48		52	%
t_{RF}	Rise and Fall Time[1]	Figure 4	280		510	ps

1. Measured at f_{OUT} = 266 MHz.

Electrical Characteristics – HCSL

Symbol	Description	Conditions	Min.	Max.	Units
V_{OX}	Output Differential Pair Crosspoint Voltage	Crossing Point at Max. Swing of 0.7V	250	550	mV
ΔV_{OX}	V_{OX} Variation Across All Edges			140	mV
V_{OH}	Output High Voltage	Figure 7	1.3		V
t_R	Edge Rate Rising	Differential[1] (Figure 7)	0.6	4	V/ns
t_F	Edge Rate Falling	Differential[1] (Figure 7)	0.6	4	V/ns

1. Differential output signal, ±150mV from 0V crossing.

DC Electrical Characteristics – Input/Output Loading

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{LK}	Input Leakage	Note 1	—	—	±10	µA
I_{PU}	Input Pull-up Current	USER[3:0], Note 2	—	80	120	µA
I_{PD}	Input Pull-down Current	USER[3:0]	—	80	120	µA
I_{OLK}	Tristate Leakage Output	Note 4	—	—	±10	µA
C_{IN}	Input Capacitance	Notes 2, 3, 5	—	5	7	pF
		Note 1	—		8	pF

1. Applies to clock reference inputs and feedback inputs when termination 'open'.
2. Applies to TDI, TDO, TMS and $\overline{\text{RESET}}$ inputs.
3. Applies to USER[0..3] pins.
4. Applies to all logic types when in tristated mode.
5. Applies to TCK, $\overline{\text{RESET}}$ and USER inputs.

Switching Characteristics – Timing Adders for I/O Modes

Adder Type	Description	Min.	Typ.	Max.	Units
t_{IOO} Output Adders[1, 2]					
SSTL2_out	Output Configured as SSTL2 Buffer		0.4		ns
SSTL18_out	Output Configured as SSTL18 Buffer		-0.6		ns
SSTL15_out	Output Configured as SSTL15 Buffer		-0.5		ns
HSTL_out	Output Configured as HSTL Buffer		-0.5		ns
eHSTL_out	Output Configured as eHSTL Buffer		-0.6		ns
MLVDS_out	Output Configured as MLVDS Buffer		0.25		ns
HCSL_out	Output Configured as HCSL		0.35		ns
LVDS25_out	Output Configured as LVDS25		0.25		ns
LVPECL_out	Output Configured as LVPECL		0		ns

1. Measured under standard output load conditions, see Figures 3 to 8.
2. All output adders referenced to LVDS33.

Output Test Loads

Figures 3 to 8 show the equivalent termination loads used to measure rise/fall times, output timing adders and other selected parameters as noted in the various tables of this data sheet.

Figure 3. LVDS/LVPECL Termination Load

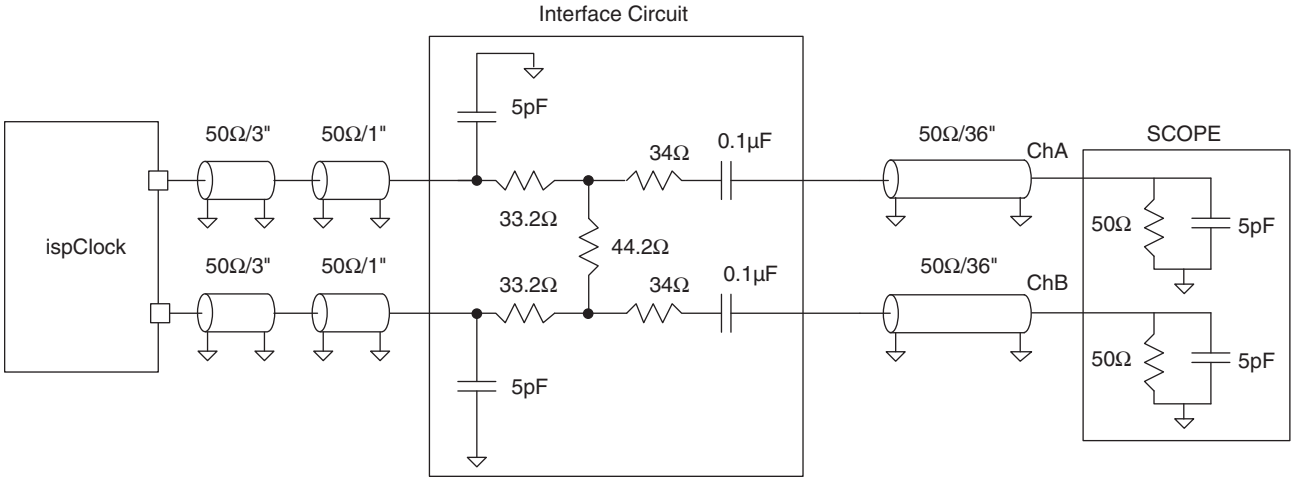


Figure 4. MLVDS Termination Load

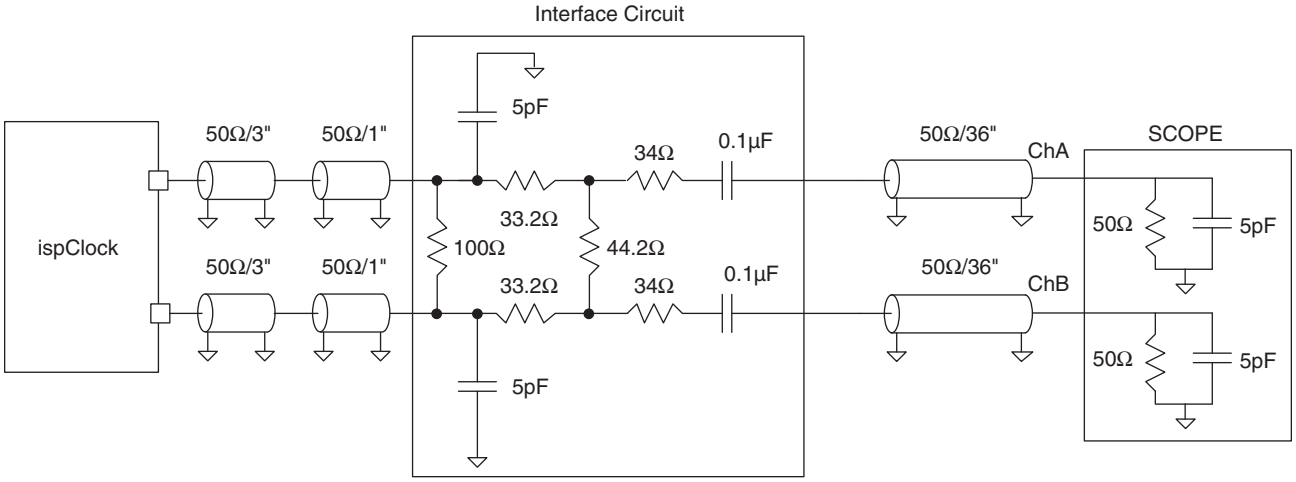


Figure 5. Differential HSTL Termination Load

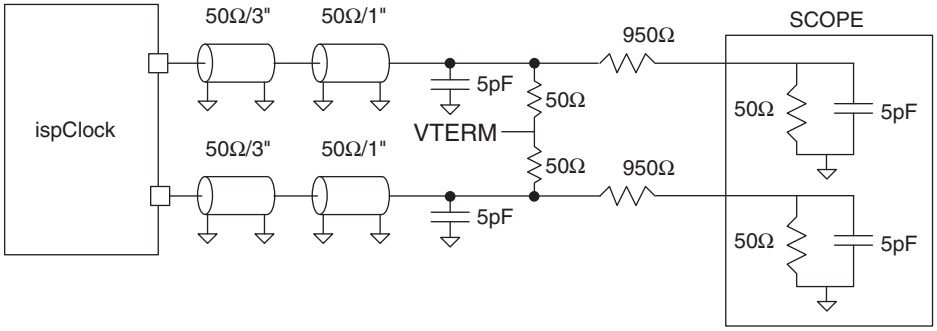


Figure 6. Differential SSTL Termination Load

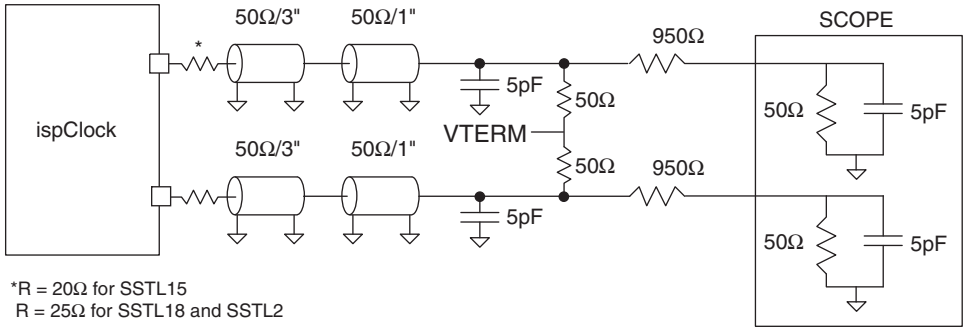


Figure 7. HCSL Termination Load

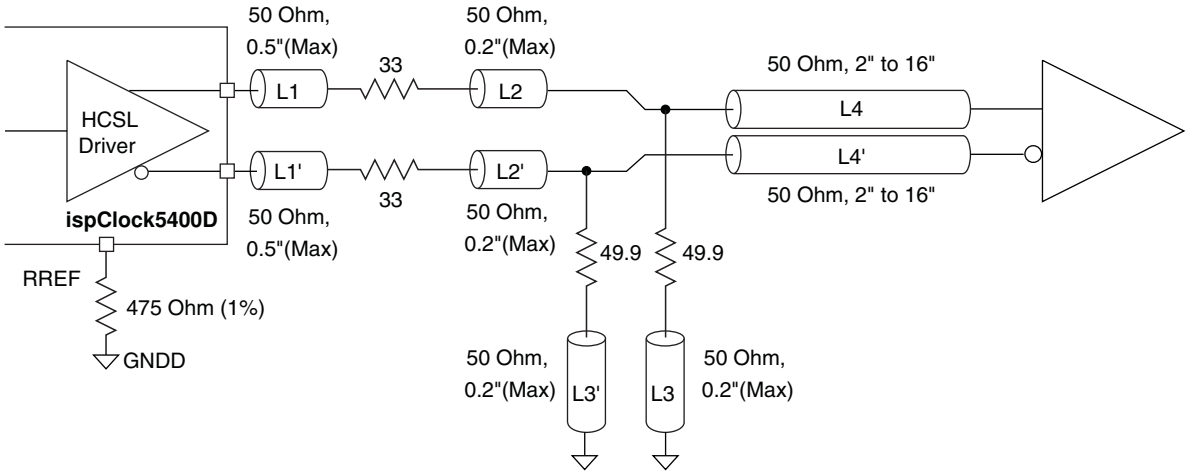
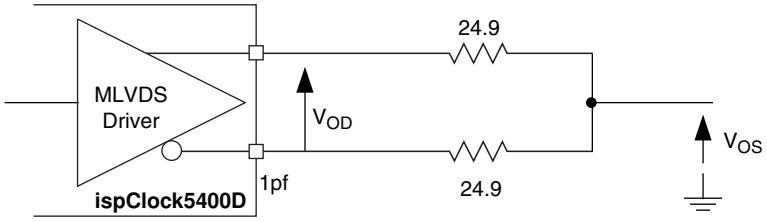
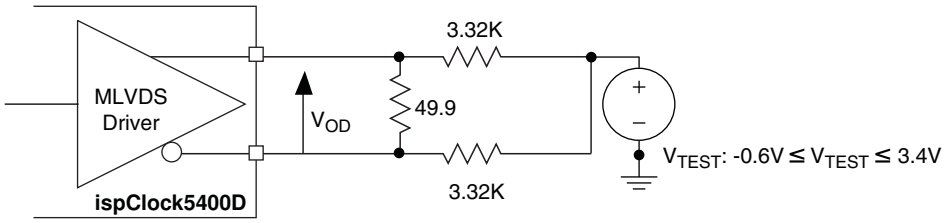


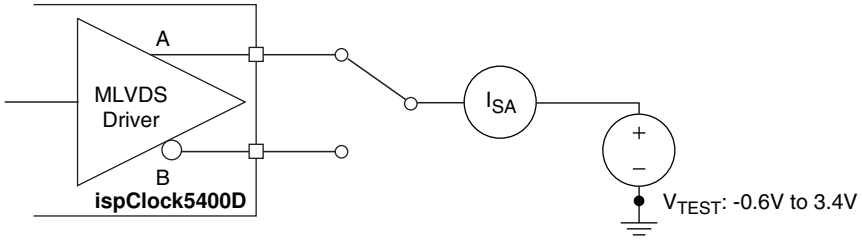
Figure 8. MLVDS Termination Load



(a) Common Mode Output Voltage Test Circuit



(b) Differential Output Voltage Test Circuit



(c) Short Circuit Curreent (I_{SA}) Test Circuit

Performance Characteristics – PLL

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{REF}, f_{FBK}	Reference and Feedback Input Frequency Range		40[1]		400[7]	MHz
$t_{CLOCKHI}$, $t_{CLOCKLO}$	Reference and Feedback Input Clock HIGH and LOW Times		900			ps
t_{RINP}, t_{FINP}	Reference and Feedback Input Rise and Fall Times	Measured Between 20% and 80% Levels			5	ns
f_{PFD}	Phase Detector Input Frequency Range		40		400[7]	MHz
f_{VCO}	V_{CO} Operating Frequency		400		800	MHz
V_{DIV}	Output Divider Range (Power of 2)		2		32	
f_{OUT}	Output Frequency Range[1]	Fine Skew Mode	25		400[5]	MHz
		Coarse Skew Mode	12.5		200[5]	MHz
t_{JIT} (cc)	Output Adjacent-Cycle Jitter[4] (1000-Cycle Sample)				29	ps (p-p)
t_{JIT} (per)	Output Period Jitter[4] (10000-Cycle Sample)				2.5	ps (RMS)
$t_{JIT(\phi)}$	Reference Clock to Feedback Jitter (2000-Cycle Sample)[6]			6.5		ps (RMS)
$t\phi$	Static Phase Offset[3]	PFD Input Frequency ≥ 100MHz	-5	45	95	ps
$t\phi_{DYN}$	Dynamic Phase Offset	Spread Spectrum Modulation Index = -0.5%			50	ps
t_{PD_FOB}	Reference to Output Propagation Delay in Non-Zero Delay Buffer Mode[2]	Time Skew Control Disabled		6		ns
$t_{PD\_FOB\_TS\_EN}$	Reference to Output Delay in Non-Zero Delay Buffer Mode[2]	Time Skew Control Enabled		7		ns
t_{DELAY}	Reference to Output Delay with Internal Feedback Mode[2]	V=2		4		ns
t_{LOCK}	PLL Lock Time	From Power-up Event		2.5	15	ms
t_{RELOCK}	PLL Relock Time	$f_{IN} = f_{OUT}$ = 100 MHz		2.5		ms

1. In PLL Bypass mode (PLL_BYPASS = HIGH), input and output will support frequencies down to 0Hz (divider chain is a fully static design).
2. Input and outputs LVPECL mode
3. Inserted feedback loop delay < 5ns
4. Measured with f_{OUT} = 100MHz, f_{VCO} = 800MHz, input and output interface set to LVDS, internal feedback.
5. Also dependent on output type.
6. Measured with f_{OUT} = 100MHz, f_{VCO} = 800MHz, input and output interface set to LVPECL, external feedback.
7. In Coarse Skew Mode, maximum input frequency is 200MHz.

Timing Specifications

Skew Matching[1]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{SKEW}	Output-Output Skew	Between any two identically configured and loaded outputs, regardless of bank, on the same device.	—	—	75	ps
$t_{SKEW-FOB}$		T-skew Disabled			75	ps
$t_{SKEW-FOB-TS-EN}$		T-skew Enabled			100	ps

1. LVPECL outputs.

Programmable Skew Control

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{PSKRANGE}$	Phase Skew Control Range[1]	Fine Skew Mode, f_{VCO} = 400 MHz	—	4.68	—	ns
		Fine Skew Mode, f_{VCO} = 800 MHz	—	2.34	—	
		Coarse Skew Mode, f_{VCO} = 400 MHz	—	9.38	—	
		Coarse Skew Mode, f_{VCO} = 800 MHz	—	4.68	—	
PSK_{STEPS}	Phase Skew Steps per Range		—	16	—	
$t_{PSKSTEP}$	Phase Skew Step Size[2]	Fine Skew Mode, f_{VCO} = 400 MHz	—	312	—	ps
		Fine Skew Mode, f_{VCO} = 800 MHz	—	156	—	
		Coarse Skew Mode, f_{VCO} = 400 MHz	—	625	—	
		Coarse Skew Mode, f_{VCO} = 800 MHz	—	312	—	
t_{PSKERR}	Phase Skew Time Error at Any Skew Setting[3]	Fine skew mode	—	10	—	ps
		Coarse skew mode	—	10	—	

1. Skew control range is a function of V_{CO} frequency (f_{VCO}). In fine skew mode $T_{SKRANGE} = 15/(8 \times f_{VCO})$. In coarse skew mode $T_{SKRANGE} = 15/(4 \times f_{VCO})$.
2. Skew step size is a function of V_{CO} frequency (f_{VCO}). In fine skew mode $T_{SKSTEP} = 1/(8 \times f_{VCO})$. In coarse skew mode $T_{SKSTEP} = 1/(4 \times f_{VCO})$.
3. Only applicable to outputs with non-zero skew settings.

Programmable Skew Control – Time Skew

Symbol	Description	Conditions	Min.	Typ.	Max.	Units
$t_{T-SK-RANGE}$	Time-Skew Control Range		—	270	—	ps
$t_{SK-STEPS}$	Number of Time-Skew Steps		—	16	—	ps
$t_{T-SK-STEP}$	Time-skew Step Size		—	18	—	ps
$t_{T-SKERR}$	Step Size Error at Any Skew Setting		—	5	—	ps

Control Functions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{DIS/OE}$	Delay Time, OEb or GOEb to Output Disabled/Enabled		—	10	20	ns
t_{PLL_RSTW}	PLL $\overline{\text{RESET}}$ Pulse Width		10	—		µs
RST_SLEW	Reset Signal Slew Rate				1	V/µs

Boundary Scan Logic

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK (BSCAN Test) Clock Cycle	40	—	ns
t_{BTCH}	TCK (BSCAN Test) Pulse Width High	20	—	ns
t_{BTCL}	TCK (BSCAN Test) Pulse Width Low	20	—	ns
t_{BTSU}	TCK (BSCAN Test) Setup Time	8	—	ns
t_{BTH}	TCK (BSCAN Test) Hold Time	10	—	ns
t_{BRF}	TCK (BSCAN Test) Rise and Fall Rate	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	10	ns
t_{BTOZ}	TAP Controller Falling Edge of Clock to Data Output Disable	—	10	ns
t_{BTVO}	TAP Controller Falling Edge of Clock to Data Output Enable	—	10	ns
$t_{BVTCPSU}$	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCPH}	BSCAN Test Capture Register Hold Time	10	—	ns
t_{BTUCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	25	ns
t_{BTUOZ}	BSCAN Test Update Register, Falling Edge of Clock to Output Disable	—	25	ns
t_{BTUOV}	BSCAN Test Update Register, Falling Edge of Clock to Output Enable	—	25	ns

JTAG Interface and Programming Mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum TCK Clock Frequency		—	—	25	MHz
t_{CKH}	TCK Clock Pulse Width, High		20	—	—	ns
t_{CKL}	TCK Clock Pulse Width, Low		20	—	—	ns
t_{ISPEN}	Program Enable Delay Time		15	—	—	µs
t_{ISPDIS}	Program Disable Delay Time		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Program		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Erase		200	—	—	µs
t_{CEN}	Falling Edge of TCK to TDO Active		—	—	15	ns
t_{CDIS}	Falling Edge of TCK to TDO Disable		—	—	15	ns
t_{SU1}	Setup Time		8	—	—	ns
t_{H}	Hold Time		10	—	—	ns
t_{CO}	Falling Edge of TCK to Valid Output		—	—	15	ns
t_{PWV}	Verify Pulse Width		30	—	—	µs
t_{PWP}	Programming Pulse Width		20	—	—	ms
t_{BEW}	Bulk Erase Pulse Width		200	—	—	ms

I²C Port Characteristics

Symbol	Definition	100KHz		400KHz		Units
		Min.	Max.	Min.	Max.	
F_{I^2C}	I^2C clock/data rate		100		400	KHz
$T_{SU;STA}$	After start	4.7		0.6		us
$T_{HD;STA}$	After start	4		0.6		us
$T_{SU;DAT}$	Data setup	250		100		ns
$T_{SU;STO}$	Stop setup	4		0.6		us
$T_{HD;DAT}$	Data hold; SCL= Vih_min = 2.1V	0.3	3.45	0.3	0.9	us
T_{LOW}	Clock low period	4.7		1.3		us
T_{HIGH}	Clock high period	4		0.6		us
T_F	Fall time; 2.25V to 0.65V		300		300	ns
T_R	Rise time; 0.65V to 2.25V		1000		300	ns
$T_{TIMEOUT}$	Detect clock low timeout	25	35	25	35	ms
T_{POR}	Device must be operational after power-on reset	500		500		ms
T_{BUF}	Bus free time between stop and start condition	4.7		1.3		us

Timing Diagrams

Figure 9. Erase (User Erase or Erase All) Timing Diagram

Figure 10. Programming Timing Diagram

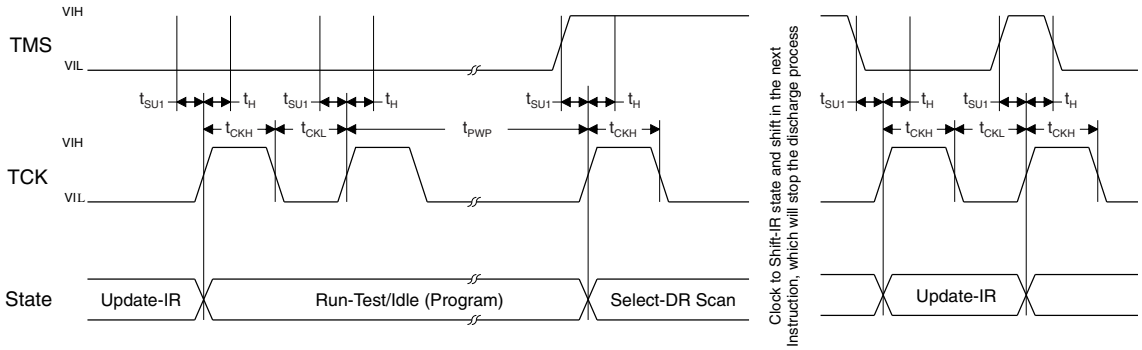


Figure 11. Verify Timing Diagram

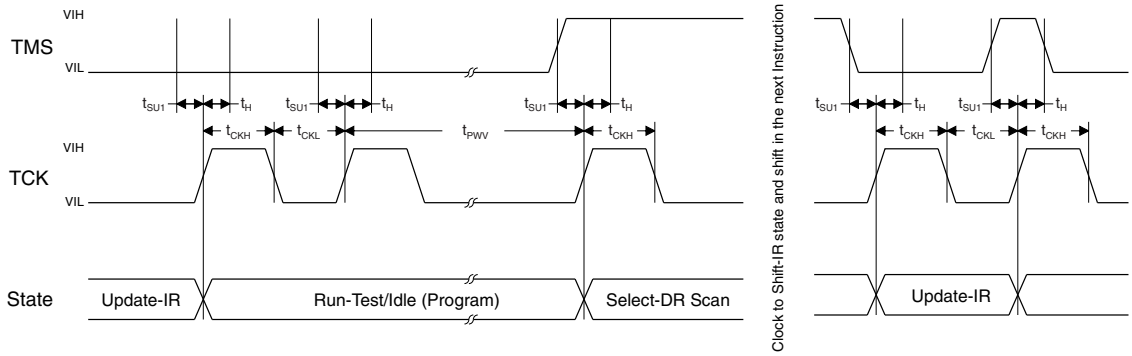
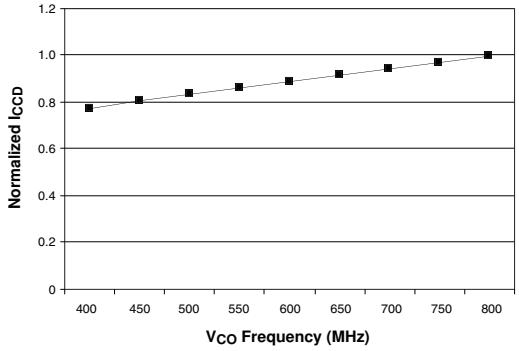


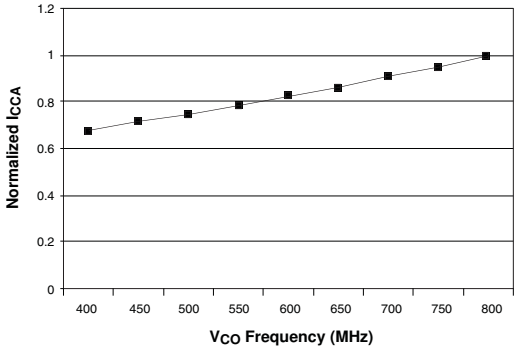
Figure 12. Discharge Timing Diagram

Typical Performance Characteristics

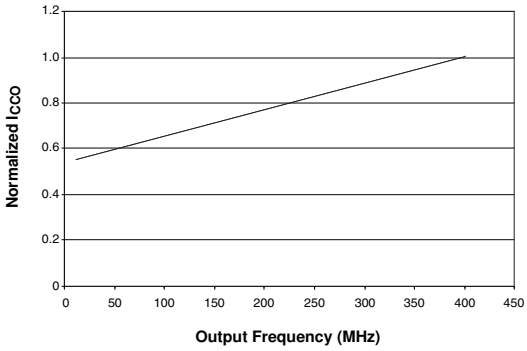
Normalized I_{CCD} vs. V_{CO} Frequency (I_{CCD} Value Normalized to V_{CO} at 800 MHz)



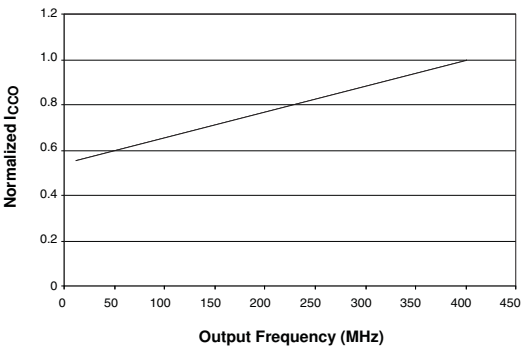
Normalized I_{CCA} vs. V_{CO} Frequency (I_{CCA} Value Normalized to V_{CO} at 800 MHz)



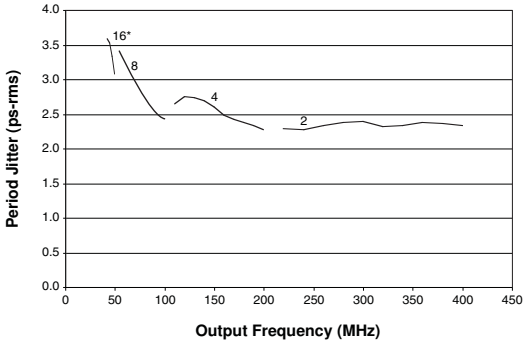
Normalized I_{CCO} vs. Output Frequency (I_{CCO} Value Normalized to Output Clock Frequency at 400 MHz, Output Logic Set to LVDS33)



Normalized I_{CCO} vs. Output Frequency (I_{CCO} Value Normalized to Output Clock Frequency at 400 MHz, Output Logic Set to LVPECL)

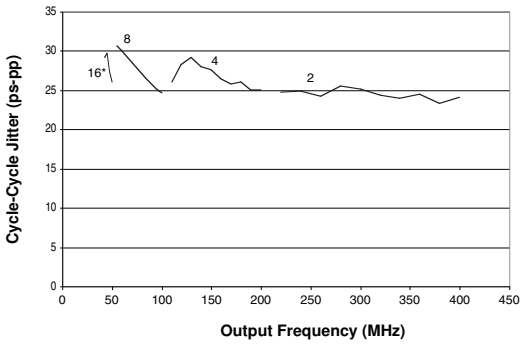


Period Jitter vs. Output Frequency



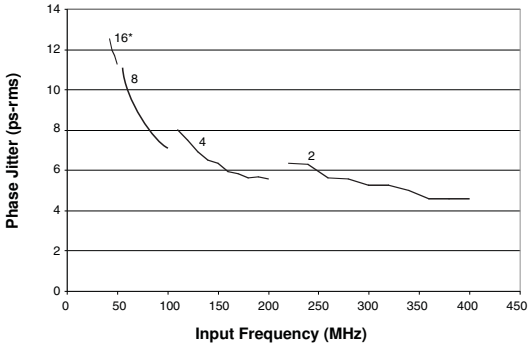
*Feedback V-Divider value.

Cyle-Cycle Jitter vs. Output Frequency



*Feedback V-Divider value.

Phase Jitter vs. Input Frequency



*Feedback V-Divider value.

Detailed Description

CleanClock PLL

The ispClock5400D provides an integral phase-locked-loop (PLL) which may be used to generate output clock signals at lower, higher, or the same frequency as a user-supplied input reference signal. The core functions of the CleanClock PLL are an edge-sensitive phase detector, a programmable loop filter, and a high-speed voltage-controlled oscillator (VCO). Any of the frequencies from the 4-output V-divider can be used as feedback to support the synthesis of different output frequencies.

Phase/Frequency Detector

The ispClock5400D provides an edge-sensitive phase/frequency detector (PFD), which means that the device will function properly over a wide range of input clock reference duty cycles. It is only necessary that the input reference clock meet specified minimum HIGH and LOW times ($t_{CLOCKHI,}$ $t_{CLOCKLO}$) for it to be properly recognized by the PFD. The PFD's output is of a classical charge-pump type, outputting charge packets which are then integrated by the PLL's loop filter. The output of the loop filter controls the VCO.

A lock-detection feature is also associated with the PFD. When the ispClock5400D is in a LOCKED state, the LOCK output signal is asserted (programmable high or low). The number of cycles required before asserting the LOCK signal in frequency-lock mode can be set from 16 through 256. The LOCK output from the PFD can be routed to one of the USER Programmable pins.

When the lock condition is lost the LOCK signal will be de-asserted immediately.

Loop Filter: The loop filter parameters are automatically selected by the PAC-Designer software depending on the feedback V-divider setting.

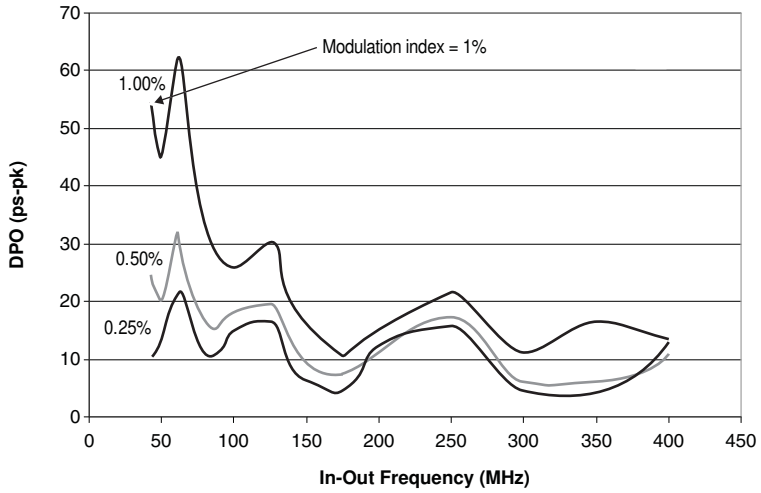
Spread Spectrum Support: The reference clock inputs of the ispClock5400D device are spread spectrum clock compatible. The tolerance limits are:

- Center spread ±0.125% to ±0.25%
- Down spread -0.25% to -0.5%
- 30-33kHz modulation frequency

Table 2. PLL Bandwidth

V-Divider	Bandwidth (MHz)
2	9.8
4	7.0
8	4.5
16	2.4

Figure 13. Dynamic Phase Offset (DPO)



VCO

The operating frequency of the on-chip VCO of the ispClock5400D ranges from 400MHz to 800MHz. The VCO is implemented using differential circuit design techniques which minimize the influence of power supply noise on measured output jitter. The VCO is also used to set the phase skew step size. Using the VCO as the basis for controlling output phase skew allows for highly precise and consistent phase skew generation, both from device-to-device, as well as channel-to-channel within the same device.

Output V-dividers

The ispClock5400D incorporates a set of four dividers which provide the ability to synthesize output frequencies differing from that of the reference clock input. The division values of these V-dividers are set to 2, 4, 8 and 16. In Coarse Skew Mode, the division values are set to 4, 8, 16 and 32.

When the PLL is selected (PLL_BYPASS=LOW) and locked, the output frequency of each V-divider (f_k) may be calculated as:

$$f_k = f_{ref} \frac{V_{fbk}}{V_k} \quad (1)$$

where

f_K is the frequency of V-divider k
f_{REF} is the input reference frequency
V_{FBK} is the division ratio of the V-divider used to close the PLL feedback path
V_K is the output divider K

Note that because the feedback may be taken from any V-divider, V_k and V_{fbk} may refer to the same divider.

PLL_BYPASS Mode

The PLL_BYPASS mode is provided so that input reference signals can be coupled through to the outputs without using the PLL functions. When PLL_BYPASS mode is enabled (PLL_BYPASS=HIGH), the reference clock is routed directly to the inputs of the V-dividers. The output frequency for a given V-divider (f_K) will be determined by

$$f_k = \frac{f_{REF}}{V_K} \quad (2)$$

When PLL_BYPASS mode is enabled, features such as lock detect and phase skew generation are unavailable. The PLL can be bypassed through I^2C or through the USER pins.

Internal/External Feedback Support

The PLL feedback path can be sourced internally or externally through an output bank. When the internal feedback path is selected, one can use all output pins for clock distribution. The programmable phase skew feature for the feedback path is available in the internal feedback mode. However, both phase and time skew features are available for the feedback path in the external feedback mode.

Reference and External Feedback Inputs

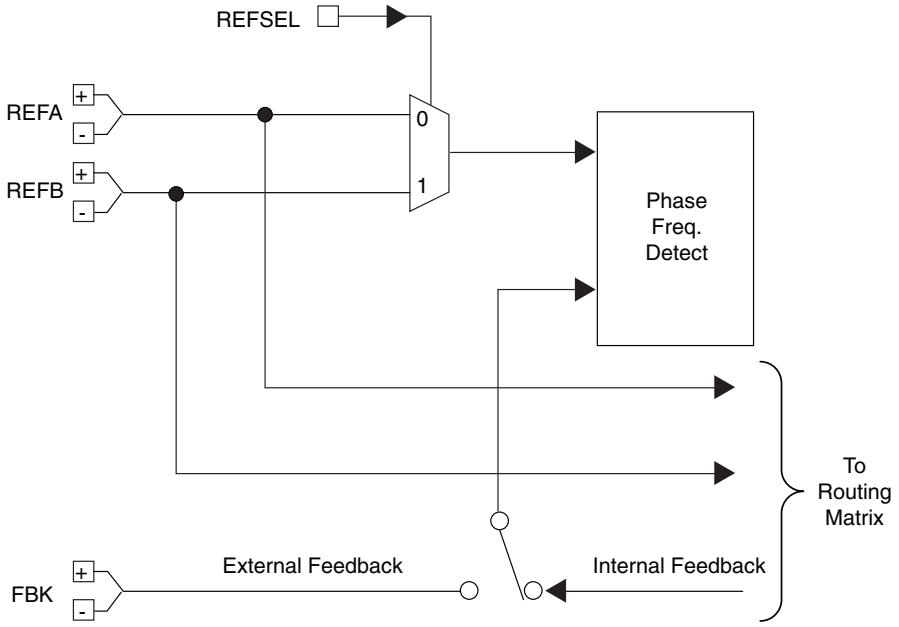
The ispClock5400D provides configurable, internally-terminated inputs for both clock reference and feedback signals.

The reference clock inputs pins (REFA, REFB) can be interfaced with two differential clocks. The active clock selection control through REFSEL signal. The REFSEL signal can be driven either by one of the USER pins or through the I^2C interface.

Supported input logic reference standards:

- LVDS
- LVPECL
- SSTL2
- SSTL18
- SSTL15
- HSTL
- eHSTL
- HCSL
- LVCMOS

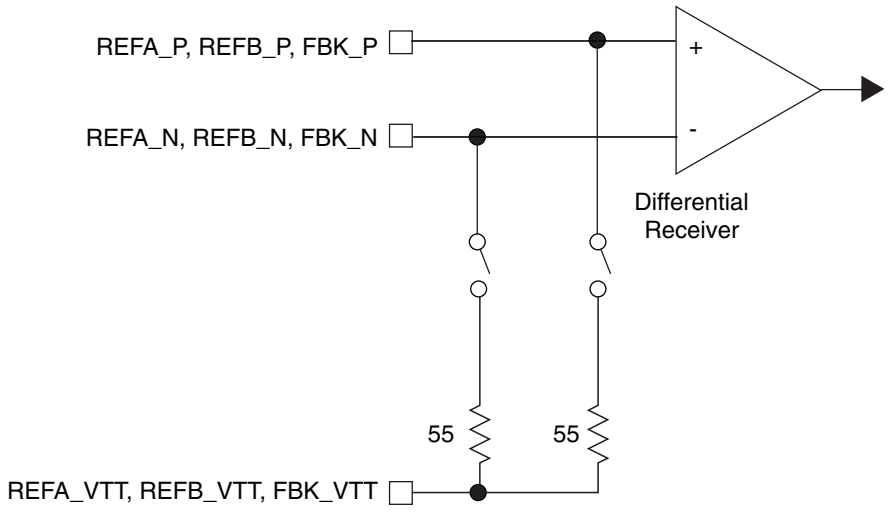
Figure 14. Reference and Feedback Input



Input Receiver Termination Configuration

Each input features internal 55 Ohm termination resistors as shown in Figure 15. The REFA, REFB and FBK inputs terminate to REFA_VTT, REFB_VTT, and FBK_VTT respectively. If external termination resistors are used, these internal termination resistors can be disconnected through PAC-Designer software.

Figure 15. Input Receiver Termination Configuration

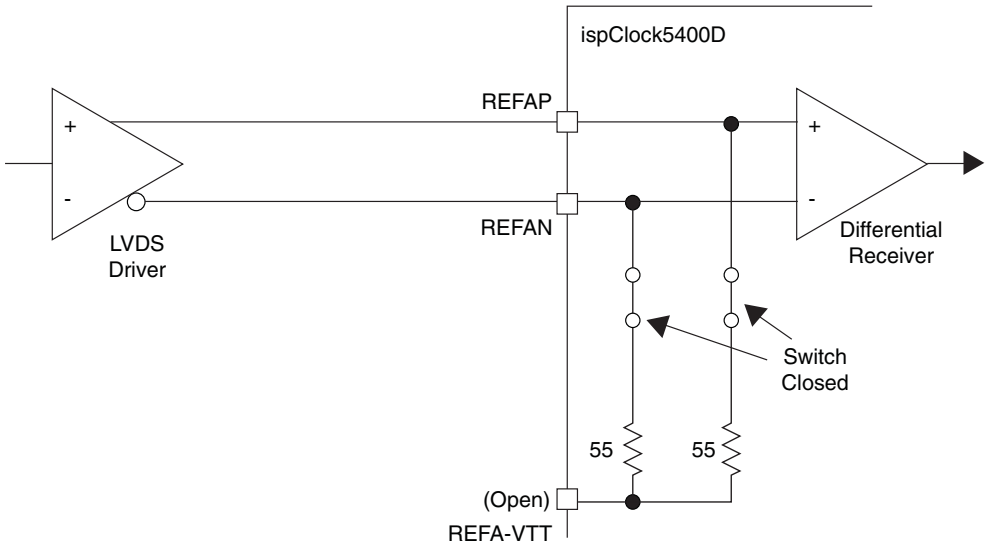


The following usage guidelines are suggested for interfacing to supported logic families.

LVPECL/LVDS

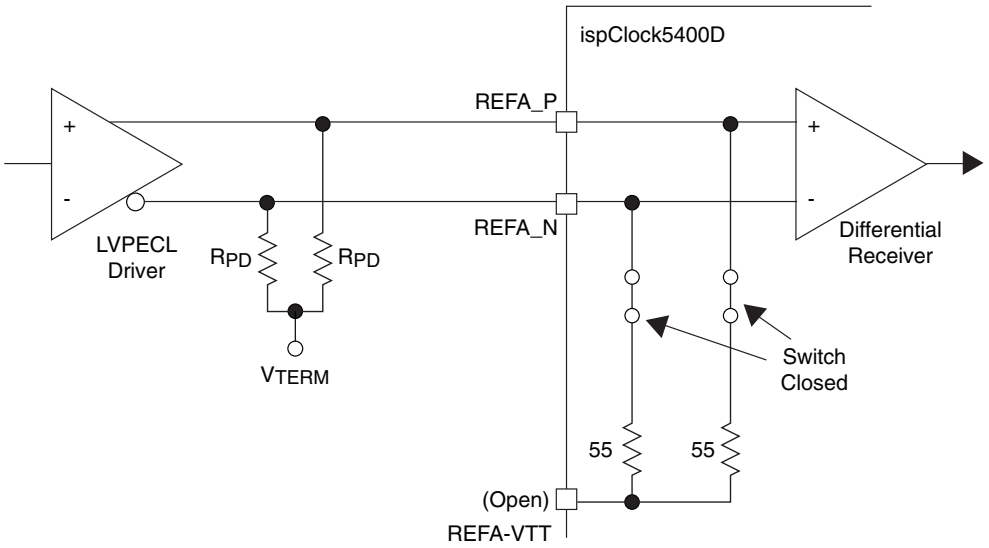
Both termination resistors in the receiver should be engaged. The VTT pin should be left floating. This creates a floating 110Ω differential termination resistance across the input terminals. The LVDS termination configuration is shown in Figure 16.

Figure 16. LVDS Input Receiver Configuration



Note that while a floating 110Ω resistor forms a complete termination for an LVDS signal line, additional circuitry may be required to satisfactorily terminate a differential LVPECL signal. This is because a true bipolar LVPECL output driver typically requires an external DC 'pull-down' path to a V_{TERM} termination voltage (typically VCC-2V) to properly bias its open emitter output stage. The pull-down should be implemented with external resistors placed close to the LVPECL driver (Figure 17)

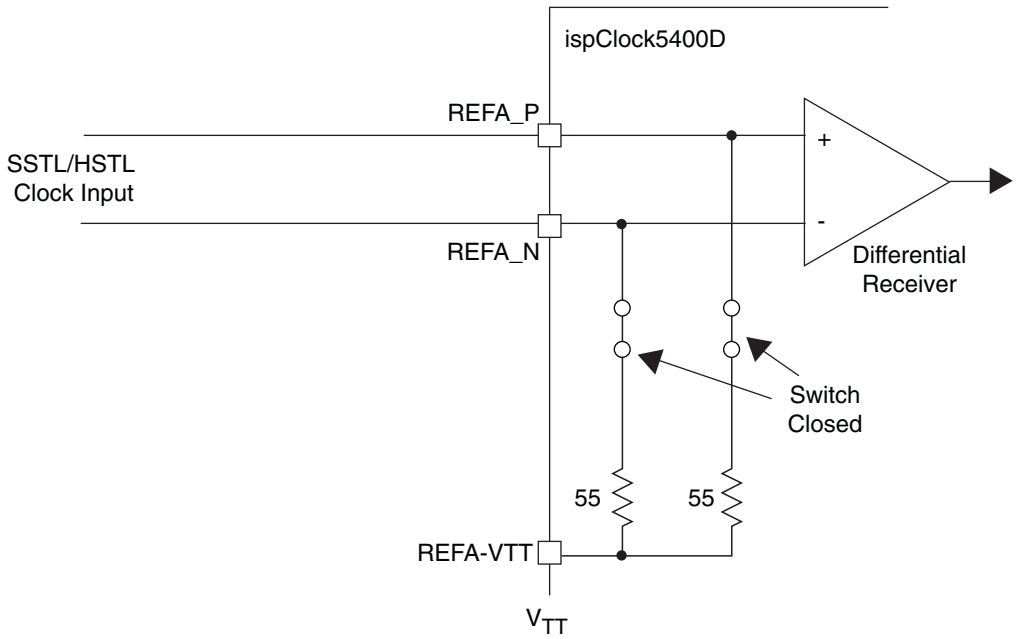
Figure 17. LVPECL Input Receiver Configuration



SSTL/HSTL

To interface the ispClock5400D with the SSTL or HSTL signals, close the switch connecting the REFP and REFN signals to termination resistors. Connect the VTT pin to a voltage half of the supply voltage of the clock input.

Figure 18. SSTL/HSTL Input Receiver Configuration

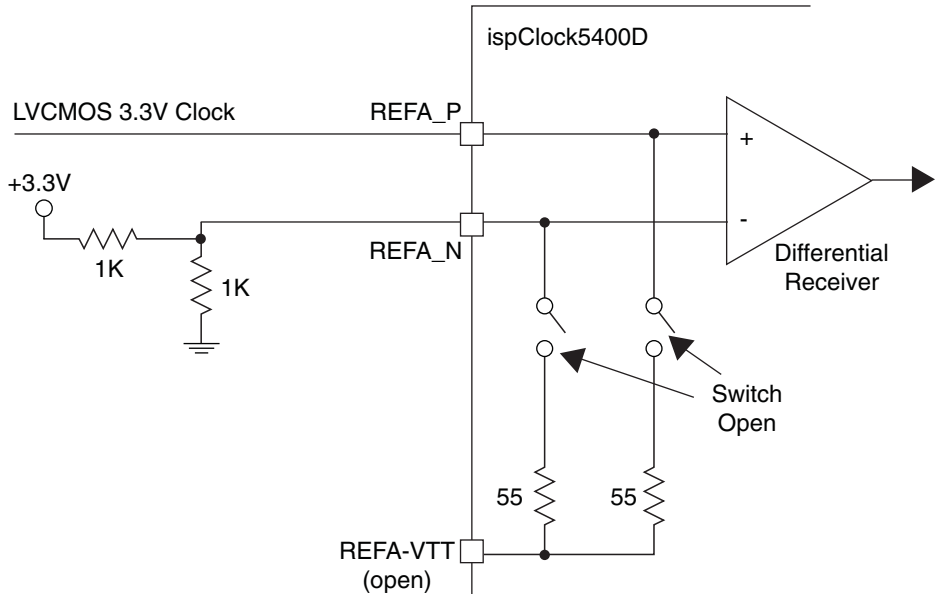


LVCMOS

The ispClock5400D input section can be connected to single ended signals such as the LVCMOS3.3V by connecting it directly to REFAP pin while the threshold is provided by the REFAN terminal at 1.65V (= 3.3V ÷ 2). The threshold reference voltage can be derived by a potential divider using 2, 1K ohm resistors.

Note: To minimize the noise injection into the receiver, the 3.3V at the input of the potential divider should be sufficiently filtered. The GND limb of the potential divider should be connected to the GND pin of the source.

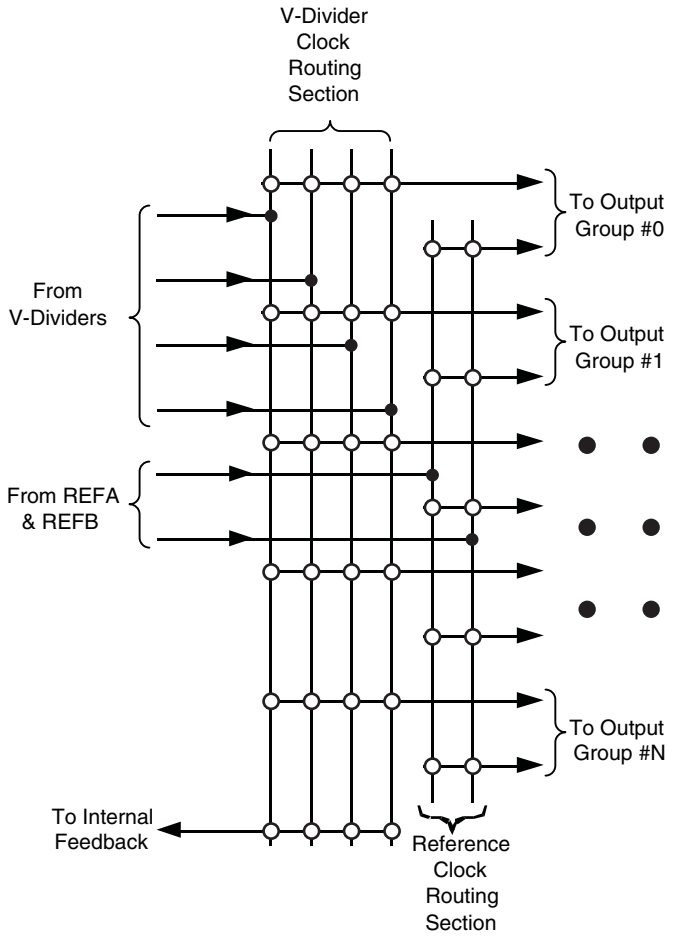
Figure 19. LVCMOS Input Receiver Configuration



Output Routing Matrix

There are two sections in the Output Routing Matrix: the V-divider clock routing section and the REF clock routing section. The V-divider routing section enables connecting any output group and the internal feedback path to any of the output V-dividers. The Ref clock routing section can route either of the Ref clocks to any output group.

Figure 20. ispClock5400D Output Routing Matrix



FlexiClock Output Section

The FlexiClock output block distributes clock received from the Output Routing Matrix. The signalling interface of each of the differential clock outputs can be individually programmed. The output voltage swing is controlled by the associated output VCC and GND pins. The VCCO, the GNDO and the associated differential clock output pair is called an output bank.There are six output banks in the FlexiClock output section in the ispClock5406D device. The FlexiClock output section the ispClock5610D supports 10 output banks.

Output Groups

The ispClock5400D provides multiple banks, with each bank supporting a high-speed clock output and the associated VCCO and GND pins. Two adjacent banks form an Output Group (Bank 0 and Bank 1 belong to Group #0, Bank 2 and Bank 3 belong to Group #2, and so on). There are ten banks (five Output Groups) in the ispClock5410D and three output groups in the ispClock5406D device. The outputs may be independently enabled or disabled, either from E^2CMOS configuration or by USER pins or through I^2C. Additionally, each bank output clock can be independently programmed to provide a fixed amount of signal delay or skew, allowing the user to compensate for the effects of unequal PCB trace lengths or loading effects. Figure 21 shows a block diagram of an ispClock5400D Output Group and its associated skew control. The two outputs in an Output Group share the connection to the Output Routing Matrix.

Because of the high edge rates which can be generated by the ispClock5400D clock output drivers, the VCCO power supply pin for each output bank should be individually bypassed. Low ESR capacitors with values ranging from 0.01 to 0.1 µF may be used for this purpose. Each bypass capacitor should be placed as close to its respec-