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ispClock™5500 Family

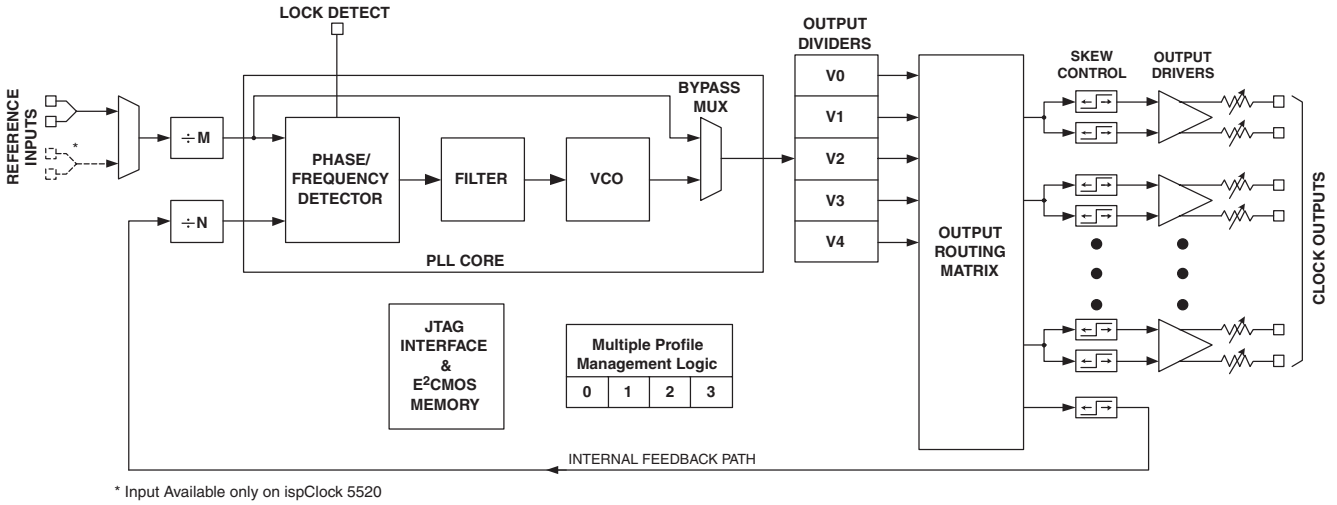
In-System Programmable Clock Generator with Universal Fan-Out Buffer

March 2005 **Data Sheet**

Features

- **10MHz to 320MHz Input/Output Operation**
- **Low Output to Output Skew (<50ps)**
- **Low Jitter Peak-to-Peak(<70ps)**
- **Up to 20 Programmable Fan-out Buffers**
  - Programmable output standards and individual enable controls
    - LVTTL, LVCMOS, HSTL, SSTL, LVDS, LVPECL
  - Programmable output impedance
    - 40 to 70Ω in 5Ω increments
  - Programmable slew rate
  - Up to 10 banks with individual V_{CCO} and GND
    - 1.5V, 1.8V, 2.5V, 3.3V
- **Fully Integrated High-Performance PLL**
  - Programmable lock detect
  - Multiply and divide ratio controlled by
    - Input divider (5 bits)
    - Internal feedback divider (5 bits)
    - Five output dividers (5 bits)
  - Programmable On-chip Loop Filter
- **Precision Programmable Phase Adjustment (Skew) Per Output**
  - 16 settings; minimum step size 195ps
    - Locked to VCO frequency
  - Up to +/- 12ns skew range
  - Coarse and fine adjustment modes
- **Up to Five Clock Frequency Domains**
- **Flexible Clock Reference Inputs**
  - Programmable input standards
    - LVTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL
  - Clock A/B selection multiplexer
  - Programmable precision termination
- **Four User-programmable Profiles Stored in E²CMOS® Memory**
  - Supports both test and multiple operating configurations
- **Full JTAG Boundary Scan Test In-System Programming Support**
- **Exceptional Power Supply Noise Immunity**
- **Commercial (0 to 70°C) and Industrial (-40 to 85°C) Temperature Ranges**
- **100-pin and 48-pin TQFP Packages**
- **Applications**
  - Circuit board common clock generation and distribution
  - PLL-based frequency generation
  - High fan-out clock buffer

Product Family Block Diagram



* Input Available only on ispClock 5520

General Description and Overview

The ispClock5510 and ispClock5520 are in-system-programmable high-fanout PLL-based clock drivers designed for use in high performance communications and computing applications. The ispClock5510 provides up to 10 single-ended or five differential clock outputs, while the ispClock5520 provides up to 20 single-ended or 10 differential clock outputs. Each pair of outputs may be independently configured to support separate I/O standards (LVDS, LVPECL, LVTTL, LVCMOS, SSTL, HSTL) and output frequency. In addition, each output provides independent programmable control of termination, slew-rate, and timing skew. All configuration information is stored on-chip in non-volatile E^2CMOS memory.

The ispClock5500's PLL and divider systems supports the synthesis of clock frequencies differing from that of the reference input through the provision of programmable input and feedback dividers. A set of five post-PLL V-dividers provides additional flexibility by supporting the generation of five separate output frequencies. Loop feedback may be taken from the output of any of the five V-dividers.

The core functions of all members of the ispClock5500 family are identical, the differences between devices being restricted to the number of inputs and outputs, as shown in the following table. Figures 1 and 2 show functional block diagrams of the ispClock5510 and ispClock5520.

Table 1. ispClock5500 Family Members

Device	Ref. Input Pairs	Clock Outputs
ispClock5510	1	10
ispClock5520	2	20

Figure 1. ispClock5510 Functional Block Diagram

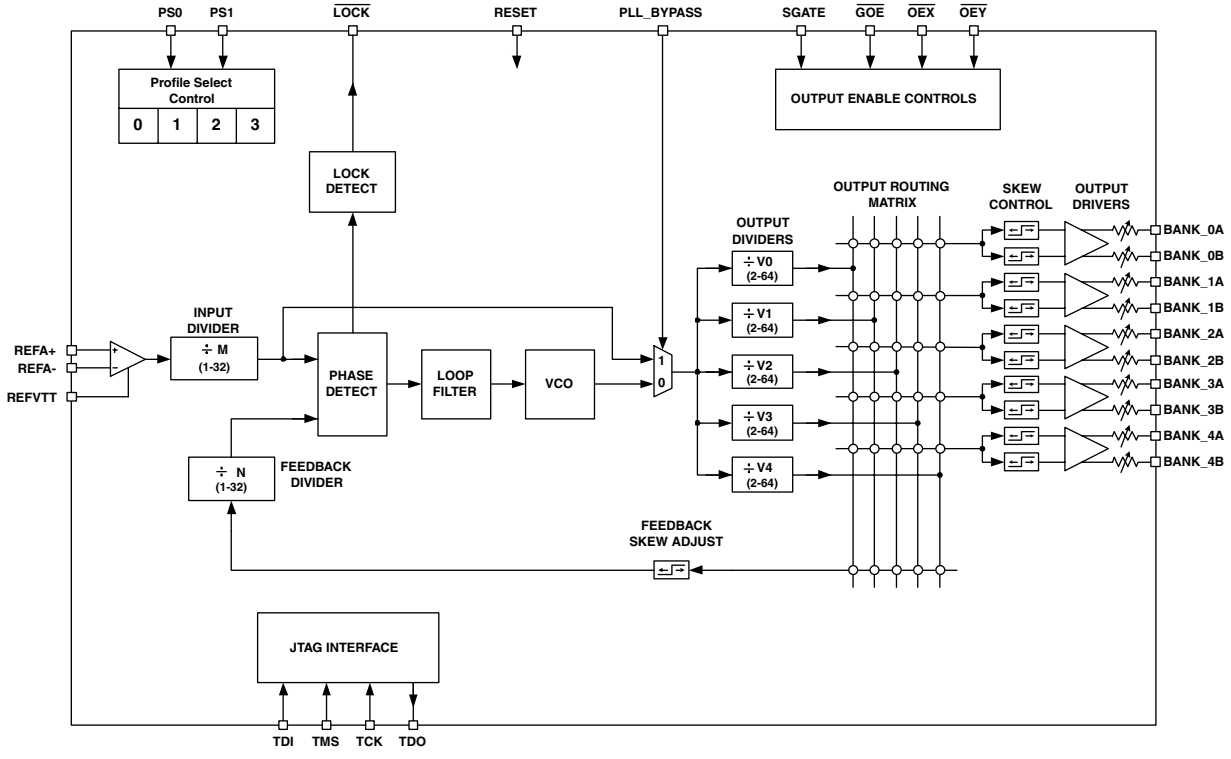
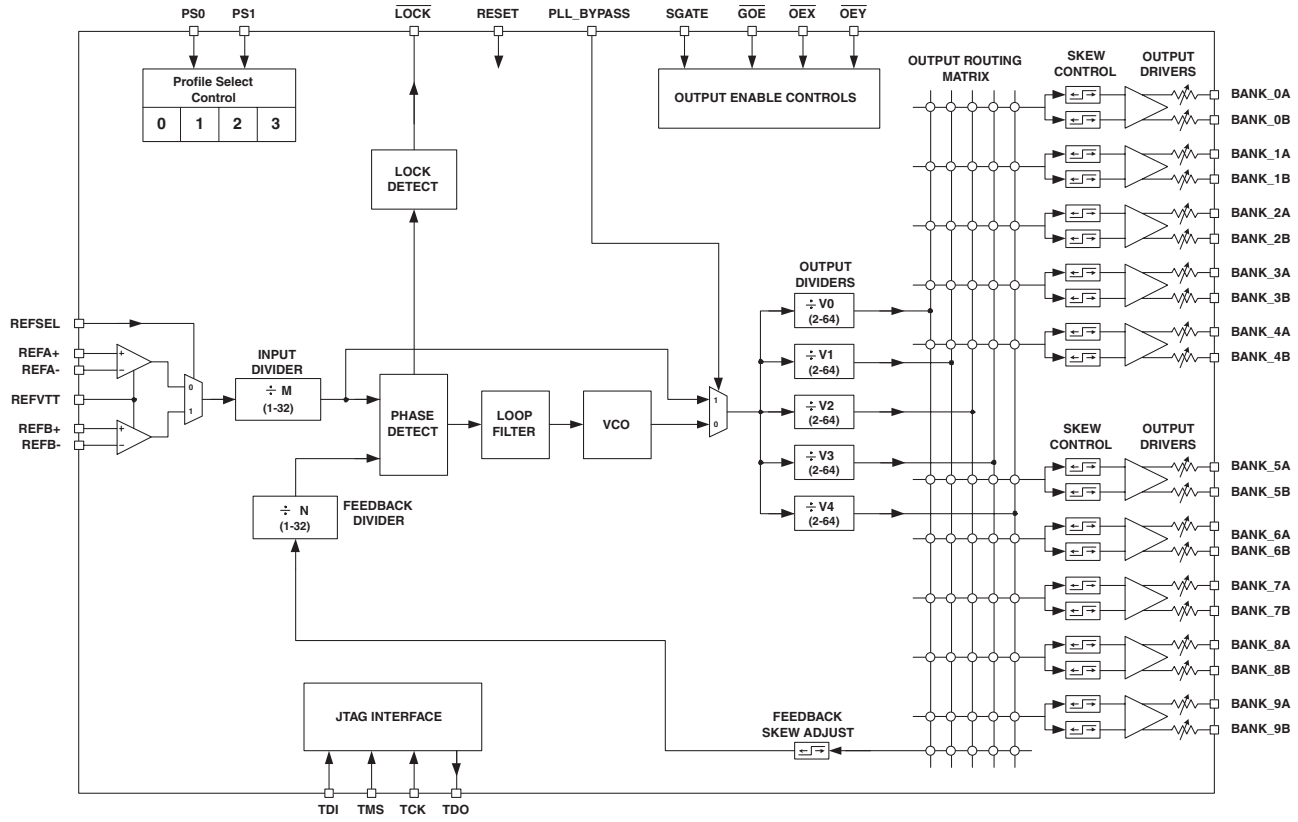


Figure 2. ispClock5520 Functional Block Diagram



Absolute Maximum Ratings

	ispClock5500V
Core Supply Voltage V_{CCD}	-0.5 to 5.5V
PLL Supply Voltage V_{CCA}	-0.5 to 5.5V
JTAG Supply Voltage V_{CCJ}	-0.5 to 5.5V
Output Driver Supply Voltage V_{CCO}	-0.5 to 4.5V
Input Voltage	-0.5 to 4.5V
Output Voltage[1]	-0.5 to 4.5V
Storage Temperature	-65 to 150°C
Junction Temperature with power supplied	-40 to 130°C

1. When applied to an output when in high-Z condition

Recommended Operating Conditions

Symbol	Parameter	Conditions	ispClock5500V		Units
			Min.	Max.	
V_{CCD}	Core Supply Voltage		3.0	3.6	V
V_{CCJ}	JTAG I/O Supply Voltage		1.62	3.6	V
V_{CCA}	Analog Supply Voltage		3.0	3.6	V
$V_{CCASLEW}$	V_{CCA} Turn-on Ramp Rate		—	0.033	V/µs
T_{JOP}	Operating Junction Temperature	Commercial	0	100	°C
		Industrial	-40	115	
T_A	Ambient Operating Temperature	Commercial	0	70[1]	°C
		Industrial	-40	85[1]	

1. Device power dissipation may also limit maximum ambient operating temperature.

Recommended Operating Conditions – V_{CCO} vs. Logic Standard

Logic Standard		V_{CCO} (V)			V_{REF} (V)			V_{TT} (V)		
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL		3.0	3.3	3.6	—	—	—	—	—	—
LVCMOS 1.8V		1.71	1.8	1.89	—	—	—	—	—	—
LVCMOS 2.5V		2.375	2.5	2.625	—	—	—	—	—	—
LVCMOS 3.3V		3.0	3.3	3.6	—	—	—	—	—	—
SSTL2 Class 1		2.375	2.5	2.625	1.15	1.25	1.35	V_{REF} - 0.04	—	V_{REF} + 0.04
SSTL3 Class 1		3.0	3.3	3.6	1.30	1.50	1.70	V_{REF} - 0.05	V_{REF}	V_{REF} + 0.05
HSTL Class 1		1.425	1.5	1.575	0.68	0.75	0.90	—	0.5 x V_{CCO}	—
LVPECL (Differential)		3.0V	3.3V	3.6V	—	—	—	—	—	—
LVDS	V_{CCO} = 2.5V	2.375	2.5V	2.625	—	—	—	—	—	—
	V_{CCO} = 3.3V	3.0	3.3	3.6	—	—	—	—	—	—

Note: '—' denotes V_{REF} or V_{TT} not applicable to this logic standard

E^2CMOS Memory Write/Erase Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Erase/Reprogram Cycles		1000	—	—	

Performance Characteristics – Power Supply

Symbol	Parameter	Conditions	Typ.	Max.	Units
I_{CCD}	Core Supply Current	ispClock5510, f_{VCO} = 640MHz	100	110	mA
		ispClock5520, f_{VCO} = 640MHz	130	150	mA
I_{CCA}	Analog Supply Current	f_{VCO} = 640MHz	5.5	7	mA
I_{CCO}	Output Driver Supply Current (per Bank)	V_{CCO} = 1.8V[1], LVCMOS V_{CCO} = 2.5V[1], LVCMOS V_{CCO} = 3.3V[1], LVCMOS V_{CCO} = 3.3V[2], LVDS	13 18 24 7.5	15 24 35 8	mA
I_{CCJ}	JTAG I/O Supply Current (static)	V_{CCJ} = 1.8V V_{CCJ} = 2.5V V_{CCJ} = 3.3V	200 300 300	300 400 400	µA

1. Supply current consumed by each bank, both outputs active, 18pF load, 320MHz output frequency.
2. Supply current consumed by each bank, 100Ω/5pF differential load, 320MHz output frequency.

DC Electrical Characteristics – Single-ended Logic

Logic Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min.	Max.	Min.	Max.				
LVTTL/LVCMOS 3.3V	-0.3	0.8	2	3.6	0.4	V_{CCO} - 0.4	4[1]	-4[1]
LVCMOS 1.8V	-0.3	0.68	1.07	3.6	0.4	V_{CCO} - 0.4	4[1]	-4[1]
LVCMOS 2.5V	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	4[1]	-4[1]
SSTL2 Class 1	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54[2]	V_{CCO} - 0.81[2]	7.6	-7.6
SSTL3 Class 1	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.9[2]	V_{CCO} - 1.3[2]	8	-8
HSTL Class 1	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4[3]	V_{CCO} - 0.4[3]	8	-8

1. Specified for 50Ω internal series output termination.
2. Specified for 40Ω internal series output termination.
3. Specified for ≈20Ω internal series output termination.

DC Electrical Characteristics – LVDS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{ICM}	Common Mode Input Voltage	V_{THD} ≤ 100mV	$V_{THD}/2$	—	2.0	V
		V_{THD} ≤ 150mV	$V_{THD}/2$		2.325	V
V_{THD}	Differential Input Threshold		±100	—	—	mV
V_{IN}	Input Voltage		0	—	2.4	V
V_{OH}	Output High Voltage	R_T = 100Ω	—	1.375	1.60	V
V_{OL}	Output Low Voltage	R_T = 100Ω	0.9	1.03	—	V
V_{OD}	Output Voltage Differential	R_T = 100Ω	250	400	480	mV
ΔV_{OD}	Change in V_{OD} between H and L		—	—	50	mV
V_{OS}	Output Voltage Offset	Common Mode Output Voltage	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50	mV
I_{SA}	Output Short Circuit Current	V_{OD} = 0V, Outputs Shorted to GND	—	—	24	mA
I_{SAB}	Output Short Circuit Current	V_{OD} = 0V, Outputs Shorted to Each Other	—	—	12	mA

DC Electrical Characteristics – Differential LVPECL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input Voltage High	V_{CCD} = 3.0 to 3.6V	V_{CCD} - 1.17	—	V_{CCD} - 0.88	V
		V_{CCD} = 3.3V	2.14	—	2.42	
V_{IL}	Input Voltage Low	V_{CCD} = 3.0 to 3.6V	V_{CCD} - 1.81	—	V_{CCD} - 1.48	V
		V_{CCD} = 3.3V	1.49	—	1.83	
V_{OH}	Output High Voltage[1]	V_{CCO} = 3.0 to 3.6V	V_{CCO} - 1.07	—	V_{CCO} - 0.88	V
		V_{CCO} = 3.3V	2.23	—	2.42	
V_{OL}	Output Low Voltage[1]	V_{CCO} = 3.0 to 3.6V	V_{CCO} - 1.81	—	V_{CCO} - 1.62	V
		V_{CCO} = 3.3V	1.49	—	1.68	

1. 100Ω differential termination.

DC Electrical Characteristics – Input/Output Loading

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{LK}	Input Leakage	Note 1	—	—	±10	µA
I_{PU}	Input Pull-up Current	Note 2	—	80	120	µA
I_{PD}	Input Pull-down Current	Note 3	—	120	150	µA
I_{OLK}	Tristate Leakage Output	Note 4	—	—	±10	µA
C_{IN}	Input Capacitance	Notes 2, 3, 5	—	8	10	pF
		Note 6	—	13.5	15	pF

1. Applies to clock reference inputs when termination ‘open’.
2. Applies to TDI, TMS inputs.
3. Applies to REFSEL, PS0, PS1, $\overline{GOE}$, SGATE, PLL_BYPASS, $\overline{OEX}$ and $\overline{OEY}$.
4. Applies to all logic types when in tristated mode.
5. Applies to $\overline{OEX}$, $\overline{OEY}$, TCK, RESET inputs.
6. Applies to REFA+, REFA-, REFB+, REFB-.

Switching Characteristics – Timing Adders for I/O Modes

Adder Type	Base Parameter(s)	Description	Min.	Typ.	Max.	Units
t_{IOI} Input Adders[2]						
LVTTL_in		Using LVTTL Standard	—	0	—	ns
LVCMOS18_in		Using LVCMOS 1.8V Standard	—	0	—	ns
LVCMOS25_in		Using LVCMOS 2.5V Standard	—	0	—	ns
LVCMOS33_in		Using LVCMOS 3.3V Standard	—	0	—	ns
SSTL2_in		Using SSTL2 Standard	—	0.4	—	ns
SSTL3_in		Using SSTL3 Standard	—	0.4	—	ns
HSTL_in		Using HSTL Standard	—	0.4	—	ns
LVDS_in		Using LVDS Standard	—	1.8	—	ns
LVPECL_in		Using LVPECL Standard	—	1.8	—	ns
t_{IOO} Output Adders[1, 3]						
LVTTL_out		Output Configured as LVTTL Buffer	—	0.1	—	ns
LVCMOS18_out		Output Configured as LVCMOS 1.8V Buffer	—	0.1	—	ns
LVCMOS25_out		Output Configured as LVCMOS 2.5V Buffer	—	0.1	—	ns
LVCMOS33_out		Output Configured as LVCMOS 3.3V Buffer	—	0.1	—	ns
SSTL2_out		Output Configured as SSTL2 Buffer	—	0.1	—	ns
SSTL3_out		Output Configured as SSTL3 Buffer	—	0.1	—	ns
HSTL_out		Output Configured as HSTL Buffer	—	0.1	—	ns
LVDS_out		Output Configured as LVDS Buffer	—	0.1	—	ns
LVPECL_out		Output Configured as LVPECL Buffer	—	0	—	ns
t_{IOS} Output Slew Rate Adders[1]						
Slew_1		Output Slew_1 (Fastest)	—	0	—	ps
Slew_2		Output Slew_2	—	330	—	ps
Slew_3		Output Slew_3	—	660	—	ps
Slew_4		Output Slew_4 (Slowest)	—	1320	—	ps

1. Measured under standard output load conditions – see Figures 3-5.
2. All input adders referenced to LVTTL.
3. All output adders referenced to LVPECL.

Output Rise and Fall Times – Typical Values[1, 2]

Output Type	Slew 1 (Fastest)		Slew 2		Slew 3		Slew 4 (Slowest)		Units
	t_R	t_F	t_R	t_F	t_R	t_F	t_R	t_F	
LVTTL	0.65	0.45	0.85	0.60	1.20	0.90	1.75	1.30	ns
LVCMOS 1.8V	0.90	0.40	1.05	0.50	1.40	0.80	2.00	1.20	ns
LVCMOS 2.5V	0.70	0.40	0.90	0.55	1.20	0.85	1.80	1.20	ns
LVCMOS 3.3V	0.65	0.45	0.85	0.60	1.20	0.90	1.75	1.30	ns
SSTL2	0.65	0.40	0.90	0.60	1.35	0.85	2.30	1.40	ns
SSTL3	0.65	0.40	0.90	0.60	1.35	0.85	2.30	1.40	ns
HSTL	0.85	0.30	1.00	0.50	1.50	0.70	2.55	1.10	ns
LVDS[3]	0.25	0.20	—	—	—	—	—	—	ns
LVPECL[3]	0.20	0.20	—	—	—	—	—	—	ns

1. See Figures 3-5 for test conditions.
2. Measured between 20% and 80% points.
3. Only the 'fastest' slew rate is available in LVDS and LVPECL modes.

Output Test Loads

Figures 3-5 show the equivalent termination loads used to measure rise/fall times, output timing adders and other selected parameters as noted in the various tables of this data sheet.

Figure 3. CMOS Termination Load

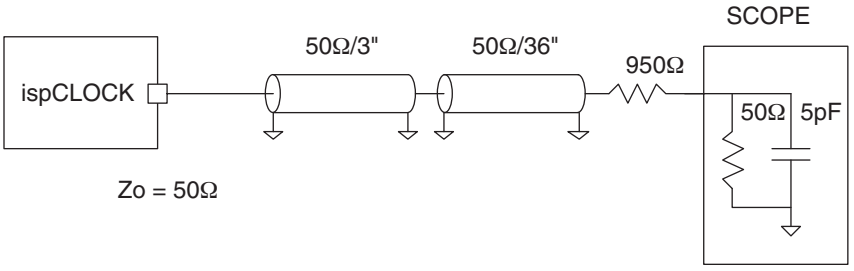


Figure 4. HSTL/SSTL Termination Load

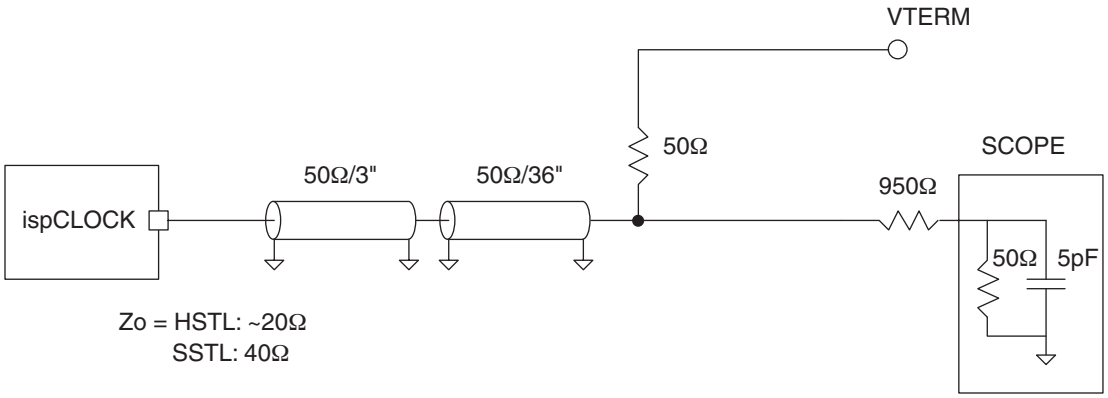
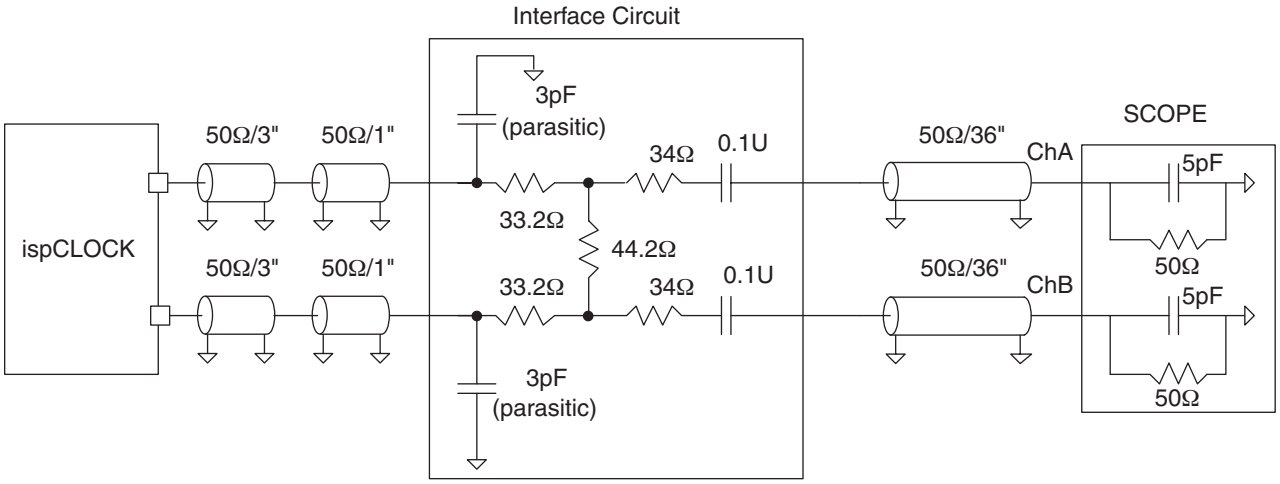


Figure 5. LVDS/LVPECL Termination Load



Programmable Input and Output Termination Characteristics

Symbol	Parameter	Conditions	V_{CCO} Voltage	Min.	Typ.	Max.	Units
R_{IN}	Input Resistance	Rin=40Ω setting		36	—	44	Ω
		Rin=45Ω setting		40.5	—	49.5	
		Rin=50Ω setting		45	—	55	
		Rin=55Ω setting		49.5	—	60.5	
		Rin=60Ω setting		54	—	66	
		Rin=65Ω setting		59	—	71.5	
		Rin=70Ω setting		61	—	77	
R_{OUT}	Output Resistance[1]	Rout≈20Ω setting	VCCO=3.3V	—	14	—	Ω
			VCCO=2.5V	—	14	—	
			VCCO=1.8V	—	14	—	
			VCCO=1.5V	—	14	—	
		Rout≈40Ω setting	VCCO=3.3V	-9%	38	9%	
			VCCO=2.5V	-11%	40	11%	
			VCCO=1.8V	-13%	40	13%	
		Rout≈45Ω setting	VCCO=3.3V	-10%	45	10%	
			VCCO=2.5V	-12%	45	12%	
			VCCO=1.8V	-14%	44	14%	
		Rout≈50Ω setting	VCCO=3.3V	-8%	50	8%	
			VCCO=2.5V	-9%	49	9%	
			VCCO=1.8V	-13%	49	13%	
		Rout≈55Ω setting	VCCO=3.3V	-9%	55	9%	
			VCCO=2.5V	-11%	55	11%	
			VCCO=1.8V	-13%	55	13%	
		Rout≈60Ω setting	VCCO=3.3V	-8%	59	8%	
			VCCO=2.5V	-9%	59	9%	
			VCCO=1.8V	-14%	59	14%	
		Rout≈65Ω setting	VCCO=3.3V	-8%	65	8%	
			VCCO=2.5V	-9%	64	9%	
			VCCO=1.8V	-13%	64	13%	
		Rout≈70Ω setting	VCCO=3.3V	-9%	72	9%	
			VCCO=2.5V	-10%	70	10%	
			VCCO=1.8V	-12%	69	12%	

1. Guaranteed by characterization.

Performance Characteristics – PLL

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{REF}	Reference input frequency range		10	—	320	MHz
$t_{CLOCKHI}$, $t_{CLOCKLO}$	Reference input clock HIGH and LOW times		1.25	—	—	ns
t_{RINP}, t_{FINP}	Input rise and fall times	Measured between 20% and 80% levels	—	—	5	ns
M_{DIV}	M-divider range		1	—	32	
N_{DIV}	N-Divider range		1	—	32	
f_{PFD}	Phase detector input frequency range[2]		10	—	320	MHz
f_{VCO}	VCO operating frequency		320	—	640	MHz
V_{DIV}	Output Divider range	Even integer values only	2	—	64	
f_{OUT}	Output frequency range[1]	Fine Skew Mode, f_{VCO} = 640MHz	10	—	320	MHz
		Coarse Skew Mode, f_{VCO} = 640MHz	5	—	160	MHz
t_{JIT} (cc)	Output adjacent-cycle jitter	1000 cycle sample[3]	—	55	70	ps (p-p)
t_{JIT} (per)	Output period jitter	10000 cycle sample[3]	—	11	14	ps (RMS)
$t_{JIT(\phi)}$	Reference clock to output jitter	6000 cycle sample[3]	—	170	—	ps (RMS)
$t\phi$	Static phase offset	PFD input frequency ≥ 100MHz[5]	—	-500	—	ps
DC_{ERR}	Output duty cycle error (see Table 3 for nominal values)[4]	Output type LVDS, V_{CCO} = 3.3V[6]	—	—	260	ps
		Output type LVCMOS 3.3V[6] f_{OUT} > 100 MHz	—	—	300	ps
t_{CO_BYPASS}	Reference clock to output delay, PLL bypass mode	Inputs and Outputs configured to LVCMOS 3.3V standard	—	5	—	ns
t_L	PLL Lock time	From Power-up event	—	150	500	µs
		From Reset event	—	15	50	µs
PSR	Power supply rejection, period jitter vs. power supply noise	f_{IN} = f_{OUT} = 100MHz VCCA = VCCD = VCCO modulated with 100kHz sinusoidal stimulus	—	0.05	—	$\frac{ps(RMS)}{mV(p\text{-}p)}$

1. In PLL Bypass mode (PLL_BYPASS = HIGH), output will support frequencies down to 0Hz (divider chain is a fully static design).
2. Dividers should be set so that they provide the phase detector with signals of 10MHz or greater for loop stability.
3. f_{IN} = f_{OUT} = 100 MHz, M = N = 1, V = 6, output type LVPECL.
4. Variation in duty cycle expressed in ps. To obtain duty cycle percentage error ($\%_{ERR}$) for a given output frequency (f_{OUT}), $\%_{ERR}$ = 100 x f_{OUT} x DC_{ERR}.
5. Input and outputs LVPECL mode.
6. See Figures 3-5 for output loads.

Timing Specifications

Skew Matching

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{SKEW}	Output-output Skew	Between any two identically configured and loaded outputs regardless of bank.	—	—	50	ps

Programmable Skew Control

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{SKRANGE}$	Skew Control Range[1]	Fine Skew Mode, f_{VCO} = 320 MHz	—	5.86	—	ns
		Fine Skew Mode, f_{VCO} = 640 MHz	—	2.93	—	
		Coarse Skew Mode, f_{VCO} = 320 MHz	—	11.72	—	
		Coarse Skew Mode, f_{VCO} = 640 MHz	—	5.86	—	
SK_{STEPS}	Skew Steps per range		—	16	—	
t_{SKSTEP}	Skew Step Size[2]	Fine Skew Mode, f_{VCO} = 320 MHz	—	390	—	ps
		Fine Skew Mode, f_{VCO} = 640 MHz	—	195	—	
		Coarse Skew Mode, f_{VCO} = 320 MHz	—	780	—	
		Coarse Skew Mode, f_{VCO} = 640 MHz	—	390	—	
t_{SKERR}	Skew Time Accuracy[3]	Fine skew mode	—	30	—	ps
		Coarse skew mode	—	50	—	

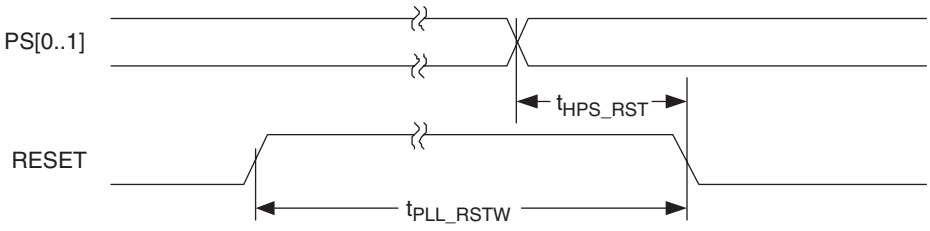
1. Skew control range is a function of VCO frequency (f_{VCO}). In fine skew mode $T_{SKRANGE} = 15/(8 \times f_{VCO})$. In coarse skew mode $T_{SKRANGE} = 15/(4 \times f_{VCO})$.
2. Skew step size is a function of VCO frequency (f_{VCO}). In fine skew mode $T_{SKSTEP} = 1/(8 \times f_{VCO})$. In coarse skew mode $T_{SKSTEP} = 1/(4 \times f_{VCO})$.
3. Only applicable to outputs with non-zero skew settings.

Control Functions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{DIS/OE}$	Delay Time, $\overline{OEX}$ or $\overline{OEY}$ to Output Disabled/ Enabled		—	10	20	ns
$t_{DIS/GOE}$	Delay Time, $\overline{GOE}$ to Output Disabled/Enabled		—	10	20	ns
$t_{SUSGATE}$	Setup Time, SGATE to Output Clock Start/ Stop		3	—	—	cycles[1]
t_{PLL_RSTW}	PLL Reset Pulse Width		15	—	—	µs
t_{HPS_RST}	Hold time for RESET past change in PS[0..1]		20	—	—	ns

1. Output clock cycles for the particular output being controlled.

Figure 6. RESET and Profile Select Timing



Timing Specifications (Cont.)

Boundary Scan Logic

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK (BSCAN Test) Clock Cycle	40	—	ns
t_{BTCH}	TCK (BSCAN Test) Pulse Width High	20	—	ns
t_{BTCL}	TCK (BSCAN Test) Pulse Width Low	20	—	ns
t_{BTSU}	TCK (BSCAN Test) Setup Time	8	—	ns
t_{BTH}	TCK (BSCAN Test) Hold Time	10	—	ns
t_{BRF}	TCK (BSCAN Test) Rise and Fall Rate	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	10	ns
t_{BTOZ}	TAP Controller Falling Edge of Clock to Data Output Disable	—	10	ns
t_{BTVO}	TAP Controller Falling Edge of Clock to Data Output Enable	—	10	ns
$t_{BVTCPSU}$	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCPH}	BSCAN Test Capture Register Hold Time	10	—	ns
t_{BTUCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	25	ns
t_{BTUOZ}	BSCAN Test Update Register, Falling Edge of Clock to Output Disable	—	25	ns
t_{BTUOV}	BSCAN Test Update Register, Falling Edge of Clock to Output Enable	—	25	ns

JTAG Interface and Programming Mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum TCK Clock Frequency		—	—	25	MHz
t_{CKH}	TCK Clock Pulse Width, High		20	—	—	ns
t_{CKL}	TCK Clock Pulse Width, Low		20	—	—	ns
t_{ISPEN}	Program Enable Delay Time		15	—	—	µs
t_{ISPDIS}	Program Disable Delay Time		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Program		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Erase		200	—	—	µs
t_{CEN}	Falling Edge of TCK to TDO Active		—	—	15	ns
t_{CDIS}	Falling Edge of TCK to TDO Disable		—	—	15	ns
t_{SU1}	Setup Time		8	—	—	ns
t_{H}	Hold Time		10	—	—	ns
t_{CO}	Falling Edge of TCK to Valid Output		—	—	15	ns
t_{PWV}	Verify Pulse Width		30	—	—	µs
t_{PWP}	Programming Pulse Width		20	—	—	ms
t_{BEW}	Bulk Erase Pulse Width		200	—	—	ms

Timing Diagrams

Figure 7. Erase (User Erase or Erase All) Timing Diagram

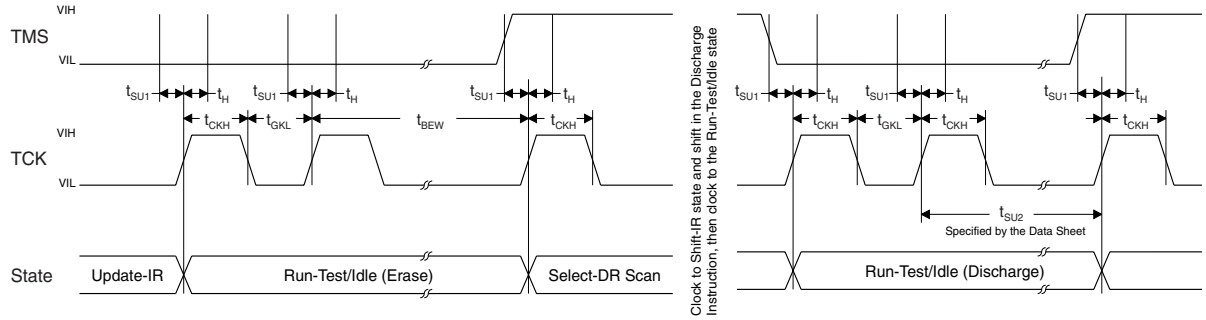


Figure 8. Programming Timing Diagram

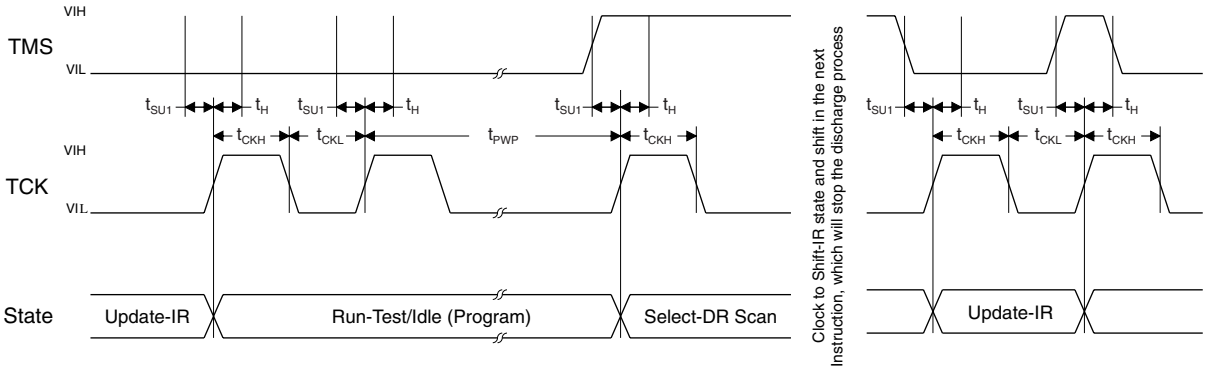


Figure 9. Verify Timing Diagram

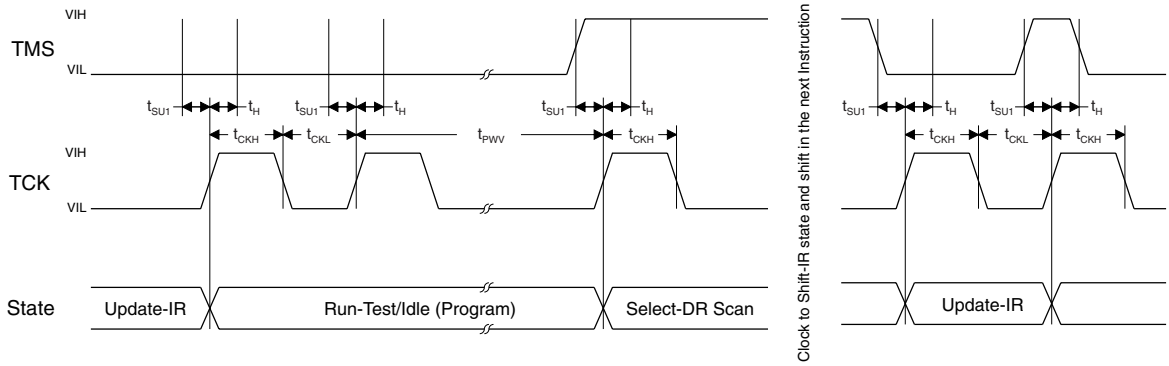
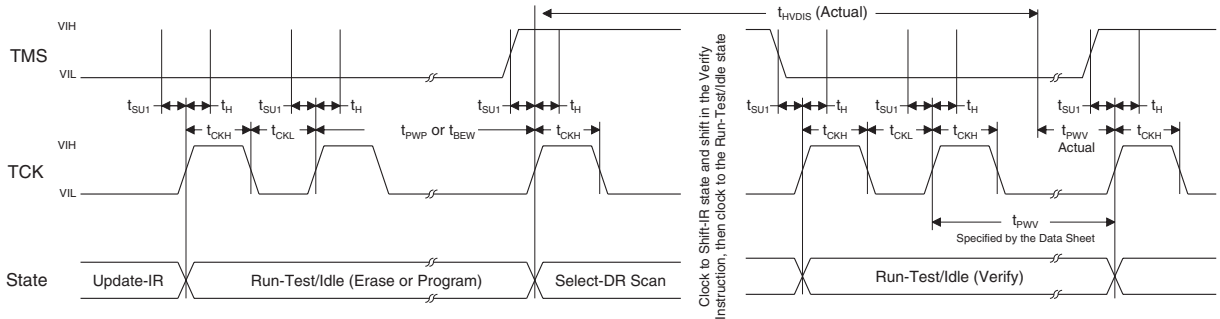
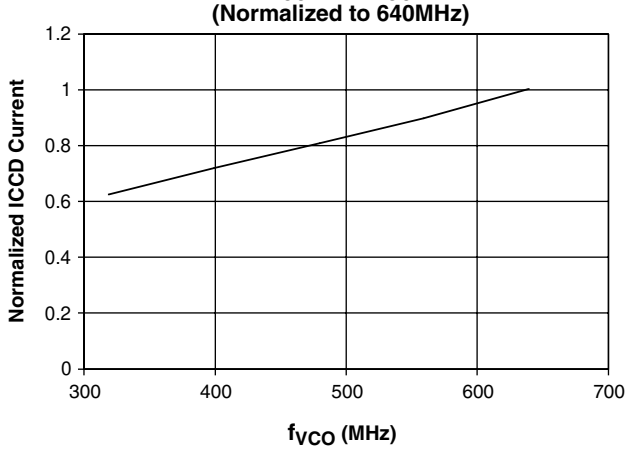


Figure 10. Discharge Timing Diagram

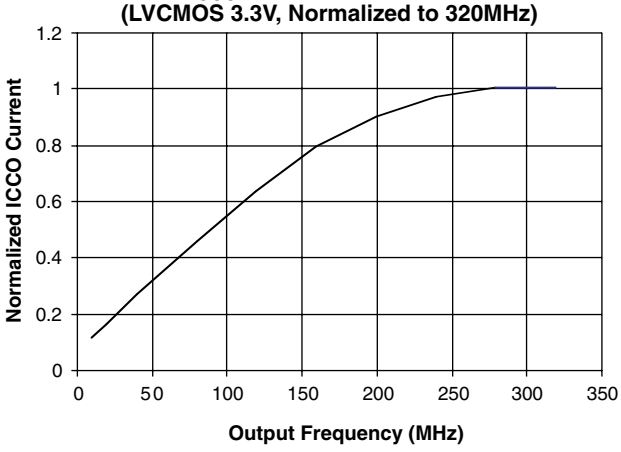


Typical Performance Characteristics

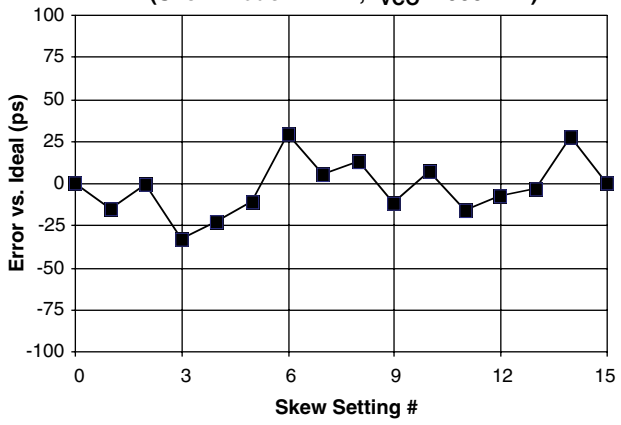
I_{CCD} vs. f_{VCO} (Normalized to 640MHz)



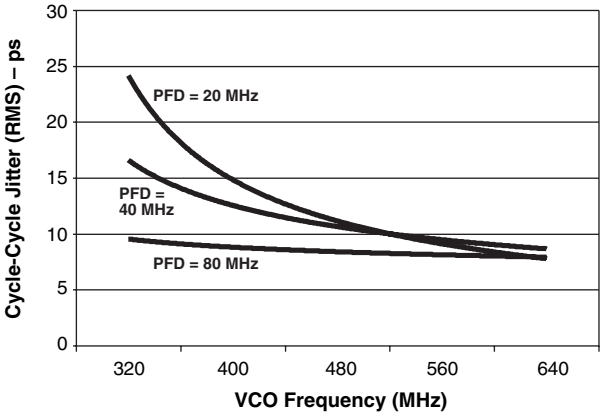
I_{CCO} vs. Output Frequency (LVCMOS 3.3V, Normalized to 320MHz)



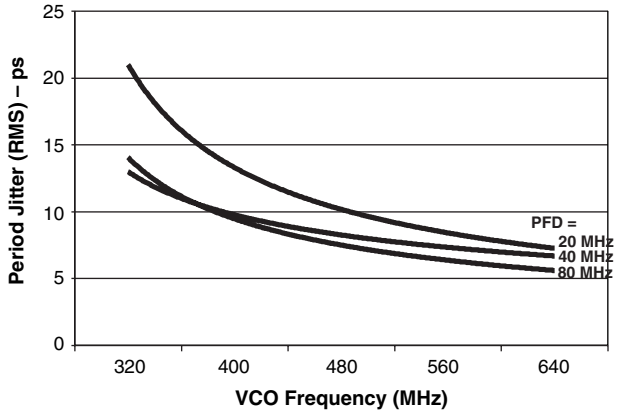
Typical Skew Error vs. Setting (Skew Mode = FINE, f_{VCO} = 600MHz)



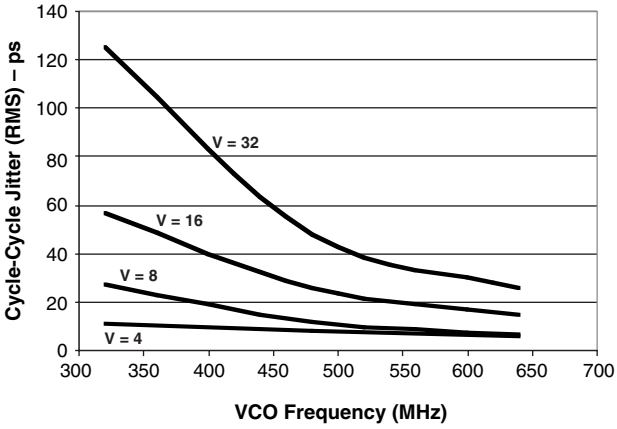
Cycle-Cycle Jitter vs. VCO Frequency V=4



Period Jitter vs. VCO Frequency V=4

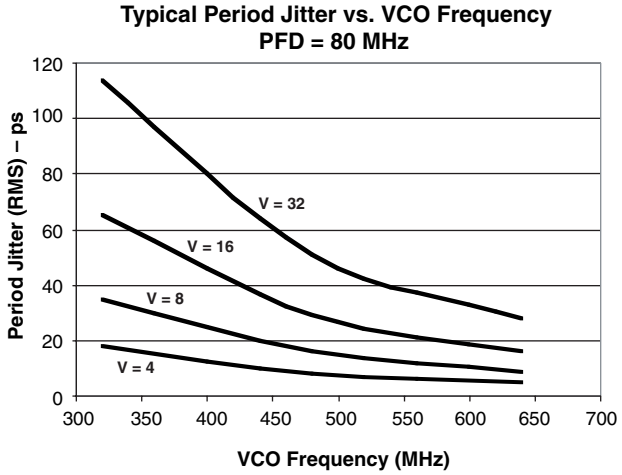


Typical Cycle-Cycle Jitter vs. VCO Frequency PFD = 80 MHz



*PFD = Phase/Frequency Detector

Typical Performance Characteristics (Cont.)



Detailed Description

PLL Subsystem

The ispClock5500 provides an integrated phase-locked-loop (PLL) which may be used to generate output clock signals at lower, higher, or the same frequency as a user-supplied input reference signal. The core functions of the PLL are an edge-sensitive phase detector, a programmable loop filter, and a high-speed voltage-controlled oscillator (VCO). Additionally, a set of programmable input, output and feedback dividers (M, N, V[1..5]) are provided to support the synthesis of different output frequencies.

Phase/Frequency Detector

The ispClock5500 provides an edge-sensitive phase/frequency detector (PFD), which means that the device will function properly over a wide range of input clock reference duty cycles. It is only necessary that the input reference clock meet specified minimum HIGH and LOW times ($t_{CLOCKHI}$, $t_{CLOCKLO}$) for it to properly recognized by the PFD. The PFD's output is of a classical charge-pump type, outputting charge packets which are then integrated by the PLL's loop filter.

A lock-detection feature is also associated with the PFD. When the ispClock5500 is in a LOCKED state, the $\overline{LOCK}$ output pin goes LOW. The lock detector has two operating modes; phase lock mode and frequency lock mode. In phase-lock mode, the $\overline{LOCK}$ signal is asserted if the phases of the reference and internal feedback signals match, whereas in frequency-lock mode the $\overline{LOCK}$ signal is asserted when the frequencies of the internal feedback and reference signals match. The option of which mode to use is programmable and may be set using PAC-Designer software (available from Lattice's web site at www.latticesemi.com).

In phase-lock mode the lock detector asserts the $\overline{LOCK}$ signal as soon as a lock condition is determined. In frequency-lock mode, however, the PLL must be in a locked condition for a set number of phase detector cycles before the $\overline{LOCK}$ signal will be asserted. The number of cycles required before asserting the $\overline{LOCK}$ signal in frequency-lock mode can be set from 16 through 256, in increments of 16.

The $\overline{LOCK}$ signal is generated in response to certain phase or frequency matches being detected at the input of the phase-frequency detector. Therefore it is possible that the $\overline{LOCK}$ signal may be asserted before the PLL has completely stabilized, and may change state while the PLL is in the process of stabilizing. Additionally, the output dividers are resynchronized in response to the frequency lock detector detecting a lock condition, even when the lock detector is set to phase mode. The frequency lock detector and phase lock detector are completely independent circuits.

Because the frequency lock detector requires a user-selectable number of cycles (16-256) to determine a lock condition, it is possible for the dividers to experience a resynchronization event a short time after a phase lock condition is detected. This may result in an glitch or missing clock cycle on one or more of the outputs. For all of the

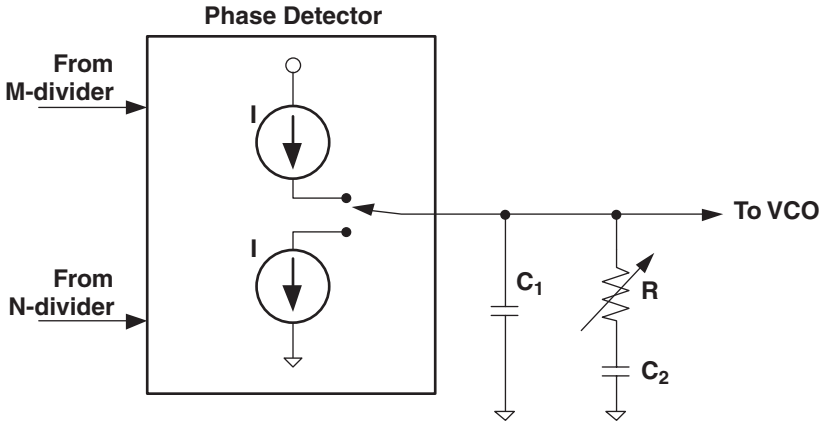
above reasons, it is recommended that when using phase-detect mode, the user wait a small amount of time (~25µs) between the time the $\overline{LOCK}$ signal is first asserted and the time at which the output clock signals are assumed to be completely stable.

When the lock condition is lost the $\overline{LOCK}$ signal will be de-asserted immediately in both phase-lock and frequency-lock detection modes. In frequency-lock mode, however, if the input reference signal is stopped, the $\overline{LOCK}$ output may continue to be asserted. In phase-lock mode, a loss of the input reference signal will always result in de-assertion of the $\overline{LOCK}$ output.

Loop Filter

A simplified schematic for the ispClock5500 loop filter is shown in Figure 11. The filter's capacitors are fixed, and the response is controlled by setting the value of the phase-detector's output current source's and the value of the variable resistor. The phase detector output current has 14 possible settings, ranging from 3µA to 55µA, while the resistor may be set to any one of six values ranging from 2.3K to 9.3K. This provides a total of 84 unique I-R combinations which may be selected.

Figure 11. ispClock5500 Loop Filter (Simplified)



Because the selection of an optimal PLL loop filter can be a daunting task, PAC-Designer offers a set of default filter settings which will provide acceptable performance for most applications. The primary criterion for selecting one of these settings is the total division factor used in the feedback path. This factor is the ratio between the VCO output frequency and the feedback V-divider output frequency which is the product of the N-divider and $V_{feedback}$-divider (N x $V_{feedback}$). Table 2 lists these default settings and conditions under which they should be used.

Table 2. PAC-Designer Recommended Loop Filter Settings

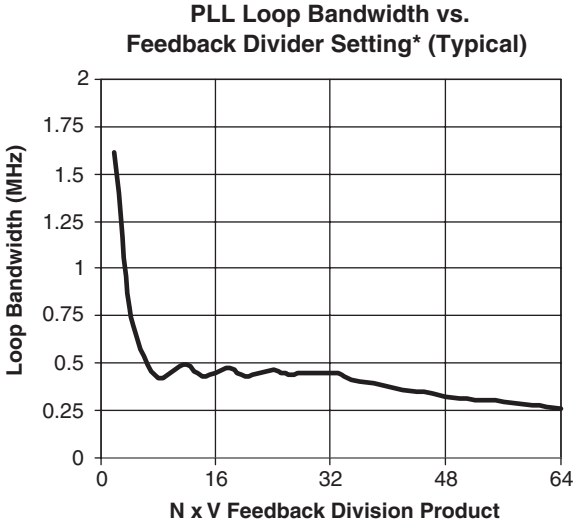
N x V_{FBK}	I (µA)	R (kΩ)
2 to 8	5	2.3
10	7	2.3
12 to 14	9	2.3
16	11	2.3
18 to 20	13	2.3
22	15	2.3
24 to 26	17	2.3
28	19	2.3
30	21	2.3
32 to 64	22	2.3

The choice of loop filter parameters can have significant effects on settling time, output jitter, and whether the PLL will be fundamentally stable and be able to lock to an incoming signal. The values recommended in Table 2 were

chosen to provide maximum loop stability while still providing exceptional jitter performance. Please note that when the skew mode is set to 'coarse', the effective value of NxV must be doubled. Refer to the section titled 'Coarse Skew Mode' on page 30 for more details.

The PLL's loop bandwidth is a function of both the divider configuration and the loop filter settings. Figure 12 shows the loop bandwidth as a function of the total feedback division ratio (N x V_{FBK}). For each NxV feedback divider point in this plot, the PLL loop filter was set to the corresponding value recommended in Table 2. The use of non-recommended loop filter settings may result in significantly different bandwidths for a given NxV divider setting.

Figure 12. PLL Loop Bandwidth vs. Feedback Divider Setting (nominal)



*loop filter configured to recommended setting

VCO

The ispClock5500 provides an internal VCO which provides an output frequency ranging from 320MHz to 640MHz. The VCO is implemented using differential circuit design techniques which minimize the influence of power supply noise on measured output jitter. The VCO is also used to generate skews as a function of the total VCO period. Using the VCO as the basis for controlling output skew allows for highly precise and consistent skew generation, both from device-to-device, as well as channel-to-channel within the same device.

M, N, and V Dividers

The ispClock5500 incorporates a set of programmable dividers which provide the ability to synthesize output frequencies differing from that of the reference clock input.

The input, or M, divider prescales the input reference frequency, and can be programmed with integer values over the range of 1 to 32. To achieve low levels of output jitter, it is best to use the smallest M divider value possible.

The feedback, or N, divider prescales the feedback frequency and like the M divider, can also be programmed with integer values ranging from 1 to 32.

Each one of the five output, or V, dividers can be independently programmed to provide even division ratios ranging from 2 to 64.

When the PLL is selected (PLL_BYPASS=LOW) and locked, the output frequency of each V divider (f_k) may be calculated as:

$$f_k = f_{ref} \frac{N \times V_{fbk}}{M \times V_k} \quad (1)$$

where

f_k is the frequency of V divider k
f_{ref} is the input reference frequency
M and N are the input and feedback divider settings
V_{fbk} is the setting of the V divider used to close the PLL feedback path
V_k is the setting of the V divider used to provide output k

Note that because the feedback may be taken from any V divider, V_k and V_{fbk} may refer to the same divider.

Because the VCO has an operating frequency range spanning 320 MHz to 640 MHz, and the V dividers provide division ratios from 2 to 64, the ispClock5500 can generate output signals ranging from 5MHz to 320 MHz. For performance and stability reasons, however, there are several constraints which should be followed when selecting divider values:

- Use the smallest feasible value for the M divider
- The output frequency from the M (and N) divider should be greater or equal to 10 MHz.
- The product of the N divider and the V divider used to close the PLL's feedback loop should be less than or equal to 64 ($N \times V_{fbk} \leq 64$)

Output Duty Cycle

The ispClock5500's output duty cycle varies as a function of the V divider used to generate that output. If the V-divider setting is either 2 or a multiple of 4, the nominal output duty cycle will be exactly 50%. All other V divider settings will result in non-50% output duty cycles. Table 3 summarizes the nominal output duty cycle as a function of the V divider setting. Note that if the output is inverted, the duty cycle will be equal to 100%-DC%, where DC% is the duty cycle indicated in the table. For example, with a V divider of 14, the non-inverted duty cycle from Table 3 will be 43%. For an inverted output, the duty cycle will be 100%-43% or 57%.

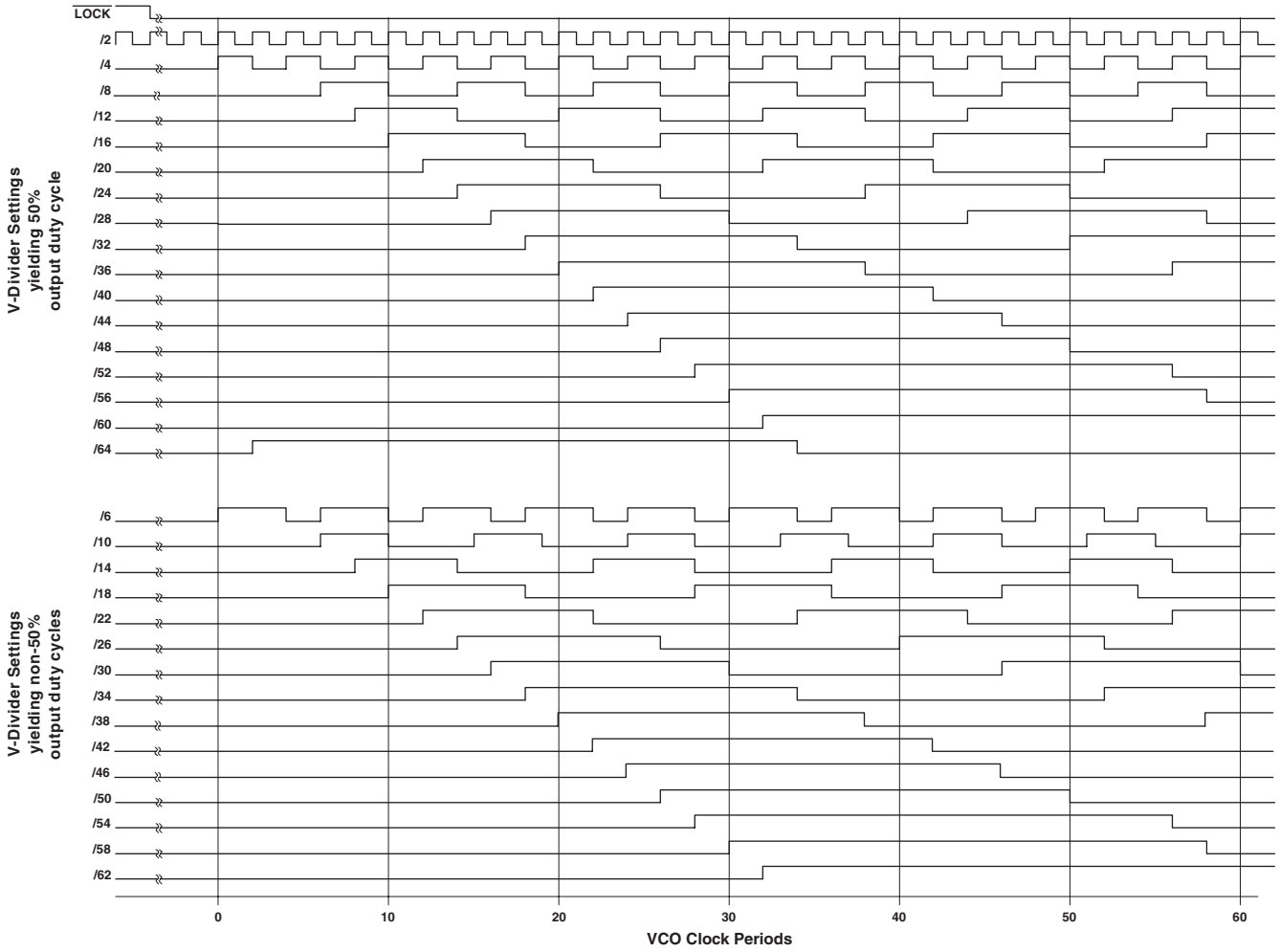
Table 3. Nominal Output Duty Cycle vs. V-Divider Setting

Divider Settings with 50% Output Duty Cycle	
V	**DC%**
2	50
4	
8	
12	
16	
20	
24	
28	
32	
36	
40	
44	
48	
52	
56	
60	
64	

Divider Settings with Non-50% Output Duty Cycles	
V	**DC%**
6	33
10	40
14	43
18	44
22	45
26	46
30	47
34	47
38	47
42	48
46	48
50	48
54	48
58	48
62	48

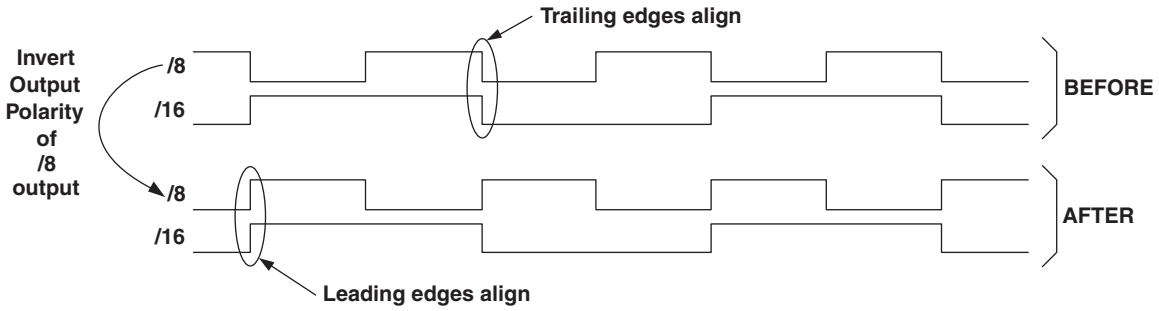
Figure 13 shows the relative timing for a V-divider as a function of its 32 possible divisor settings (2-64) as the PLL locks. If two V-dividers are configured with the same divisor, their outputs will be synchronized. If these two V-dividers are fed to separate outputs, and the skew settings for these two outputs are identical, then the corresponding rising and falling edges for the two outputs will occur simultaneously.

Figure 13. ispClock5500 Output Divider Timing Relationships Among Various Divisors



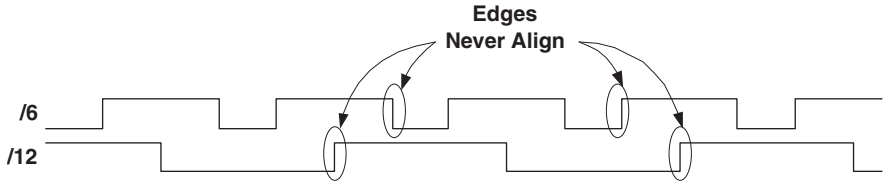
If two V-dividers are configured with different divisors, however, their outputs may not necessarily have aligned edges, even in cases where one divisor is an integer multiple of the other (e.g. 6 and 12). In cases where the divisor is set to either 2 or a multiple of 4, the output duty cycle will be 50% (top set of waveforms in Figure 13), and the rising edges (or falling edges) of outputs driven from different divisors may be aligned by inverting one or more of the outputs as shown in Figure 14.

Figure 14. Flipping Polarity to Edge Align Two Outputs



For V-divider combinations in which one or more of the V-dividers is configured to a value that is not divisible by 4 (e.g. 6), there exists the possibility that neither rising nor falling edges may align. For example, when V-divider values of 6 and 12 are chosen, the two resulting outputs will have no edge alignment, as shown in Figure 15. Note that because the offset is 2 VCO periods in this case, it is not possible to use the skew adjustment feature to force any of the edges into perfect alignment as the skew control units provide a maximum delay of 1.875 VCO periods.

Figure 15. Timing Relationship Between V-divider Values of 6 and 12



PLL_BYPASS Mode

The PLL_BYPASS mode is provided so that input reference signals can be coupled through to the outputs without using the PLL functions. When PLL_BYPASS mode is enabled (PLL_BYPASS=HIGH), the output of the M divider is routed directly to the inputs of the V dividers. In PLL_BYPASS mode, the nominal values of the V dividers are halved, so that they provide division ratios ranging from 1 to 32. The divide-by-1 setting, however, is invalid and will produce undefined results. The output frequency for a given V divider (f_k) will be determined by

$$f_k = \frac{f_{ref} \times 2}{M \times V_k} \quad (2)$$

Please note that PLL_BYPASS mode is provided primarily for testing purposes. When PLL_BYPASS mode is enabled, features such as lock detect and skew generation are unavailable.

Reference Inputs

The ispClock5500 provides sets of configurable, internally-terminated inputs for clock reference signals. In normal operation, the clock reference input (REFB) is connected to the system clock from which the output signals are to be derived.

The ispClock5510 provides one input signal pair for reference input, while the ispClock5520 provides two input pairs for reference signals. To select between reference inputs, the ispClock5520 provides a CMOS-compatible digital input called REFSEL. Table 4 shows the behavior of this control input:

Table 4. REFSEL Operation for ispClock5520

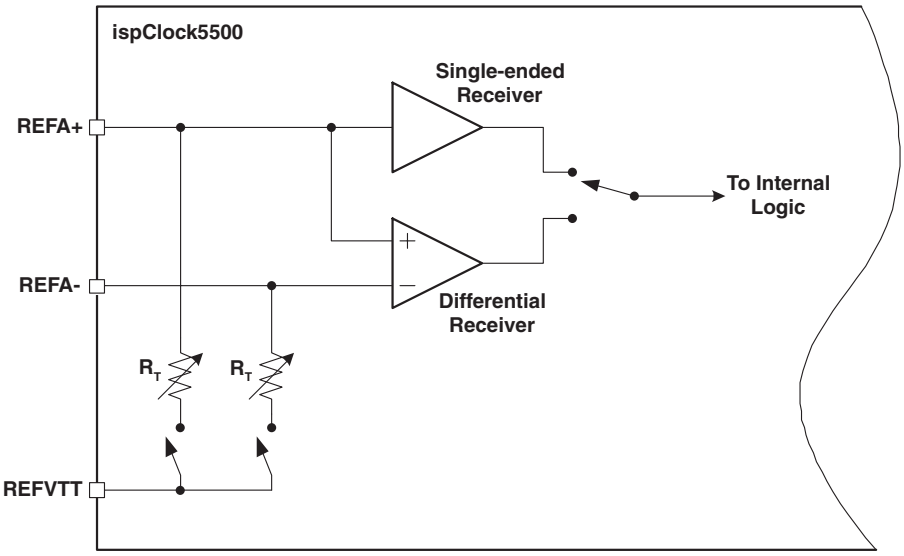
REFSEL	Selected Input Pair
0	REFA+/-
1	REFB+/-

Clock reference inputs may be configured to interface to signals from the following logic families with little or no external support circuitry:

- LVTTL (3.3V)
- LVCMOS (1.8V, 2.5V, 3.3V)
- SSTL2
- SSTL3
- HSTL
- LVDS
- LVPECL (differential, 3.3V)

Each input also features internal programmable termination resistors, as shown in Figure 16.

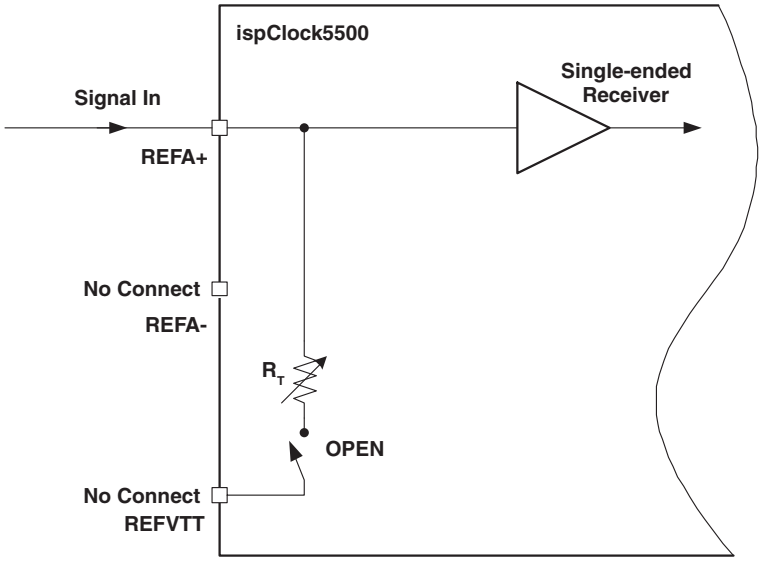
Figure 16. ispClock5500 Clock Reference Input Structure (REFA+/- Pair Shown)



The following usage guidelines are suggested for interfacing to supported logic families.

LVTTL (3.3V), LVCMOS (1.8V, 2.5V, 3.3V)
The receiver should be set to LVCMOS or LVTTL mode, and the input signal should be connected to the '+' terminal of the input pair (e.g. REFA+). The '-' input terminal should be left floating. CMOS transmission lines are generally source terminated, so all termination resistors should be set to the OPEN state. Figure 17 shows the proper configuration. Please note that because switching thresholds are different for LVCMOS running at 1.8V, there is a separate configuration setting for this particular standard.

Figure 17. LVCMOS/LVTTL Input Receiver Configuration

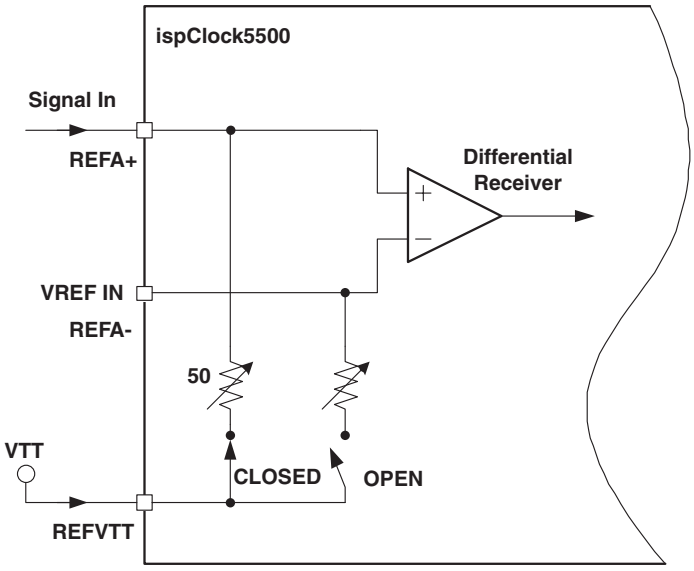


HSTL, SSTL2, SSTL3

The receiver should be set to HSTL/SSTL mode, and the input signal should be fed into the '+' terminal of the input pair. The '-' input terminal should be tied to the appropriate V_{ref} value, and the REFVTT terminal should be tied to a V_{TT} termination supply. The positive input's terminating resistor should be engaged and set to 50Ω. Figure 18 shows an appropriate configuration. Refer to the "Recommended Operating Conditions - Supported Logic Standards" table in this data sheet for suitable values of V_{REF} and $V_{TT.}$

One important point to note is that the termination supplies must have low impedance and be able to both source and sink current without experiencing fluctuations. These requirements generally preclude the use of a resistive divider network, which has an impedance comparable to the resistors used, or of commodity-type linear voltage regulators, which can only source current. The best way to develop the necessary termination voltages is with a regulator specifically designed for this purpose. Because SSTL and HSTL logic is commonly used for high-performance memory busses, a suitable termination voltage supply is often already available in the system.

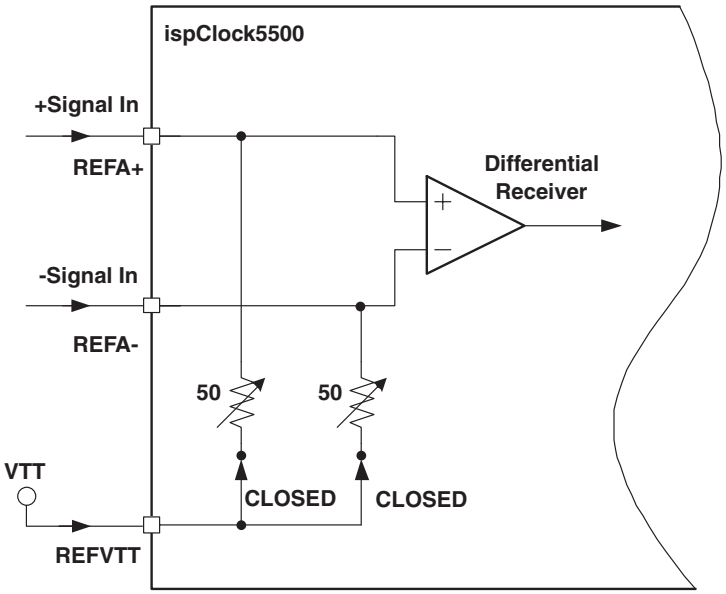
Figure 18. SSTL2, SSTL3, HSTL Receiver Configuration



Differential HSTL and SSTL

HSTL and SSTL are sometimes used in a differential form, especially for distributing clocks in high-speed memory systems. Figure 19 shows how ispClock5500 reference input should be configured for accepting these standards. The major difference between the differential and single-ended forms of these logic standards is that in the differential cases, the REFA- input is used as a signal input, not a reference level, and that both terminating resistors are engaged and set to 50Ω.

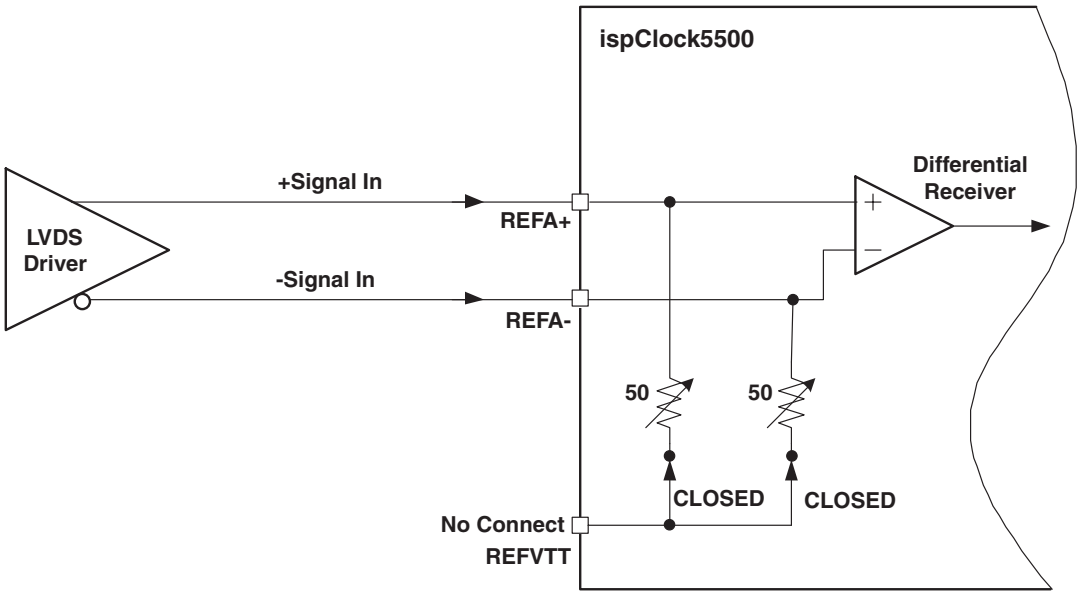
Figure 19. Differential HSTL/SSTL Receiver Configuration



LVDS/Differential LVPECL

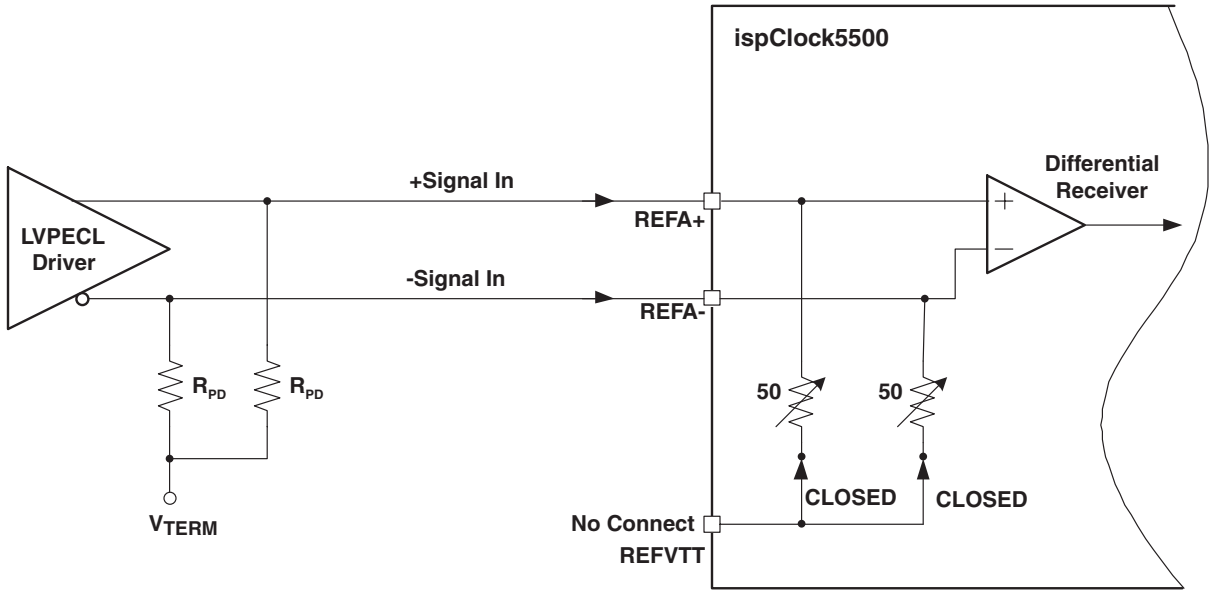
The receiver should be set to LVDS or LVPECL mode as required and both termination resistors should be engaged and set to 50Ω. The REFVTT pin, however, should be left unconnected. This creates a floating 100Ω differential termination resistance across the input terminals. The LVDS termination configuration is shown in Figure 20.

Figure 20. LVDS Input Receiver Configuration



Note that while a floating 100Ω resistor forms a complete termination for an LVDS signal line, additional circuitry may be required to satisfactorily terminate a differential LVPECL signal. This is because a true bipolar LVPECL output driver typically requires an external DC 'pull-down' path to a V_{TERM} termination voltage (typically VCC-2V) to properly bias its open emitter output stage. When interfacing to an LVPECL input signal, the ispClock5500's internal termination resistors should not be used for this pull-down function, as they may be damaged from excessive current. The pull-down should be implemented with external resistors placed close to the LVPECL driver (Figure 21)

Figure 21. LVPECL Input Receiver Configuration



Please note that while the above discussions specify using 50Ω termination impedances, the actual impedance required to properly terminate the transmission line and maintain good signal integrity may vary from this ideal. The actual impedance required will be a function of the driver used to generate the signal and the transmission medium used (PCB traces, connectors and cabling). The ispClock5500's ability to adjust input impedance over a range of 40Ω to 70Ω allows the user to adapt his circuit to non-ideal behaviors from the rest of the system without having to swap out components.

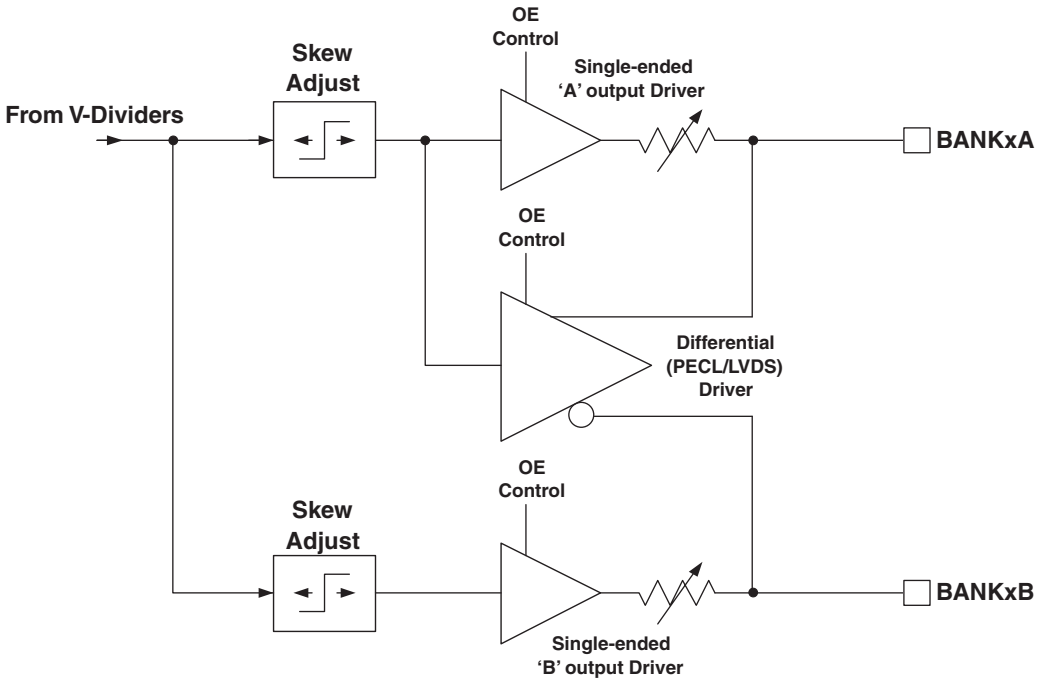
Output Drivers

The ispClock5500 provide banks of configurable, internally-terminated high-speed dual-output line drivers. The ispClock5510 provides five driver banks, while the ispClock5520 provides ten. Each of these driver banks may be configured to provide either a single differential output signal, or a pair of single-ended output signals. Programmable internal source-series termination allows the ispClock5500 to be matched to transmission lines with impedances ranging from 40 to 70 Ohms. The outputs may be independently enabled or disabled, either from E^2CMOS configuration or by external control lines. Additionally, each can be independently programmed to provide a fixed amount of signal delay or skew, allowing the user to compensate for the effects of unequal PCB trace lengths or loading effects. Figure 22 shows a block diagram of a typical ispClock5500 output driver bank and associated skew control.

Because of the high edge rates which can be generated by the ispClock5500's clock output drivers, the VCCO power supply pin for each output bank should be individually bypassed. Low ESR capacitors with values ranging from 0.01 to 0.1 µF may be used for this purpose. Each bypass capacitor should be placed as close to its respective output bank power pins (VCCO and GNDO) pins as is possible to minimize interconnect length and associated parasitic inductances.

In the case where an output bank is unused, the associated VCCO pin may be either left floating or tied to ground to reduce quiescent power consumption. We recommend, however, that all unused VCCO pins be tied to ground where possible. All GNDD pins must be tied to ground, regardless of whether or not the associated bank is used.

Figure 22. ispClock5500 Output Driver and Skew Control



Each of the ispClock5500's output driver banks can be configured to support the following logic outputs:

- LVTTL
- LVCMOS (1.8V, 2.5V, 3.3V)
- SSTL2
- SSTL3
- HSTL
- LVDS
- Differential LVPECL (3.3V)

To provide LVTTL, LVCMOS, SSTL2, SSTL3, and HSTL outputs, the CMOS output drivers in each bank are enabled. These circuits provide logic outputs which swing from ground to the VCCO supply rail. The choice of VCCO to be supplied to a given bank is determined by the logic standard to which that bank is configured. Because each pair of outputs has its own VCCO supply pin, each bank can be independently configured to support a different logic standard. Note that the two outputs associated with a bank must necessarily be configured to the same logic standard. The source impedance of each of the two outputs in each bank may be independently set over a range of 40Ω to 70Ω in 5Ω steps. A low impedance option (≈20Ω) is also provided for cases where low source termination is desired on a given output, such as when using HSTL output mode.

Control of output slew rate is also provided in LVTTL, LVCMOS, SSTL2, SSTL3, and HSTL output modes. Four output slew-rate settings are provided, as specified in the "Output Rise Times" and "Output Fall Times" tables in this data sheet.

To provide LVDS and differential LVPECL outputs, a separate driver is used which provides the correct LVDS or LVPECL logic levels when operating from a 3.3V VCCO. Because both LVDS and differential LVPECL transmission lines are normally terminated with a single 100Ω resistor between the '+' and '-' signal lines at the far end, the