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ispClock™5600A Family

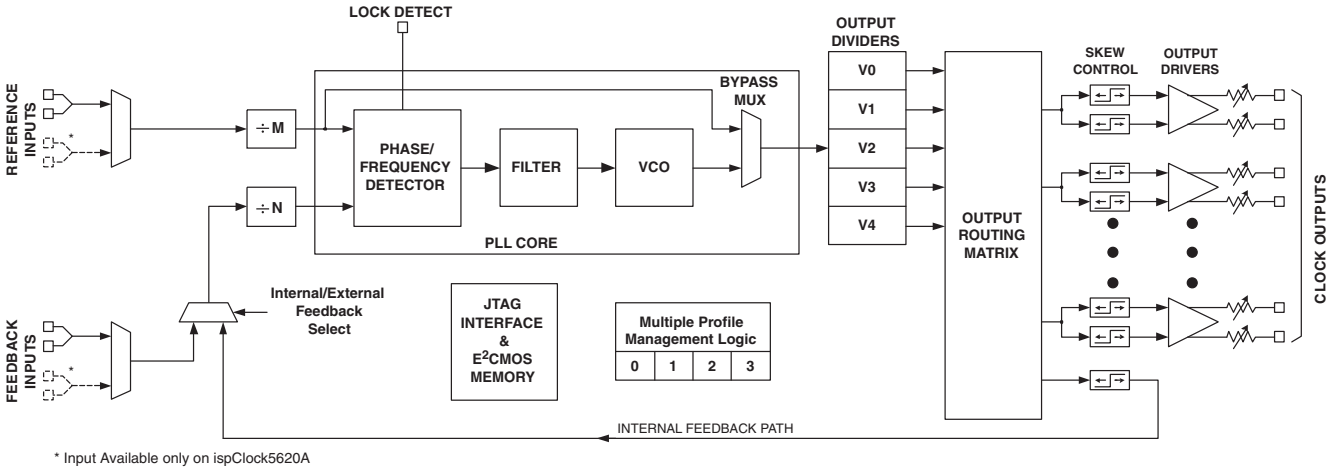
In-System Programmable, Enhanced Zero-Delay Clock Generator with Universal Fan-Out Buffer

June 2008 Data Sheet DS1019

Features

- **8MHz to 400MHz Input/Output Operation**
- **Low Output to Output Skew (<50ps)**
- **Low Jitter Peak-to-Peak**
- **Up to 20 Programmable Fan-out Buffers**
  - Programmable output standards and individual enable controls
    - LVTTL, LVCMOS, HSTL, eHSTL, SSTL, LVDS, LVPECL, Differential HSTL, SSTL
  - Programmable output impedance
    - 40 to 70Ω in 5Ω increments
  - Programmable slew rate
  - Up to 10 banks with individual V_{CCO} and GND
    - 1.5V, 1.8V, 2.5V, 3.3V
- **Fully Integrated High-Performance PLL**
  - Programmable lock detect
  - Multiply and divide ratio controlled by
    - Input divider (1 to 40)
    - Feedback divider (1 to 40)
    - Five output dividers (2 to 80)
  - Programmable on-chip loop filter
  - Compatible with spread spectrum clocks
- **Precision Programmable Phase Adjustment (Skew) Per Output**
  - 16 settings; minimum step size 156ps
    - Locked to VCO frequency
  - Up to +/- 12ns skew range
  - Coarse and fine adjustment modes
- **Up to Five Clock Frequency Domains**
- **Flexible Clock Reference and External Feedback Inputs**
  - Programmable input standards
    - LVTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL, Differential HSTL, SSTL
  - Clock A/B selection multiplexer
  - Feedback A/B selection multiplexer
  - Programmable termination
- **All Inputs and Outputs are Hot Socket Compliant**
- **Four User-programmable Profiles Stored in E²CMOS® Memory**
  - Supports both test and multiple operating configurations
- **Full JTAG Boundary Scan Test In-System Programming Support**
- **Exceptional Power Supply Noise Immunity**
- **Commercial (0 to 70°C) and Industrial (-40 to 85°C) Temperature Ranges**
- **100-pin and 48-pin TQFP Packages**
- **Applications**
  - Circuit board common clock generation and distribution
  - PLL-based frequency generation
  - High fan-out clock buffer
  - Zero-delay clock buffer

Product Family Block Diagram



* Input Available only on ispClock5620A

General Description and Overview

The ispClock5610A and ispClock5620A are in-system-programmable high-fanout enhanced zero delay clock generators designed for use in high performance communications and computing applications. The ispClock5610A provides up to 10 single-ended or five differential clock outputs, while the ispClock5620A provides up to 20 single-ended or 10 differential clock outputs. Each pair of outputs may be independently configured to support separate I/O standards (LVDS, LVPECL, LVTTL, LVCMOS, SSTL, HSTL) and output frequency. In addition, each output provides independent programmable control of termination, slew-rate, and timing skew. All configuration information is stored on-chip in non-volatile E^2CMOS memory.

The ispClock5600A's PLL and divider systems supports the synthesis of multiple clock frequencies derived from the reference input through the provision of programmable input and feedback dividers. A set of five post-PLL V-dividers provides additional flexibility by supporting the generation of five separate output frequencies. Loop feedback may be taken internally from the output of any of the five V-dividers, or externally through FBKA+/- or FBKB+/- pins.

The core functions of all members of the ispClock5600A family are identical, the differences between devices being restricted to the number of inputs and outputs, as shown in the following table. Figures 1 and 2 show functional block diagrams of the ispClock5610A and ispClock5620A.

Table 1-1. ispClock5600A Family Members

Device	Ref. Input Pairs	Feedback Input Pairs	Clock Outputs
ispClock5610A	1	1	10
ispClock5620A	2	2	20

Figure 1-1. ispClock5610A Functional Block Diagram

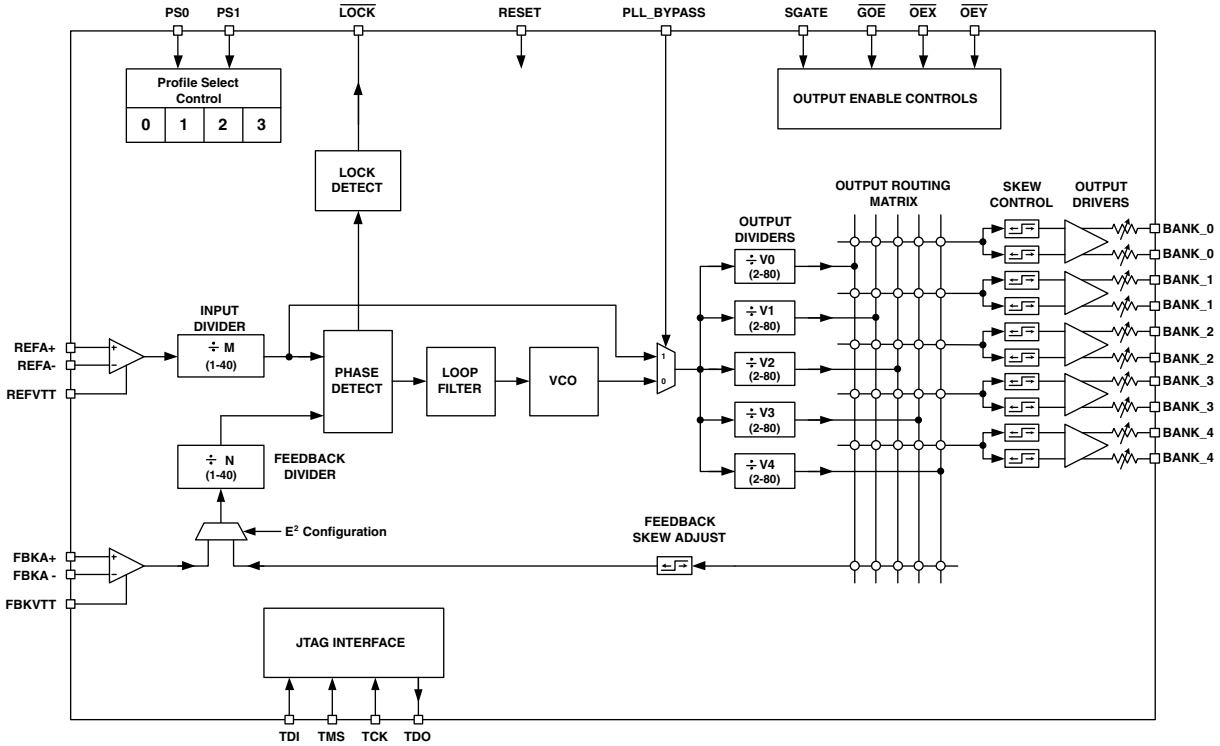
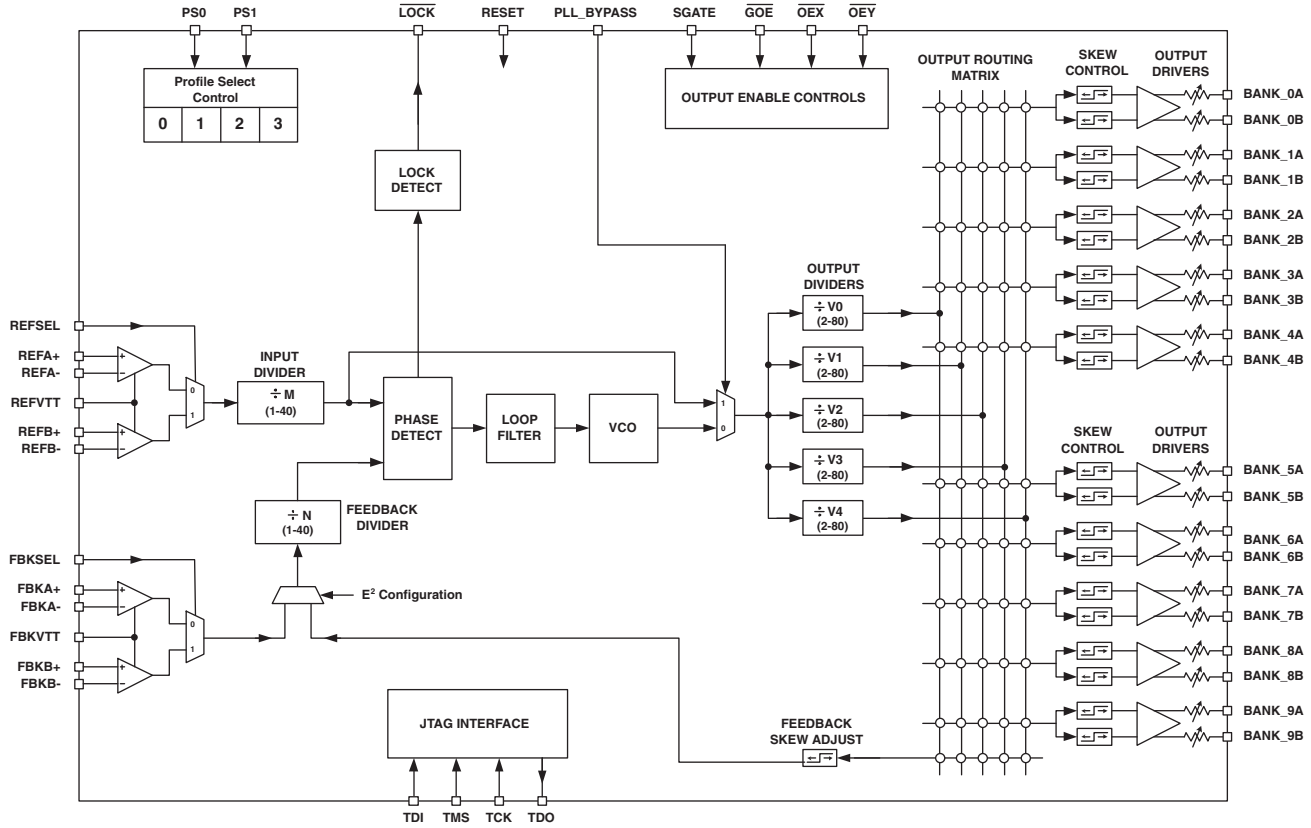


Figure 1-2. ispClock5620A Functional Block Diagram



Absolute Maximum Ratings

	ispClock5600A
Core Supply Voltage V_{CCD}	-0.5 to 5.5V
PLL Supply Voltage V_{CCA}	-0.5 to 5.5V
JTAG Supply Voltage V_{CCJ}	-0.5 to 5.5V
Output Driver Supply Voltage V_{CCO}	-0.5 to 4.5V
Input Voltage	-0.5 to 4.5V
Output Voltage[1]	-0.5 to 4.5V
Storage Temperature	-65 to 150°C
Junction Temperature with power supplied	-40 to 130°C

1. When applied to an output when in high-Z condition

Recommended Operating Conditions

Symbol	Parameter	Conditions	ispClock5600A		Units
			Min.	Max.	
V_{CCD}	Core Supply Voltage		3.0	3.6	V
V_{CCJ}	JTAG I/O Supply Voltage		2.25	3.6	V
V_{CCA}	Analog Supply Voltage		3.0	3.6	V
$V_{CCXSLEW}$	V_{CC} Turn-on Ramp Rate	All supply pins	—	0.33	V/µs
T_{JOP}	Operating Junction Temperature	Commercial	0	130	°C
		Industrial	-40	130	
T_A	Ambient Operating Temperature	Commercial	0	70[1]	°C
		Industrial	-40	85[1]	

1. Device power dissipation may also limit maximum ambient operating temperature.

Recommended Operating Conditions – V_{CCO} vs. Logic Standard

Logic Standard		V_{CCO} (V)			V_{REF} (V)			V_{TT} (V)		
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL		3.0	3.3	3.6	—	—	—	—	—	—
LVCMOS 1.8V		1.71	1.8	1.89	—	—	—	—	—	—
LVCMOS 2.5V		2.375	2.5	2.625	—	—	—	—	—	—
LVCMOS 3.3V		3.0	3.3	3.6	—	—	—	—	—	—
SSTL1.8		1.71	1.8	1.89	0.84	0.90	0.95	—	0.5 x V_{CCO}	—
SSTL2 Class 1		2.375	2.5	2.625	1.15	1.25	1.35	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL3 Class 1		3.0	3.3	3.6	1.30	1.50	1.70	V_{REF} - 0.05	V_{REF}	V_{REF} + 0.05
HSTL Class 1		1.425	1.5	1.575	0.68	0.75	0.90	—	0.5 x V_{CCO}	—
eHSTL Class 1		1.71	1.8	1.89	0.84	0.90	0.95	—	0.5 x V_{CCO}	—
LVPECL (Differential)		3.0V	3.3V	3.6V	—	—	—	—	—	—
LVDS	V_{CCO} = 2.5V	2.375	2.5V	2.625	—	—	—	—	—	—
	V_{CCO} = 3.3V	3.0	3.3	3.6	—	—	—	—	—	—

Note: '—' denotes V_{REF} or V_{TT} not applicable to this logic standard

E²CMOS Memory Write/Erase Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Erase/Reprogram Cycles		1000	—	—	

Performance Characteristics – Power Supply

Symbol	Parameter	Conditions	Typ.	Max.	Units
I_{CCD}	Core Supply Current[3]	ispClock5610A f_{VCO} = 800MHz	110	125	mA
		ispClock5620A f_{VCO} = 800MHz	130	150	mA
I_{CCA}	Analog Supply Current[3]	f_{VCO} = 800MHz	5.5	7	mA
I_{CCO}	Output Driver Supply Current (per Bank)	V_{CCO} = 1.8V[1], LVCMOS, f_{OUT} = 266MHz	16	18	mA
		V_{CCO} = 2.5V[1], LVCMOS, f_{OUT} = 266MHz	21	27	mA
		V_{CCO} = 3.3V[1], LVCMOS, f_{OUT} = 266MHz	27	38	mA
		V_{CCO} = 3.3V[2], LVDS, f_{OUT} = 400MHz	8	10	mA
I_{CCJ}	JTAG I/O Supply Current (static)	V_{CCJ} = 1.8V		300	µA
		V_{CCJ} = 2.5V		400	µA
		V_{CCJ} = 3.3V		400	µA

1. Supply current consumed by each bank, both outputs active, 5pF load.
2. Supply current consumed by each bank, 100Ω, 5pf differential load.
3. All unused REFCLK and feedbacks connected to ground.

DC Electrical Characteristics – Single-ended Logic

Logic Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min.	Max.	Min.	Max.				
LVTTL/LVCMOS 3.3V	-0.3	0.8	2	3.6	0.4	V_{CCO} - 0.4	12[2, 3]	-12[2, 3]
LVCMOS 1.8V	-0.3	0.68	1.07	3.6	0.4	V_{CCO} - 0.4	12[2, 3]	-12[2, 3]
LVCMOS 2.5V	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	12[2, 3]	-12[2, 3]
SSTL2 Class 1	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54[2]	V_{CCO} - 0.81[1]	7.6	-7.6
SSTL3 Class 1	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.9[2]	V_{CCO} - 1.3[1]	8	-8
HSTL Class 1	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4[3]	V_{CCO} - 0.4[2]	8	-8
eHSTL Class 1	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4[3]	V_{CCO} - 0.4[2]	8	-8

1. Specified for 40Ω internal series output termination.
2. Specified for ≈20Ω internal series output termination, fast slew rate setting.
3. For slower slew rate setting I_{OH}, I_{OL} = 8mA.

DC Electrical Characteristics – LVDS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{ICM}	Common Mode Input Voltage	$V_{THD} \leq 100mV$	$V_{THD}/2$	—	2.0	V
		$V_{THD} \leq 150mV$	$V_{THD}/2$		2.325	V
V_{THD}	Differential Input Threshold		±100	—	—	mV
V_{IN}	Input Voltage		0	—	2.4	V
V_{OH}	Output High Voltage	$R_T = 100\Omega$	—	1.375	1.60	V
V_{OL}	Output Low Voltage	$R_T = 100\Omega$	0.9	1.03	—	V
V_{OD}	Output Voltage Differential	$R_T = 100\Omega$	250	400	480	mV
ΔV_{OD}	Change in V_{OD} Between H and L		—	—	50	mV
V_{OS}	Output Voltage Offset	Common Mode Output Voltage	1.10	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50	mV
I_{SA}	Output Short Circuit Current	V_{OD} = 0V, Outputs Shorted to GND	—	—	24	mA
I_{SAB}	Output Short Circuit Current	V_{OD} = 0V, Outputs Shorted to Each Other	—	—	12	mA

DC Electrical Characteristics – Differential LVPECL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input Voltage High	V_{CCD} = 3.0 to 3.6V	V_{CCD} - 1.17	—	V_{CCD} - 0.88	V
		V_{CCD} = 3.3V	2.14	—	2.42	
V_{IL}	Input Voltage Low	V_{CCD} = 3.0 to 3.6V	V_{CCD} - 1.81	—	V_{CCD} - 1.48	V
		V_{CCD} = 3.3V	1.49	—	1.83	
V_{OH}	Output High Voltage[1]	V_{CCO} = 3.0 to 3.6V	V_{CCO} - 1.07	—	V_{CCO} - 0.88	V
		V_{CCO} = 3.3V	2.23	—	2.42	
V_{OL}	Output Low Voltage[1]	V_{CCO} = 3.0 to 3.6V	V_{CCO} - 1.81	—	V_{CCO} - 1.62	V
		V_{CCO} = 3.3V	1.49	—	1.68	

1. 100Ω differential termination.

Electrical Characteristics – Differential SSTL18

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CCO}	Output Supply Voltage		1.71	1.8	1.89	V
V_{IL}	Low-Logic Level Input Voltage				0.61	V
V_{IH}	Hi Logic Level Input Voltage		1.17			V
V_{SWING}	AC Differential Output Voltage		0.64			V
V_{IX}	Input Pair Differential Crosspoint Voltage		V_{REF} -175mV		V_{REF} +175mV	V
TCKD	Clock Duty Cycle	Load Conditions (Figure 1-6)	45		55	%

Electrical Characteristics – Differential SSTL2

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
$V_{SWING(DC)}$	DC Differential Input Voltage Swing		-0.03		3.225	V
$V_{SWING(AC)}$	AC Input Differential Voltage		0.62		3.225	V
V_{IX}	Input Pair Differential Crosspoint Voltage		V_{REF} - 200 mV		V_{REF} + 200 mV	V
TCKD	Clock Duty Cycle	Load Conditions (Figure 1-6)	45		55	%

Electrical Characteristics – Differential HSTL

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Output Supply Voltage		1.425	1.5	1.575	V
$V_{SWING(DC)}$	DC Differential Input Voltage Swing		-0.03		V_{CCD}	V
$V_{SWING(AC)}$	AC Input Differential Voltage		0.4		V_{CCD}	V
V_{IX}	Input Pair Differential Crosspoint Voltage		0.68		0.9	V
TCKD	Clock Duty Cycle	Load Conditions (Figure 1-6)	45		55	%

Electrical Characteristics – Differential eHSTL

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Output Supply Voltage		1.7	1.8	1.9	V
$V_{SWING(DC)}$	DC Differential Input Voltage Swing		-0.03		V_{CCD}	V
$V_{SWING(AC)}$	AC Input Differential Voltage		0.4		V_{CCD}	V
V_{IX}	Input Pair Differential Crosspoint Voltage		0.68		0.9	V
TCKD	Clock Duty Cycle	Load Conditions (Figure 1-6)	45		55	%

DC Electrical Characteristics – Input/Output Loading

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{LK}	Input Leakage	Note 1	—	—	±10	µA
I_{PU}	Input Pull-up Current	Note 2	—	80	120	µA
I_{PD}	Input Pull-down Current	Note 3	—	120	150	µA
I_{OLK}	Tristate Leakage Output	Note 4	—	—	±10	µA
C_{IN}	Input Capacitance	Notes 2, 3, 5	—	8	10	pF
		Note 6	—	13.5	15	pF

1. Applies to clock reference inputs when termination ‘open’.
2. Applies to TDI, TMS inputs.
3. Applies to REFSEL, PS0, PS1, $\overline{GOE}$, SGATE and PLL_BYPASS, FBKSEL, OEX, OEY.
4. Applies to all logic types when in tristated mode.
5. Applies to OEX, OEY, TCK, RESET inputs.
6. Applies to REFA+, REFA-, REFB+, REFB-, FBKA+, FBKA-, FBKB+, FBKB-.

Switching Characteristics – Timing Adders for I/O Modes

Adder Type	Description	Min.	Typ.	Max.	Units
t_{IOI} Input Adders[2]					
LVTTL_in	Using LVTTL Standard	0	0	0	ps
LVCMOS18_in	Using LVCMOS 1.8V Standard	-99	80	315	ps
LVCMOS25_in	Using LVCMOS 2.5V Standard	0	0	0	ps
LVCMOS33_in	Using LVCMOS 3.3V Standard	0	0	0	ps
SSTL18_in	Using SSTL18 Standard	10	360	642	ps
SSTL2_in	Using SSTL2 Standard	64	420	679	ps
SSTL3_in	Using SSTL3 Standard	34	380	630	ps
HSTL_in	Using HSTL Standard	231	672	1064	ps
eHSTL_in	Using eHSTL Standard	128	514	846	ps
LVDS_in	Using LVDS Standard	118	426	651	ps
LVPECL_in	Using LVPECL Standard	201	593	937	ps
t_{IOO} Output Adders[1, 3]					
LVTTL_out	Output Configured as LVTTL Buffer	116	395	553	ps
LVCMOS18_out	Output Configured as LVCMOS 1.8V Buffer	155	510	730	ps
LVCMOS25_out	Output Configured as LVCMOS 2.5V Buffer	124	387	592	ps
LVCMOS33_out	Output Configured as LVCMOS 3.3V Buffer	116	395	553	ps
SSTL2_out	Output Configured as SSTL2 Buffer	-109	66	209	ps
SSTL3_out	Output Configured as SSTL3 Buffer	-97	78	242	ps
SSTL18_out_diff	Output Configured as SSTL18 Buffer (Differential)	-153	41	228	ps
HSTL_out_diff	Output Configured as HSTL Buffer (Differential)	-4	180	402	ps
eHSTL_out_diff	Output Configured as eHSTL Buffer (Differential)	-16	173	375	ps
SSTL_out_diff	Output Configured as SSTL2 Buffer (Differential)	-146	83	305	ps
LVDS_out	Output Configured as LVDS Buffer	0	0	0	ps
LVPECL_out	Output Configured as LVPECL Buffer	-187	-17	57	ps
t_{IOS} Output Slew Rate Adders[1]					
Slew_1	Output Slew_1 (Fastest)	—	0	—	ps
Slew_2	Output Slew_2	—	330	—	ps
Slew_3	Output Slew_3	—	660	—	ps
Slew_4	Output Slew_4 (Slowest)	—	1320	—	ps

1. Measured under standard output load conditions. See Figures 1-3-1-5.
2. All input adders referenced to LVCMOS33.
3. All output adders referenced to LVDS.

Output Rise and Fall Times – Typical Values[1, 2]

Output Type	Slew 1 (Fastest)		Slew 2		Slew 3		Slew 4 (Slowest)		Units
	t_R	t_F	t_R	t_F	t_R	t_F	t_R	t_F	
LVTTL	0.54	0.76	0.60	0.87	0.78	1.26	1.05	1.88	ns
LVCMOS 1.8V	0.75	0.69	0.88	0.78	0.83	1.11	1.20	1.68	ns
LVCMOS 2.5V	0.57	0.69	0.65	0.78	0.99	0.98	1.65	1.51	ns
LVCMOS 3.3V	0.55	0.77	0.60	0.87	0.78	1.26	1.05	1.88	ns
SSTL18	0.55	0.40	—	—	—	—	—	—	ns
SSTL2	0.50	0.40	—	—	—	—	—	—	ns
SSTL3	0.50	0.45	—	—	—	—	—	—	ns
HSTL	0.60	0.45	—	—	—	—	—	—	ns
eHSTL	0.55	0.40	—	—	—	—	—	—	ns
LVDS[3]	0.25	0.20	—	—	—	—	—	—	ns
LVPECL[3]	0.20	0.20	—	—	—	—	—	—	ns

1. See Figures 1-3-1-5 for test conditions.
2. Measured between 20% and 80% points.
3. Only the 'fastest' slew rate is available in LVDS and LVPECL modes.

Output Test Loads

Figures 1-3-1-5 show the equivalent termination loads used to measure rise/fall times, output timing adders and other selected parameters as noted in the various tables of this data sheet.

Figure 1-3. CMOS Termination Load

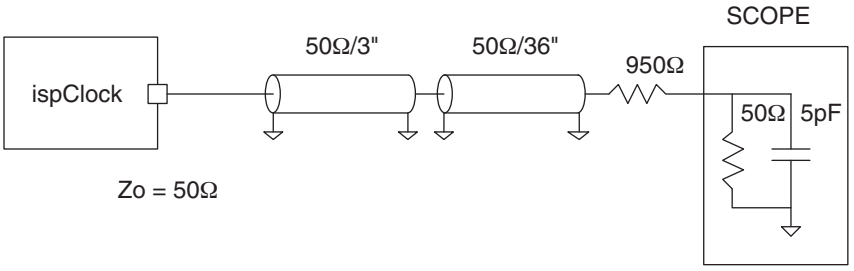


Figure 1-4. eHSTL/HSTL/SSTL Termination Load

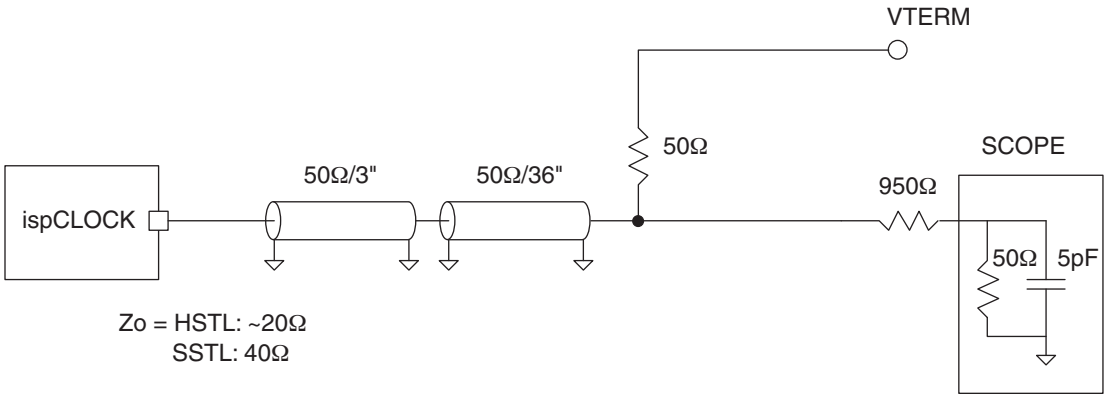


Figure 1-5. LVDS/LVPECL Termination Load

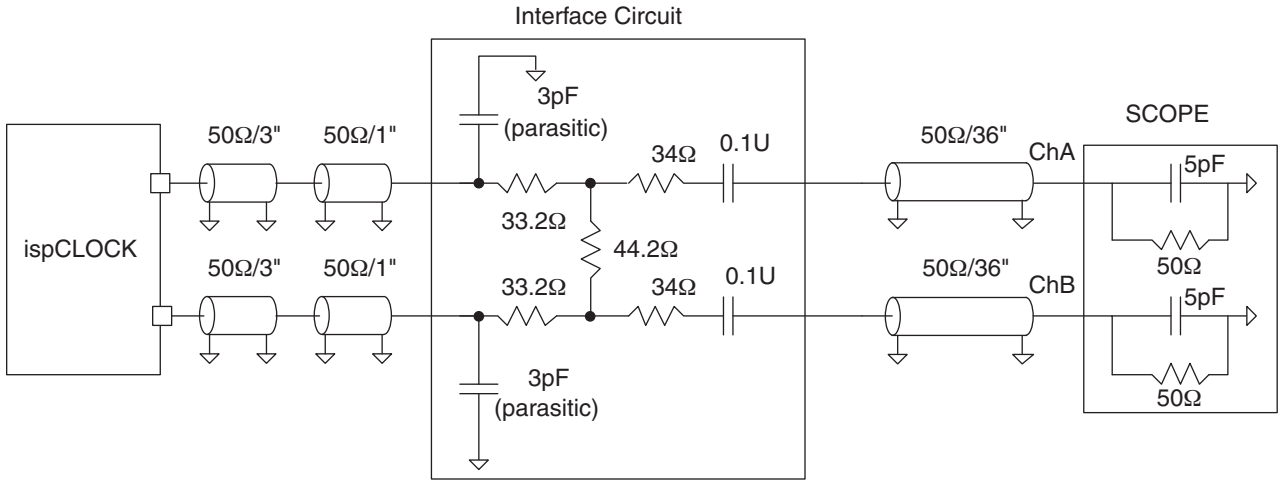
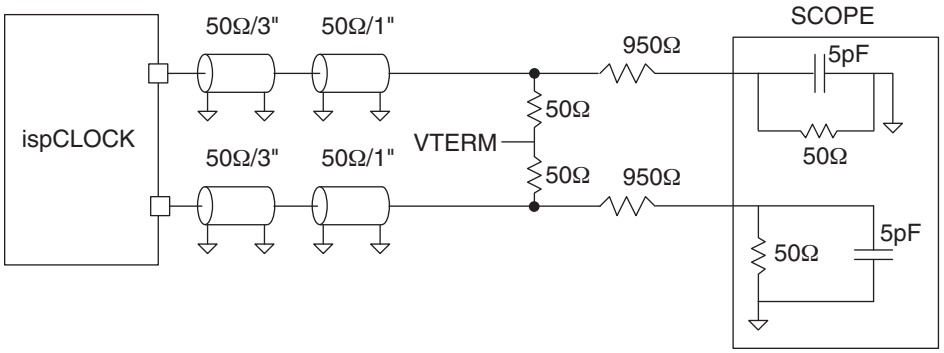


Figure 1-6. Differential HSTL/SSTL Termination Load



Programmable Input and Output Termination Characteristics

Symbol	Parameter	Conditions	V_{CCO} Voltage	Min.	Typ.	Max.	Units
R_{IN}	Input Resistance	Rin=40Ω setting		36	—	44	Ω
		Rin=45Ω setting		40.5	—	49.5	
		Rin=50Ω setting		45	—	55	
		Rin=55Ω setting		49.5	—	60.5	
		Rin=60Ω setting		54	—	66	
		Rin=65Ω setting		59	—	71.5	
		Rin=70Ω setting		61	—	77	
R_{OUT}	Output Resistance[1]	Rout≈20Ω setting	VCCO=3.3V	—	15	—	Ω
			VCCO=2.5V	—	15	—	
			VCCO=1.8V	—	16	—	
			VCCO=1.5V	—	14	—	
		Rout≈40Ω setting	VCCO=3.3V	-9%	40	9%	
			VCCO=2.5V	-11%	40	11%	
			VCCO=1.8V	-13%	41	13%	
		Rout≈45Ω setting	VCCO=3.3V	-10%	45	10%	
			VCCO=2.5V	-12%	45	12%	
			VCCO=1.8V	-14%	48	14%	
		Rout≈50Ω setting	VCCO=3.3V	-8%	50	8%	
			VCCO=2.5V	-9%	50	9%	
			VCCO=1.8V	-13%	54	13%	
		Rout≈55Ω setting	VCCO=3.3V	-9%	55	9%	
			VCCO=2.5V	-11%	55	11%	
			VCCO=1.8V	-13%	59	13%	
		Rout≈60Ω setting	VCCO=3.3V	-8%	59	8%	
			VCCO=2.5V	-9%	59	9%	
			VCCO=1.8V	-14%	63	14%	
		Rout≈65Ω setting	VCCO=3.3V	-8%	65	8%	
			VCCO=2.5V	-9%	64	9%	
			VCCO=1.8V	-13%	69	13%	
		Rout≈70Ω setting	VCCO=3.3V	-9%	72	9%	
			VCCO=2.5V	-10%	70	10%	
			VCCO=1.8V	-12%	74	12%	

1. Guaranteed by characterization.

Performance Characteristics – PLL

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
f_{REF}, f_{FBK}	Reference and feedback input frequency range			8		400	MHz
$t_{CLOCKHI}$, $t_{CLOCKLO}$	Reference and feedback input clock HIGH and LOW times	M-Divider and N-Divider not bypassed.		1.25			ns
t_{RINP}, t_{FINP}	Reference and feedback input rise and fall times	Measured between 20% and 80% levels				5	ns
M_{DIV}	M-divider range			1		40	
N_{DIV}	N-Divider range			1		40	
f_{PFD}	Phase detector input frequency range[2]			8		400	MHz
f_{VCO}	VCO operating frequency			320		800	MHz
V_{DIV}	Output Divider range	Even integer values only		2		80	
f_{OUT}	Output frequency range[1]	Fine Skew Mode, f_{VCO} = 800MHz	All differential options	4		400	MHz
			All single-ended options	4		266	MHz
		Coarse Skew Mode, f_{VCO} = 800MHz		2.5		200	MHz
t_{JIT} (cc)	Output adjacent-cycle jitter[6] (1000 cycle sample)	f_{PFD} ≥ 100MHz				70	ps (p-p)
t_{JIT} (per)	Output period jitter[6] (10000 cycle sample)	f_{PFD} ≥ 100MHz				12	ps (RMS)
$t_{JIT(\phi)}$	Reference clock to output jitter[6] (2000 cycle sample)	f_{PFD} ≥ 100MHz				50	ps (RMS)
$t\phi$	Static phase offset[5]			-100		200	ps
t_{DELAY}	Reference clock to output delay	Internal feedback mode[4]			2.25		ns
DC	Output duty cycle	Output type LVCMOS 3.3V[3] f_{OUT} >100 MHz		45		55	%
$t_{PDBY-PASS}$	Reference clock to output propagation delay	M=1, V=2	Input: LVPECL Output: LVPECL	6.2		8.8	ns
			Input: LVCMOS Output: LVCMOS	6		8.25	ns
t_{LOCK}	PLL lock time	From Power-up event			150		µs
		From Reset event			15		µs
t_{RELOCK}	PLL relock time	To same reference frequency			15		µs
		To different frequency			150		µs
PSR	Power supply rejection, period jitter vs. power supply noise	$f_{IN} = f_{OUT}$ = 100MHz $V_{CCA} = V_{CCD} = V_{CCO}$ modulated with 100kHz sinusoidal stimulus			0.05		$\frac{ps(RMS)}{mV(p-p)}$

1. In PLL Bypass mode (PLL_BYPASS = HIGH), output will support frequencies down to 0Hz (divider chain is a fully static design).
2. Dividers should be set so that they provide the phase detector with signals of 8MHz or greater for loop stability.
3. See Figures 1-3-1-5 for output loads.
4. Input and outputs LVPECL mode
5. Inserted feedback loop delay < 7ns
6. Measured with f_{OUT} = 100MHz, f_{VCO} = 600MHz, input and output interface set to LVPECL.

Timing Specifications

Skew Matching

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{SKEW}	Output-output Skew	Between any two identically configured and loaded outputs regardless of bank.	—	—	50	ps

Programmable Skew Control

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{SKRANGE}$	Skew Control Range[1]	Fine Skew Mode, f_{VCO} = 320 MHz	—	5.86	—	ns
		Fine Skew Mode, f_{VCO} = 800 MHz	—	2.34	—	
		Coarse Skew Mode, f_{VCO} = 320 MHz	—	11.72	—	
		Coarse Skew Mode, f_{VCO} = 800 MHz	—	4.68	—	
SK_{STEPS}	Skew Steps per range		—	16	—	
t_{SKSTEP}	Skew Step Size[2]	Fine Skew Mode, f_{VCO} = 320 MHz	—	390	—	ps
		Fine Skew Mode, f_{VCO} = 800 MHz	—	156	—	
		Coarse Skew Mode, f_{VCO} = 320 MHz	—	780	—	
		Coarse Skew Mode, f_{VCO} = 800 MHz	—	312	—	
t_{SKERR}	Skew Time Error[3]	Fine skew mode	—	30	—	ps
		Coarse skew mode	—	50	—	

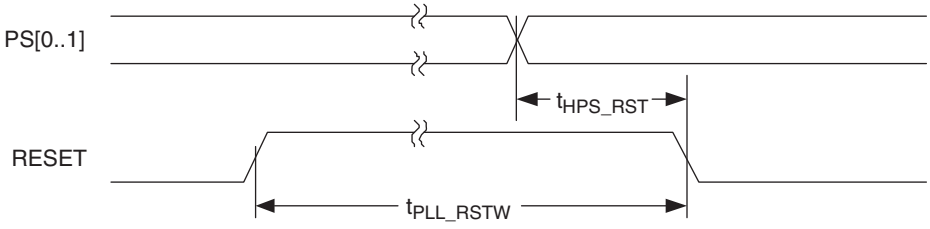
1. Skew control range is a function of VCO frequency (f_{VCO}). In fine skew mode $T_{SKRANGE} = 15/(8 \times f_{VCO})$. In coarse skew mode $T_{SKRANGE} = 15/(4 \times f_{VCO})$.
2. Skew step size is a function of VCO frequency (f_{VCO}). In fine skew mode $T_{SKSTEP} = 1/(8 \times f_{VCO})$. In coarse skew mode $T_{SKSTEP} = 1/(4 \times f_{VCO})$.
3. Only applicable to outputs with non-zero skew settings.

Control Functions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{DIS/OE}$	Delay Time, $\overline{OEX}$ or $\overline{OEY}$ to Output Disabled/ Enabled		—	10	20	ns
$t_{DIS/GOE}$	Delay Time, $\overline{GOE}$ to Output Disabled/Enabled		—	10	20	ns
$t_{SUSGATE}$	Setup Time, SGATE to Output Clock Start/ Stop		3	—	—	cycles[1]
t_{PLL_RSTW}	PLL Reset Pulse Width[2]		1	—	—	ms
t_{RSTW}	Logic Reset Pulse Width[3]		20	—	—	ns
t_{HPS_RST}	Hold time for RESET past change in PS[0..1]		20	—	—	ns

1. Output clock cycles for the particular output being controlled.
2. Will completely reset PLL.
3. Will only reset digital logic.

Figure 1-7. RESET and Profile Select Timing



Timing Specifications (Cont.)

Boundary Scan Logic

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK (BSCAN Test) Clock Cycle	40	—	ns
t_{BTCH}	TCK (BSCAN Test) Pulse Width High	20	—	ns
t_{BTCL}	TCK (BSCAN Test) Pulse Width Low	20	—	ns
t_{BTSU}	TCK (BSCAN Test) Setup Time	8	—	ns
t_{BTH}	TCK (BSCAN Test) Hold Time	10	—	ns
t_{BRF}	TCK (BSCAN Test) Rise and Fall Rate	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	10	ns
t_{BTOZ}	TAP Controller Falling Edge of Clock to Data Output Disable	—	10	ns
t_{BTVO}	TAP Controller Falling Edge of Clock to Data Output Enable	—	10	ns
$t_{BVTCPSU}$	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCPH}	BSCAN Test Capture Register Hold Time	10	—	ns
t_{BTUCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	25	ns
t_{BTUOZ}	BSCAN Test Update Register, Falling Edge of Clock to Output Disable	—	25	ns
t_{BTUOV}	BSCAN Test Update Register, Falling Edge of Clock to Output Enable	—	25	ns

JTAG Interface and Programming Mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum TCK Clock Frequency		—	—	25	MHz
t_{CKH}	TCK Clock Pulse Width, High		20	—	—	ns
t_{CKL}	TCK Clock Pulse Width, Low		20	—	—	ns
t_{ISPEN}	Program Enable Delay Time		15	—	—	µs
t_{ISPDIS}	Program Disable Delay Time		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Program		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Erase		200	—	—	µs
t_{CEN}	Falling Edge of TCK to TDO Active		—	—	15	ns
t_{CDIS}	Falling Edge of TCK to TDO Disable		—	—	15	ns
t_{SU1}	Setup Time		8	—	—	ns
t_{H}	Hold Time		10	—	—	ns
t_{CO}	Falling Edge of TCK to Valid Output		—	—	15	ns
t_{PWV}	Verify Pulse Width		30	—	—	µs
t_{PWP}	Programming Pulse Width		20	—	—	ms
t_{BEW}	Bulk Erase Pulse Width		200	—	—	ms

Timing Diagrams

Figure 1-8. Erase (User Erase or Erase All) Timing Diagram

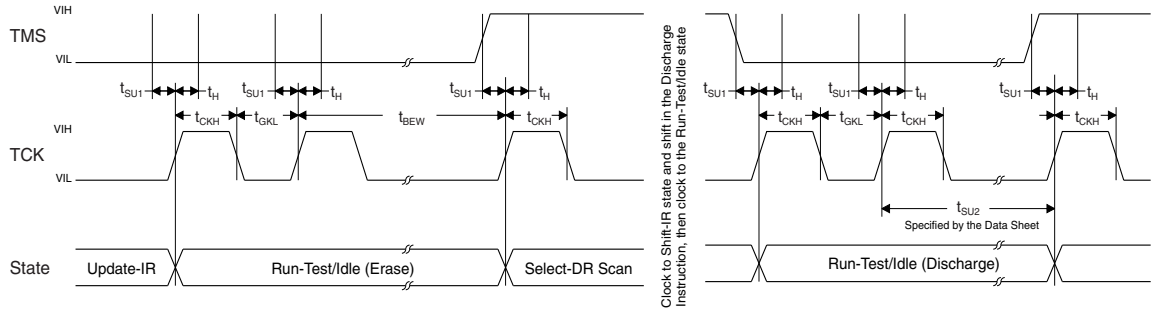


Figure 1-9. Programming Timing Diagram

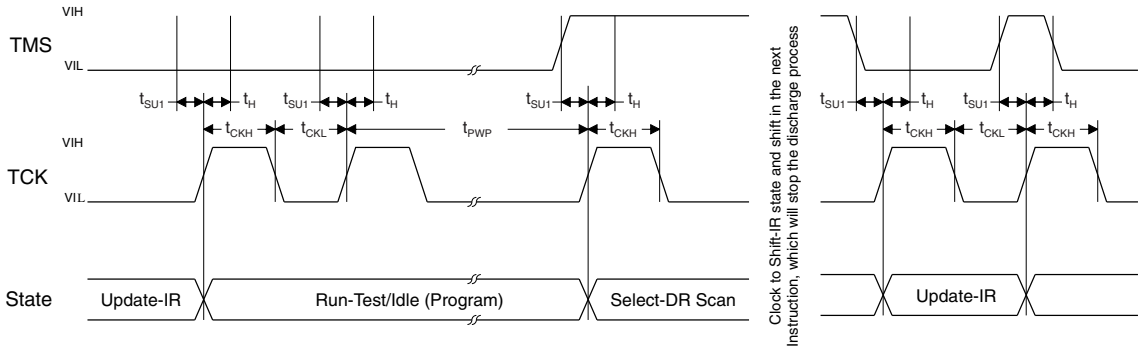


Figure 1-10. Verify Timing Diagram

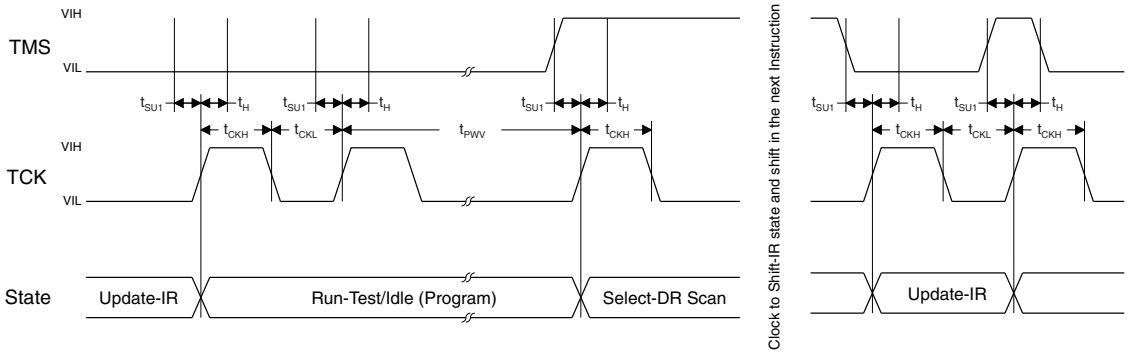
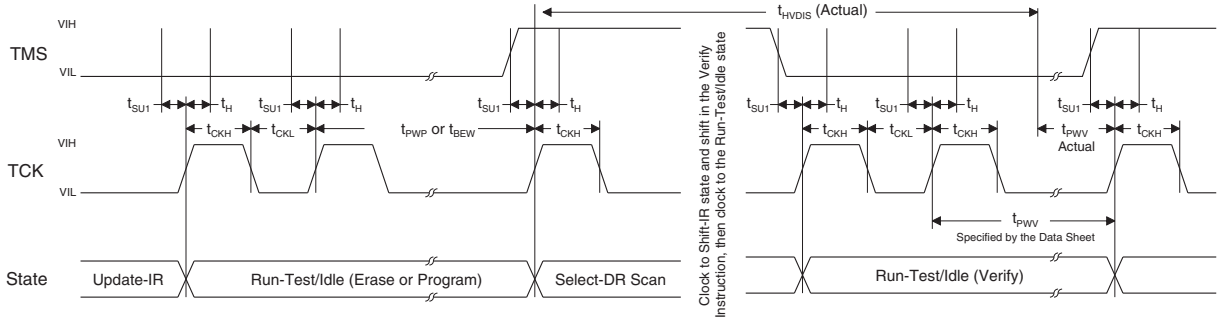
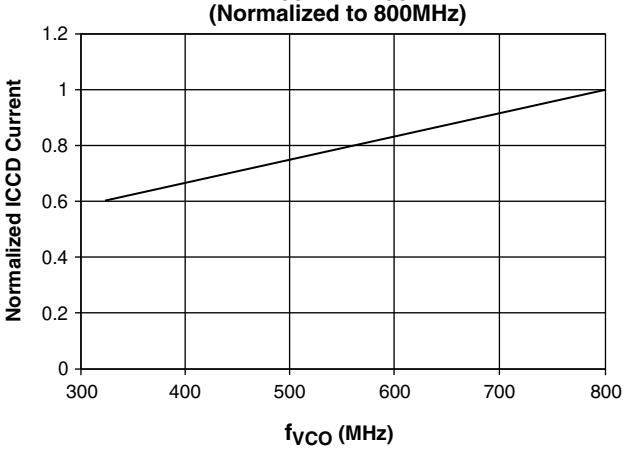


Figure 1-11. Discharge Timing Diagram

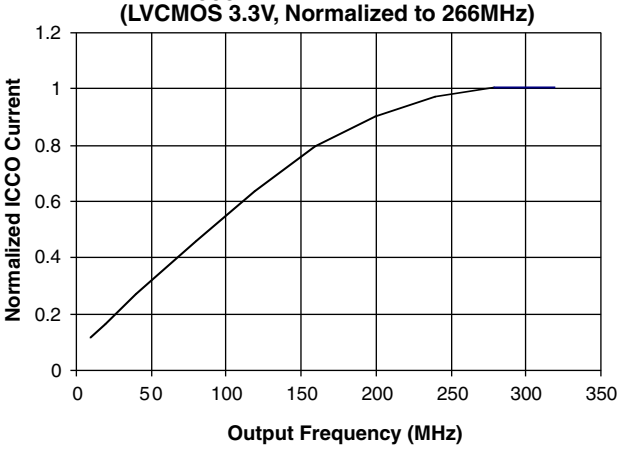


Typical Performance Characteristics

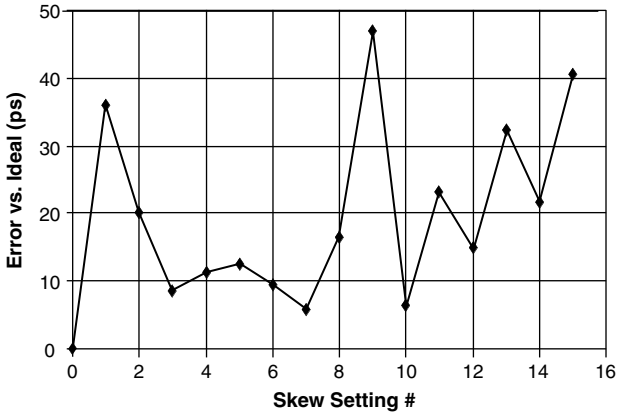
I_{CCD} vs. f_{VCO} (Normalized to 800MHz)



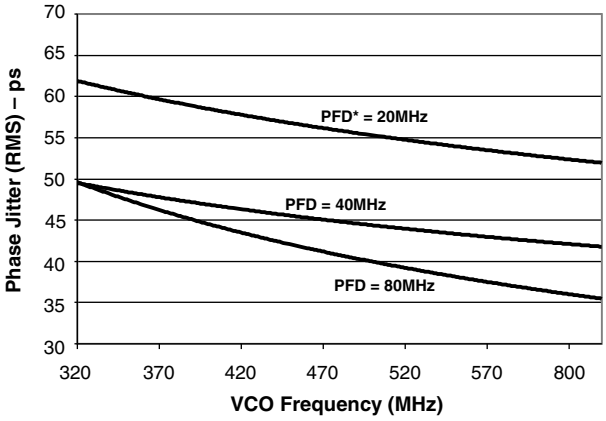
I_{CCO} vs. Output Frequency (LVCMOS 3.3V, Normalized to 266MHz)



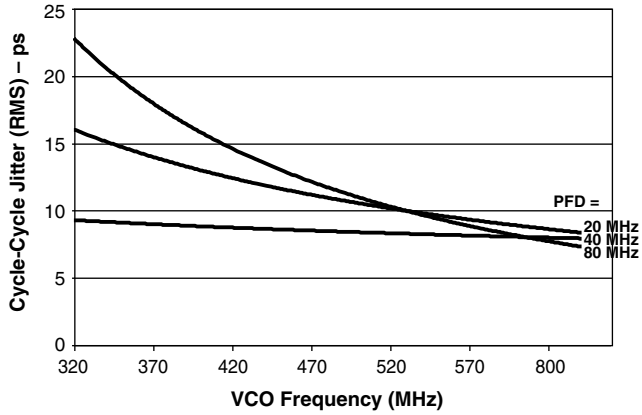
Typical Skew Error vs. Setting (Skew Mode = FINE, f_{VCO} = 800MHz)



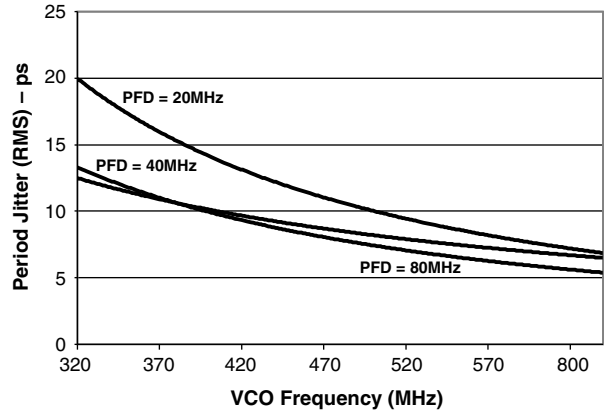
Phase Jitter vs. VCO Frequency V=4



Cycle-Cycle Jitter vs. VCO Frequency V=4

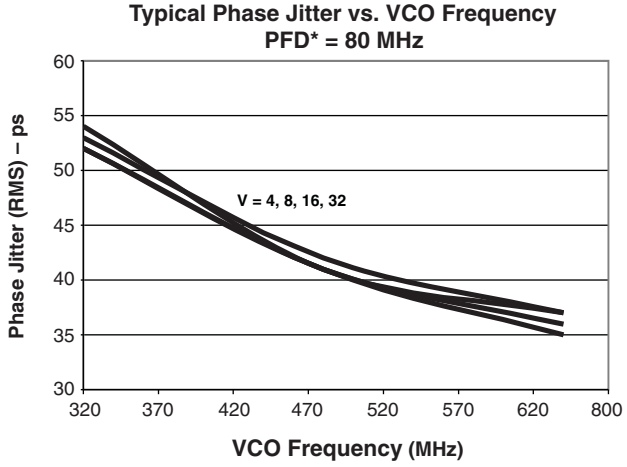


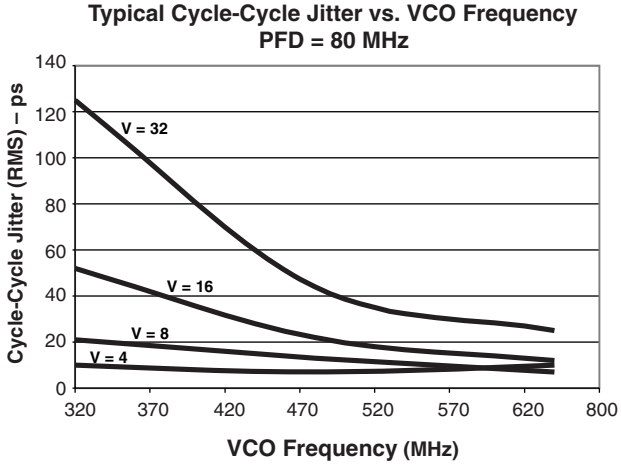
Period Jitter vs. VCO Frequency V=4

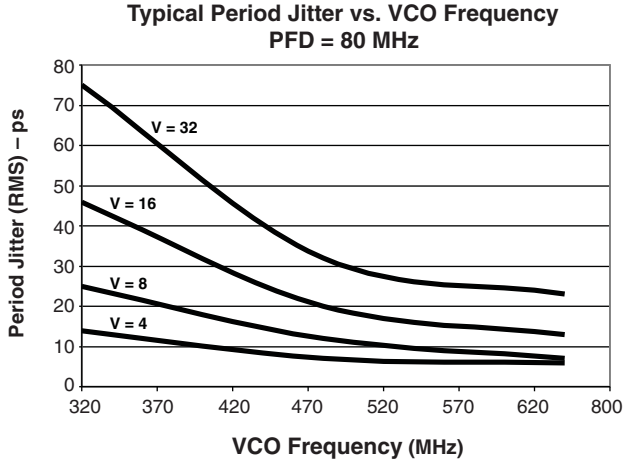


*PFD = Phase/Frequency Detector

Typical Performance Characteristics (Cont.)







*PFD = Phase/Frequency Detector

Detailed Description

PLL Subsystem

The ispClock5600A provides an integral phase-locked-loop (PLL) which may be used to generate output clock signals at lower, higher, or the same frequency as a user-supplied input reference signal. The core functions of the PLL are an edge-sensitive phase detector, a programmable loop filter, and a high-speed voltage-controlled oscillator (VCO). Additionally, a set of programmable input, output and feedback dividers (M, N, V[1..5]) is provided to support the synthesis of different output frequencies.

Phase/Frequency Detector

The ispClock5600A provides an edge-sensitive phase/frequency detector (PFD), which means that the device will function properly over a wide range of input clock reference duty cycles. It is only necessary that the input reference clock meet specified minimum HIGH and LOW times ($t_{CLOCKHI,}$ $t_{CLOCKLO}$) for it to be properly recognized by the PFD. The PFD's output is of a classical charge-pump type, outputting charge packets which are then integrated by the PLL's loop filter.

A lock-detection feature is also associated with the PFD. When the ispClock5600A is in a LOCKED state, the LOCK output pin goes LOW. The lock detector has two operating modes: Phase Lock Detect mode and Frequency

Lock Detect mode. In Phase Lock Detect mode, the LOCK signal is asserted if the phases of the reference and feedback signals match, whereas in Frequency Lock Detect mode the LOCK signal is asserted when the frequencies of the feedback and reference signals match. The option for which mode to use is programmable and may be set using PAC-Designer software (available from the Lattice website at www.latticesemi.com).

In Phase Lock Detect mode the lock detector asserts the LOCK signal as soon as a lock condition is determined.

In Frequency Lock Detect mode, however, the PLL must be in a locked condition for a set number of phase detector cycles before the LOCK signal will be asserted. The number of cycles required before asserting the LOCK signal in frequency-lock mode can be set from 16 to 256.

When the lock condition is lost the LOCK signal will be de-asserted immediately in both Phase Lock Detect and Frequency Lock Detect modes.

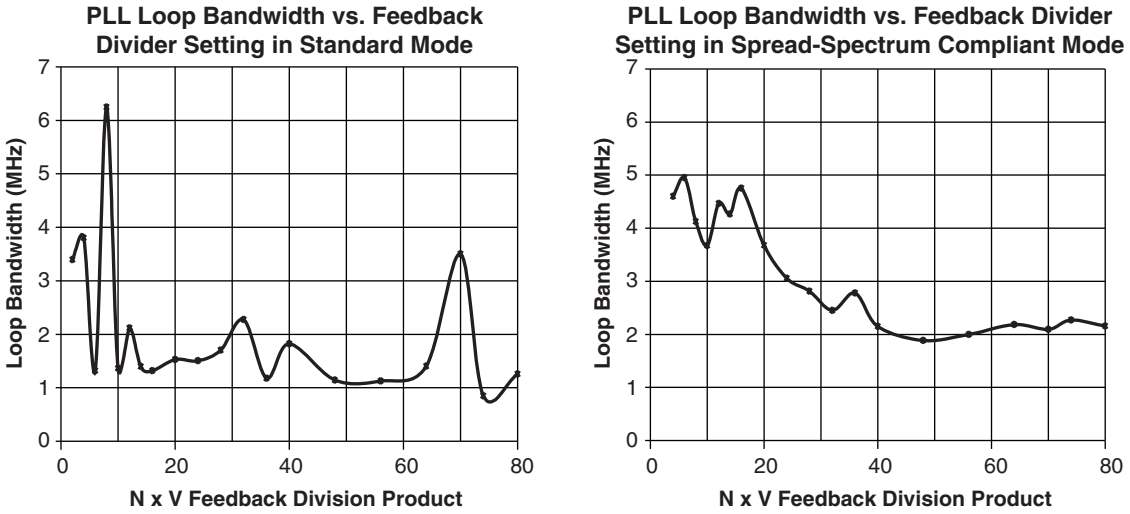
Loop Filter: The loop filter parameters for each profile are automatically selected by the PAC-Designer software depending on the following:

- Individual profile VCO operating frequency
- Individual profile NxV product
- Maximum VCO operating frequency across all used profiles

Spread Spectrum Support: The reference clock inputs of the ispClock5600A device are spread spectrum clock tolerant. The tolerance limits are:

- Center spread ±0.125% to ±2%
- Down spread -0.25% to -4%
- 30-33kHz modulation frequency

Figure 1-12. PLL Loop Bandwidth vs. Feedback Divider Setting (Nominal)



VCO

The ispClock5600A provides an internal VCO which provides an output frequency ranging from 320MHz to 800MHz. The VCO is implemented using differential circuit design techniques which minimize the influence of power supply noise on measured output jitter. The VCO is also used to generate output clock skew as a function of the total VCO period. Using the VCO as the basis for controlling output skew allows for highly precise and consistent skew generation, both from device-to-device, as well as channel-to-channel within the same device.

M-, N-, and V-Dividers

The ispClock5600A incorporates a set of programmable dividers which provide the ability to synthesize output frequencies differing from that of the reference clock input.

The input, or M-Divider prescales the input reference frequency, and can be programmed with integer values over the range of 1 to 40. To achieve low levels of output jitter, it is best to use the smallest M-Divider value possible.

The feedback, or N-Divider prescales the feedback frequency and like the M-Divider, can also be programmed with integer values ranging from 1 to 40.

Each one of the five output, or V-Dividers can be independently programmed to provide even division ratios ranging from 2 to 80.

When the PLL is selected (PLL_BYPASS=LOW) and locked, the output frequency of each V-Divider (f_k) may be calculated as:

$$f_k = f_{ref} \frac{N \times V_{fbk}}{M \times V_k} \quad (1)$$

where

f_k is the frequency of V-Divider k
f_{ref} is the input reference frequency
M and N are the input and feedback divider settings
V_{fbk} is the setting of the V-Divider used to close the PLL feedback path
V_k is the setting of the V-Divider used to provide output k

Note that because the feedback may be taken from any V-Divider, V_k and V_{fbk} may refer to the same divider.

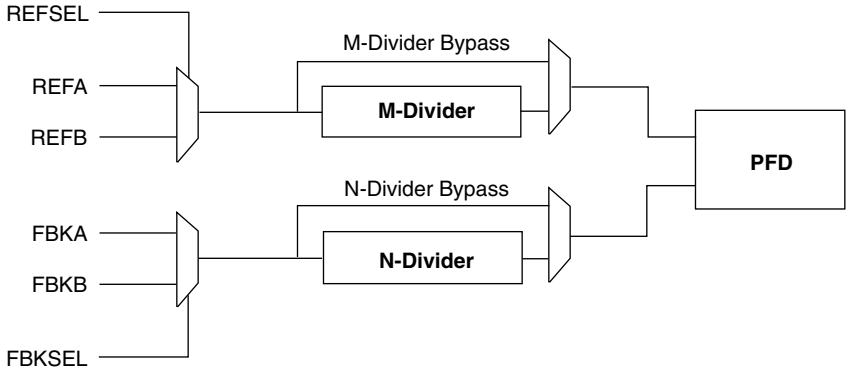
Because the VCO has an operating frequency range spanning 320 MHz to 800 MHz, and the V-Dividers provide division ratios from 2 to 80, the ispClock5600A can generate output signals ranging from 5 MHz to 400 MHz. For performance and stability reasons, however, there are several constraints which should be followed when selecting divider values:

- Use the smallest feasible value for the M-Divider
  - The output frequency from the M (and N) divider should be greater or equal to 8 MHz.
- The product of the N-Divider and the V-Divider used to close the PLL's feedback loop should be less than or equal to 80 ($N \times V_{fbk} \leq 80$)

M-Divider and N-Divider Bypass Mode

The M-Divider and the N-Divider in the ispClock5600A device can be bypassed using PAC-Designer software. M and N-Dividers should be bypassed in applications that require glitchless switching between reference and feedback clocks. However, the frequencies of these clocks should be close. If M and N-Dividers are not bypassed, one should ensure that $t_{CLOCKHI}$ and $t_{CLOCKLO}$ specifications are not violated. Otherwise, activation of the reset signal is necessary to ensure reliable switchover.

Figure 1-13. M-Divider and N-Divider Bypass Mode



Note: Bypassing M- and N-Dividers also results in reducing the number of output frequency combinations generated from a single reference clock input.

PLL_BYPASS Mode

The PLL_BYPASS mode is provided so that input reference signals can be coupled through to the outputs without using the PLL functions. When PLL_BYPASS mode is enabled (PLL_BYPASS=HIGH), the output of the M-Divider is routed directly to the inputs of the V-Dividers. In PLL_BYPASS mode, the nominal values of the V-Dividers are halved, so that they provide division ratios ranging from 1 to 40. The output frequency for a given V-Divider (f_k) will be determined by

$$f_k = \frac{f_{ref} \times 2}{M \times V_k} \quad (2)$$

Please note that PLL_BYPASS mode is provided primarily for testing purposes. When PLL_BYPASS mode is enabled, features such as lock detect and skew generation are unavailable.

Reference and External Feedback Inputs

The ispClock5600A provides sets of configurable, internally-terminated inputs for both clock reference and feedback signals. In normal operation, one of the clock reference input pairs (REFA+/- or REFB+/-) is used as a clock input.

The external feedback inputs make it possible to compensate for input to output delay through external means. This makes it possible to provide output clocks which have very low skews in relation to the reference clock regardless of loading effects.

The ispClock5610A provides one input signal pair for reference input and one input pair for external feedback, while the ispClock5620A provides two pairs for reference signals and two pairs for feedback. To select between reference and feedback inputs, the ispClock5620A provides two CMOS-compatible digital inputs called REFSEL and FBKSEL. Table 1-2 shows the behavior of these two control inputs.

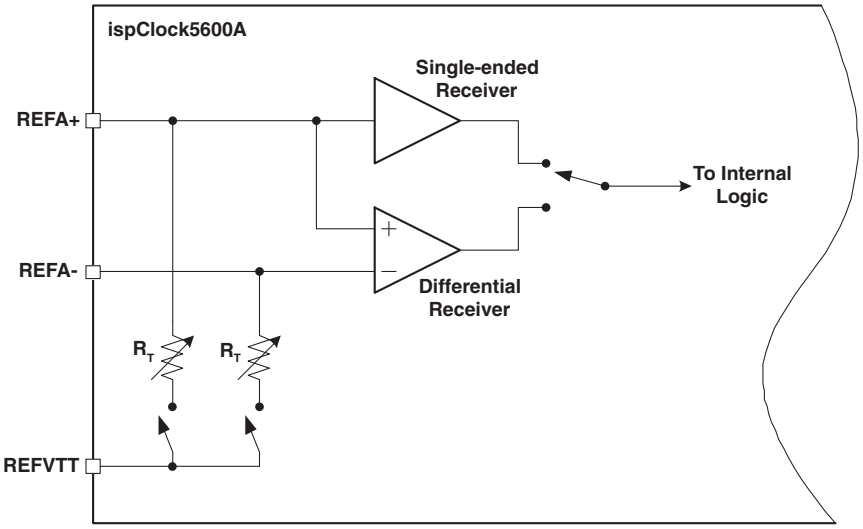
Table 1-2. REFSEL and FBKSEL Operation for ispClock5620A

REFSEL	Selected Input Pair	FBKSEL	Selected Input Pair
0	REFA+/-	0	FBKA+/-
1	REFB+/-	1	FBKB+/-

- LVTTL (3.3V)
- LVCMOS (1.8V, 2.5V, 3.3V)
- SSTL2
- SSTL3
- HSTL
- eHSTL
- Differential SSTL1.8
- Differential SSTL2
- Differential SSTL3
- Differential HSTL
- LVDS
- LVPECL (differential, 3.3V)

Each input also features internal programmable termination resistors, as shown in Figure 1-14. Note that all reference inputs (REFA+, REFA-, REFB+, REFB-) terminate to the REFVTT pin, while all feedback inputs (FBKA+, FBKA-, FBKB+, FBKB-) terminate to the FBKVTT pin.

Figure 1-14. ispClock5600A Clock Reference and Feedback Input Structure (REFA+/- Pair Shown)

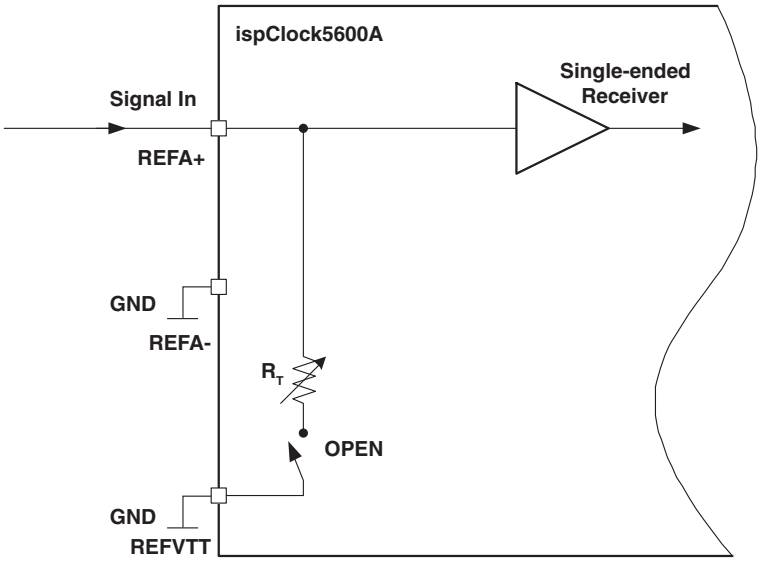


The following usage guidelines are suggested for interfacing to supported logic families.

LVTTL (3.3V), LVCMOS (1.8V, 2.5V, 3.3V)

The receiver should be set to LVCMOS or LVTTL mode, and the input signal should be connected to the '+' terminal of the input pair (e.g. REFA+). The '-' input terminal should be connected to GND. In addition, REFVTT should also be tied to GND. CMOS transmission lines are generally source terminated, so all termination resistors should be set to the OPEN state. Figure 1-15 shows the proper configuration. Please note that because switching thresholds are different for LVCMOS running at 1.8V, there is a separate configuration setting for this particular standard.

Figure 1-15. LVCMOS/LVTTL Input Receiver Configuration



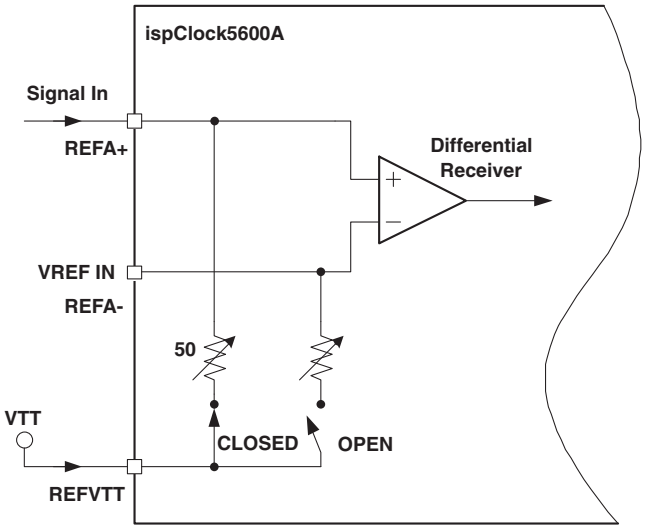
HSTL, eHSTL, SSTL2, SSTL3

The receiver should be set to HSTL/SSTL mode, and the input signal should be fed into the '+' terminal of the input pair. The '-' input terminal should be tied to the appropriate V_{REF} value, and the associated REFVTT or FBKVTT terminal should be tied to a V_{TT} termination supply. The positive input's terminating resistor should be engaged and set to 50Ω. Figure 1-16 shows an appropriate configuration. Refer to the "Recommended Operating Conditions - Supported Logic Standards" table in this data sheet for suitable values of V_{REF} and $V_{TT.}$ If one of the REF or FBK

pairs is not used, tie the unused pins REF+ and REF- to GND. In addition, if external feedback is not used, tied FBVTT to GND.

One important point to note is that the termination supplies must have low impedance and be able to both source and sink current without experiencing fluctuations. These requirements generally preclude the use of a resistive divider network, which has an impedance comparable to the resistors used, or of commodity-type linear voltage regulators, which can only source current. The best way to develop the necessary termination voltages is with a regulator specifically designed for this purpose. Because SSTL and HSTL logic is commonly used for high-performance memory busses, a suitable termination voltage supply is often already available in the system.

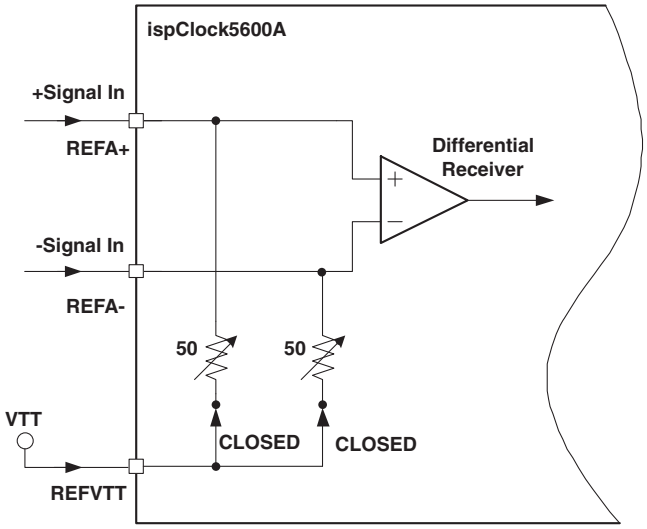
Figure 1-16. SSTL2, SSTL3, eHSTL, HSTL Receiver Configuration



Differential HSTL and SSTL

HSTL and SSTL are sometimes used in a differential form, especially for distributing clocks in high-speed memory systems. Figure 1-17 shows how ispClock5600A reference input should be configured for accepting these standards. The major difference between differential and single-ended forms of these logic standards is that in the differential case, the REFA- input is used as a signal input, not a reference level, and that both terminating resistors are engaged and set to 50Ω. If one of the REF or FBK pairs is not used, tie the unused REF+ and REF- pins to GND. If external feedback is not used, tie FBVTT to GND as well.

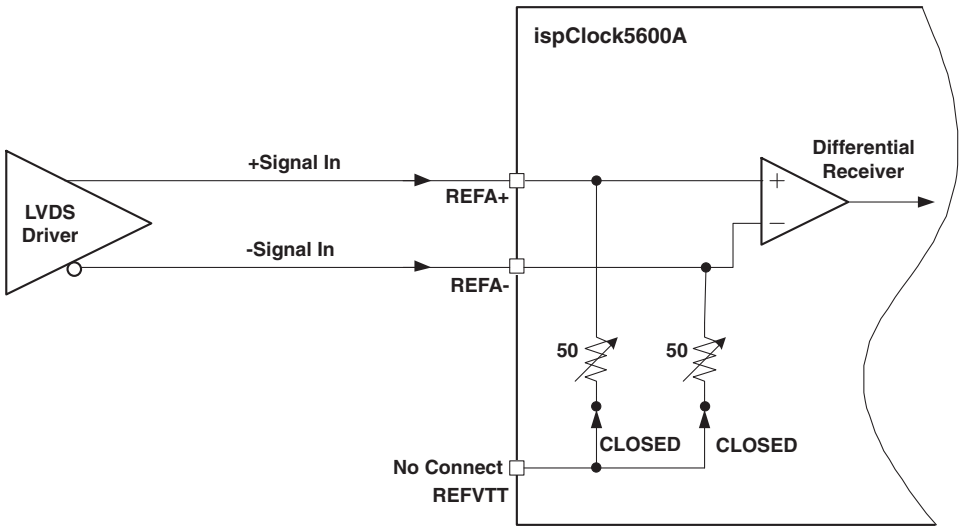
Figure 1-17. Differential HSTL/SSTL Receiver Configuration



LVDS/Differential LVPECL

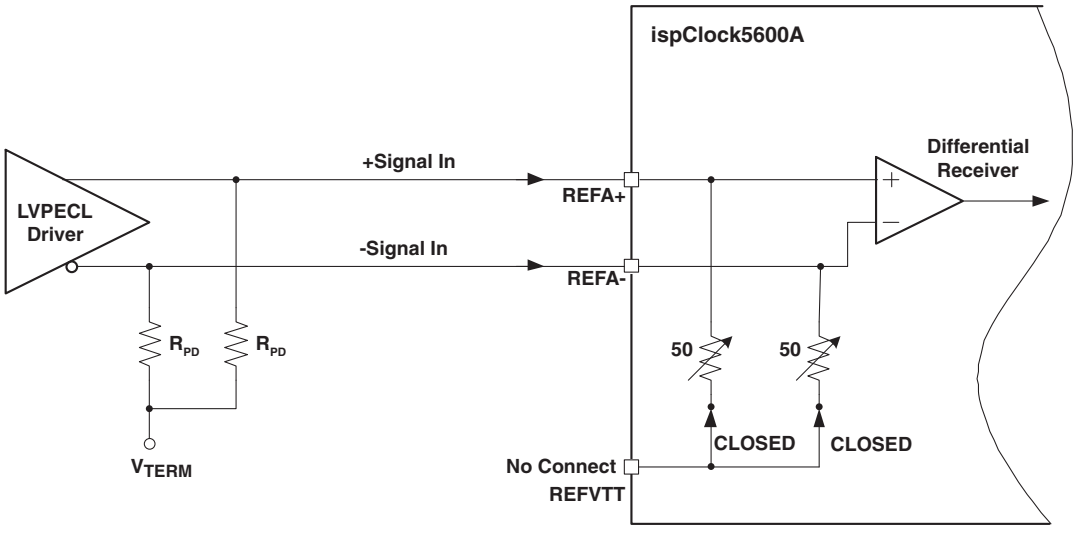
The receiver should be set to LVDS or LVPECL mode as required and both termination resistors should be engaged and set to 50Ω. The associated REFVTT or FBKVTT pin, however, should be left unconnected. This creates a floating 100Ω differential termination resistance across the input terminals. The LVDS termination configuration is shown in Figure 1-18.

Figure 1-18. LVDS Input Receiver Configuration



Note that while a floating 100Ω resistor forms a complete termination for an LVDS signal line, additional circuitry may be required to satisfactorily terminate a differential LVPECL signal. This is because a true bipolar LVPECL output driver typically requires an external DC 'pull-down' path to a V_{TERM} termination voltage (typically VCC-2V) to properly bias its open emitter output stage. When interfacing to an LVPECL input signal, the ispClock5600A's internal termination resistors should not be used for this pull-down function, as they may be damaged from excessive current. The pull-down should be implemented with external resistors placed close to the LVPECL driver (Figure 1-19)

Figure 1-19. LVPECL Input Receiver Configuration



Please note that while the above discussions specify using 50Ω termination impedances, the actual impedance required to properly terminate the transmission line and maintain good signal integrity may vary from this ideal. The

actual impedance required will be a function of the driver used to generate the signal and the transmission medium used (PCB traces, connectors and cabling). The ispClock5600A's ability to adjust input impedance over a range of 40Ω to 70Ω allows the user to adapt his circuit to non-ideal behaviors from the rest of the system without having to swap out components.

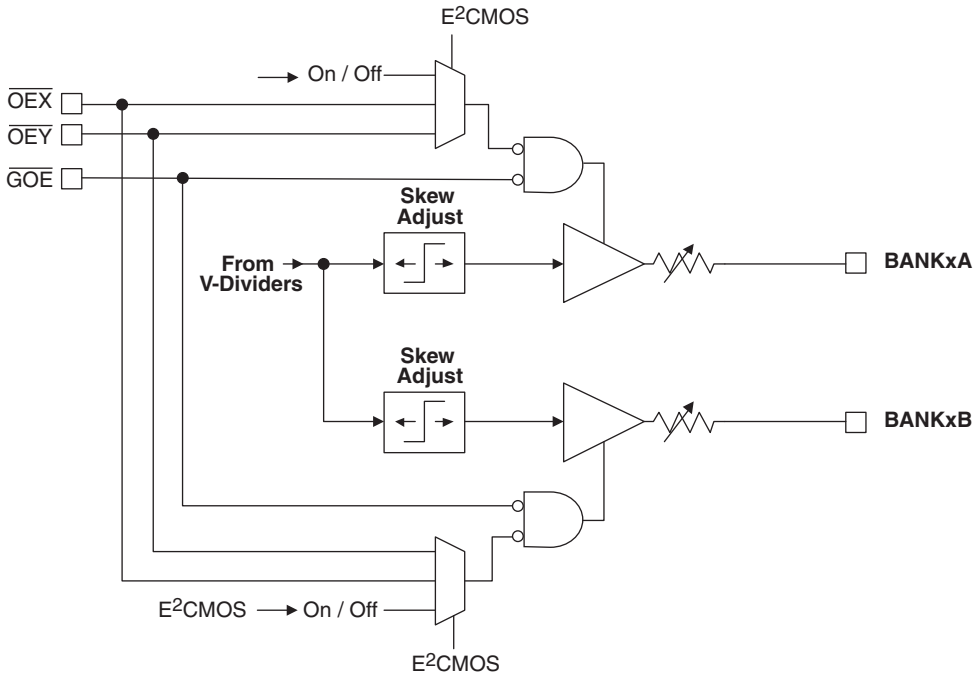
Output Drivers

The ispClock5600A provide banks of configurable, internally-terminated high-speed dual-output line drivers. The ispClock5610A provides five driver banks, while the ispClock5620A provides ten. Each of these driver banks may be configured to provide either a single differential output signal, or a pair of single-ended output signals. Programmable internal source-series termination allows the ispClock5600A to be matched to transmission lines with impedances ranging from 40 to 70 Ohms. The outputs may be independently enabled or disabled, either from E^2CMOS configuration or by external control lines. Additionally, each can be independently programmed to provide a fixed amount of signal delay or skew, allowing the user to compensate for the effects of unequal PCB trace lengths or loading effects. Figure 1-20 shows a block diagram of a typical ispClock5600A output driver bank and associated skew control.

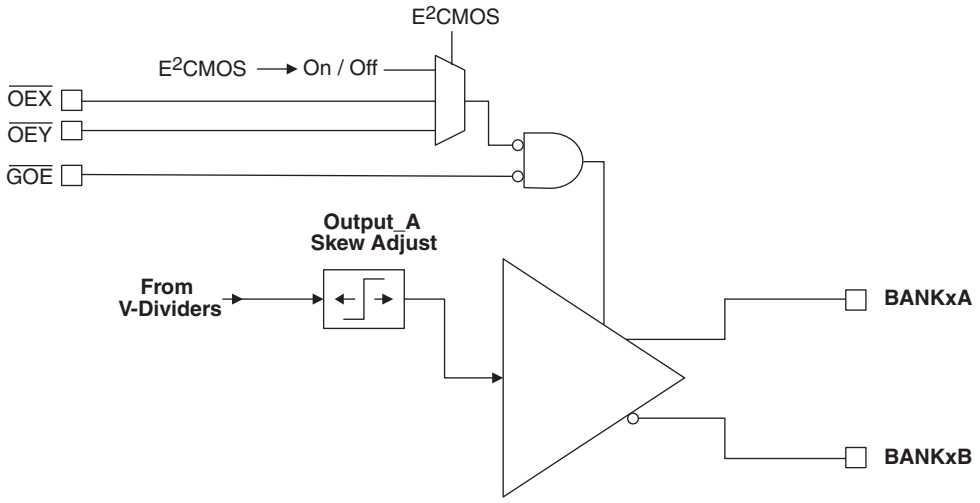
Because of the high edge rates which can be generated by the ispClock5600A's clock output drivers, the VCCO power supply pin for each output bank should be individually bypassed. Low ESR capacitors with values ranging from 0.01 to 0.1 µF may be used for this purpose. Each bypass capacitor should be placed as close to its respective output bank power pins (VCCO and GNDO) pins as is possible to minimize interconnect length and associated parasitic inductances.

In the case where an output bank is unused, the associated VCCO pin may be either left floating or tied to ground to reduce quiescent power consumption. We recommend, however, that all unused VCCO pins be tied to ground where possible. All GND0 pins must be tied to ground, regardless of whether or not the associated bank is used.

Figure 1-20. ispClock5600A Output Driver and Skew Control



(a) Single-ended Configuration Output Driver and Skew Control



(b) Differential Configuration Output Driver and Skew Control