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## Features

### ■ 10MHz to 320MHz Input/Output Operation

### ■ Low Output to Output Skew (<50ps)

### ■ Low Jitter Peak-to-Peak (<60ps)

### ■ Up to 20 Programmable Fan-out Buffers

- Programmable output standards and individual enable controls
  - LVTTTL, LVCMOS, HSTL, SSTL, LVDS, LVPECL
- Programmable output impedance
  - 40 to 70Ω in 5Ω increments
- Programmable slew rate
- Up to 10 banks with individual V<sub>CCO</sub> and GND
  - 1.5V, 1.8V, 2.5V, 3.3V

### ■ Fully Integrated High-Performance PLL

- Programmable lock detect
- Multiply and divide ratio controlled by
  - Input divider (5 bits)
  - Feedback divider (5 bits)
  - Five output dividers (5 bits)
- Programmable On-chip Loop Filter

### ■ Precision Programmable Phase Adjustment (Skew) Per Output

- 16 settings; minimum step size 195ps
  - Locked to VCO frequency

- Up to +/- 12ns skew range
- Coarse and fine adjustment modes

### ■ Up to Five Clock Frequency Domains

### ■ Flexible Clock Reference and External Feedback Inputs

- Programmable input standards
  - LVTTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL
- Clock A/B selection multiplexer
- Feedback A/B selection multiplexer
- Programmable termination

### ■ Four User-programmable Profiles Stored in E<sup>2</sup>CMOS<sup>®</sup> Memory

- Supports both test and multiple operating configurations

### ■ Full JTAG Boundary Scan Test In-System Programming Support

### ■ Exceptional Power Supply Noise Immunity

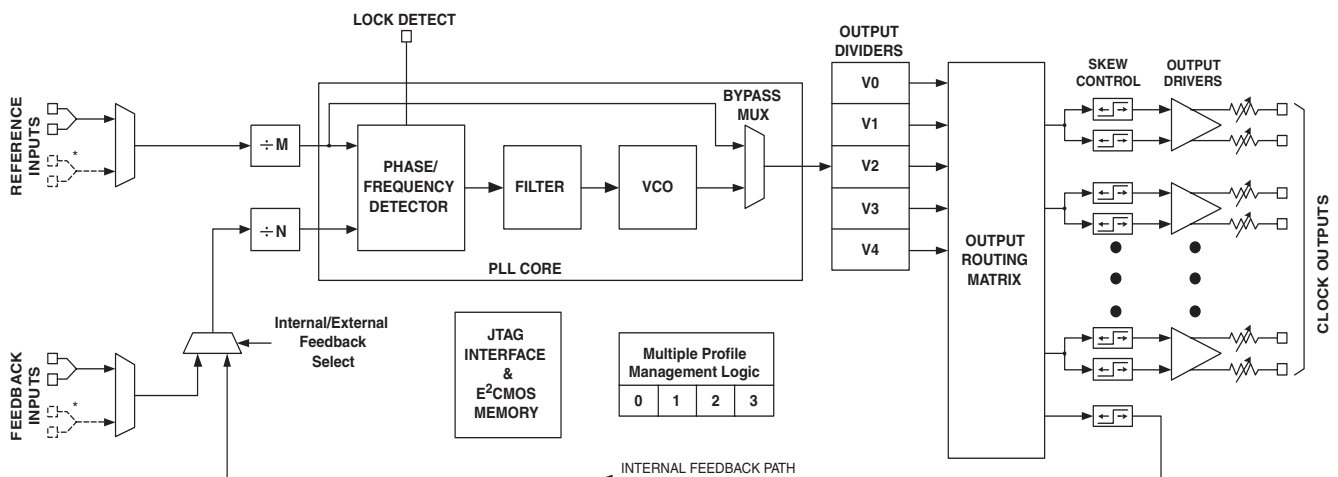
### ■ Commercial (0 to 70°C) and Industrial (-40 to 85°C) Temperature Ranges

### ■ 100-pin and 48-pin TQFP Packages

### ■ Applications

- Circuit board common clock generation and distribution
- PLL-based frequency generation
- High fan-out clock buffer
- Zero-delay clock buffer

## Product Family Block Diagram



\* Input Available only on ispClock5620

## General Description and Overview

The ispClock5610 and ispClock5620 are in-system-programmable high-fanout PLL-based clock drivers designed for use in high performance communications and computing applications. The ispClock5610 provides up to 10 single-ended or five differential clock outputs, while the ispClock5620 provides up to 20 single-ended or 10 differential clock outputs. Each pair of outputs may be independently configured to support separate I/O standards (LVDS, LVPECL, LVTTTL, LVCMOS, SSTL, HSTL) and output frequency. In addition, each output provides independent programmable control of termination, slew-rate, and timing skew. All configuration information is stored on-chip in non-volatile E<sup>2</sup>CMOS memory.

The ispClock5600's PLL and divider systems supports the synthesis of clock frequencies differing from that of the reference input through the provision of programmable input and feedback dividers. A set of five post-PLL V-dividers provides additional flexibility by supporting the generation of five separate output frequencies. Loop feedback may be taken internally from the output of any of the five V-dividers, or externally through FBKA+/- or FBKB+/- pins.

The core functions of all members of the ispClock5600 family are identical, the differences between devices being restricted to the number of inputs and outputs, as shown in the following table. Figures 1 and 2 show functional block diagrams of the ispClock5610 and ispClock5620.

**Table 1. ispClock5600 Family Members**

Device	Ref. Input Pairs	Feedback Input Pairs	Clock Outputs
ispClock5610	1	1	10
ispClock5620	2	2	20

**Figure 1. ispClock5610 Functional Block Diagram**

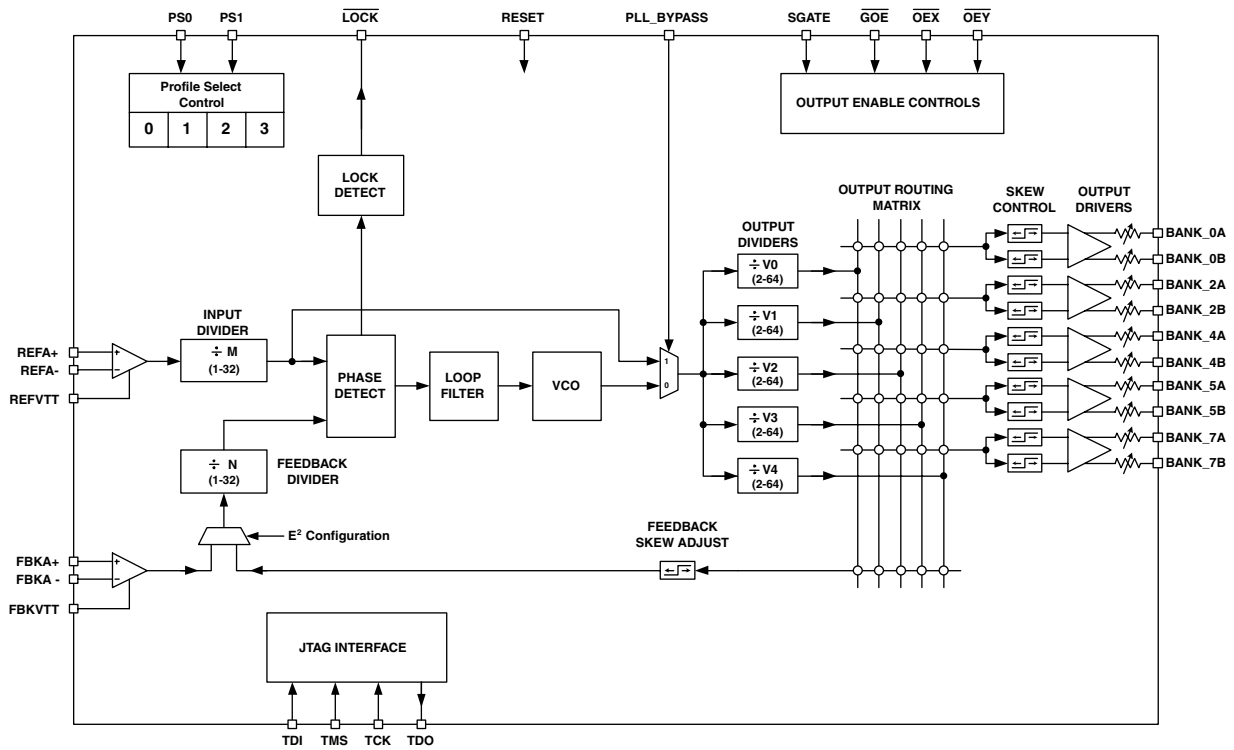
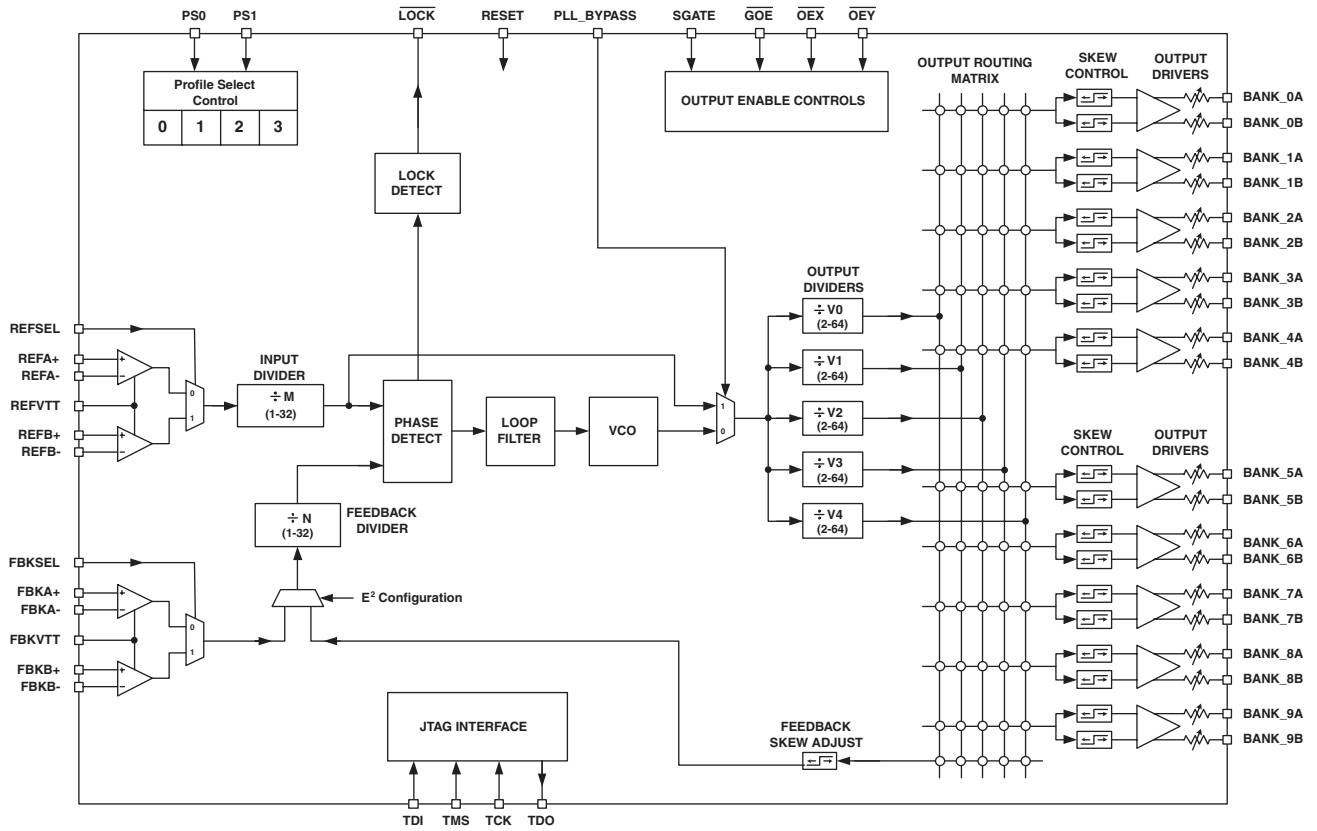




Figure 2. ispClock5620 Functional Block Diagram



## Absolute Maximum Ratings

### ispClock5600V

Core Supply Voltage $V_{CCD}$	-0.5 to 5.5V
PLL Supply Voltage $V_{CCA}$	-0.5 to 5.5V
JTAG Supply Voltage $V_{CCJ}$	-0.5 to 5.5V
Output Driver Supply Voltage $V_{CCO}$	-0.5 to 4.5V
Input Voltage	-0.5 to 4.5V
Output Voltage <sup>1</sup>	-0.5 to 4.5V
Storage Temperature	-65 to 150°C
Junction Temperature with power supplied	-40 to 130°C

1. When applied to an output when in high-Z condition

## Recommended Operating Conditions

Symbol	Parameter	Conditions	ispClock5600V		Units
			Min.	Max.	
$V_{CCD}$	Core Supply Voltage		3.0	3.6	V
$V_{CCJ}$	JTAG I/O Supply Voltage		1.62	3.6	V
$V_{CCA}$	Analog Supply Voltage		3.0	3.6	V
$V_{CCXSLEW}$	$V_{CC}$ Turn-on Ramp Rate	All supply pins	—	0.33	V/ $\mu$ s
$T_{JOP}$	Operating Junction Temperature	Commercial	0	100	°C
		Industrial	-40	115	
$T_A$	Ambient Operating Temperature	Commercial	0	70 <sup>1</sup>	°C
		Industrial	-40	85 <sup>1</sup>	

1. Device power dissipation may also limit maximum ambient operating temperature.

## Recommended Operating Conditions – $V_{CCO}$ vs. Logic Standard

Logic Standard	$V_{CCO}$ (V)			$V_{REF}$ (V)			$V_{TT}$ (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTTL	3.0	3.3	3.6	—	—	—	—	—	—
LVC MOS 1.8V	1.71	1.8	1.89	—	—	—	—	—	—
LVC MOS 2.5V	2.375	2.5	2.625	—	—	—	—	—	—
LVC MOS 3.3V	3.0	3.3	3.6	—	—	—	—	—	—
SSTL2 Class 1	2.375	2.5	2.625	1.15	1.25	1.35	$V_{REF} - 0.04$	—	$V_{REF} + 0.04$
SSTL3 Class 1	3.0	3.3	3.6	1.30	1.50	1.70	$V_{REF} - 0.05$	$V_{REF}$	$V_{REF} + 0.05$
HSTL Class 1	1.425	1.5	1.575	0.68	0.75	0.90	—	$0.5 \times V_{CCO}$	—
LVPECL (Differential)	3.0V	3.3V	3.6V	—	—	—	—	—	—
LVDS	$V_{CCO} = 2.5V$	2.375	2.5V	2.625	—	—	—	—	—
	$V_{CCO} = 3.3V$	3.0	3.3	3.6	—	—	—	—	—

Note: ‘—’ denotes  $V_{REF}$  or  $V_{TT}$  not applicable to this logic standard

## E<sup>2</sup>CMOS Memory Write/Erase Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Erase/Reprogram Cycles		1000	—	—	

## Performance Characteristics – Power Supply

Symbol	Parameter	Conditions	Typ.	Max.	Units
I <sub>CCD</sub>	Core Supply Current	ispClock5610 f <sub>VCO</sub> = 640MHz	110	120	mA
		ispClock5620 f <sub>VCO</sub> = 640MHz	150	160	mA
I <sub>CCA</sub>	Analog Supply Current	f <sub>VCO</sub> = 640MHz	5.5	7	mA
I <sub>CCO</sub>	Output Driver Supply Current (per Bank)	V <sub>CCO</sub> = 1.8V <sup>1</sup> , LVCMOS	13	15	mA
		V <sub>CCO</sub> = 2.5V <sup>1</sup> , LVCMOS	18	24	
		V <sub>CCO</sub> = 3.3V <sup>1</sup> , LVCMOS	24	35	
		V <sub>CCO</sub> = 3.3V <sup>2</sup> , LVDS	7.5	8	
I <sub>CCJ</sub>	JTAG I/O Supply Current (static)	V <sub>CCJ</sub> = 1.8V	200	300	μA
		V <sub>CCJ</sub> = 2.5V	300	400	
		V <sub>CCJ</sub> = 3.3V	300	400	

1. Supply current consumed by each bank, both outputs active, 18pF load, 320MHz output frequency.

2. Supply current consumed by each bank, 100Ω, 5pf differential load, 320MHz output frequency.

## DC Electrical Characteristics – Single-ended Logic

Logic Standard	V <sub>IL</sub> (V)		V <sub>IH</sub> (V)		V <sub>OL</sub> Max. (V)	V <sub>OH</sub> Min. (V)	I <sub>OL</sub> (mA)	I <sub>OH</sub> (mA)
	Min.	Max.	Min.	Max.				
LVTTL/LVCMOS 3.3V	-0.3	0.8	2	3.6	0.4	V <sub>CCO</sub> - 0.4	4 <sup>1</sup>	-4 <sup>1</sup>
LVCMOS 1.8V	-0.3	0.68	1.07	3.6	0.4	V <sub>CCO</sub> - 0.4	4 <sup>1</sup>	-4 <sup>1</sup>
LVCMOS 2.5V	-0.3	0.7	1.7	3.6	0.4	V <sub>CCO</sub> - 0.4	4 <sup>1</sup>	-4 <sup>1</sup>
SSTL2 Class 1	-0.3	V <sub>REF</sub> - 0.18	V <sub>REF</sub> + 0.18	3.6	0.54 <sup>2</sup>	V <sub>CCO</sub> - 0.81 <sup>2</sup>	7.6	-7.6
SSTL3 Class 1	-0.3	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	3.6	0.9 <sup>2</sup>	V <sub>CCO</sub> - 1.3 <sup>2</sup>	8	-8
HSTL Class 1	-0.3	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	3.6	0.4 <sup>3</sup>	V <sub>CCO</sub> - 0.4 <sup>3</sup>	8	-8

1. Specified for 50Ω internal series output termination.

2. Specified for 40Ω internal series output termination.

3. Specified for ≈20Ω internal series output termination.

## DC Electrical Characteristics – LVDS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V <sub>ICM</sub>	Common Mode Input Voltage	V <sub>THD</sub> ≤ 100mV	V <sub>THD</sub> /2	—	2.0	V
		V <sub>THD</sub> ≤ 150mV	V <sub>THD</sub> /2	—	2.325	V
V <sub>THD</sub>	Differential Input Threshold		±100	—	—	mV
V <sub>IN</sub>	Input Voltage		0	—	2.4	V
V <sub>OH</sub>	Output High Voltage	R <sub>T</sub> = 100Ω	—	1.375	1.60	V
V <sub>OL</sub>	Output Low Voltage	R <sub>T</sub> = 100Ω	0.9	1.03	—	V
V <sub>OD</sub>	Output Voltage Differential	R <sub>T</sub> = 100Ω	250	400	480	mV
ΔV <sub>OD</sub>	Change in V <sub>OD</sub> between H and L		—	—	50	mV
V <sub>OS</sub>	Output Voltage Offset	Common Mode Output Voltage	1.125	1.20	1.375	V
ΔV <sub>OS</sub>	Change in V <sub>OS</sub> Between H and L		—	—	50	mV
I <sub>SA</sub>	Output Short Circuit Current	V <sub>OD</sub> = 0V, Outputs Shorted to GND	—	—	24	mA
I <sub>SAB</sub>	Output Short Circuit Current	V <sub>OD</sub> = 0V, Outputs Shorted to Each Other	—	—	12	mA

### DC Electrical Characteristics – Differential LVPECL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>IH</sub>	Input Voltage High	V <sub>CCD</sub> = 3.0 to 3.6V	V <sub>CCD</sub> - 1.17	—	V <sub>CCD</sub> - 0.88	V
		V <sub>CCD</sub> = 3.3V	2.14	—	2.42	
V <sub>IL</sub>	Input Voltage Low	V <sub>CCD</sub> = 3.0 to 3.6V	V <sub>CCD</sub> - 1.81	—	V <sub>CCD</sub> - 1.48	V
		V <sub>CCD</sub> = 3.3V	1.49	—	1.83	
V <sub>OH</sub>	Output High Voltage <sup>1</sup>	V <sub>CCO</sub> = 3.0 to 3.6V	V <sub>CCO</sub> - 1.07	—	V <sub>CCO</sub> - 0.88	V
		V <sub>CCO</sub> = 3.3V	2.23	—	2.42	
V <sub>OL</sub>	Output Low Voltage <sup>1</sup>	V <sub>CCO</sub> = 3.0 to 3.6V	V <sub>CCO</sub> - 1.81	—	V <sub>CCO</sub> - 1.62	V
		V <sub>CCO</sub> = 3.3V	1.49	—	1.68	

1. 100Ω differential termination.

### DC Electrical Characteristics – Input/Output Loading

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I <sub>LK</sub>	Input Leakage	Note 1	—	—	±10	μA
I <sub>PU</sub>	Input Pull-up Current	Note 2	—	80	120	μA
I <sub>PD</sub>	Input Pull-down Current	Note 3	—	120	150	μA
I <sub>OLK</sub>	Tristate Leakage Output	Note 4	—	—	±10	μA
C <sub>IN</sub>	Input Capacitance	Notes 2, 3, 5	—	8	10	pF
		Note 6	—	13.5	15	pF

- 1. Applies to clock reference inputs when termination 'open'.
- 2. Applies to TDI, TMS inputs.
- 3. Applies to REFSEL, PS0, PS1,  $\overline{\text{GOE}}$ , SGATE and PLL\_BYPASS.
- 4. Applies to all logic types when in tristated mode.
- 5. Applies to OEX, OEY, TCK, RESET inputs.
- 6. Applies to REFA+, REFA-, REFB+, REFB-, FBKA+, FBKA-, FBKB+, FBKB-.

### Switching Characteristics – Timing Adders for I/O Modes

Adder Type	Description	Min.	Typ.	Max.	Units
<b>t<sub>IOI</sub> Input Adders<sup>2</sup></b>					
LVTTTL_in	Using LVTTTL Standard	0	0	0	ns
LVC MOS18_in	Using LVC MOS 1.8V Standard	0.20	0.45	0.70	ns
LVC MOS25_in	Using LVC MOS 2.5V Standard	0	0	0	ns
LVC MOS33_in	Using LVC MOS 3.3V Standard	0	0	0	ns
SSTL2_in	Using SSTL2 Standard	1.15	1.35	1.60	ns
SSTL3_in	Using SSTL3 Standard	1.15	1.35	1.60	ns
HSTL_in	Using HSTL Standard	1.15	1.35	1.60	ns
LVDS_in	Using LVDS Standard	1.15	1.35	1.60	ns
LVPECL_in	Using LVPECL Standard	1.15	1.35	1.60	ns
<b>t<sub>IOO</sub> Output Adders<sup>1,3</sup></b>					
LVTTTL_out	Output Configured as LVTTTL Buffer	-0.10	0.15	0.45	ns
LVC MOS18_out	Output Configured as LVC MOS 1.8V Buffer	-0.15	0.15	0.55	ns
LVC MOS25_out	Output Configured as LVC MOS 2.5V Buffer	-0.10	0.15	0.45	ns
LVC MOS33_out	Output Configured as LVC MOS 3.3V Buffer	-0.10	0.15	0.45	ns
SSTL2_out	Output Configured as SSTL2 Buffer	-0.10	0.15	0.45	ns
SSTL3_out	Output Configured as SSTL3 Buffer	-0.10	0.15	0.45	ns
HSTL_out	Output Configured as HSTL Buffer	0	0.15	0.45	ns
LVDS_out	Output Configured as LVDS Buffer	0	0	0	ns
LVPECL_out	Output Configured as LVPECL Buffer	0	0	0	ns
<b>t<sub>IOS</sub> Output Slew Rate Adders<sup>1</sup></b>					
Slew_1	Output Slew_1 (Fastest)	—	0	—	ps
Slew_2	Output Slew_2	—	330	—	ps
Slew_3	Output Slew_3	—	660	—	ps
Slew_4	Output Slew_4 (Slowest)	—	1320	—	ps

1. Measured under standard output load conditions – see Figures 3-5.

2. All input adders referenced to LVTTTL.

3. All output adders referenced to LVPECL.

### Output Rise and Fall Times – Typical Values<sup>1,2</sup>

Output Type	Slew 1 (Fastest)		Slew 2		Slew 3		Slew 4 (Slowest)		Units
	t <sub>R</sub>	t <sub>F</sub>	t <sub>R</sub>	t <sub>F</sub>	t <sub>R</sub>	t <sub>F</sub>	t <sub>R</sub>	t <sub>F</sub>	
LVTTTL	0.65	0.45	0.85	0.60	1.20	0.90	1.75	1.30	ns
LVC MOS 1.8V	0.90	0.40	1.05	0.50	1.40	0.80	2.00	1.20	ns
LVC MOS 2.5V	0.70	0.40	0.90	0.55	1.20	0.85	1.80	1.20	ns
LVC MOS 3.3V	0.65	0.45	0.85	0.60	1.20	0.90	1.75	1.30	ns
SSTL2	0.65	0.40	0.90	0.60	1.35	0.85	2.30	1.40	ns
SSTL3	0.65	0.40	0.90	0.60	1.35	0.85	2.30	1.40	ns
HSTL	0.85	0.30	1.00	0.50	1.50	0.70	2.55	1.10	ns
LVDS <sup>3</sup>	0.25	0.20	—	—	—	—	—	—	ns
LVPECL <sup>3</sup>	0.20	0.20	—	—	—	—	—	—	ns

1. See Figures 3-5 for test conditions.

2. Measured between 20% and 80% points.

3. Only the 'fastest' slew rate is available in LVDS and LVPECL modes.



### Output Test Loads

Figures 3-5 show the equivalent termination loads used to measure rise/fall times, output timing adders and other selected parameters as noted in the various tables of this data sheet.

Figure 3. CMOS Termination Load

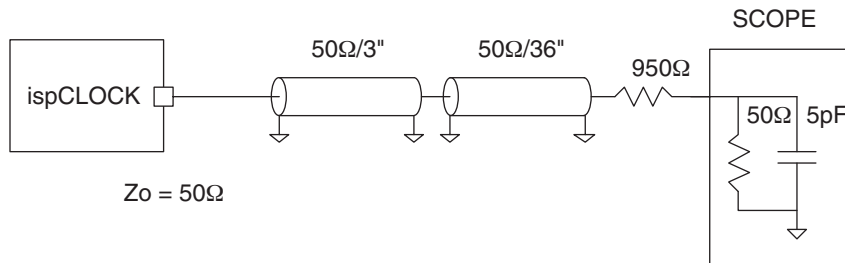


Figure 4. HSTL/SSTL Termination Load

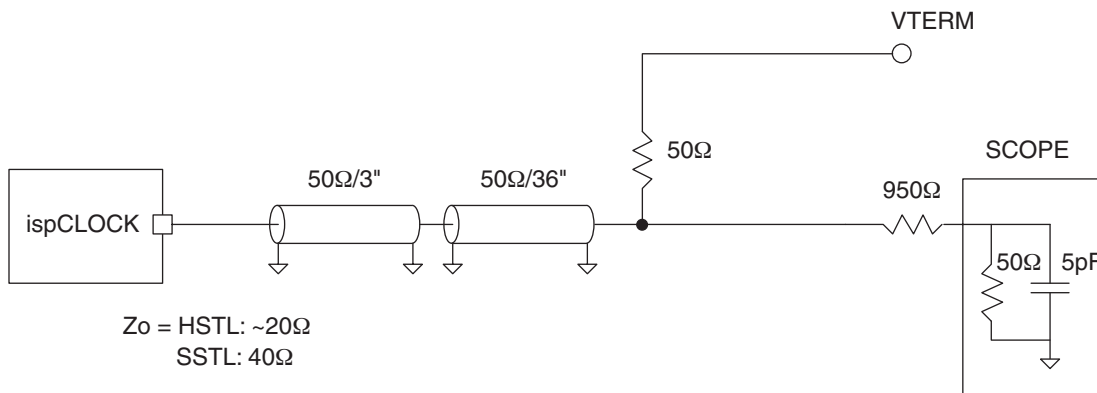
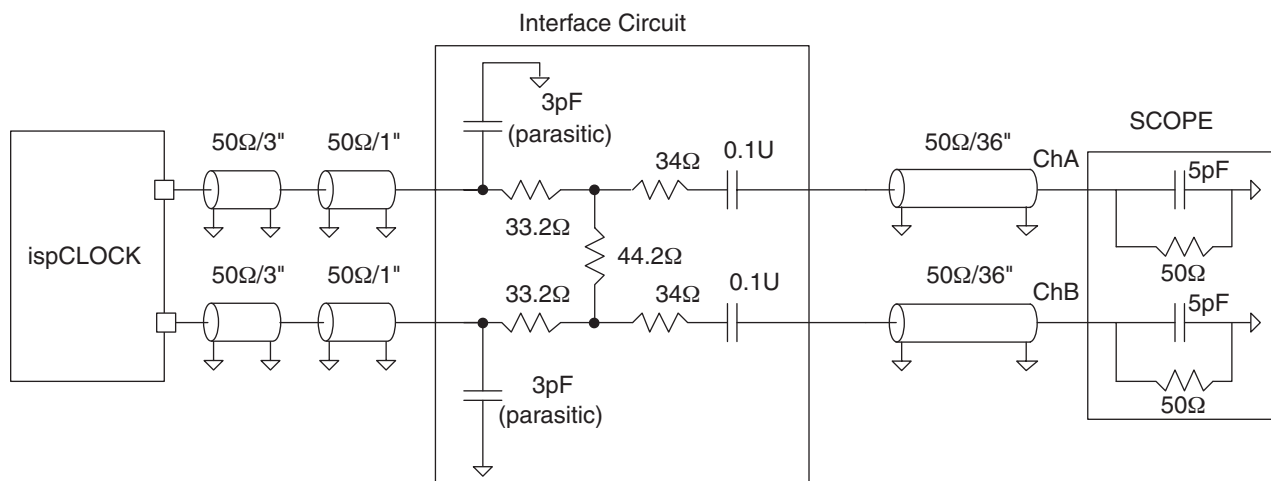


Figure 5. LVDS/LVPECL Termination Load



**Programmable Input and Output Termination Characteristics**

Symbol	Parameter	Conditions	V <sub>CCO</sub> Voltage	Min.	Typ.	Max.	Units
R <sub>IN</sub>	Input Resistance	R <sub>in</sub> =40Ω setting		36	—	44	Ω
		R <sub>in</sub> =45Ω setting		40.5	—	49.5	
		R <sub>in</sub> =50Ω setting		45	—	55	
		R <sub>in</sub> =55Ω setting		49.5	—	60.5	
		R <sub>in</sub> =60Ω setting		54	—	66	
		R <sub>in</sub> =65Ω setting		59	—	71.5	
		R <sub>in</sub> =70Ω setting		61	—	77	
R <sub>OUT</sub>	Output Resistance <sup>1</sup>	R <sub>out</sub> ≈20Ω setting	V <sub>CCO</sub> =3.3V	—	14	—	Ω
			V <sub>CCO</sub> =2.5V	—	14	—	
			V <sub>CCO</sub> =1.8V	—	14	—	
			V <sub>CCO</sub> =1.5V	—	14	—	
		R <sub>out</sub> ≈40Ω setting	V <sub>CCO</sub> =3.3V	-9%	38	9%	
			V <sub>CCO</sub> =2.5V	-11%	40	11%	
			V <sub>CCO</sub> =1.8V	-13%	40	13%	
		R <sub>out</sub> ≈45Ω setting	V <sub>CCO</sub> =3.3V	-10%	45	10%	
			V <sub>CCO</sub> =2.5V	-12%	45	12%	
			V <sub>CCO</sub> =1.8V	-14%	44	14%	
		R <sub>out</sub> ≈50Ω setting	V <sub>CCO</sub> =3.3V	-8%	50	8%	
			V <sub>CCO</sub> =2.5V	-9%	49	9%	
			V <sub>CCO</sub> =1.8V	-13%	49	13%	
		R <sub>out</sub> ≈55Ω setting	V <sub>CCO</sub> =3.3V	-9%	55	9%	
			V <sub>CCO</sub> =2.5V	-11%	55	11%	
			V <sub>CCO</sub> =1.8V	-13%	55	13%	
		R <sub>out</sub> ≈60Ω setting	V <sub>CCO</sub> =3.3V	-8%	59	8%	
			V <sub>CCO</sub> =2.5V	-9%	59	9%	
			V <sub>CCO</sub> =1.8V	-14%	59	14%	
		R <sub>out</sub> ≈65Ω setting	V <sub>CCO</sub> =3.3V	-8%	65	8%	
			V <sub>CCO</sub> =2.5V	-9%	64	9%	
			V <sub>CCO</sub> =1.8V	-13%	64	13%	
		R <sub>out</sub> ≈70Ω setting	V <sub>CCO</sub> =3.3V	-9%	72	9%	
			V <sub>CCO</sub> =2.5V	-10%	70	10%	
V <sub>CCO</sub> =1.8V	-12%		69	12%			

1. Guaranteed by characterization.

## Performance Characteristics – PLL

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$f_{REF}, f_{FBK}$	Reference and feedback input frequency range		10	—	320	MHz
$t_{CLOCKHI}, t_{CLOCKLO}$	Reference and feedback input clock HIGH and LOW times		1.25	—	—	ns
$t_{RINP}, t_{FINP}$	Reference and feedback input rise and fall times	Measured between 20% and 80% levels	—	—	5	ns
$M_{DIV}$	M-divider range		1	—	32	
$N_{DIV}$	N-Divider range		1	—	32	
$f_{PFD}$	Phase detector input frequency range <sup>2</sup>		10	—	320	MHz
$f_{VCO}$	VCO operating frequency		320	—	640	MHz
$V_{DIV}$	Output Divider range	Even integer values only	2	—	64	
$f_{OUT}$	Output frequency range <sup>1</sup>	Fine Skew Mode, $f_{VCO} = 640\text{MHz}$	10	—	320	MHz
		Coarse Skew Mode, $f_{VCO} = 640\text{MHz}$	5	—	160	MHz
$t_{JIT}(\text{cc})$	Output adjacent-cycle jitter (1000 cycle sample)	Loop filter from Table 2 <sup>3</sup>	—	45	60	ps (p-p)
		Loop filter from Table 3 <sup>8</sup>	—	45	70	ps (p-p)
$t_{JIT}(\text{per})$	Output period jitter (10000 cycle sample)	Loop filter from Table 2 <sup>3</sup>	—	8	10	ps (RMS)
		Loop filter from Table 3 <sup>8</sup>	—	9	12	ps (RMS)
$t_{JIT}(\phi)$	Reference clock to output jitter (6000 cycle sample)	Loop filter from Table 2 <sup>3</sup>	—	NA	NA	ps (RMS)
		Loop filter from Table 3 <sup>8</sup>	—	38	50	ps (RMS)
$t_{\phi}$	Static phase offset	PFD input frequency $\geq 100\text{MHz}$ <sup>7</sup>	-375	-75	225	ps
		PFD input frequency $< 100\text{MHz}$ <sup>7</sup>	-37.5	—	22.5	mUI <sup>6</sup>
$t_{DELAY}$	Reference clock to output delay	Internal feedback mode <sup>7</sup>	0.3	0.45	0.6	ns
$DC_{ERR}$	Output duty cycle error (see Table 4 for nominal values) <sup>4</sup>	Output type LVDS, $V_{CCO} = 3.3\text{V}$ <sup>5</sup>	—	—	260	ps
		Output type LVCMOS 3.3V <sup>5</sup> $f_{OUT} > 100\text{MHz}$	—	—	300	ps
$t_{PDBYPASS}$	Reference clock to output propagation delay	$M=1, V=2$	—	6	—	ns
$t_L$	PLL Lock time	From Power-up event	—	150	500	$\mu\text{s}$
		From Reset event	—	15	50	$\mu\text{s}$
PSR	Power supply rejection, period jitter vs. power supply noise	$f_{IN} = f_{OUT} = 100\text{MHz}$ $V_{CCA} = V_{CCD} = V_{CCO}$ modulated with 100kHz sinusoidal stimulus	—	0.05	—	$\frac{\text{ps(RMS)}}{\text{mV(p-p)}}$

1. In PLL Bypass mode (PLL\_BYPASS = HIGH), output will support frequencies down to 0Hz (divider chain is a fully static design).

2. Dividers should be set so that they provide the phase detector with signals of 10MHz or greater for loop stability.

3.  $f_{IN} = f_{OUT} = 100\text{MHz}$ ,  $M = N = 1$ ,  $V = 6$ , output type LVPECL.

4. Variation in duty cycle expressed in ps. To obtain duty cycle percentage error (%<sub>ERR</sub>) for a given output frequency ( $f_{OUT}$ ), %<sub>ERR</sub> = 100 x  $f_{OUT} \times DC_{ERR}$ .

5. See Figures 3-5 for output loads.

6. milli-Unit Interval

7. Input and outputs LVPECL mode

8.  $f_{IN} = 100\text{MHz}$ ,  $M = 1$ ,  $N = 3$ ,  $V = 2$ , output type LVPECL.

## Timing Specifications

### Skew Matching

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{SKREW}$	Output-output Skew	Between any two identically configured and loaded outputs regardless of bank.	—	—	50	ps

### Programmable Skew Control

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{SKRANGE}$	Skew Control Range <sup>1</sup>	Fine Skew Mode, $f_{VCO} = 320$ MHz	—	5.86	—	ns
		Fine Skew Mode, $f_{VCO} = 640$ MHz	—	2.93	—	
		Coarse Skew Mode, $f_{VCO} = 320$ MHz	—	11.72	—	
		Coarse Skew Mode, $f_{VCO} = 640$ MHz	—	5.86	—	
$SK_{STEPS}$	Skew Steps per range		—	16	—	
$t_{SKSTEP}$	Skew Step Size <sup>2</sup>	Fine Skew Mode, $f_{VCO} = 320$ MHz	—	390	—	ps
		Fine Skew Mode, $f_{VCO} = 640$ MHz	—	195	—	
		Coarse Skew Mode, $f_{VCO} = 320$ MHz	—	780	—	
		Coarse Skew Mode, $f_{VCO} = 640$ MHz	—	390	—	
$t_{SKERR}$	Skew Time Error <sup>3</sup>	Fine skew mode	—	30	—	ps
		Coarse skew mode	—	50	—	

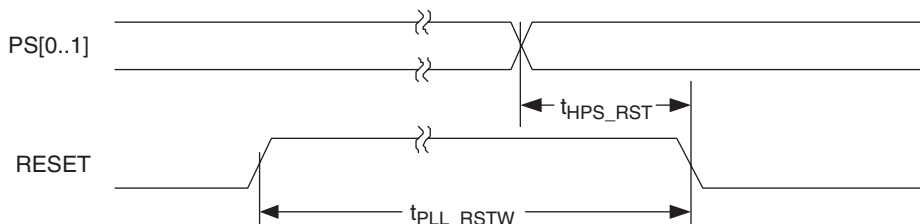
1. Skew control range is a function of VCO frequency ( $f_{VCO}$ ). In fine skew mode  $T_{SKRANGE} = 15/(8 \times f_{VCO})$ .  
In coarse skew mode  $T_{SKRANGE} = 15/(4 \times f_{VCO})$ .
2. Skew step size is a function of VCO frequency ( $f_{VCO}$ ). In fine skew mode  $T_{SKSTEP} = 1/(8 \times f_{VCO})$ .  
In coarse skew mode  $T_{SKSTEP} = 1/(4 \times f_{VCO})$ .
3. Only applicable to outputs with non-zero skew settings.

### Control Functions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{DIS/OE}$	Delay Time, $\overline{OE}X$ or $\overline{OE}Y$ to Output Disabled/Enabled		—	10	20	ns
$t_{DIS/GOE}$	Delay Time, $\overline{GOE}$ to Output Disabled/Enabled		—	10	20	ns
$t_{SUSGATE}$	Setup Time, SGATE to Output Clock Start/Stop		3	—	—	cycles <sup>1</sup>
$t_{PLL\_RSTW}$	PLL Reset Pulse Width <sup>2</sup>		1	—	—	ms
$t_{RSTW}$	Logic Reset Pulse Width <sup>3</sup>		20	—	—	ns
$t_{HPS\_RST}$	Hold time for RESET past change in PS[0..1]		20	—	—	ns

1. Output clock cycles for the particular output being controlled.
2. Will completely reset PLL.
3. Will only reset digital logic.

Figure 6. RESET and Profile Select Timing



## Timing Specifications (Cont.)

### Boundary Scan Logic

Symbol	Parameter	Min.	Max.	Units
$t_{BTCP}$	TCK (BSCAN Test) Clock Cycle	40	—	ns
$t_{BTCH}$	TCK (BSCAN Test) Pulse Width High	20	—	ns
$t_{BTCL}$	TCK (BSCAN Test) Pulse Width Low	20	—	ns
$t_{BTSU}$	TCK (BSCAN Test) Setup Time	8	—	ns
$t_{BTH}$	TCK (BSCAN Test) Hold Time	10	—	ns
$t_{BRF}$	TCK (BSCAN Test) Rise and Fall Rate	50	—	mV/ns
$t_{BTCO}$	TAP Controller Falling Edge of Clock to Valid Output	—	10	ns
$t_{BTOZ}$	TAP Controller Falling Edge of Clock to Data Output Disable	—	10	ns
$t_{BTVO}$	TAP Controller Falling Edge of Clock to Data Output Enable	—	10	ns
$t_{BVTCP}$	BSCAN Test Capture Register Setup Time	8	—	ns
$t_{BTCPH}$	BSCAN Test Capture Register Hold Time	10	—	ns
$t_{BTUCO}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	25	ns
$t_{BTUOZ}$	BSCAN Test Update Register, Falling Edge of Clock to Output Disable	—	25	ns
$t_{BTUOV}$	BSCAN Test Update Register, Falling Edge of Clock to Output Enable	—	25	ns

### JTAG Interface and Programming Mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$f_{MAX}$	Maximum TCK Clock Frequency		—	—	25	MHz
$t_{CKH}$	TCK Clock Pulse Width, High		20	—	—	ns
$t_{CKL}$	TCK Clock Pulse Width, Low		20	—	—	ns
$t_{ISPEN}$	Program Enable Delay Time		15	—	—	$\mu$ s
$t_{ISPDIS}$	Program Disable Delay Time		30	—	—	$\mu$ s
$t_{HVDIS}$	High Voltage Discharge Time, Program		30	—	—	$\mu$ s
$t_{HVDIS}$	High Voltage Discharge Time, Erase		200	—	—	$\mu$ s
$t_{CEN}$	Falling Edge of TCK to TDO Active		—	—	15	ns
$t_{CDIS}$	Falling Edge of TCK to TDO Disable		—	—	15	ns
$t_{SU1}$	Setup Time		8	—	—	ns
$t_H$	Hold Time		10	—	—	ns
$t_{CO}$	Falling Edge of TCK to Valid Output		—	—	15	ns
$t_{PWV}$	Verify Pulse Width		30	—	—	$\mu$ s
$t_{PWP}$	Programming Pulse Width		20	—	—	ms
$t_{BEW}$	Bulk Erase Pulse Width		200	—	—	ms



## Timing Diagrams

Figure 7. Erase (User Erase or Erase All) Timing Diagram

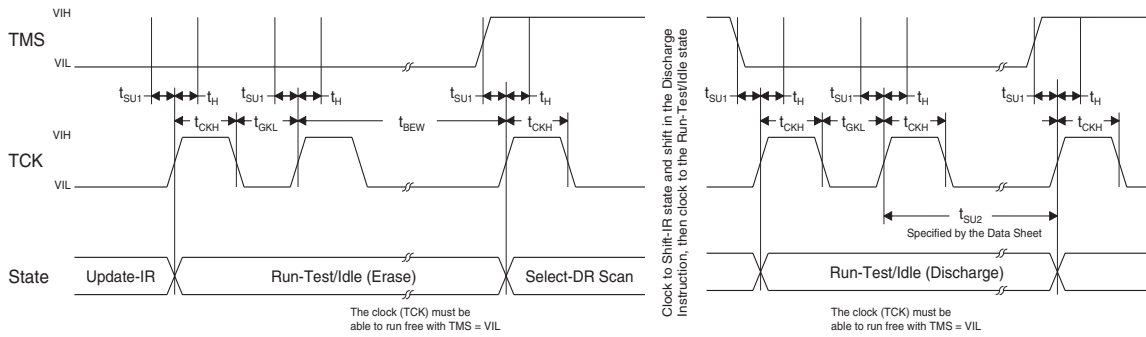


Figure 8. Programming Timing Diagram

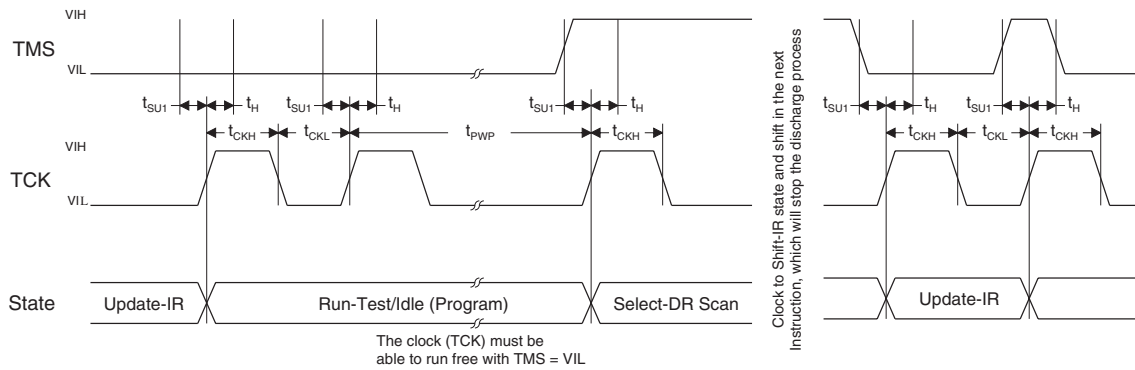


Figure 9. Verify Timing Diagram

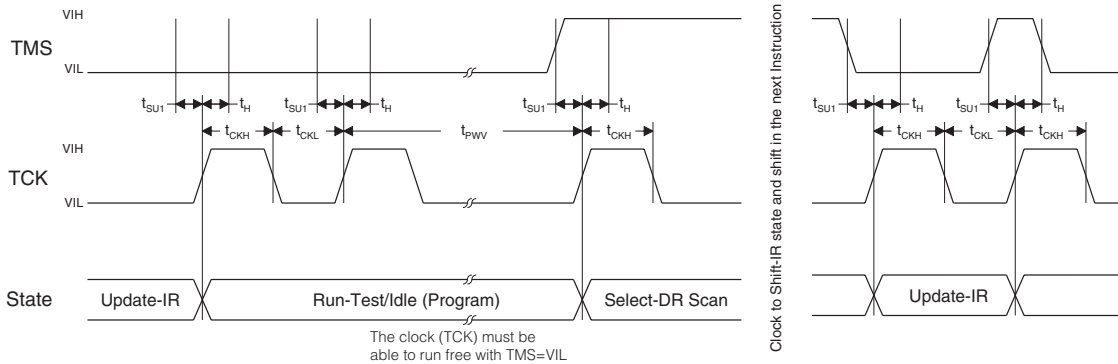
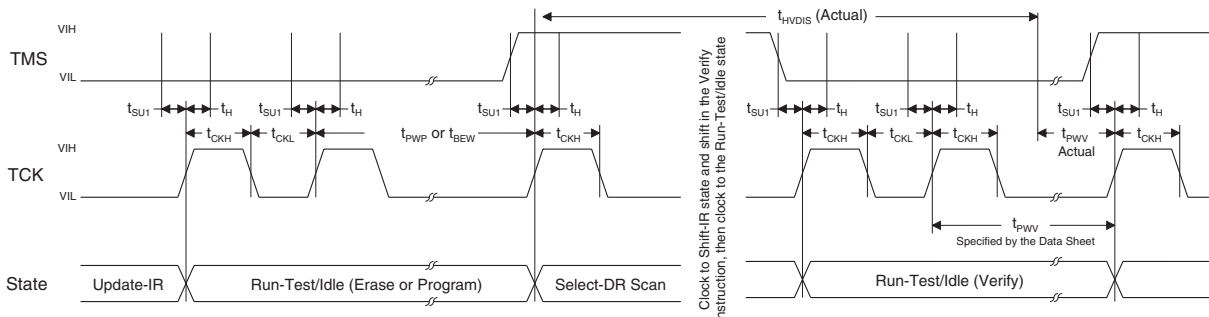
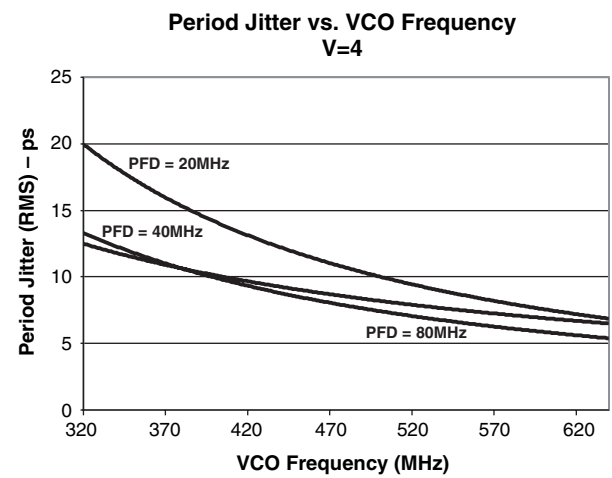
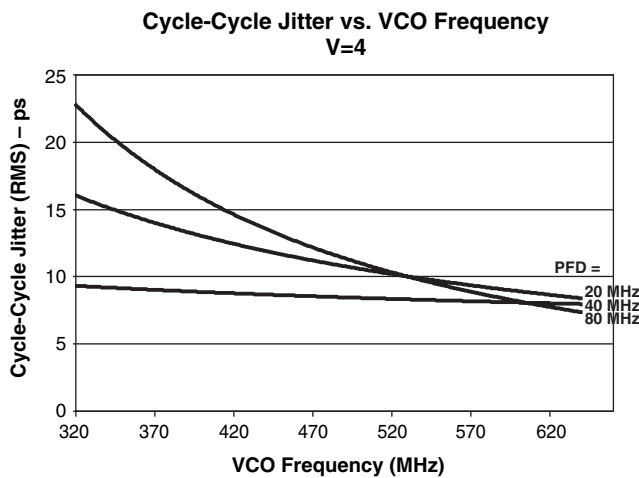
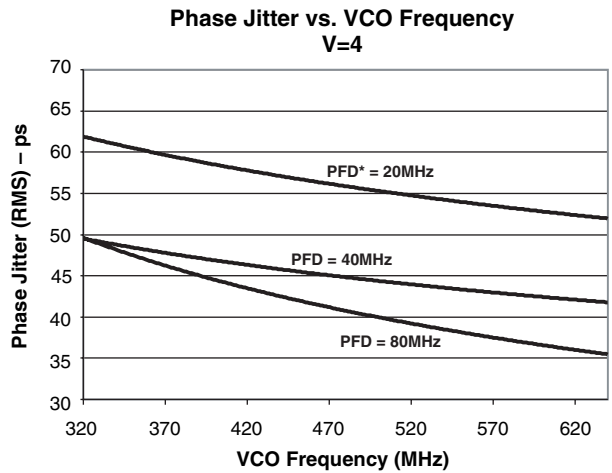
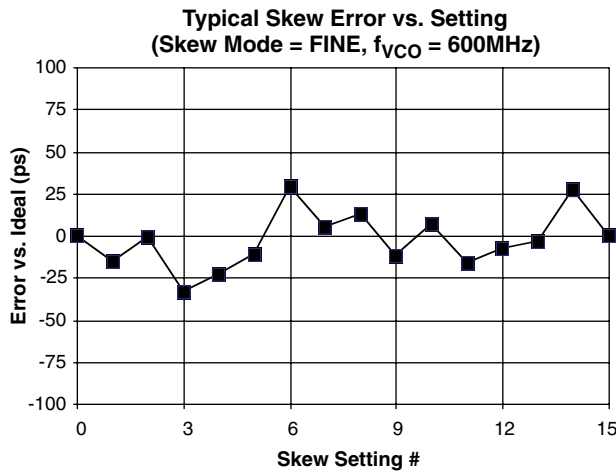
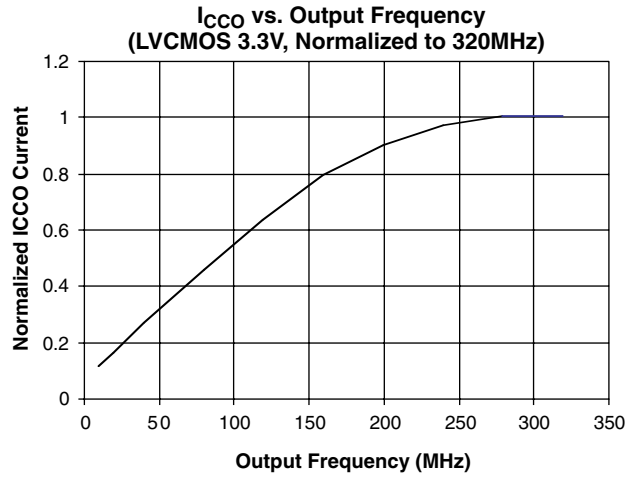
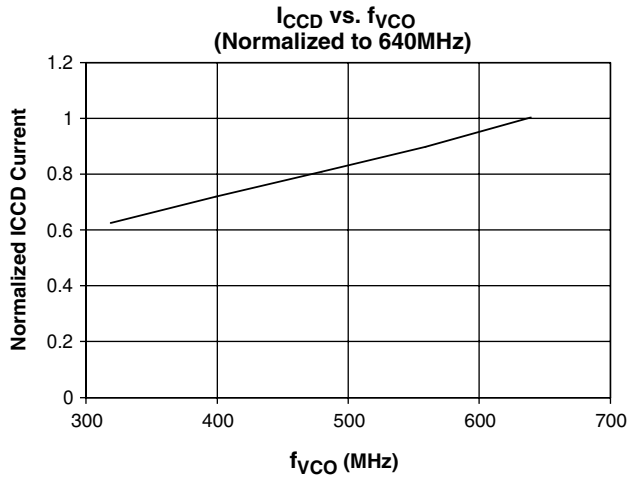


Figure 10. Discharge Timing Diagram

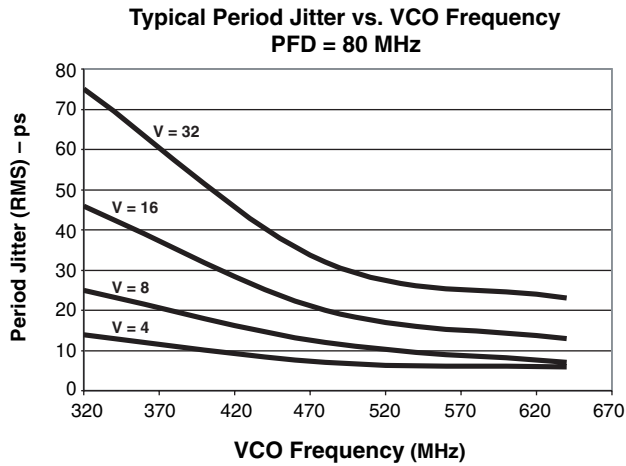
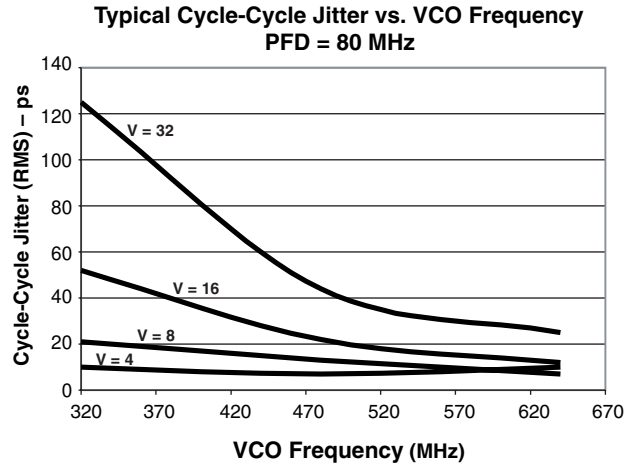
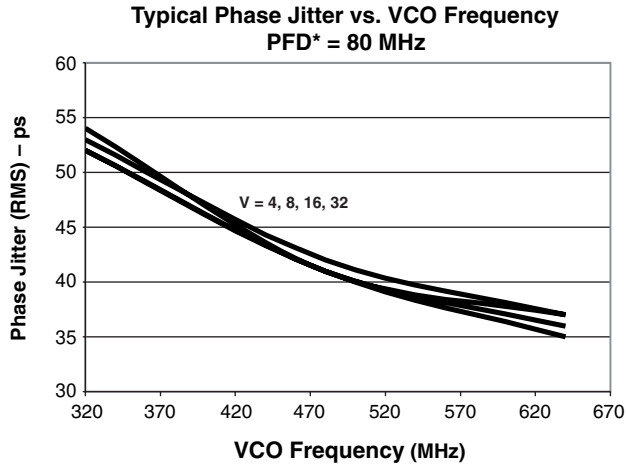


Typical Performance Characteristics



\*PFD = Phase/Frequency Detector

## Typical Performance Characteristics (Cont.)



\*PFD = Phase/Frequency Detector

## Detailed Description

### PLL Subsystem

The ispClock5600 provides an integral phase-locked-loop (PLL) which may be used to generate output clock signals at lower, higher, or the same frequency as a user-supplied input reference signal. The core functions of the PLL are an edge-sensitive phase detector, a programmable loop filter, and a high-speed voltage-controlled oscillator (VCO). Additionally, a set of programmable input, output and feedback dividers (M, N, V[1..5]) is provided to support the synthesis of different output frequencies.

### Phase/Frequency Detector

The ispClock5600 provides an edge-sensitive phase/frequency detector (PFD), which means that the device will function properly over a wide range of input clock reference duty cycles. It is only necessary that the input reference clock meet specified minimum HIGH and LOW times ( $t_{\text{CLOCKHI}}$ ,  $t_{\text{CLOCKLO}}$ ) for it to be properly recognized by the PFD. The PFD's output is of a classical charge-pump type, outputting charge packets which are then integrated by the PLL's loop filter.

A lock-detection feature is also associated with the PFD. When the ispClock5600 is in a LOCKED state, the  $\overline{\text{LOCK}}$  output pin goes LOW. The lock detector has two operating modes; phase lock mode and frequency lock mode. In

phase-lock mode, the  $\overline{\text{LOCK}}$  signal is asserted if the phases of the reference and feedback signals match, whereas in frequency-lock mode the  $\overline{\text{LOCK}}$  signal is asserted when the frequencies of the feedback and reference signals match. The option of which mode to use is programmable and may be set using PAC-Designer software (available from the Lattice web site at [www.latticesemi.com](http://www.latticesemi.com)).

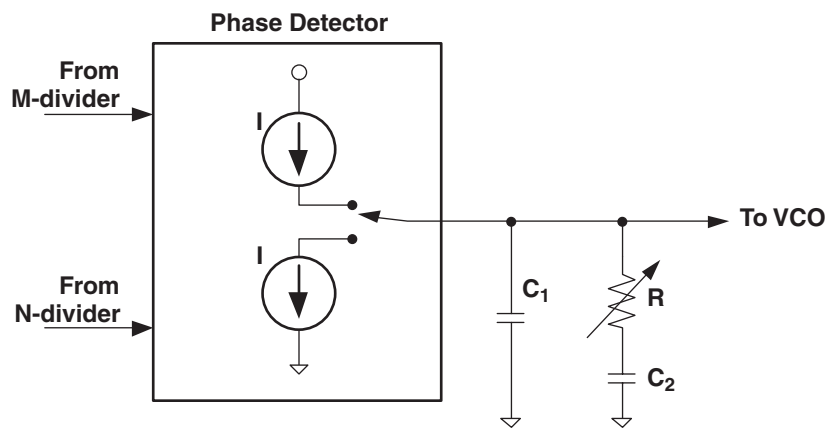
In phase-lock mode the lock detector asserts the  $\overline{\text{LOCK}}$  signal as soon as a lock condition is determined. In frequency-lock mode, however, the PLL must be in a locked condition for a set number of phase detector cycles before the  $\overline{\text{LOCK}}$  signal will be asserted. The number of cycles required before asserting the  $\overline{\text{LOCK}}$  signal in frequency-lock mode can be set from 16 through 256.

When the lock condition is lost the  $\overline{\text{LOCK}}$  signal will be de-asserted immediately in both phase-lock and frequency-lock detection modes. In frequency-lock mode, however, if the input reference signal is stopped, the  $\overline{\text{LOCK}}$  output may continue to be asserted. In phase-lock mode, a loss of the input reference signal will always result in de-assertion of the  $\overline{\text{LOCK}}$  output.

### Loop Filter

A simplified schematic for the ispClock5600 loop filter is shown in Figure 11. The filter's capacitors are fixed, and the response is controlled by setting the value of the phase-detector's output current source's and the value of the variable resistor. The phase detector output current has 14 possible settings, ranging from  $3\mu\text{A}$  to  $55\mu\text{A}$ , while the resistor may be set to any one of six values ranging from 2.3K to 9.3K. This provides a total of 84 unique I-R combinations which may be selected.

**Figure 11. ispClock5600 Loop Filter (Simplified)**



Because the selection of an optimal PLL loop filter can be a daunting task, PAC-Designer offers a set of default filter settings which will provide acceptable performance for most applications. The primary criterion for selecting one of these settings is the total division factor used in the feedback path. This factor is the ratio between the VCO output frequency and the feedback V-divider output frequency which is the product of the N-divider and  $V_{\text{feedback}}$ -divider ( $N \times V_{\text{feedback}}$ ). Table 2 and Table 3 list the default loop filter settings that correspond to all possible allowable  $V \times V_{\text{feedback}}$  values. Table 2 should be used to minimize cycle to cycle and period jitter while Table 3 should be used to optimize overall jitter performance including phase jitter.

**Table 2. Filter Settings for Minimizing Cycle-Cycle and Period Jitter**

<b>N x V<sub>FBK</sub></b>	<b>I (μA)</b>	<b>R (kΩ)</b>
2 to 8	5	2.3
10	7	2.3
12 to 14	9	2.3
16	11	2.3
18 to 20	13	2.3
22	15	2.3
24 to 26	17	2.3
28	19	2.3
30	21	2.3
32 to 64	22	2.3

Note: Do not use this setting if phase jitter performance optimization is required.

**Table 3. Filter Settings for Optimizing Overall Jitter (Recommended)**

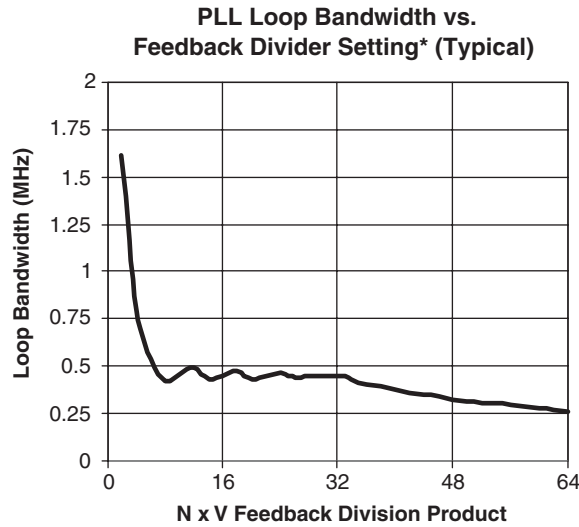
<b>N x V<sub>FBK</sub></b>	<b>I (μA)</b>	<b>R (kΩ)</b>
2	17	2.3
4 to 6	33	2.3
8 to 14	55	2.3
16 to 22	55	3.7
24 to 52	55	5.1
54 to 62	55	7.9

Note that the choice of loop filter parameters can have significant effects on settling time, output jitter, and whether the PLL will be fundamentally stable and be able to lock to an incoming signal. The values recommended in Table 2 and Table 3 were chosen to provide maximum loop stability while still providing exceptional jitter performance. Please note that when the skew mode is set to ‘coarse’, the effective value of NxV must be considered to have doubled. Refer to the section titled ‘Coarse Skew Mode’ on page 30 for further details.

The PLL’s loop bandwidth is a function of both the divider configuration and the loop filter settings. Figure 12 shows the loop bandwidth as a function of the total feedback division ratio (N x V<sub>FBK</sub>). For each NxV feedback divider point in this plot, the PLL loop filter was set to the corresponding value recommended in Table 2. The use of non-recommended loop filter settings may result in significantly different bandwidths for a given NxV divider setting.



Figure 12. PLL Loop Bandwidth vs. Feedback Divider Setting (nominal)



\*loop filter configured to recommended setting

**VCO**

The ispClock5600 provides an internal VCO which provides an output frequency ranging from 320MHz to 640MHz. The VCO is implemented using differential circuit design techniques which minimize the influence of power supply noise on measured output jitter. The VCO is also used to generate skews as a function of the total VCO period. Using the VCO as the basis for controlling output skew allows for highly precise and consistent skew generation, both from device-to-device, as well as channel-to-channel within the same device.

**M, N, and V Dividers**

The ispClock5600 incorporates a set of programmable dividers which provide the ability to synthesize output frequencies differing from that of the reference clock input.

The input, or M divider prescales the input reference frequency, and can be programmed with integer values over the range of 1 to 32. To achieve low levels of output jitter, it is best to use the smallest M divider value possible.

The feedback, or N divider prescales the feedback frequency and like the M divider, can also be programmed with integer values ranging from 1 to 32.

Each one of the five output, or V dividers can be independently programmed to provide even division ratios ranging from 2 to 64.

When the PLL is selected (PLL\_BYPASS=LOW) and locked, the output frequency of each V divider (f<sub>k</sub>) may be calculated as:

$$f_k = f_{ref} \frac{N \times V_{fbk}}{M \times V_k} \tag{1}$$

where

- f<sub>k</sub> is the frequency of V divider k
- f<sub>ref</sub> is the input reference frequency
- M and N are the input and feedback divider settings
- V<sub>fbk</sub> is the setting of the V divider used to close the PLL feedback path
- V<sub>k</sub> is the setting of the V divider used to provide output k

Note that because the feedback may be taken from any V divider, V<sub>k</sub> and V<sub>fbk</sub> may refer to the same divider.

Because the VCO has an operating frequency range spanning 320 MHz to 640 MHz, and the V dividers provide division ratios from 2 to 64, the ispClock5600 can generate output signals ranging from 5MHz to 320 MHz. For performance and stability reasons, however, there are several constraints which should be followed when selecting divider values:

- Use the smallest feasible value for the M divider
- The output frequency from the M (and N) divider should be greater or equal to 10 MHz.
- The product of the N divider and the V divider used to close the PLL's feedback loop should be less than or equal to 64 ( $N \times V_{fbk} \leq 64$ )

**Output Duty Cycle**

The ispClock5600's output duty cycle varies as a function of the V divider used to generate that output. If the V-divider setting is either 2 or a multiple of 4, the nominal output duty cycle will be exactly 50%. All other V divider settings will result in non-50% output duty cycles. Table 4 summarizes the nominal output duty cycle as a function of the V divider setting. Note that if the output is inverted, the duty cycle will be equal to 100%-DC%, where DC% is the duty cycle indicated in the table. For example, with a V divider of 14, the non-inverted duty cycle from Table 4 will be 43%. For an inverted output, the duty cycle will be 100%-43% or 57%.

**Table 4. Nominal Output Duty Cycle vs. V-divider Setting**

Divider Settings with 50% Output Duty Cycle		Divider Settings with Non-50% Output Duty Cycles	
V	DC%	V	DC%
2	50	6	33
4		10	40
8		14	43
12		18	44
16		22	45
20		26	46
24		30	47
28		34	47
32		38	47
36		42	48
40		46	48
44		50	48
48		54	48
52		58	48
56		62	48
60			
64			

**Device Start-up Behavior**

The outputs of the ispClock5600 always start up edge aligned. When the V-divider is set to a value of 2 and the output skew is set to a value greater than 8, the first clock cycle immediately following power-up could be incomplete (runt cycle). For all the remaining conditions, no runt clocks will be generated after power-up.

**PLL\_BYPASS Mode**

The PLL\_BYPASS mode is provided so that input reference signals can be coupled through to the outputs without using the PLL functions. When PLL\_BYPASS mode is enabled (PLL\_BYPASS=HIGH), the output of the M divider is routed directly to the inputs of the V dividers. In PLL\_BYPASS mode, the nominal values of the V dividers are

halved, so that they provide division ratios ranging from 1 to 32. The output frequency for a given V divider ( $f_k$ ) will be determined by

$$f_k = \frac{f_{\text{ref}} \times 2}{M \times V_k} \quad (2)$$

Please note that PLL\_BYPASS mode is provided primarily for testing purposes. When PLL\_BYPASS mode is enabled, features such as lock detect and skew generation are unavailable.

## Reference and External Feedback Inputs

The ispClock5600 provide sets of configurable, internally-terminated inputs for both clock reference and feedback signals. In normal operation, the one of the clock reference input pairs (REFA+/- or REFB+/-) is used as a clock input.

The external feedback inputs make it possible to sample an output signal at the point of delivery. This makes it possible to provide output clocks which have very low skews in relation to the reference clock regardless of loading effects.

The ispClock5610 provides one input signal pair for reference input and one input pair for external feedback, while the ispClock5620 provides two pairs for reference signals and two pairs for feedback. To select between reference and feedback inputs, the ispClock5620 provides two CMOS-compatible digital inputs called REFSEL and FBKSEL. Table 5 shows the behavior of these two control inputs.

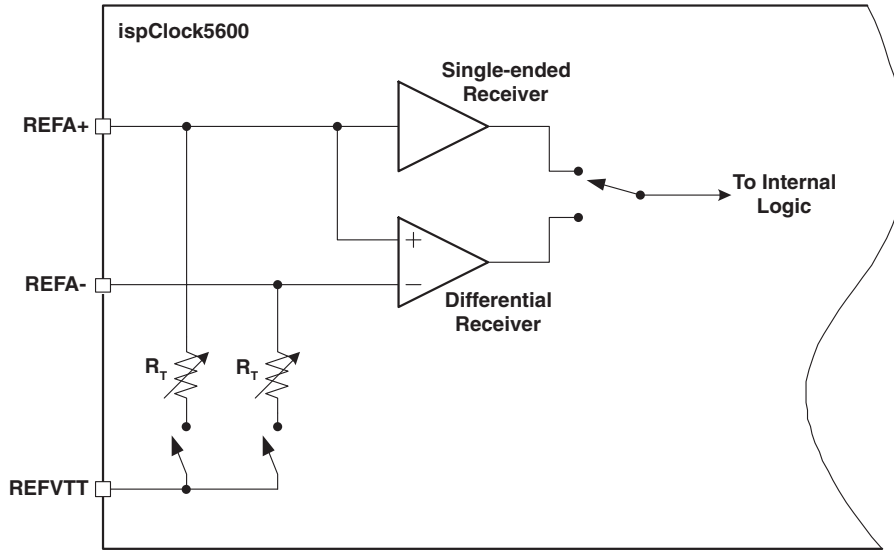
**Table 5. REFSEL and FBKSEL Operation for ispClock5620**

REFSEL	Selected Input Pair	FBKSEL	Selected Input Pair
0	REFA+/-	0	FBKA+/-
1	REFB+/-	1	FBKB+/-

- LVTTTL (3.3V)
- LVCMOS (1.8V, 2.5V, 3.3V)
- SSTL2
- SSTL3
- HSTL
- Differential SSTL2
- Differential SSTL3
- Differential HSTL
- LVDS
- LVPECL (differential, 3.3V)

Each input also features internal programmable termination resistors, as shown in Figure 13. Note that all reference inputs (REFA+, REFA-, REFB+, REFB-) terminate to the REFVTT pin, while all feedback inputs (FBKA+, FBKA-, FBKB+, FBKB-) terminate to the FBKVTT pin.

Figure 13. ispClock5600 Clock Reference and Feedback Input Structure (REFA+/- Pair Shown)

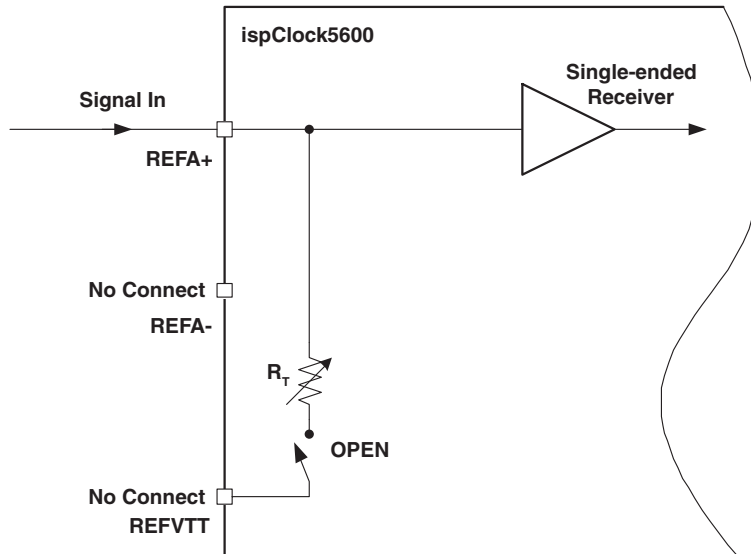


The following usage guidelines are suggested for interfacing to supported logic families.

**LVTTTL (3.3V), LVCMOS (1.8V, 2.5V, 3.3V)**

The receiver should be set to LVCMOS or LVTTTL mode, and the input signal should be connected to the '+' terminal of the input pair (e.g. REFA+). The '-' input terminal should be left floating. CMOS transmission lines are generally source terminated, so all termination resistors should be set to the OPEN state. Figure 14 shows the proper configuration. Please note that because switching thresholds are different for LVCMOS running at 1.8V, there is a separate configuration setting for this particular standard.

Figure 14. LVCMOS/LVTTTL Input Receiver Configuration

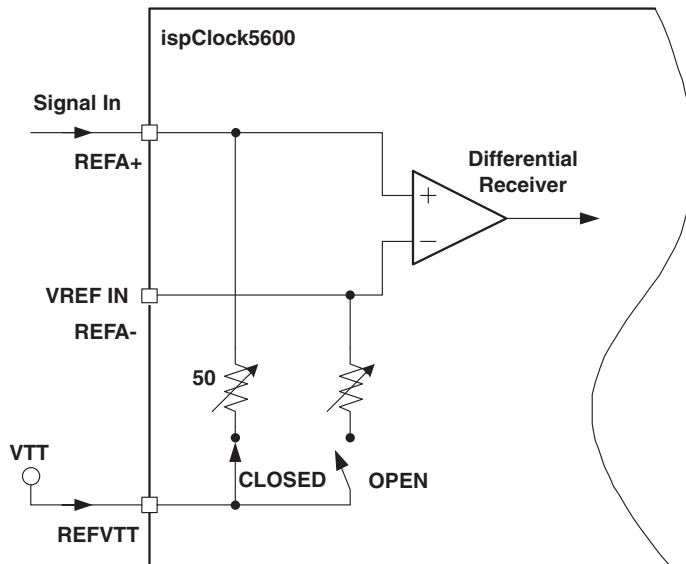


**HSTL, SSTL2, SSTL3**

The receiver should be set to HSTL/SSTL mode, and the input signal should be fed into the '+' terminal of the input pair. The '-' input terminal should be tied to the appropriate  $V_{REF}$  value, and the associated REFVTT or FBKVTT terminal should be tied to a  $V_{TT}$  termination supply. The positive input's terminating resistor should be engaged and set to 50Ω. Figure 15 shows an appropriate configuration. Refer to the "Recommended Operating Conditions - Supported Logic Standards" table in this data sheet for suitable values of  $V_{REF}$  and  $V_{TT}$ .

One important point to note is that the termination supplies must have low impedance and be able to both source and sink current without experiencing fluctuations. These requirements generally preclude the use of a resistive divider network, which has an impedance comparable to the resistors used, or of commodity-type linear voltage regulators, which can only source current. The best way to develop the necessary termination voltages is with a regulator specifically designed for this purpose. Because SSTL and HSTL logic is commonly used for high-performance memory busses, a suitable termination voltage supply is often already available in the system.

Figure 15. SSTL2, SSTL3, HSTL Receiver Configuration

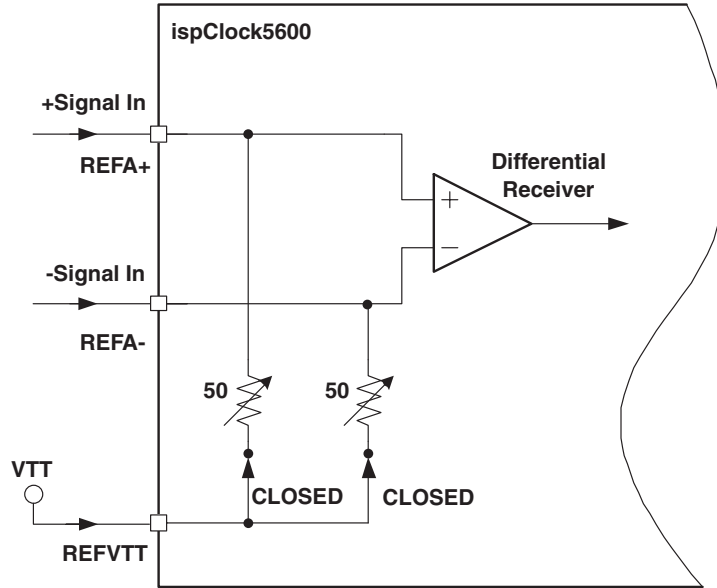




**Differential HSTL and SSTL**

HSTL and SSTL are sometimes used in a differential form, especially for distributing clocks in high-speed memory systems. Figure 16 shows how ispClock5600 reference input should be configured for accepting these standards. The major difference between differential and single-ended forms of these logic standards is that in the differential case, the REFA- input is used as a signal input, not a reference level, and that both terminating resistors are engaged and set to 50Ω.

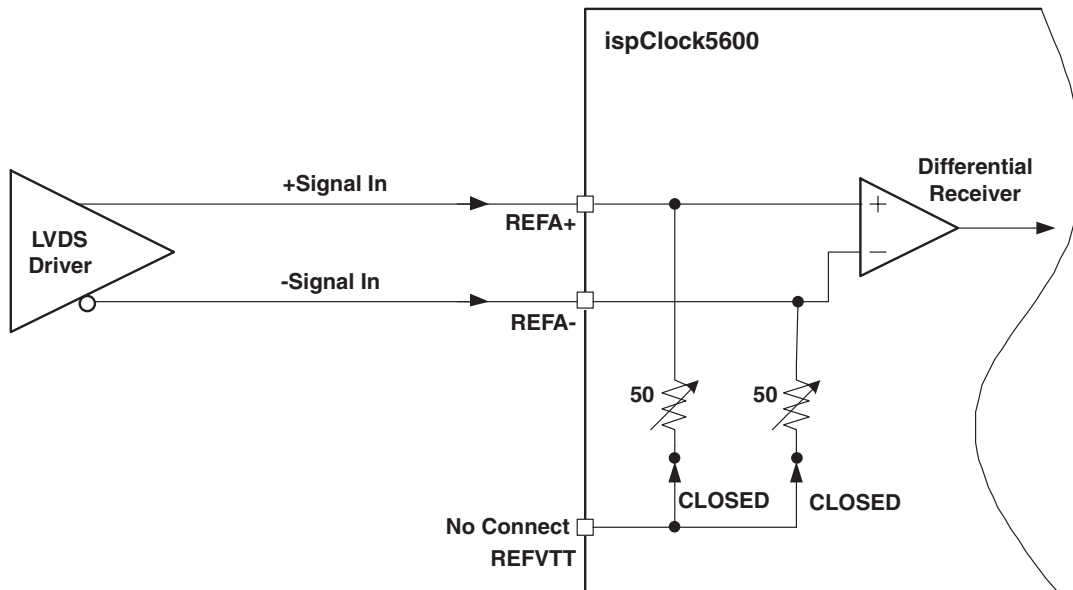
**Figure 16. Differential HSTL/SSTL Receiver Configuration**



**LVDS/Differential LVPECL**

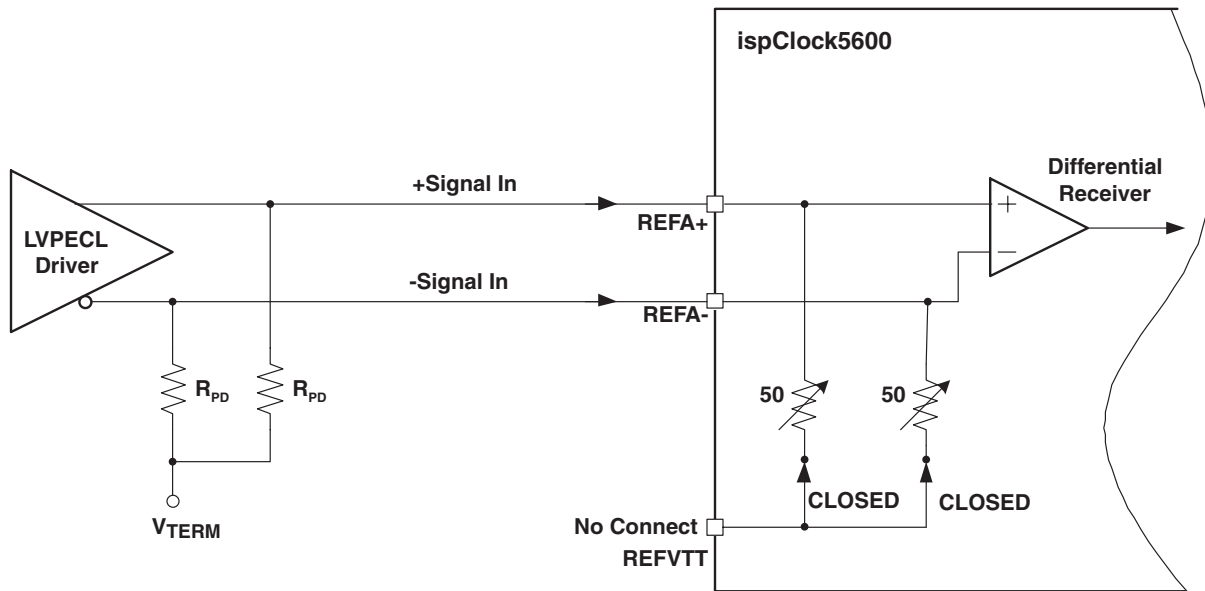
The receiver should be set to LVDS or LVPECL mode as required and both termination resistors should be engaged and set to 50Ω. The associated REFVTT or FBKVTT pin, however, should be left unconnected. This creates a floating 100Ω differential termination resistance across the input terminals. The LVDS termination configuration is shown in Figure 17.

**Figure 17. LVDS Input Receiver Configuration**



Note that while a floating  $100\Omega$  resistor forms a complete termination for an LVDS signal line, additional circuitry may be required to satisfactorily terminate a differential LVPECL signal. This is because a true bipolar LVPECL output driver typically requires an external DC 'pull-down' path to a  $V_{\text{TERM}}$  termination voltage (typically  $V_{\text{CC}}-2\text{V}$ ) to properly bias its open emitter output stage. When interfacing to an LVPECL input signal, the ispClock5600's internal termination resistors should not be used for this pull-down function, as they may be damaged from excessive current. The pull-down should be implemented with external resistors placed close to the LVPECL driver (Figure 18)

**Figure 18. LVPECL Input Receiver Configuration**



Please note that while the above discussions specify using  $50\Omega$  termination impedances, the actual impedance required to properly terminate the transmission line and maintain good signal integrity may vary from this ideal. The actual impedance required will be a function of the driver used to generate the signal and the transmission medium used (PCB traces, connectors and cabling). The ispClock5600's ability to adjust input impedance over a range of  $40\Omega$  to  $70\Omega$  allows the user to adapt his circuit to non-ideal behaviors from the rest of the system without having to swap out components.

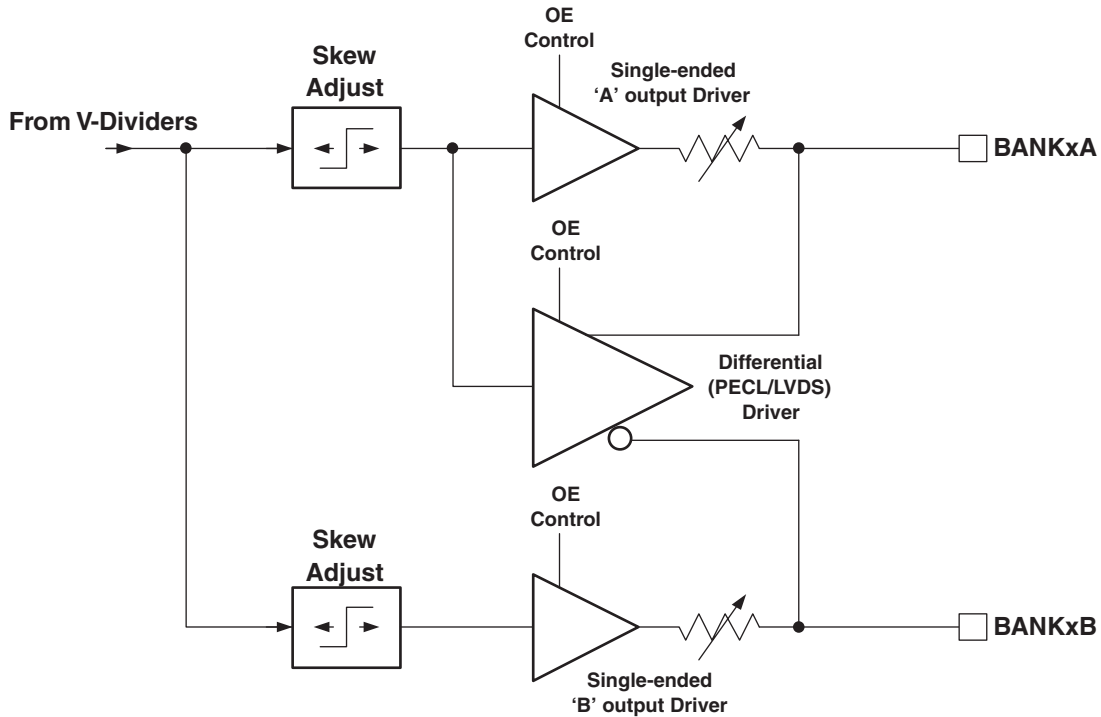
## Output Drivers

The ispClock5600 provide banks of configurable, internally-terminated high-speed dual-output line drivers. The ispClock5610 provides five driver banks, while the ispClock5620 provides ten. Each of these driver banks may be configured to provide either a single differential output signal, or a pair of single-ended output signals. Programmable internal source-series termination allows the ispClock5600 to be matched to transmission lines with impedances ranging from  $40$  to  $70$  Ohms. The outputs may be independently enabled or disabled, either from  $E^2\text{CMOS}$  configuration or by external control lines. Additionally, each can be independently programmed to provide a fixed amount of signal delay or skew, allowing the user to compensate for the effects of unequal PCB trace lengths or loading effects. Figure 19 shows a block diagram of a typical ispClock5600 output driver bank and associated skew control.

Because of the high edge rates which can be generated by the ispClock5600's clock output drivers, the  $V_{\text{CCO}}$  power supply pin for each output bank should be individually bypassed. Low ESR capacitors with values ranging from  $0.01$  to  $0.1 \mu\text{F}$  may be used for this purpose. Each bypass capacitor should be placed as close to its respective output bank power pins ( $V_{\text{CCO}}$  and  $\text{GNDO}$ ) pins as is possible to minimize interconnect length and associated parasitic inductances.

In the case where an output bank is unused, the associated VCCO pin may be either left floating or tied to ground to reduce quiescent power consumption. We recommend, however, that all unused VCCO pins be tied to ground where possible. All GND0 pins must be tied to ground, regardless of whether or not the associated bank is used.

**Figure 19. ispClock5600 Output Driver and Skew Control**



Each of the ispClock5600's output driver banks can be configured to support the following logic outputs:

- LVTTTL
- LVCMOS (1.8V, 2.5V, 3.3V)
- SSTL2
- SSTL3
- HSTL
- LVDS
- Differential LVPECL (3.3V)

To provide LVTTTL, LVCMOS, SSTL2, SSTL3, and HSTL outputs, the CMOS output drivers in each bank are enabled. These circuits provide logic outputs which swing from ground to the VCCO supply rail. The choice of VCCO to be supplied to a given bank is determined by the logic standard to which that bank is configured. Because each pair of outputs has its own VCCO supply pin, each bank can be independently configured to support a different logic standard. Note that the two outputs associated with a bank must necessarily be configured to the same logic standard. The source impedance of each of the two outputs in each bank may be independently set over a range of 40Ω to 70Ω in 5Ω steps. A low impedance option (≈20Ω) is also provided for cases where low source termination is desired on a given output.

Control of output slew rate is also provided in LVTTTL, LVCMOS, SSTL2, SSTL3, and HSTL output modes. Four output slew-rate settings are provided, as specified in the “Output Rise Times” and “Output Fall Times” tables in this data sheet.

To provide LVDS and differential LVPECL outputs, a separate internal driver is used which provides the correct LVDS or LVPECL logic levels when operating from a 3.3V VCCO. Because both LVDS and differential LVPECL transmission lines are normally terminated with a single 100Ω resistor between the ‘+’ and ‘-’ signal lines at the far